NORD-50 CPU

HARDWARE MANUAL I

REVISION RECORD

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1 INTRODUCTION

The NORD-50 is designed to be an auxiliary computer in a general computer system.

NORD-50 works as a slave computer being monitored by a NORD-10 computer.

One of the main design criteria for NORD-50 was high performance on number crunching, but in addition NORD-50 is an effective general purpose computer. The intention of this manual is to give a functional description of the NORD-50 central processing unit and present information regarding maintenance. The reader is supposed to have a basic knowledge of the NORD-50 instruction set, which has been covered in a separate manual.

Floating point arithmetic is performed in separate units which are also described in other manuals.

The wordlength of NORD-50 is 32 bits for instructions and integers. A floating point number is represented in a 32 or 64 bit floating word (two consecutive 32 bit words).

The central processing unit (CPU) contains 64 general registers, each 32 bits long. 16 of the registers may be used as base or index registers, and to each of them is associated one modification register which may contain increments to the operand in certain conditional jump instructions.

64 bit registers for holding double precision floating point numbers are formed by connecting the general registers two by two to obtain 32 floating registers.

The instructions are classified in three groups. The memory reference instructions, the inter register instructions, and the argument instructions. The memory reference instructions normally affect one register and one memory word. The memory addressing may be direct or indirect. Up to 16 levels of indirect addressing may be used.

The inter register operations normally use two operand registers called source register A and source register B. The result is stored in a third register, the destination register. These three registers may be any of the general registers. The inter register double precision floating point instructions affect pairs of registers.

The argument instructions are generally two-operand instructions with one of the operands contained in the instruction itself.

2 NORD-50 SYSTEM

The NORD-50 can be divided into seven basic functional units. The main registers and arithmetic, the communication registers, memory interface, memory, external arithmetic and control unit are connected as shown in figure 2.1. Additional a display unit is connected to the CPU.

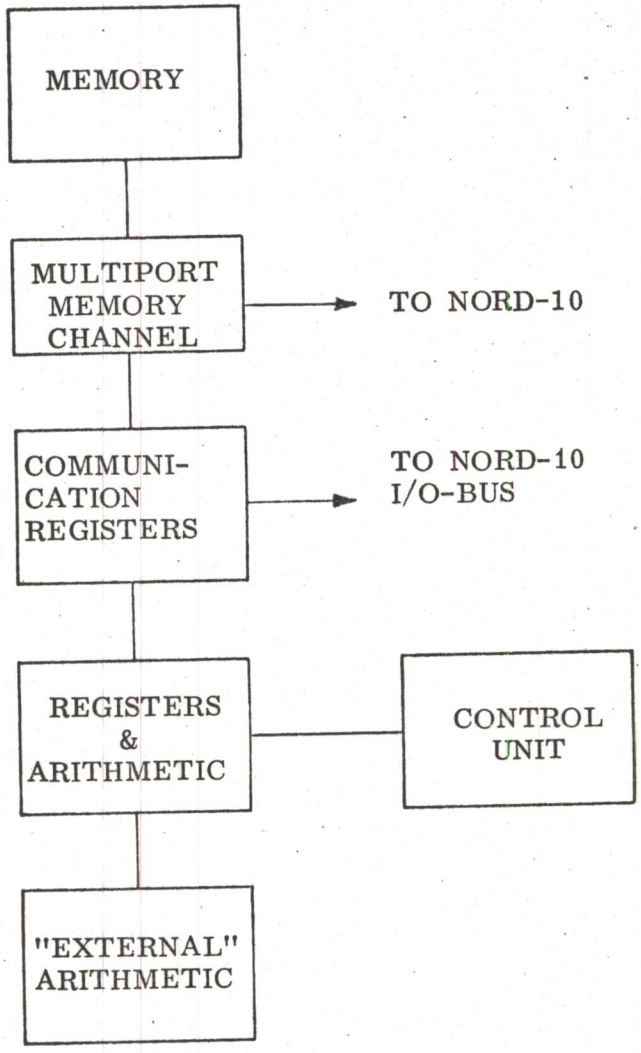


Figure 2.1 NORD-50 BLOCK DIAGRAM

2.1 Registers and Arithmetic

This unit contains 64 general data registers, main arithmetic for add, subtract and logical operations and address arithmetic. 16 of the registers may be used as base or index registers. Register 0 always contains zero.

2.2 Communication Registers

NORD-50 is operated by NORD-10 as a peripheral unit connected to the NORD-10 I/O system, and the communication unit has the necessary buffer registers to enter data on the memory address and data buses and to read the data on the same buses. Four basic modes of operation exist:

1 Idle or data transfer to/from the communication registers with NORD-10 I/O instructions.

2 EXAMINE/DEPOSIT in core memory directly from NORD-10.

3 Execution of instructions supplied by NORD-10 and data transferred directly from NORD-10 to register block. This mode is also called SIMULATED MEMORY mode.

4 Normal RUN mode where instructions and data go to/from core memory independent of NORD-10. This mode is terminated by a STOP instruction in the NORD-50 program, by NORD-10 or when a hardware error is detected.

For further details see THE NORD-10/NORD-50 COMMUNICATION SYSTEM.

2.3 Memory Interface

The memory interface has 32 bits data wordlength. This is split into two 16 bits channels, each connected to one multiport memory channel.

2.4 Memory

The multiport memory system is described in a separate manual.

2.5 External Arithmetic

To obtain a flexible and straight forward system for floating point and shift operations, the circuits for these functions are organized as separate units connected to the main system with three 64 bit buses, two for operands out and one for result.

The two external units are:

1 Divide / multiply fixed point or floating point.

2 Floating point add / subtract, normalize / denormalize, shift and bit operations.

These units are covered in separate manuals.

2.6 Control Unit

The control unit has a program counter, instruction register and other counters and registers, and it generates enabling signals and strobe pulses to all other units.

2.7 Display Unit (Figure 2.2)

The display unit is mainly for hardware and software debugging. There are totally 32 status or indicator lamps on the panel, and two push buttons. The push buttons are used to select display of Program Counter or Data Reference on the 16 bit Active Address display at the top of the panel. The display visualizes the addressed bank of 4K memory.

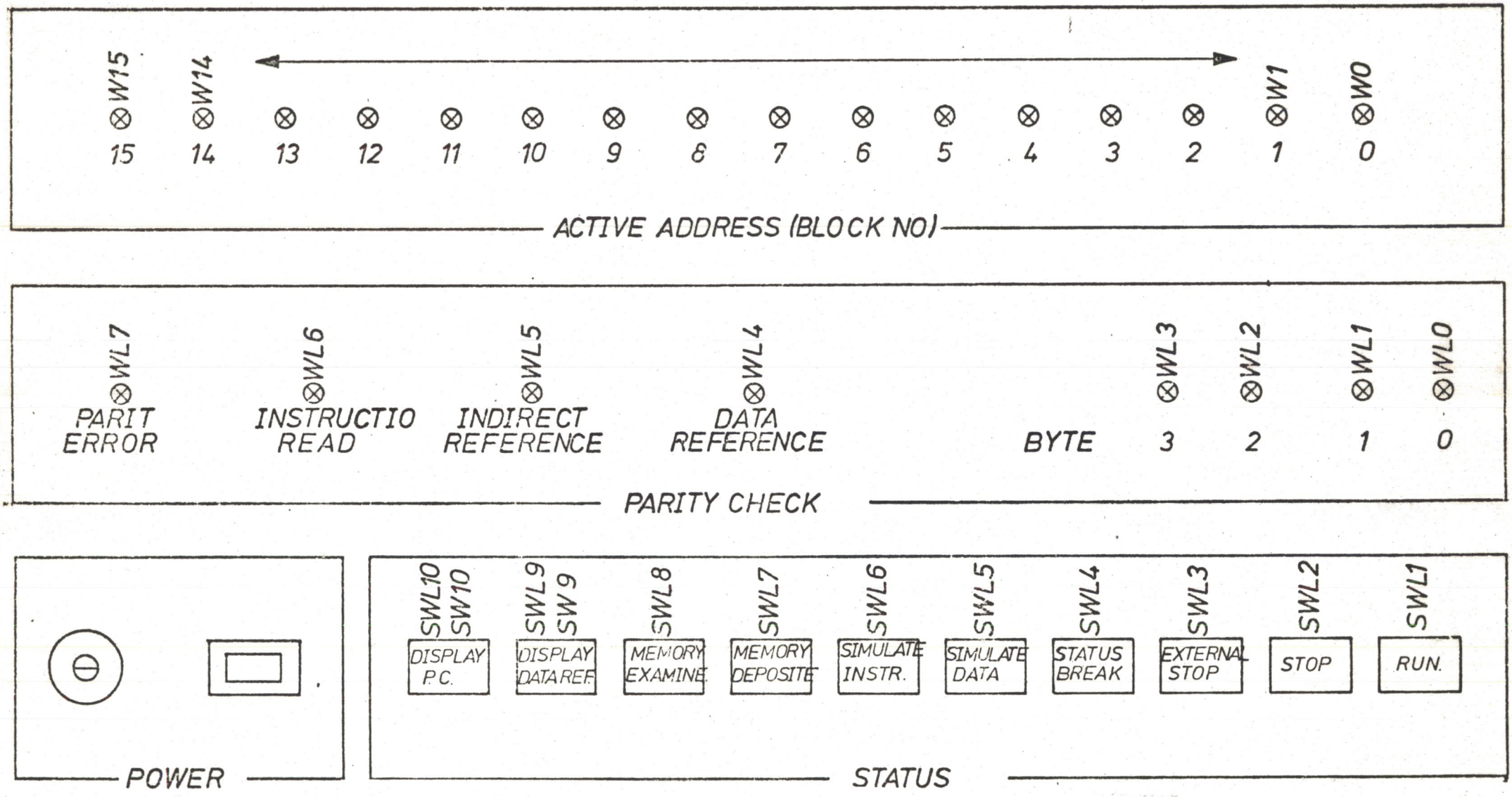
The light in the push buttons indicates which of the two (Program Counter or Data Reference) that is selected.

The eight indicator lamps in the middle of the panel are used only in case of parity error. The four lamps to the right indicate in which part of the 32 bit memory word the parity error appeared.

Byte 0 is bits 0-7, byt 1 is bits 8-15, byte 2 is bits 16-23 and byte 4 is bits 24-31.

The three next lamps indicate in what kind of reference the parity error was discovered, a Data Reference, an Indirect Reference or an Instruction Read. Note that light in the Data Reference indicator is normal with no parity error.

The leftmost indicator tells that the stop was due to a parity error.



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OPERATORPANEL NORD - 50

The two push buttons are found in the lower left corner of the panel.

In the lower right corner the run and stop conditions are visualized. If the NORD-50 is running, it is indicated by light in the RUN status, and if it is not running, it will be light in the STOP status. If the NORD-50 was stopped by external signals or internal error conditions, this will be indicated by EXTERNAL STOP respectively STATUS BREAK.

The four lamps in the middle are directly connected to the four NORD-50 modus bits M12-M15. More about those bits in the NORD-10/NORD-50 Communication System Manual.

Note: All lamps and push buttons on the panel are connected to NORD-50 I/O CONTROL 1500 in position B32.

3 COMMUNICATION SECTION

In NORD-50 are the main registers and arithmetic, the communication registers, memory address and data lines, and line drivers/receivers for external arithmetic organized on three different circuit boards, Address Arithmetic 1501, Registers 1502 and Airhtmetic Buffer 1503. A complete unit for 4 bits are formed by three boards, one of each. The 32 bit CPU thus uses eight of each board, making a total of 24. The timing and control part of the CPU uses eight different boards: N-50 I/O Control 1500, N-50 Controller 1504, Register Address 1505, Cycle Counter 1506, Arithmetic Control 1507, Chip Select 1508, Instruction Control 1510 and Timing Control 1519.

Figure 3.1 illustrates the data connection inside and between the data boards. Connections to memory, NORD-10 and external arithmetic are also indicated.

Communication between NORD-10 and NORD-50 uses 2 boards in the NORD-10 end, NORD-50 Data 1071 and Data and Address Bus Selector 1532, and 3 boards in the NORD-50 end, one Device Registers 1531 and two Data and Address Bus Selector 1532.

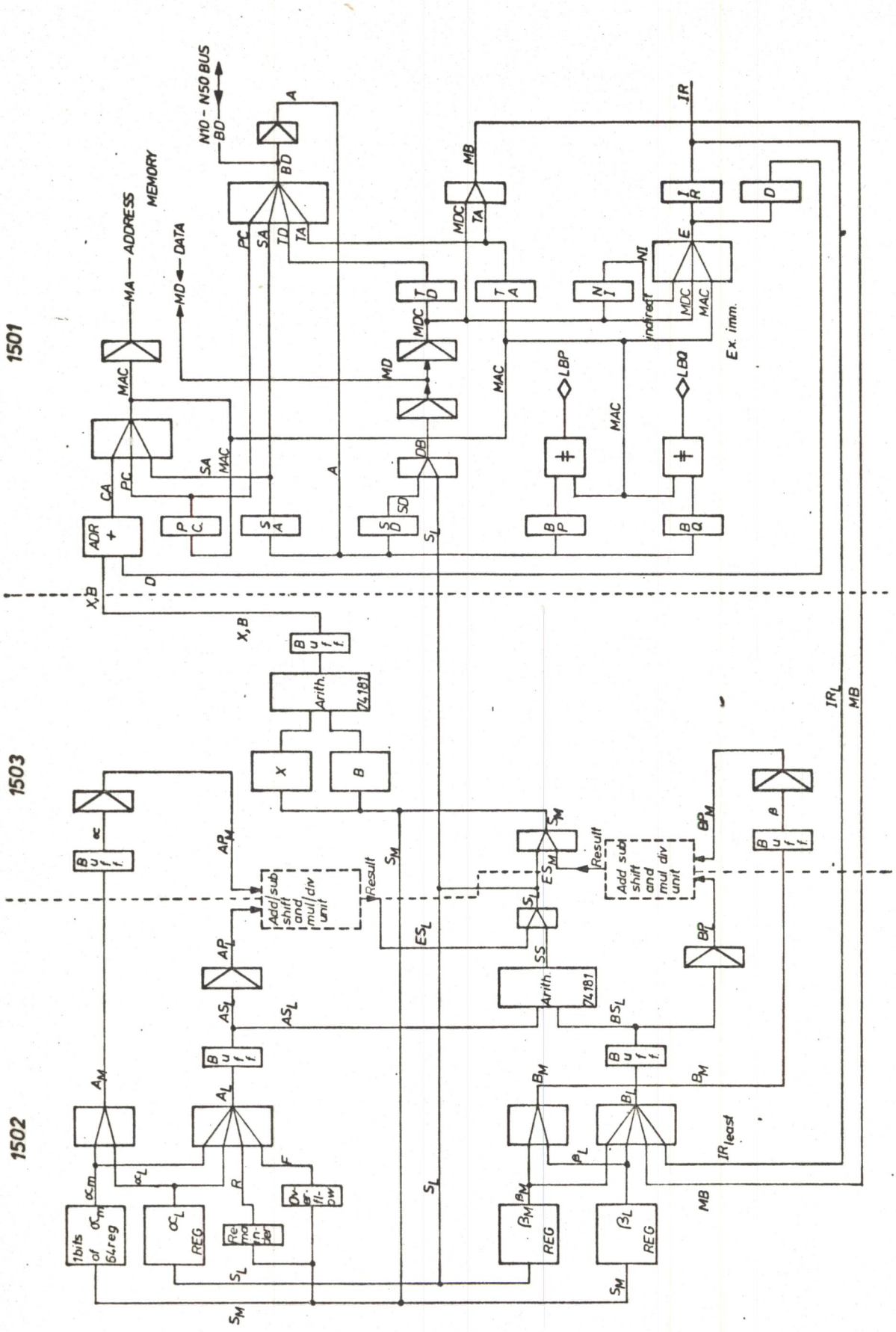


Figure 3.1

3.1 NORD-10 - NORD-50 Data Communication

NORD-10 can write into five different NORD-50 registers, and can read five different NORD-50 registers.

3.1.1 Writeable Registers

The five writeable registers are: SA (Simulated Address) (1501), SD (Simulated Data) (1501), BP (Break Point Register, Lower Limit) (1501), BQ (Break Point Register, Upper Limit) (1501) and M (NORD-50 Modus Register) (1531). The first four are 32 bits registers. All five registers are more closely described in The NORD-10/NORD-50 Communication System Manual. The first four are also described under 3.3. (The pharenthesis gives the name of the registers and the number of the printed circuit board where the registers are located.)

Writing into one of the registers is done in the following way:

1 A-register in NORD-10 is loaded with data.

2 Selected IOX-instruction is executed. Determines which register or part of register to write into.

3 Data are enabled to the differential data bus on the 1071 card together with a STR signal.

4 Six least significant bits of the NORD-10 Address Bus are constant transmitted from the 1532 card in NORD-10 to the 1532 card in pos. C26 in NORD-50 on differential lines. A line receiver on the same card is used for the STR signal (STROBE).

5 The STROBE signal is used on 1504 (B25) together with address bits 0, 1 and 5 (IOA0, IOA1 and IOA5) to determine whether it is a read or write instruction, and which part of the selected register to operate on. Address bits 3 and 4 (MAE3 and MAE4) are used on 1501 to determine which register to write into or read from.

6 IOSTR1 (1504) writes into the least significant part of SA, SD, BP or BQ.
IOSTR2 (1504) writes into the most significant part of SA, SD, BP or BQ.
LCONT (1504) writes into the Modus Register (1531).

7 Data from NORD-10 go through line receivers on 1532, position C24, to a 16 bits tri-state data bus, BD (1501, 1531 , 1532). On 1501 the data are inverted (A) and connected to SA, SD, BP and BQ registers. On 1531, ten of the bits are connected directly to the register, and the remaining six bits are buffered by an 8097.

3.1.2 Readable Registers

The readable NORD-50 registers are: PC (Program Counter) (1501), SA (Simulated Address) (1501), TA (Test Address) (1501), TD (Test Data) (1501) and NORD-50 Status Register (1531).

PC, SA, TA and TD (32 bits registers) and the Status Register are described in The NORD-10/NORD-50 Communication System Manual. The first four of them also under 3.3.

The same mechanism is used to read from a register as to write into a register, except that the tri-state data buses are used in the opposite directions.

MAE3 and MAE4 (1532, C26) select register PC, SA, TA or TD (1501). Data are enabled to BD by IORE (1504-1501) if PC, SA, TA or TD, or by RSTAT (1504) if Status Register (1531).

Data are transmitted from 1532 (C24) to NORD-10 (1071) on differential lines, enabled to the NORD-10 data bus and clocked into the A-register.

3.2 NORD-10 - NORD-50 Control

In addition to the data lines, address lines and one control line (STR) described under 3.1, two control lines are connected from NORD-10 to NORD-50, and one control line from NORD-50 to NORD-10.

The lines from NORD-10 to NORD-50 are a start line (PDEVS, DEVS) and a stop line (STOP) (1071, 1532 in C26, 1519). From NORD-50 to NORD-10 goes a completion line (DEVC, COMPL) (1519, 1071). The completion line gives NORD-10 the information that NORD-50 has stopped.

3.2.1 Start Sequence

Whe NORD-50 is started, the first instruction is fetched from the address pointed to by the SA-register (1501). Therefore this register must be loaded with the start address.

The Modus Register (M, 1531) holds information about break conditions, and must be loaded before the program is started. Therefore the start sequence can be

1 Load SA-register with start address
2 Load M-register with running and break condition
3 Activate NORD-50

or the same with 1 and 2 swapped.

Points 1 and 2 are described in the NORD-10/NORD-50 Communication System Manual.

The meaning of the different status and control bits concerning point 3 is also described in the same manual (2.2.1.2).

Note that it is possible to start NORD-50 with the activate bit (bit 2), and enable interrupt (bit 0) later on.

The activate bit will cause a start pulse (PDEVS, 1071) if the interface expects NORD-50 not to be running, but will have no influence if it expects NORD-50 to be running. A PEDVS will put the RUN flip-flop in 1-state (RFT=0). This state can be cleared by a completion pulse (COMPL-1071, DEVC-1519) from NORD-50 or by a Device Clear - Master Clear (CL-1071) form NORD-10.

3.2.2 Stop Sequences

NORD-50 can be stopped due to internal or external condition. Internal conditions are STOP instruction or status breaks. External condition is stop command.

3.2.2.1 External Stop

Stop command is given by executing IOX WI C50 with A-register bit 4 equal 1 in NORD-10. This will cause NORD-50 to stop after the instruction it is executing. If the same program should be started again at the point it was stopped, start address must be PC-1 (due to instruction prefetch).

Master Clear command can never be given if the interface expects NORD-50 to be running. If a Master Clear command is wanted while NORD-50 is running, a STOP command must be given first.

3.2.2.2 STOP Instruction

Internal stop conditions are first of all a STOP instruction. When a STOP instruction is decoded, the CPL (1519) signal will be set at time of received address ready. Together with NEXT (1506) this will give NC7 (1519), which brings NORD-50 to cycle 7, the stop-cycle.

3.2.2.3 Instruction Hang-up

The same mechanism as for STOP instruction is used for stopping NORD-50 in instruction hang-up (CNT15-1510), examine/deposit (dEXDEP-1519) and external stop (XSTOP-1532, C26). Instruction hang-up may be due to more than 16 levels of indirect addressing or EXECUTE instruction.

3.2.2.4 Overflow and Underflow

Overflow and underflow errors are only due to external arithmetic operation, and can occur at the time of ready signal from external arithmetic (RYX-1504). This is always at the end of one instruction (except from skip) and will set CPL (1519) directly (DER-1504).

Note: Corresponding modus bit must be set (M0 and M1).

3.2.2.5 Parity Error

SB7 (1504) will also set CPL (1519) directly. However, it is not obvious that the next memory request (RQ-1519) will be stopped because of the short timing between DR (1519) and RQ (1519), and the delay from DRL (1500).to PYS (1504). PYS (1504) is the "parity check window".

Parity is checked only if modus bit 2 is set. (M2).

3.2.2.6 Request Outside Memory

The last possibility for internal stop condition in NORD-50 is request outside memory. This will cause a PMHUP (1519) and the setting of SB8 (1519). It will also cause a DEVC (1519) pulse to NORD-10.

NORD-50 will be in a hanging condition, and must be given a Master Clear command. TA (1501) will hold the address that caused the hang-up.

3.2.3 NORD-10 Interrupts

If the interrupt enable flip-flop is set (RFTIE-1071), any completion will cause an interrupt on level 12 in NORD-10. The Ident code is 16_8, and the interrupt and interrupt enable flip-flop are cleared by a serviced ident.

3.3 Communication Registers

There are seven communication registers. All of them are located at the 1501 card. SA is readable and writeable. SD, BP and BQ are writeable. PC, TA and TD are readable.

SA: Start address or memory address in EXAMINE/DEPOSIT operations.

SD: Simulated data, used as memory buffer register when NORD-10 simulates main memory in NORD-50 or data input register in DEPOSIT operation.

BP: Break point register, lower limit. (See 3.4)

BQ: Break point register, upper limit. (See 3.4)

PC: NORD-50 program counter. This register will usually hold the address of the next instruction to be fetched. This means that the executed instruction will usually be PC-1 in cycle C0 and PC-2 in other cycles, due to instruction prefetch. PC is incremented by PCC00 (1510). It is loaded by MAS3 (1506).

TA: Test Address register holds the address for the last memory request or the address for a trapped request in case of address violation. Clocked by TAS1 (1510).

TD: Test Data register holds the information on the bi-directional memory data bus. It is clocked at the start and at the end of the request by TDS1 (1510).

3.4 Protect System

The memory address lines, MAC (20 bits) (1501) are constantly compared to the contents of BP and BQ registers. The results of these comparisons, LBP20 and LBQ20, are used on 1504. LBP20 means that the effective address is less than BP, and LBQ20 means that the effective address is less than BQ.

To compare the address to BP and BQ takes time (approx. 90 nsec.), and the PROT signal (1504) is therefore used to delay WP and RQ (1519) for the specified protected memory references with 100 nsec.

If M4 is set, all memory references will be protected, which means that all cycles will be delayed. M5 will delay instruction fetch (M5 and MAE5, 1504), M6 will delay data references (M6 and MAE5, 1504) and M7 will delay data store references (M7, MAE5 and WRP, 1504). M8 is used to select the addresses between BP and BQ as protected, or the addresses less than BP and greater than BQ as protected. If M8=0, the addresses from BP to BQ-1 will be protected. If M8=1, the addresses from 0 to BP-1 and the addresses from BQ and up will be protected.

If an address for a protected memory reference is within the protected area, ABPBQ (1504) will make RQE=0 (1519), which stops the RQ, brings NORD-50 to DC7 (NC7, 1519) and sets status bit 1 (SB1, 1504). A completion (DEVC, 1519) is sent to NORD-10 as response to DC7.

4 NORD-50 CONTROL SECTION

The following paragraphs describe the main control functions and sequences of operation for the different classes of instructions in NORD-50.

4.1 Basic Machine Cycles

The basic machine cycles in NORD-50 are:

DC 0 — Instruction readout, and in the case of a single memory reference instruction also instruction execution.

DC 1 — Indirect address cycle.

DC 2 — Instruction execution.

DC 3 — Instruction execution, second part, for instruction with two data references in core memory.

DC 4 — Instruction readout to the Next Instruction register (NI) in start sequence, in skip instruction effective or jump instruction effective.

DC 7 — Stop cycle. Data may be transferred to/from NORD-50 communication registers via the NORD-10 I/O system.

To describe the sequences of operations the program below is used as an example.

```
10 /    LDR 3, 20                    % 3000 ⟶ Reg.no.3
        STOP
        COMMUNICATION INFO

20 /    3000
```

The program above is entered by placing 10 in the SA-register and proper mode information in M-register using IOX instructions in NORD-10 and then executing the instruction

```
IOX WIC50
```

with the proper control information in the A-register.

The sequence of cycles for the program above will be

DC 7

DC 4 Read (10) = LDR to NI

DC 0 Transfer (NI) to IR and execute
Read (11) = STOP to NI

DC 2 Read (20) = 3000 to register no. 3

DC 0 Transfer (NI) = STOP to IR and execute
Read (12) to NI

The STOP instruction is used as completion signal to NORD-10. Note that the dataword last read from memory is always placed in the TD-register. This register, which after a STOP instruction has the same content as the location following the STOP instruction. The possible cycle transitions are shown in figure 4.1. Summary of cycle switching conditions.

DC 0 to 1 All instructions except EXC or operation code 0 when indirect address bit (IR31) is 1. Note: Indirect address is not permitted on EXC.

DC 0 to 2 All instructions not having operating code 0 when indirect address bit (IR31) is 0.

DC 0 to 4 Jump instruction effective or skip instruction effective.

DC 0 to 7 Stop instruction.

DC 1 to 0 None of the other conditions for DC 1 true.

DC 1 to 1 Indirect address bit is 1, (with "timeout" at level 16).

DC 1 to 2 Indirect address bit is 0.

DC 1 to 4 Jump indirect instruction effective.

DC 2 to 0 None of the other conditions for DC 2 are true.

DC 2 to 3 All the following instructions: XMW, ADM, MIN, LDF, STF, FAD, FSB, FMU or FDV.

DC 2 to 4 Compare skip effective.

DC 3 to 0 None of the other conditions for DC 3 are true.

DC 3 to 4 The result of the MIN instruction becomes zero.

DC 4 to 0 DC 4 always continues with DC 0.

DC 7 to 4 The instruction IOT ACT N5 is executed in NORD-10 and the mode is not supposed to be EXAMINE or DEPOSIT.

In addition to the switching conditions listed above any cycle may return to DC 7 if a hardware error is detected.

The cycle counter flip-flops and decoding of conditions above are found on CYCLE COUNTER 1506.

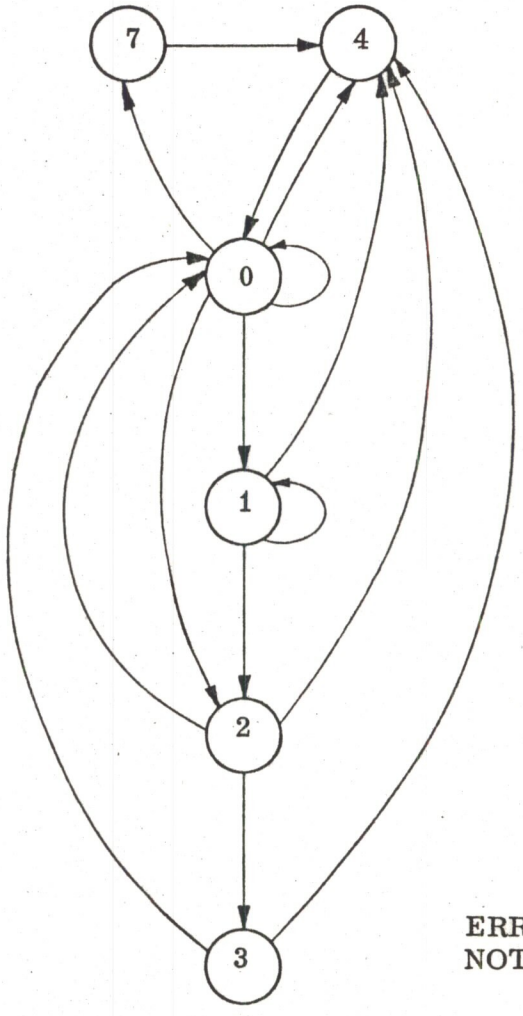


Figure 4.1 Main Cycle Switching

5 TIMING SEQUENCES

The description of timing system and sequences of operation will be given as examples of the various types of instructions. Also, cycles and timing diagrams are given for all instructions.

The different groups of instructions are:

1 Interregister and skip
2 Memory load/store
3 Jump
4 Argument (direct)
5 Memory replace
6 Execute

5.1 Interregister and Skip Instructions

Much of the design philosophy of NORD-50 has been determined by the interregister instruction. This instruction is a three-address instruction with a separate address for operand A, operand B and destination register. As all other instructions in NORD-50 all 64 registers are equal, i.e. all addresses are 6 bits. The only difference between skip and operate instructions are that the skip instruction in addition to do the specified operation tests the result and skips next instruction to the program sequence depending upon result and skip condition. If no operation except the skip test is wanted the destination address should be zero.

The interregister instructions have two different phases, register READ and register WRITE. The main timing signals are shown in figure 5.1.

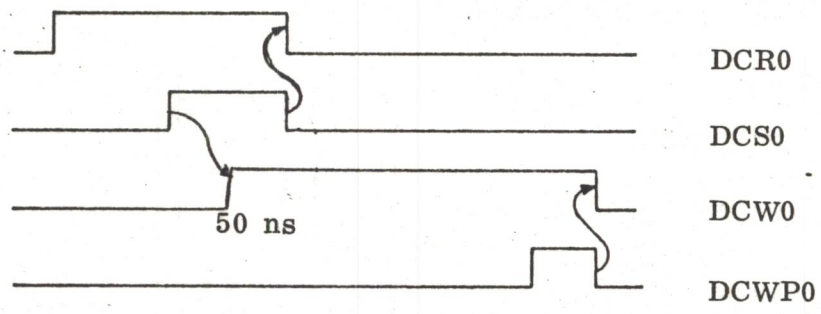


Figure 5.1 Register READ/WRITE timing

In the READ phase the register address to register block A and B respectively (see figure 3.1) are taken from the source address fields of the instructions. The output of the registers is strobed into latches (STRA1, STRB1) and the address is changed to destination address for both register blocks. At the register WRITE PULSE new information is written into both register blocks simultanously.

In parallell with the instruction execution next instruction is read from core memory. The timing of control signals between memory control unit and central processor is shown in figure 5.2.

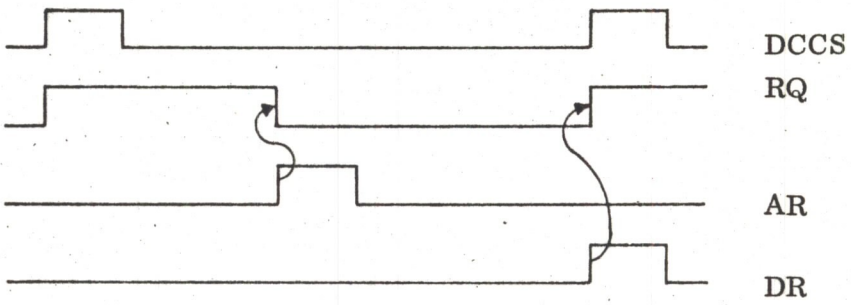


Figure 5.2 Memory Control Signals

Interregister instructions with 64 bit operands are organized to permit readout of two registers in parallell from each register block. Each register block has 64 latches which may be strobed in parallell (STRA1, STRA2, STRB1, STRB2). The organization of the registers in one block is shown in figure 5.3.

For all floating point instructions, fixed point multiply/divide, shift and bit instructions the execution of the instruction is in the "external" arithmetic. These operations have different execution times and the timing is determined by the "external" arithmetic timing control as shown in figure 5.4.

After strobing the register output into the latches the external arithmetic START signal is turned on (example SFMU). When the result is ready the external control unit returns a ready signal (RYXi) which triggers the register write pulse. For double precision (64 bits) the result is written into all 64 bits simultanously.

The only difference between interregister operation and skip instruction is the next cycle, which is DC 4 for skip effective.

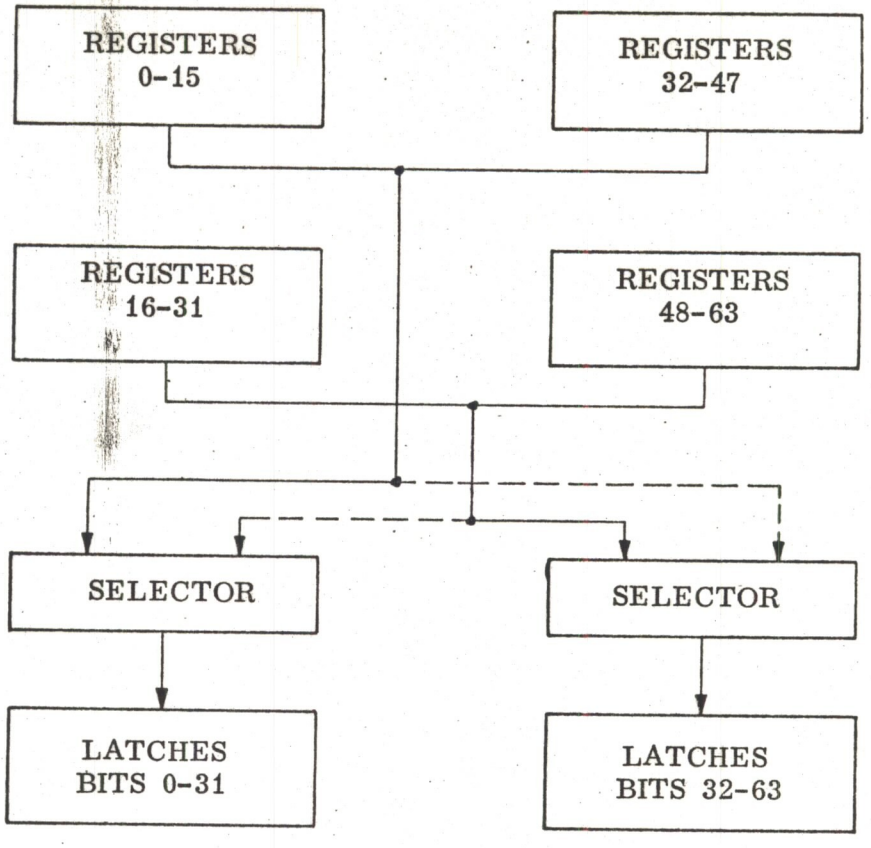


Figure 5.3

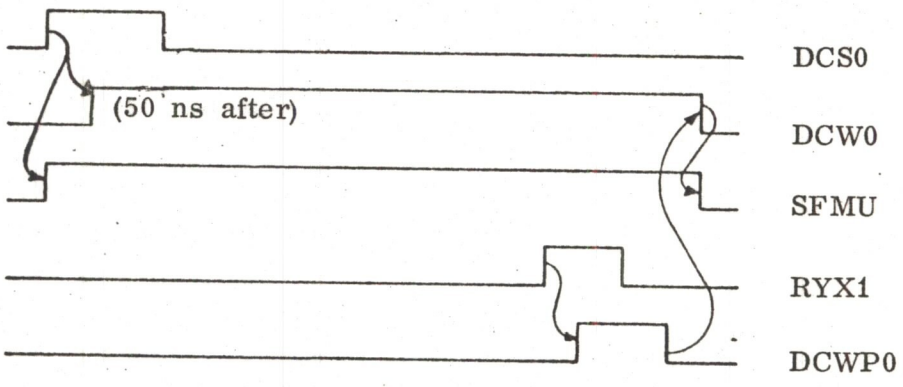


Figure 5.4 External Arithmetic Timing

5.2 Memory Load/Store

The group of instructions also includes ADD, SUB, AND and MEMORY COMPARE SKIP. Only the output of register block A is used in the operation, and the latches in register block B is used for temporary storage of the output from core memory. The data from memory enters the arithmetic via the B-bus.

The information from the A-block is read the same way as in interregister instructions in cycle DC 0. The WRITE phase of DC 2 is triggered by DATA READY (DR) as shown in figure 5.5.

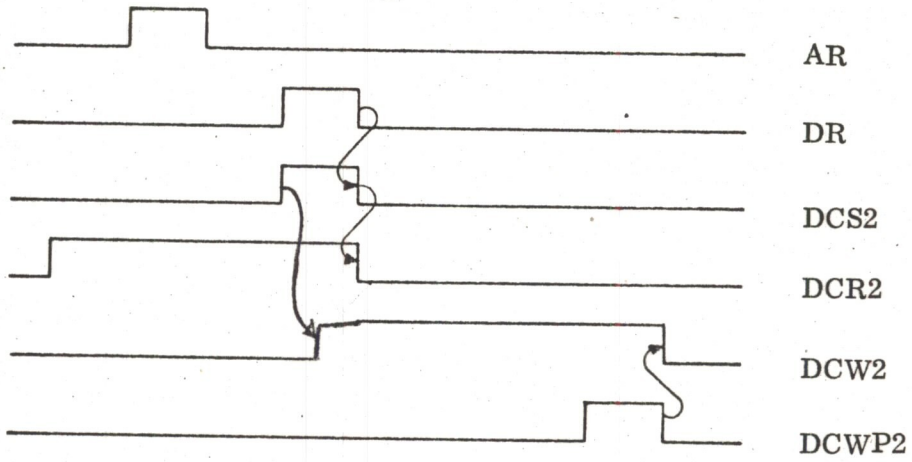


Figure 5.5. Register WRITE phase in LOAD

In the case of indirect addressing DC 1 is "inserted" between DC 0 and DC 2. The timing of DC 1 is the same as for DC 2, with register WRITE phase being triggered by DR, in this case used to compute the new memory address.

5.3 Jump Instructions

The timing of jump instructions is the same as for DC 0 of the load/store group. The next cycle depends upon the jump condition being fulfilled. If a jump is actually taking place the next cycle will be DC 4 for readout of next instruction.

Note that during the execution of the jump instruction the next instruction following immediately after the jump instruction will always be read into the NI register in DC 0.

5.4 Argument Instructions

The argument instruction uses the output from register block A as one operand. The argument itself, is transferred from the Instruction Register via the data selector of the 1502 cards (IR, RG) to the latches of register block B. The rest of the operation is identical to the interregister instructions.

5.5 Memory Replace Instructions

The memory replace instructions are the ADM, XMR and MIN instructions. These instructions have a memory READ and a memory WRITE in the same instruction.

5.6 Execute Instruction

Both the EXECUTE and the EXECUTE IMMEDIATE instructions have exceptions from normal cycles which are best described by complete timing diagrams.

5.6.1 Normal Execute

The timing diagram used to describe the execute instruction is for the following sequence:

11 / EXC 305

The numbers in the RQ (Memory Request) denotes the address being read at that request. (See Timing and Timing Diagram, 5.8.)

While the effective address of EXC instruction was calculated the next instruction was read from memory but not placed in the NI-register (NIS, 1510). Instead, the instruction in the effective address (CA) is read and placed directly in IR. While this instruction is decoded, the next instruction is read once more and this time placed in the NI-register.

5.6.2 Execute Immediate

The timing sequence in the execute immediate instruction is not identical to the other execute instruction. Instead of making a request with the calculated address (CA), a simulated memory cycle is started (ENIS=0, 1519) and CA is clocked directly into IR. (MAC →E →IR, 1501). Since no memory request is made, the memory data lines will still hold the last requested information, which is the next instruction. Therefore this is clocked into NI-register due to Data Ready of the simulated memory cycle. (DRS, 1509).

5.7 Instructions and Cycles

The list below contains the NORD-50 instructions, and which cycles each instruction uses.

The WRITE column indicates the cycles where information is written to memory.

EXT means that external arithmetic is used.

Cycles dependant on test conditions (SKIP-JUMP) are marked with pharenthesis. The same is done with cycles dependant on double precision, where both single and double precision have meanings.

Indirect address cycle is treated separately at the end of the list.

NORD-50 INSTRUCTIONS AND THEIR CYCLES

	Instruction:	Cycle:	WRITE Cycle:	Comments:
	START	7 - 4 → 0		
	STOP	0 → 7		
	RIO	0 → 0		
	SHR	0 - EXT → 0		
	SHD	0 - EXT → 0		
	BST	0 - EXT → 0		
	BCM	0 - EXT → 0		
	BCL	0 - EXT → 0		
	BSZ	0 - EXT (- 4) → 0		Cycle 4 if SKIP
0	BSO	0 - EXT (- 4) → 0		Cycle 4 if SKIP
	FIX	0 - EXT → 0		
	FLO	0 - EXT → 0		
	LRO	0 → 0		
	IRO	0 (- EXT) → 0		EXT if MPY or DIV
	FRO	0 - EXT → 0		
	IRS	0 (- 4) → 0		Cycle 4 if SKIP
	FRS	0 - EXT (- 4) → 0		Cycle 4 if SKIP
	RTJ	0 - 4 → 0		
	EXC	0 - 0 → 0		
	EXC IM	0 - 0ǂ → 0		0ǂ: Special cycle with no Memory Request
	MIN	0 - 2 - 3 (- 4) → 0	3	Cycle 4 if SKIP
	CRG	0 - 2 (- 4) → 0		Cycle 4 if SKIP
1	CRL	0 - 2 (- 4) → 0		Cycle 4 if SKIP
	CRE	0 - 2 (- 4) → 0		Cycle 4 if SKIP
	CRD	0 - 2 (- 4) → 0		Cycle 4 if SKIP
	JRP	0 (- 4) → 0		Cycle 4 if JUMP
2	JRN	0 (- 4) → 0		Cycle 4 if JUMP
	JRZ	0 (- 4) → 0		Cycle 4 if JUMP
	JRF	0 (- 4) → 0		Cycle 4 if JUMP

	Instruction:		Cycle:	WRITE Cycle:	Comments:
	JPM		0 (- 4) → 0		Cycle 4 if JUMP
3	JNM	arith.	0 (- 4) → 0		Cycle 4 if JUMP
	JZM		0 (- 4) → 0		Cycle 4 if JUMP
	JFM		0 (- 4) → 0		Cycle 4 if JUMP
	ADD		0 - 2 → 0		
4	SUB		0 - 2 → 0		
	AND		0 - 2 → 0		
	LDR		0 - 2 → 0		
	ADM		0 - 2 - 3 → 0	3	
5	XMR		0 - 2 - 3 → 0	3	
	STR		0 - 2 → 0	2	
	MPY		0 - 2 - EXT → 0		
6	DIV		0 - 2 - EXT → 0		
	LDD		0 - 2 - 3 → 0		
	STD		0 - 2 - 3 → 0	2-3	
	FAD		0 - 2 (- 3) - EXT → 0		Cycle 3 if Double precision
7	FSB		0 - 2 (- 3) - EXT → 0		Cycle 3 if Double precision
	FMU		0 - 2 (- 3) - EXT → 0		Cycle 3 if Double precision
	FDV		0 - 2 (- 3) - EXT → 0		Cycle 3 if Double precision
	DLR		0 → 0		
0	DAR		0 → 0		
	DSK		0 (- 4) → 0		Cycle 4 if SKIP
	IND. ADDR.		0 - 1 -		Write phase triggered by DR Compute new address. I, X, B and D are changed at the end of the indirect cycle. (DC1 · DR). Displacement in DC1 is 20 bits.

5.8 Timing and Timing Diagrams

Most of the timing signals used in NORD-50 are generated on TIMING CONTROL 1519. Typical timing unit is 100 nsec., which is mapped as approx. 1 cm on the timing diagrams. The timing diagrams take no notice of gate delay time, and therefore some signals may differ with 50 nsec. and even more from the timebase to which they are referred.

As an example, WP is generated some gate delays after received Data Ready, and the RQ (Memory Request) is generated 2 gate delays after WP.

The main rules are:

1 SP is generated 200 nsec. after IRS (DDCCS) or at DR (WRAR).

2 WP is generated 100 nsec. after AR if NOT PROTECT.

3 WP is generated 200 nsec. after AR if PROTECT.

4 WP is generated 100 nsec. after SP if NOT PROTECT or COND. JUMP.

5 WP is generated 200 nsec. after SP if PROTECT exclusive or COND. JUMP.

6 WP is generated 300 nsec. after SP if PROTECT and COND. JUMP.

7 WP is generated at RYX time if external arithmetic is used.

8 WP is generated 200 nsec. after SP in Indirect cycle if NOT PROTECT.

9 WP is generated 300 nsec. after SP in Indirect cycle if PROTECT.

10 WP is never generated before DR (Data Ready) is received.

11 MAH1 is generated 150 nsec. after SP in Indirect cycle.

If a signal is dependant on two or more conditions, the latest of these will determine the timing.

The timing is dependant on the memory access time and the protect system. The timing diagrams are made for an access time of 500 nsec. for read and 400 nsec. for write. Some of the diagrams are made for the timing with the protect system on, but most of them are not.

The timing diagrams are:

	Instruction	Cycles	Protect
1	Start sequence	DC7 - DC4 → DC0	No
2	Stop instruction	DC0 → DC7	
3	RIO, LRO, IRO, IRS, ARG	DC0 → DC0	No
4	IRO (MPY + DIV)	DC0 - EXT → DC0	No
5	Shift, Bit, Convert, Compare	DC0 - EXT → DC0	No
6	IRS, RTJ and DSK	DC0 - DC4 → DC0	No
7	Bit and compare with SKIP	DC0 - EXT - DC4 → DC0	No
8	Execute	DC0 - DC0 → DC0	No
9	Execute immediate	DC0 - DC0*	No
10	MIN (with SKIP)	DC0 - DC2 - DC3 (-DC4) → DC0	No
11	Instr. group 1 (with SKIP)	DC0 - DC2 (-DC4) → DC0	No
12	Instr. group 2 and 3	DC0 - (-DC4) → DC0	No
13	Instr. group 4	DC0 - DC2 → DC0	No
14	Instr. group 4	DC0 - DC2 → DC0	Yes
15	ADM and XMR	DC0 - DC2 - DC3 → DC0	No
16	LDD	DC0 - DC2 - DC3 → DC0	No
17	STR	DC0 - DC2 → DC0	No
18	STD	DC0 - DC2 - DC3 → DC0	Yes
19	MPY and DIV	DC0 - DC2 - EXT → DC0	No
20	Instr. group 7 (single)	DC0 - DC2 - EXT → DC0	No
21	Instr. group 7 (double)	DC0 - DC2 - DC3 - EXT → DC0	Yes
22	Indirect Address	DC0 - DC1 - X	No
23	Indirect Address	DC0 - DC1 - X	Yes

Notes:

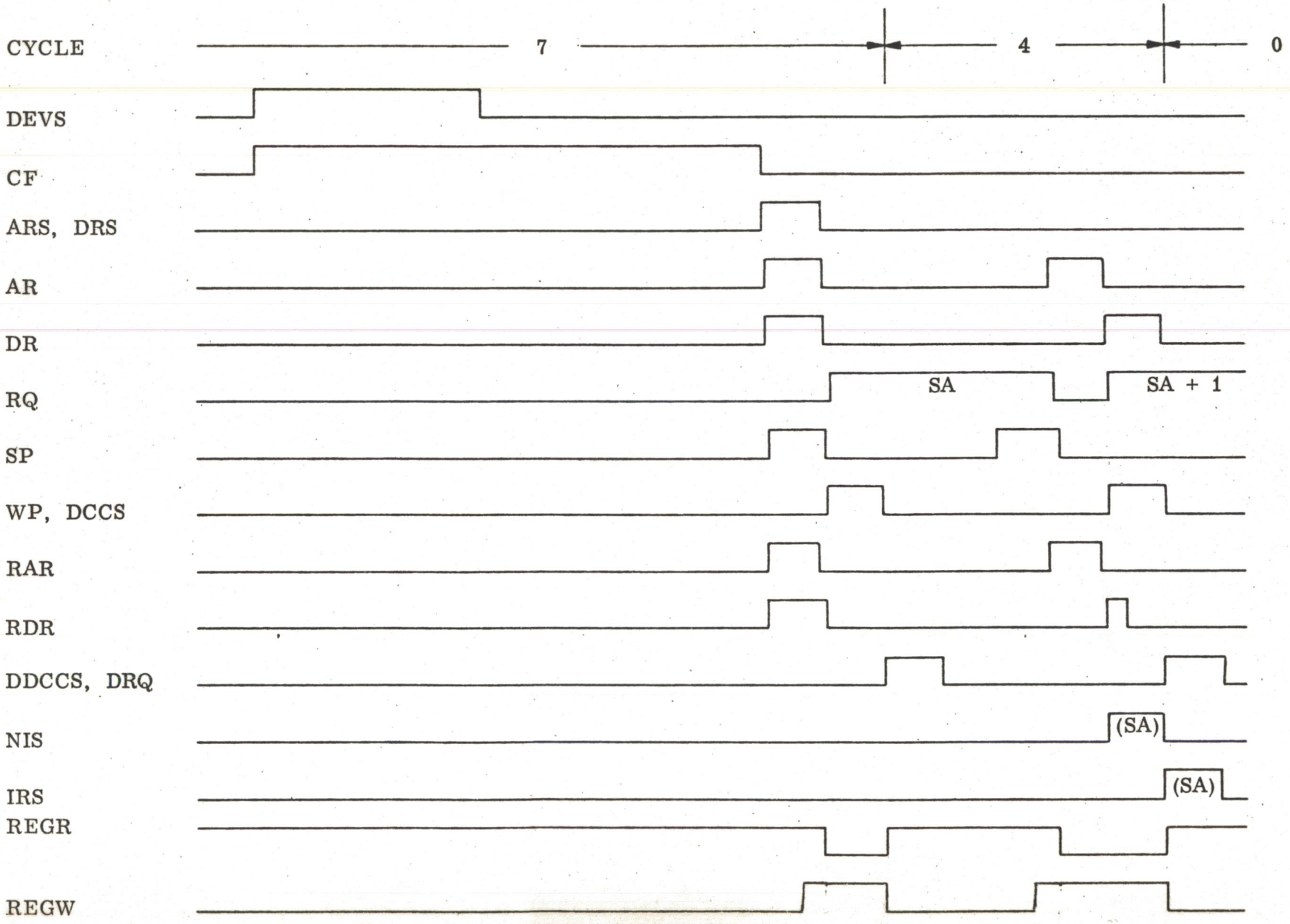
1 Most of the signal names are found in the signal definition list.

2 REGW as used internal on 1519 to generate DCWx is generated at the start of SP, external REGW at the end of SP.

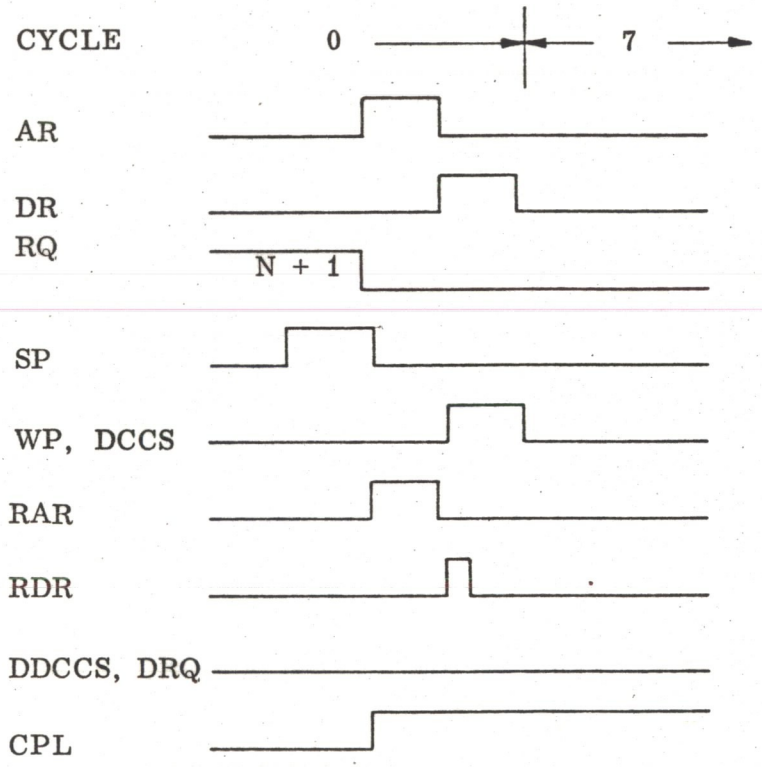
3 RAR and RDR are flip-flops remembering that Address Ready (AR) and Data Ready (DR) are received.

4 If NORD-50 is stopped due to external stop or status condition, the instruction being executed will be finished as normal, and the next cycle will be DC7.

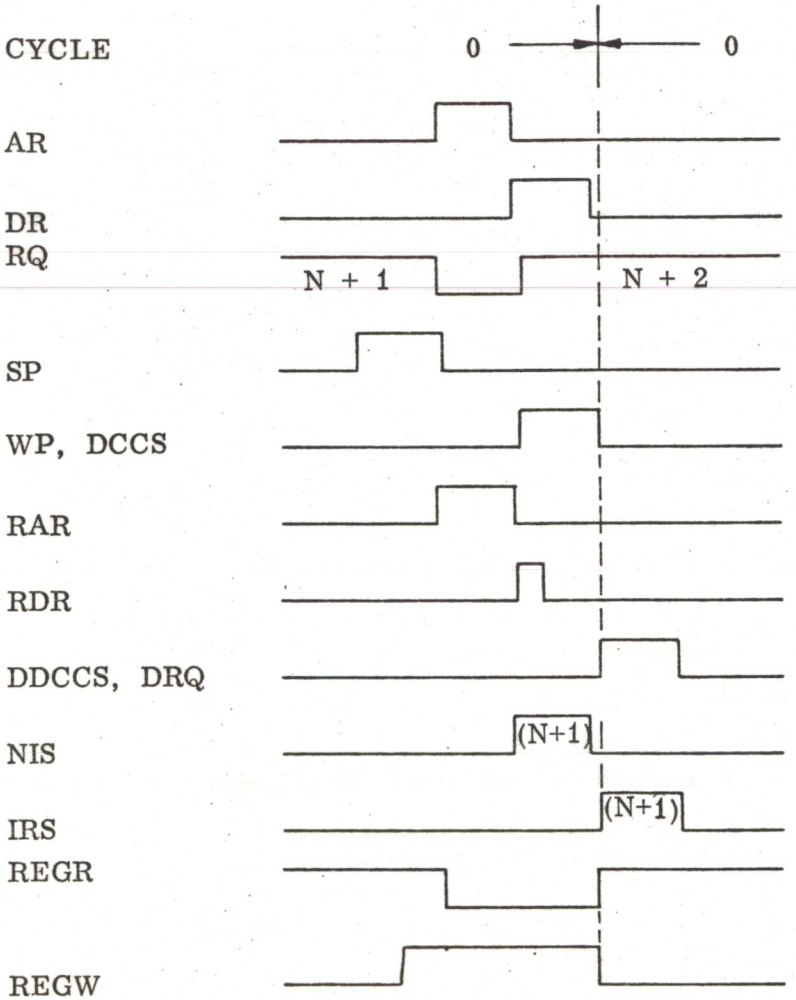
TIMING FOR START SEQUENCE: DC7 - DC4 →DC0
(WITHOUT PROTECT)



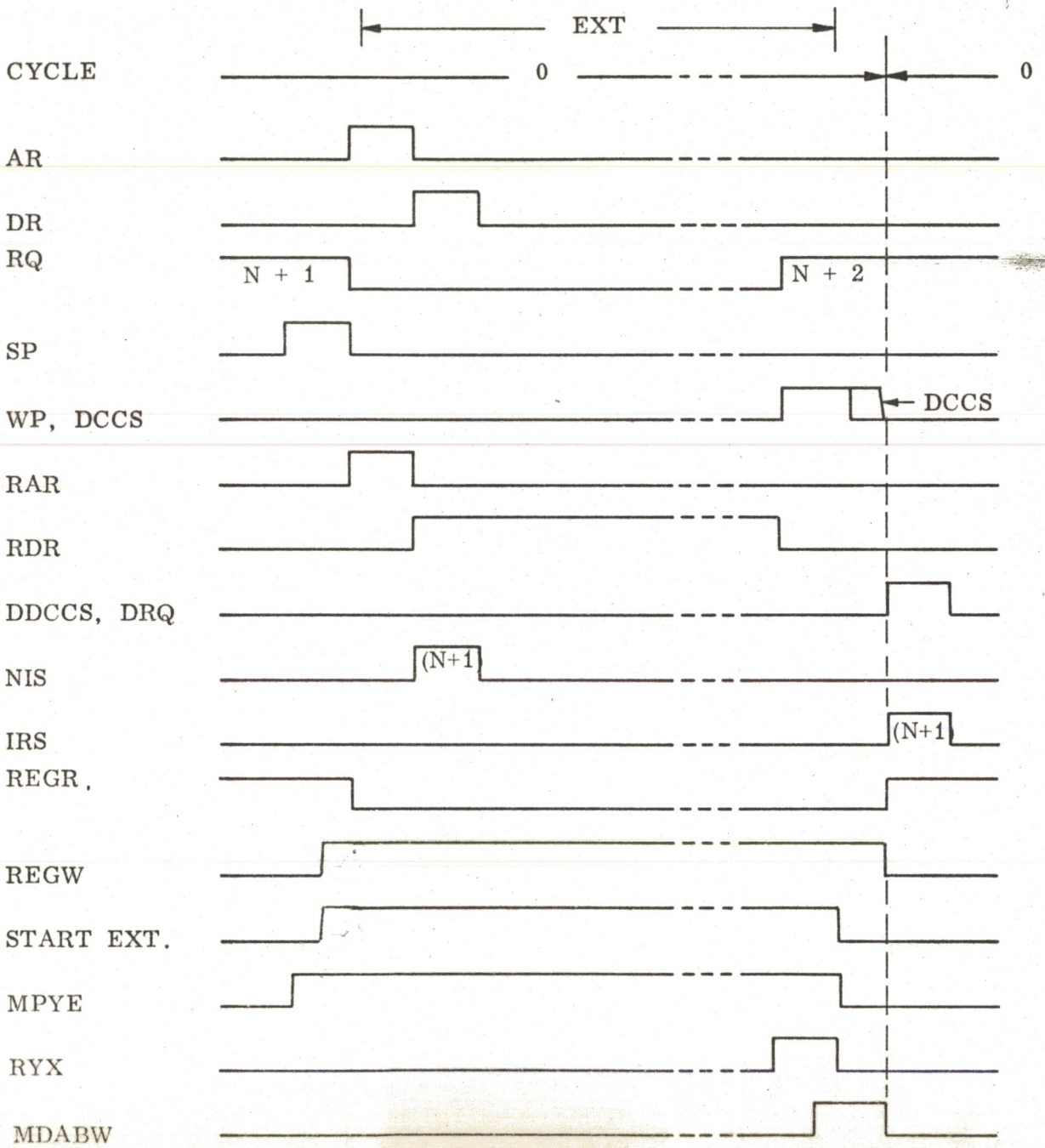
TIMING FOR STOP INSTRUCTION: DC0 - DC7



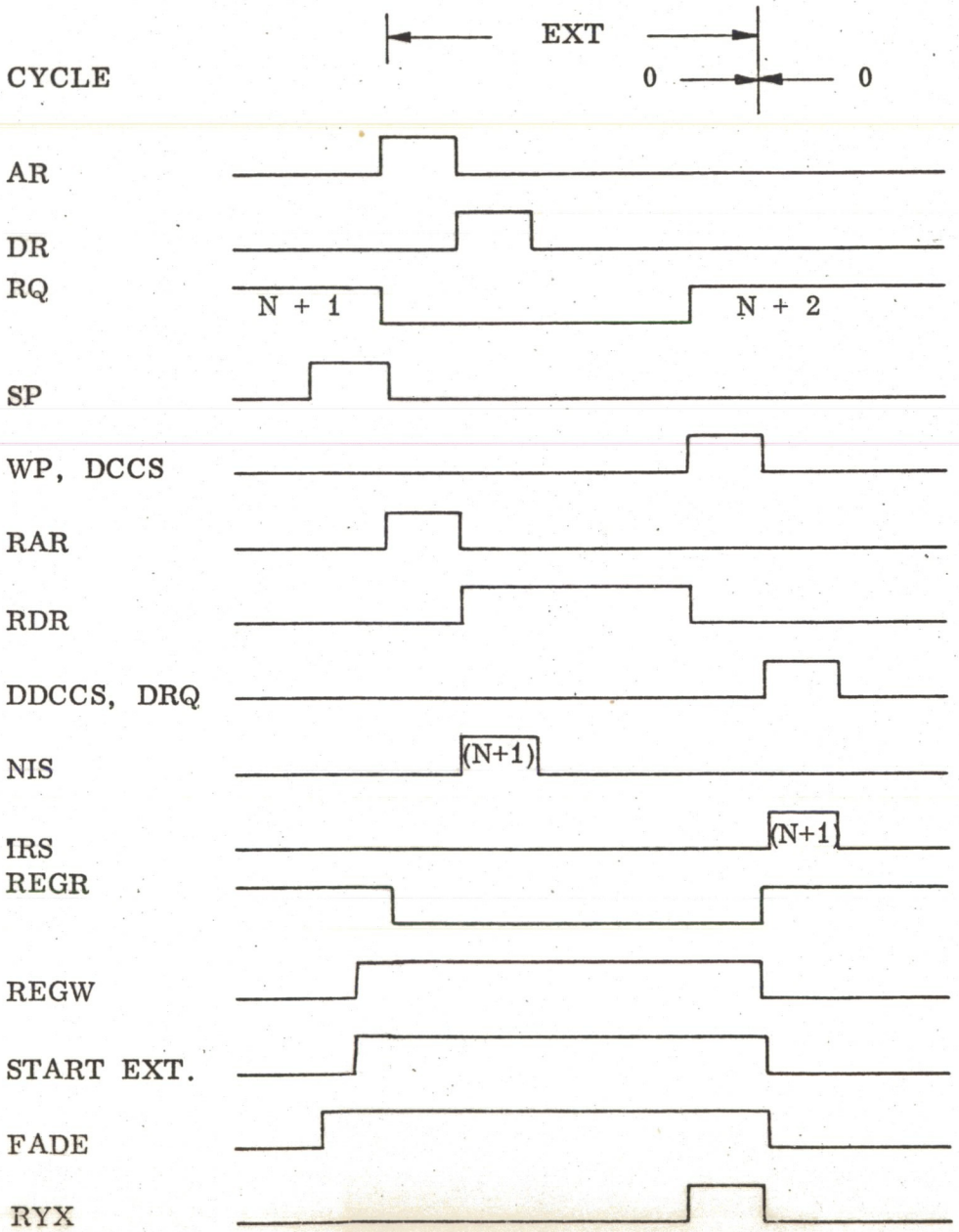
TIMING FOR RIO, LRO, IRO (EX MPY - DIV), IRS (WITHOUT SKIP), DLR, DAR and DSK (WITHOUT SKIP).
DC0 - DC0. (WITHOUT PROTECT)



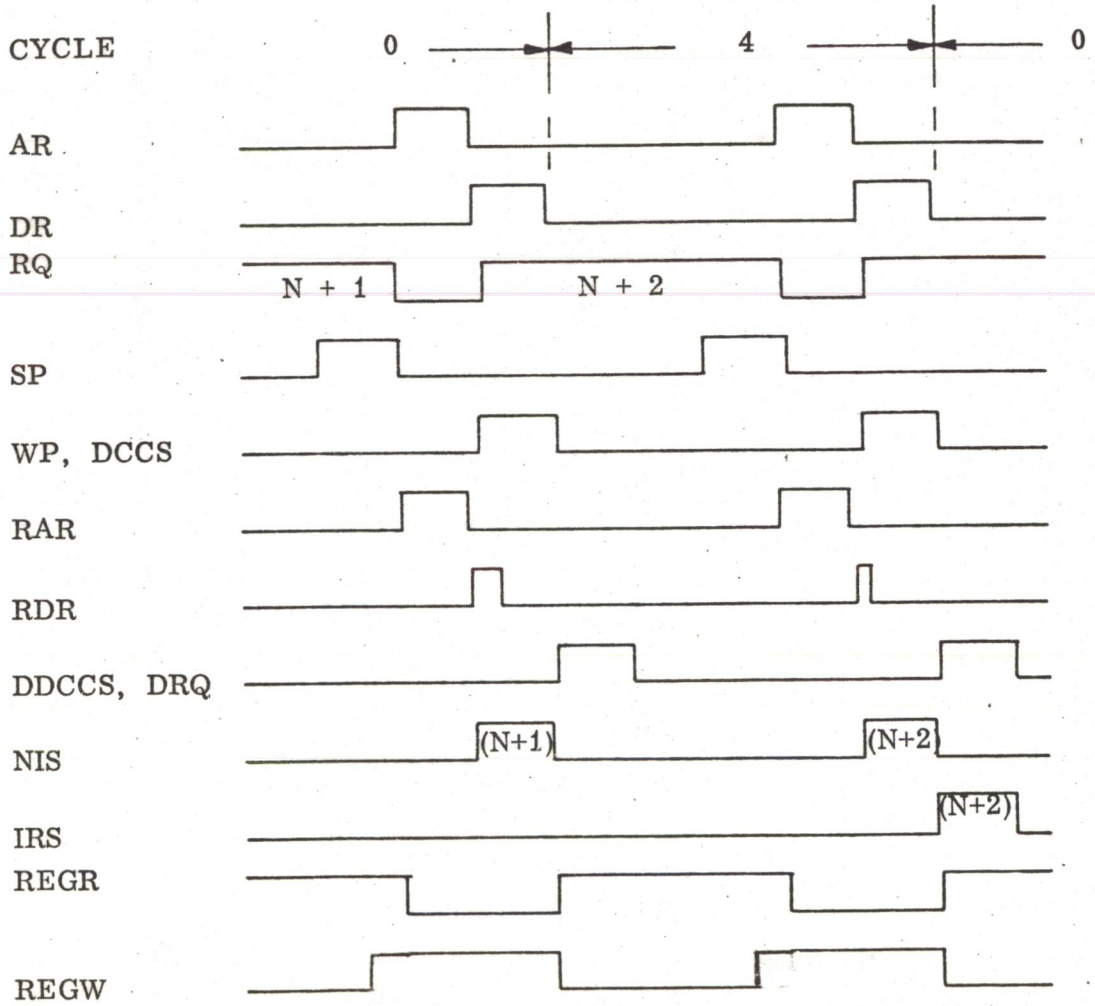
TIMING FOR IRO (MPY AND DIV) DC0 - EXT - DC0
(WITHOUT PROTECT)



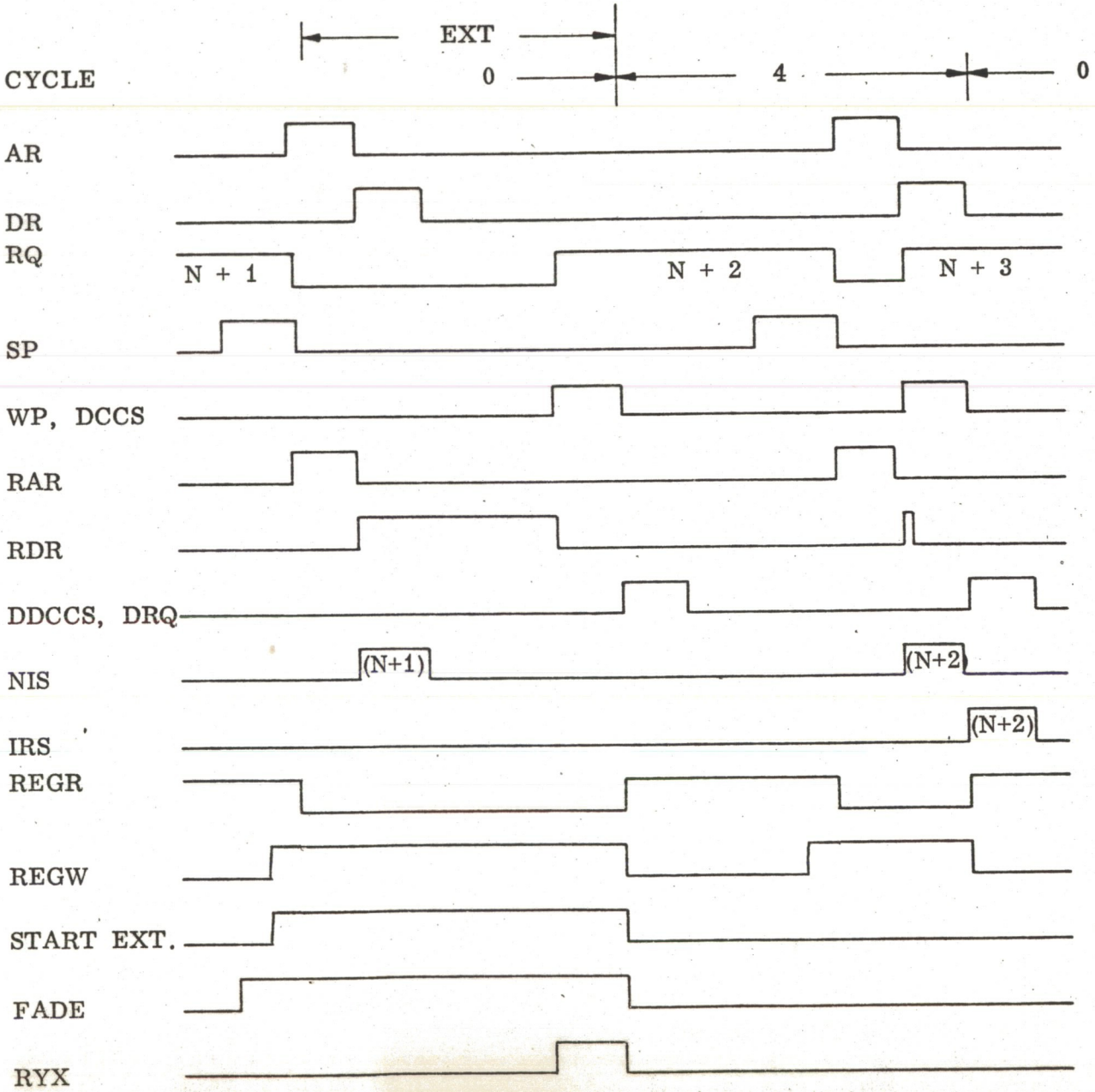
TIMING FOR SHR, SHD, BST, BCM, BCL, BSZ AND BSO (WITHOUT SKIP), FIX, FLO AND FRS (WITHOUT SKIP).
(WITHOUT PROTECT) DC0 - EXT - DC0



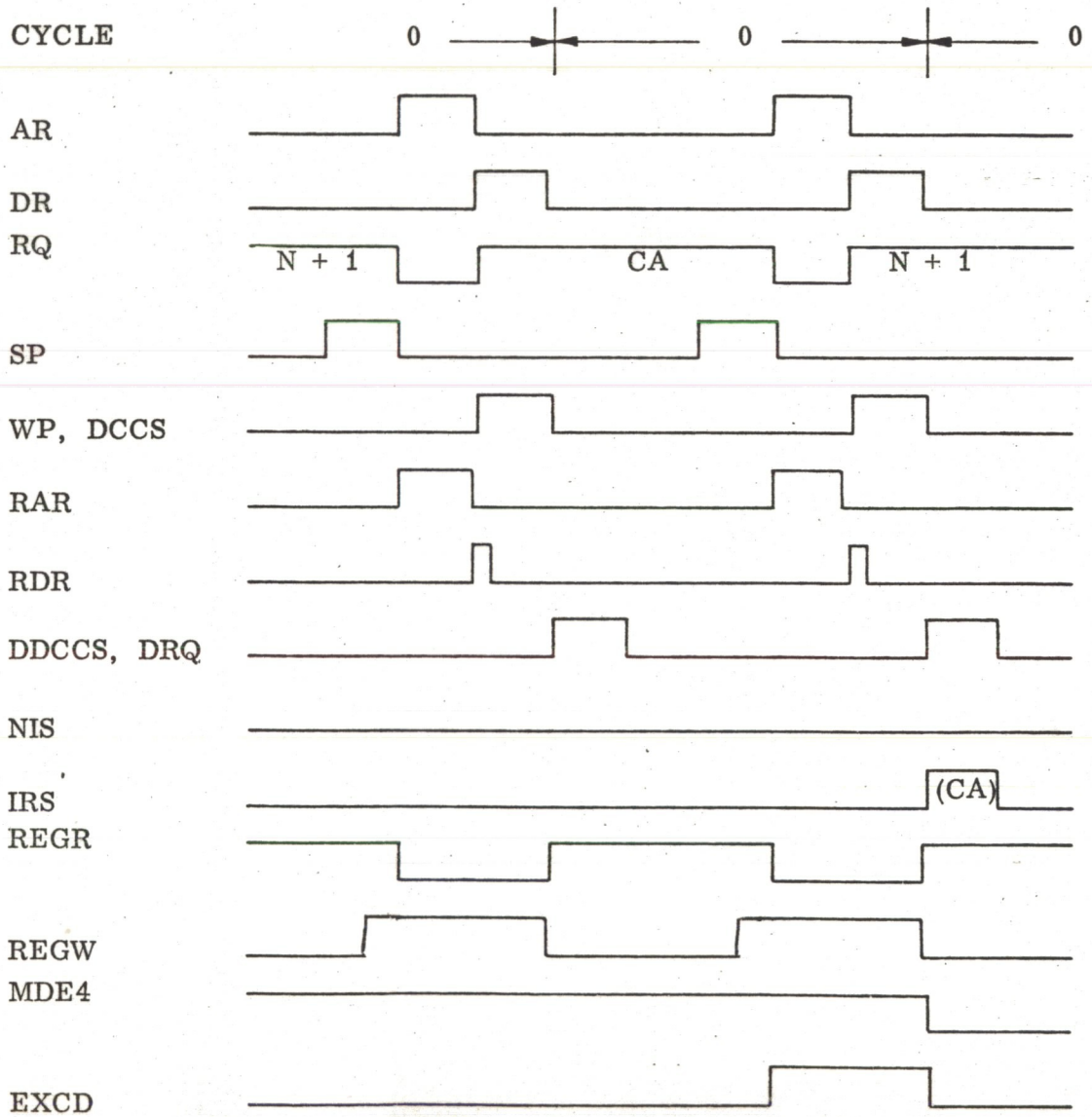
TIMING FOR IRS (WITH SKIP), RTJ AND DSK (WITH SKIP). DC0 - DC4 - DC0
(WITHOUT PROTECT)



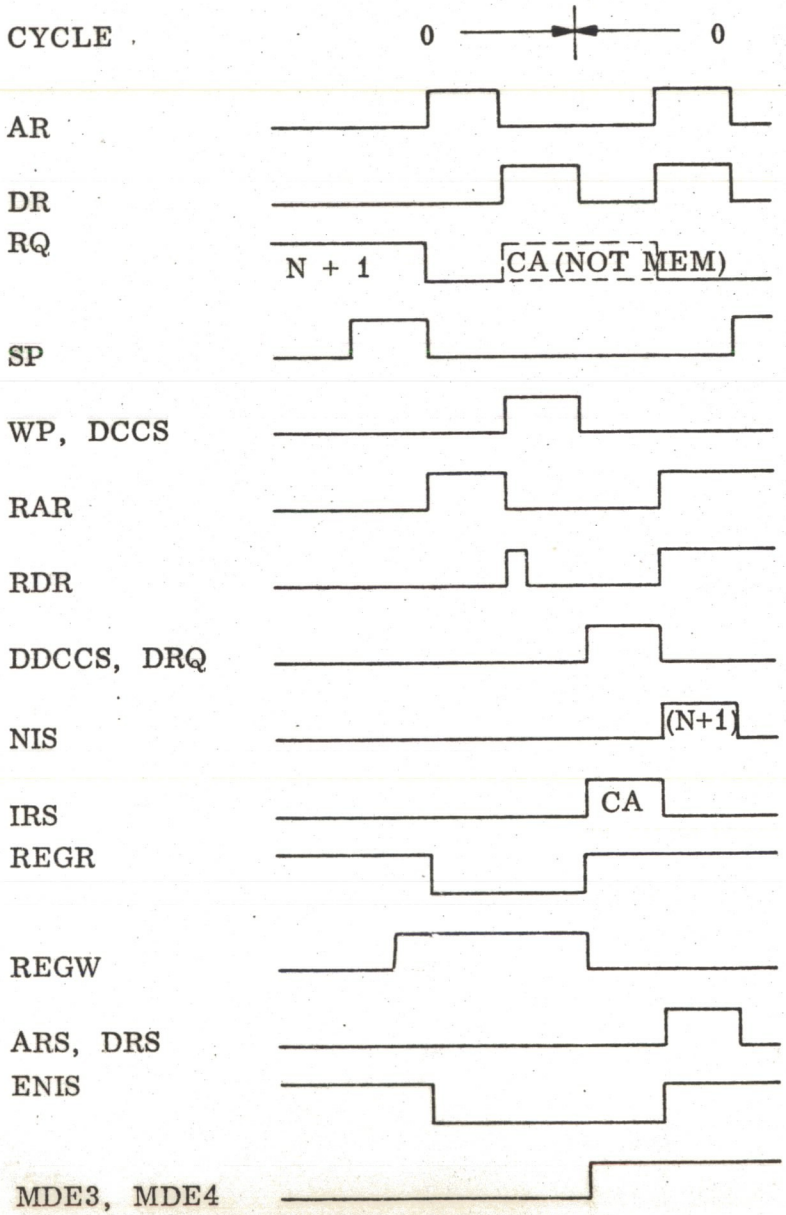
TIMING FOR BSZ, BSO, AND FRS (ALL WITH SKIP) DC0 - EXT - DC4 - DC0
(WITHOUT PROTECT)



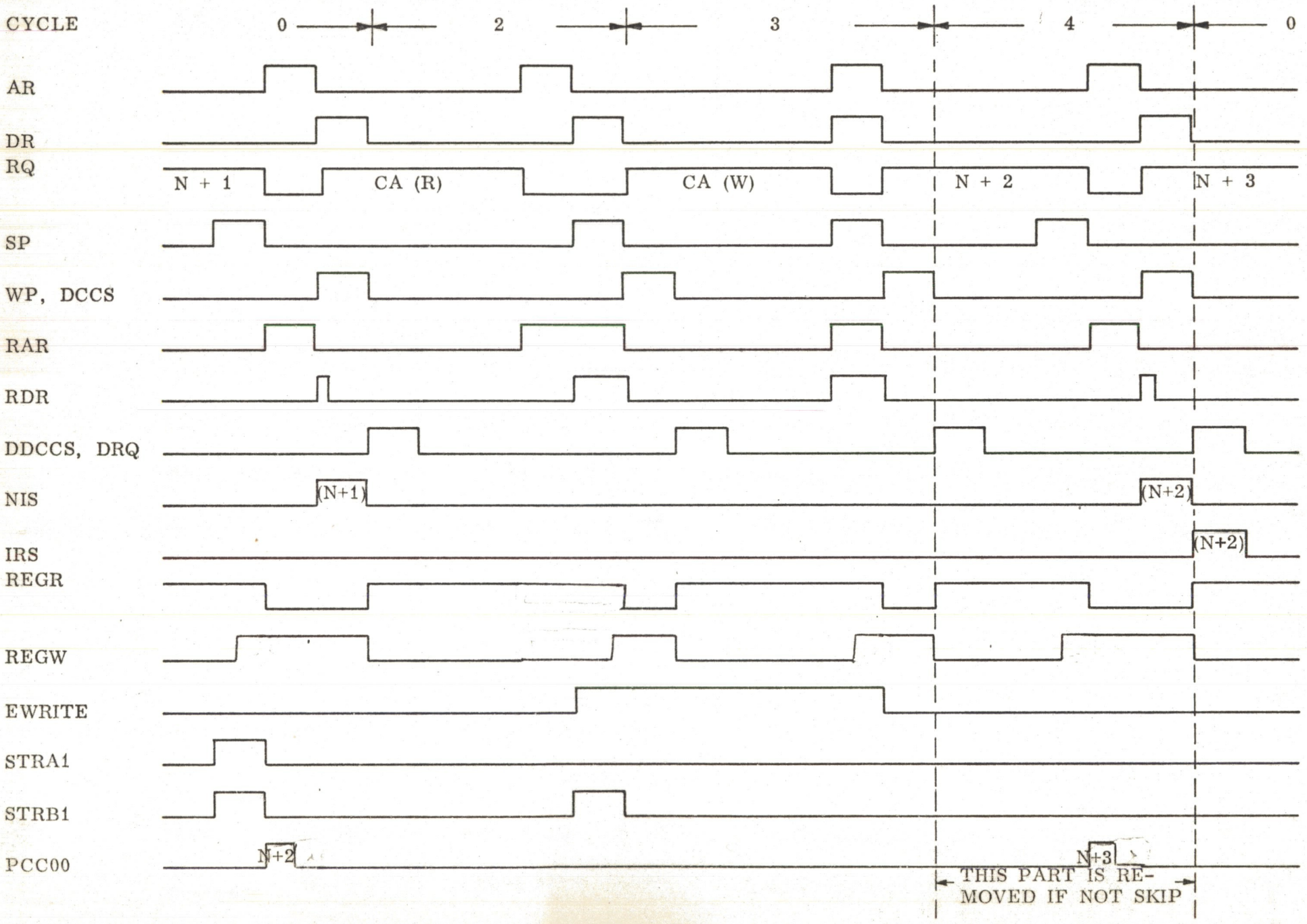
TIMING FOR EXC. DC0 - DC0 - DC0
(WITHOUT PROTECT)



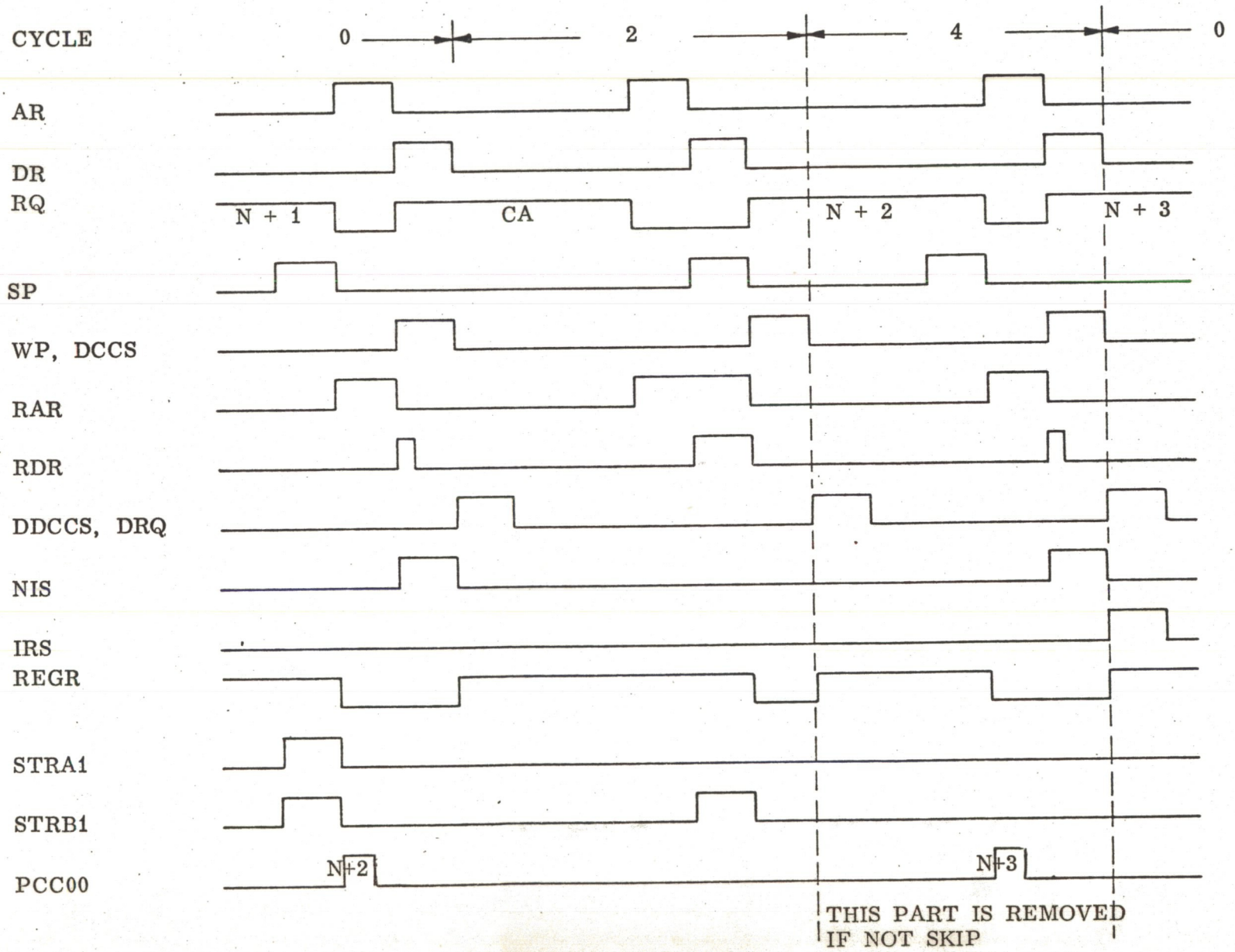
TIMING FOR EXC IM. DC0 - DC0 (SIMULATED AR AND DR)
(WITHOUT PROTECT)



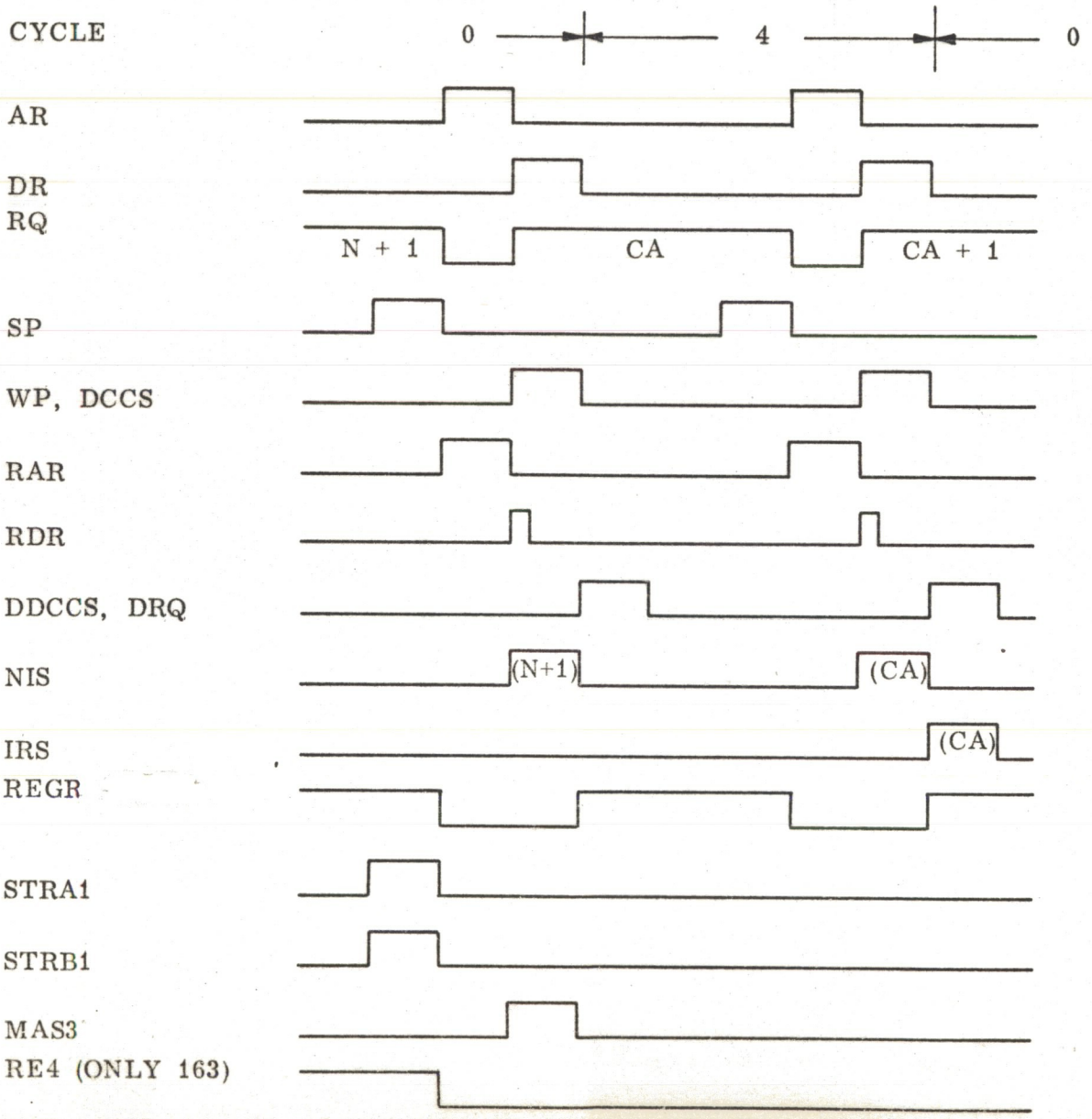
TIMING FOR MIN (WITH SKIP) DC0 - DC2 - DC4 - DC0
(WITHOUT PROTECT)



TIMING FOR INSTRUCTION GROUP 1. (CRG, CRL, CRE AND CRD WITH SKIP) DC0 - DC2 (-DC4) - DC0
(WITHOUT PROTECT)

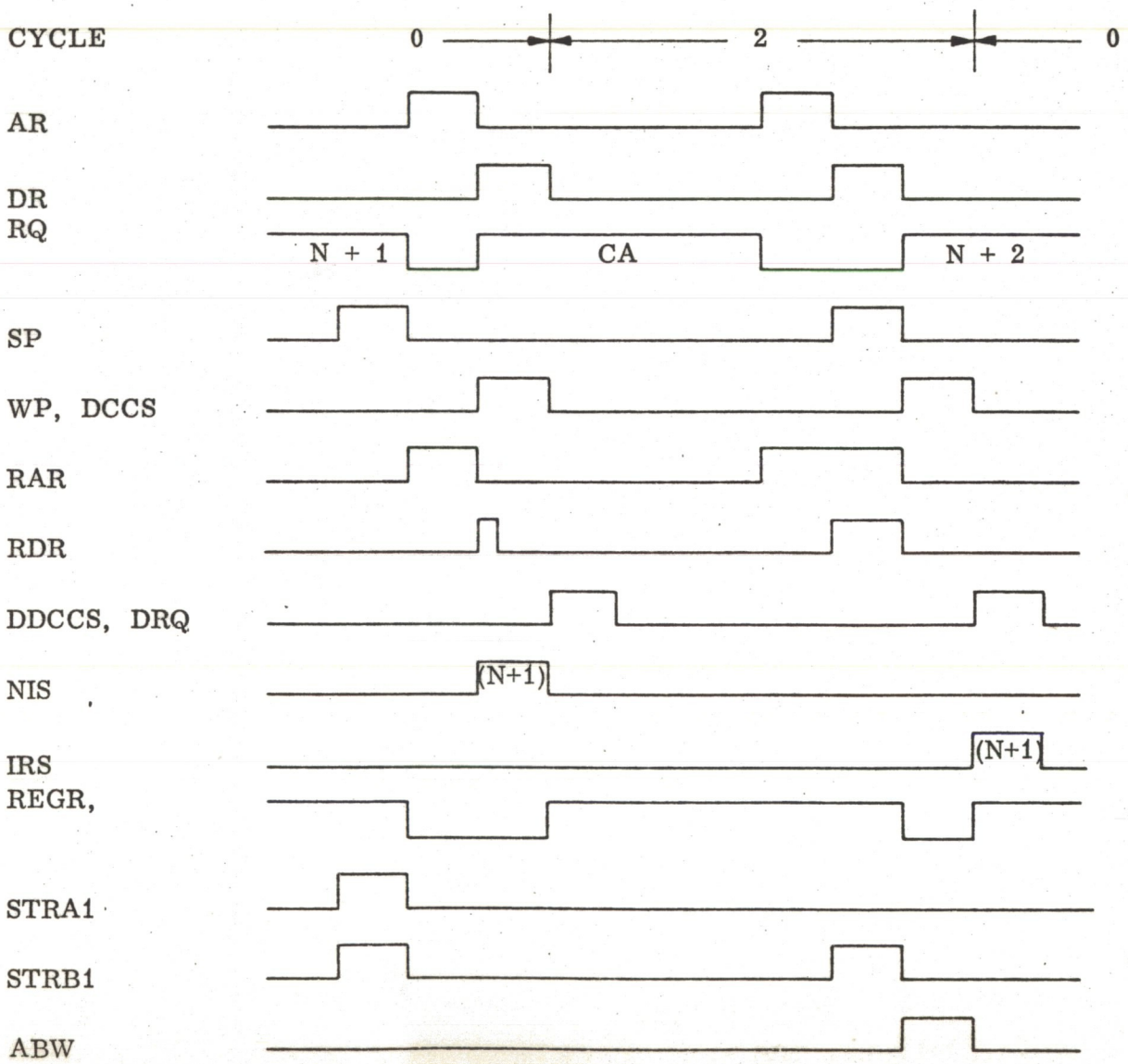


TIMING FOR INSTRUCTION GROUPS 2 AND 3. (JRP, JRN, JRZ, JRF, JPM, JNM, JZM AND JFM)
DC0 (-DC4) - DC0. (WITHOUT PROTECT)

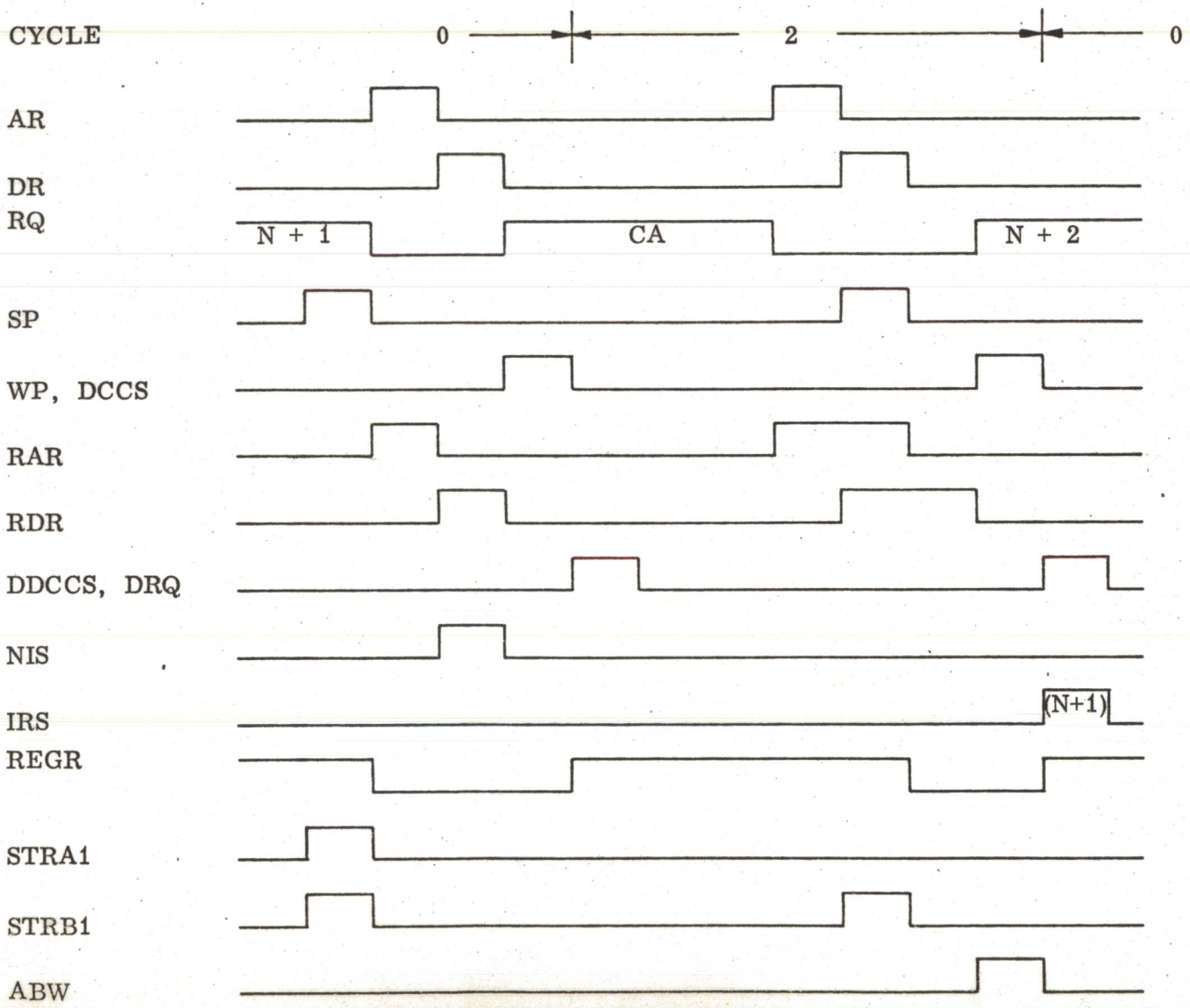


NOTE: STRB1 STROBES R+16 IF RE4=1. (MOD.REG).
" IF NOT JUMP, C0 INSTEAD OF C4, WITH N+2 AS ADDRESS.

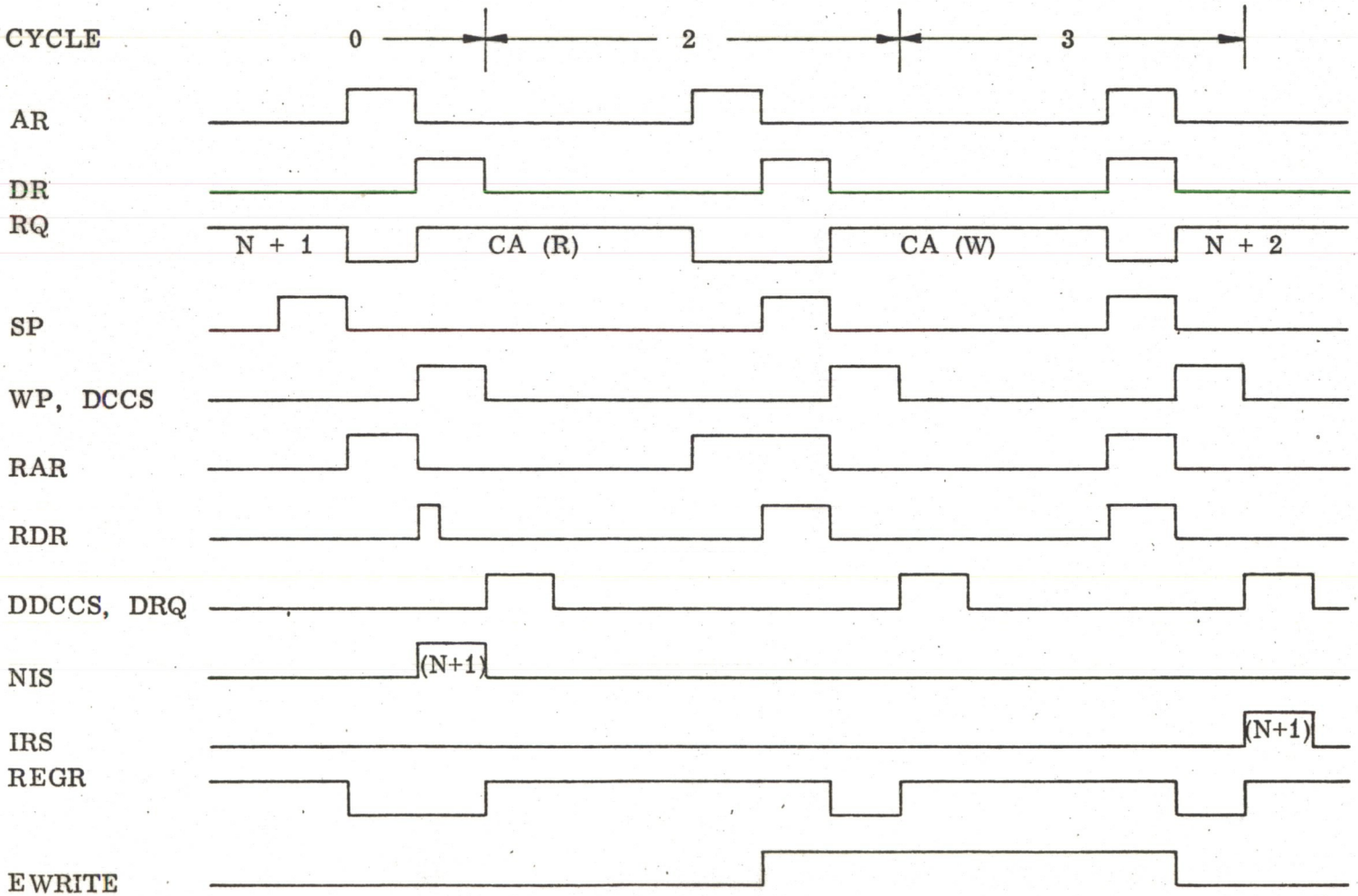
TIMING FOR INSTRUCTION GROUP 4. (ADD, SUB, AND and LDR) DC0 - DC2 - DC0
(WITHOUT PROTECT)



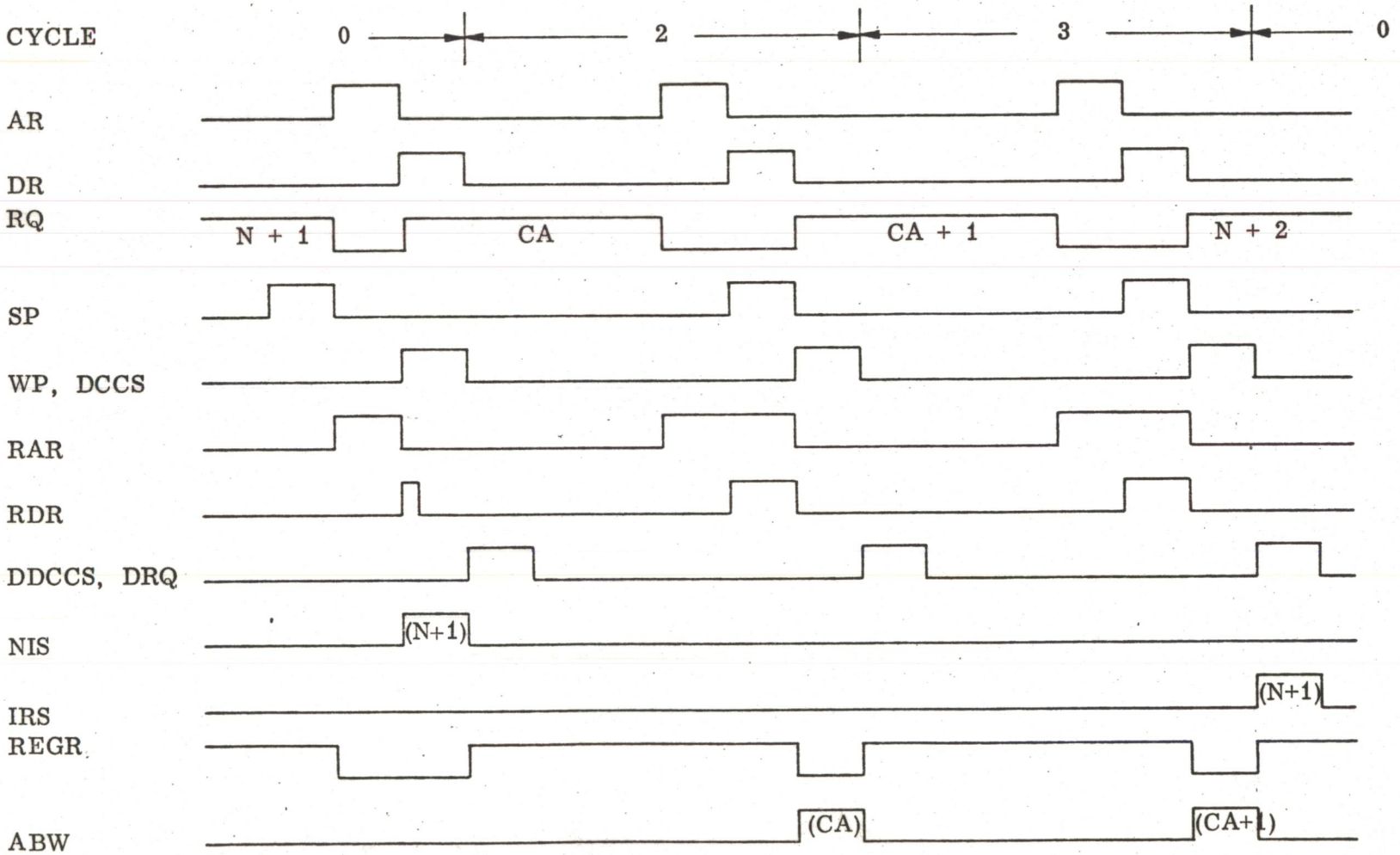
TIMING FOR INSTRUCTION GROUP 4 (ADD, SUB, AND and LDR) DC0 - DC2 - DC0
(WITH PROTECT)



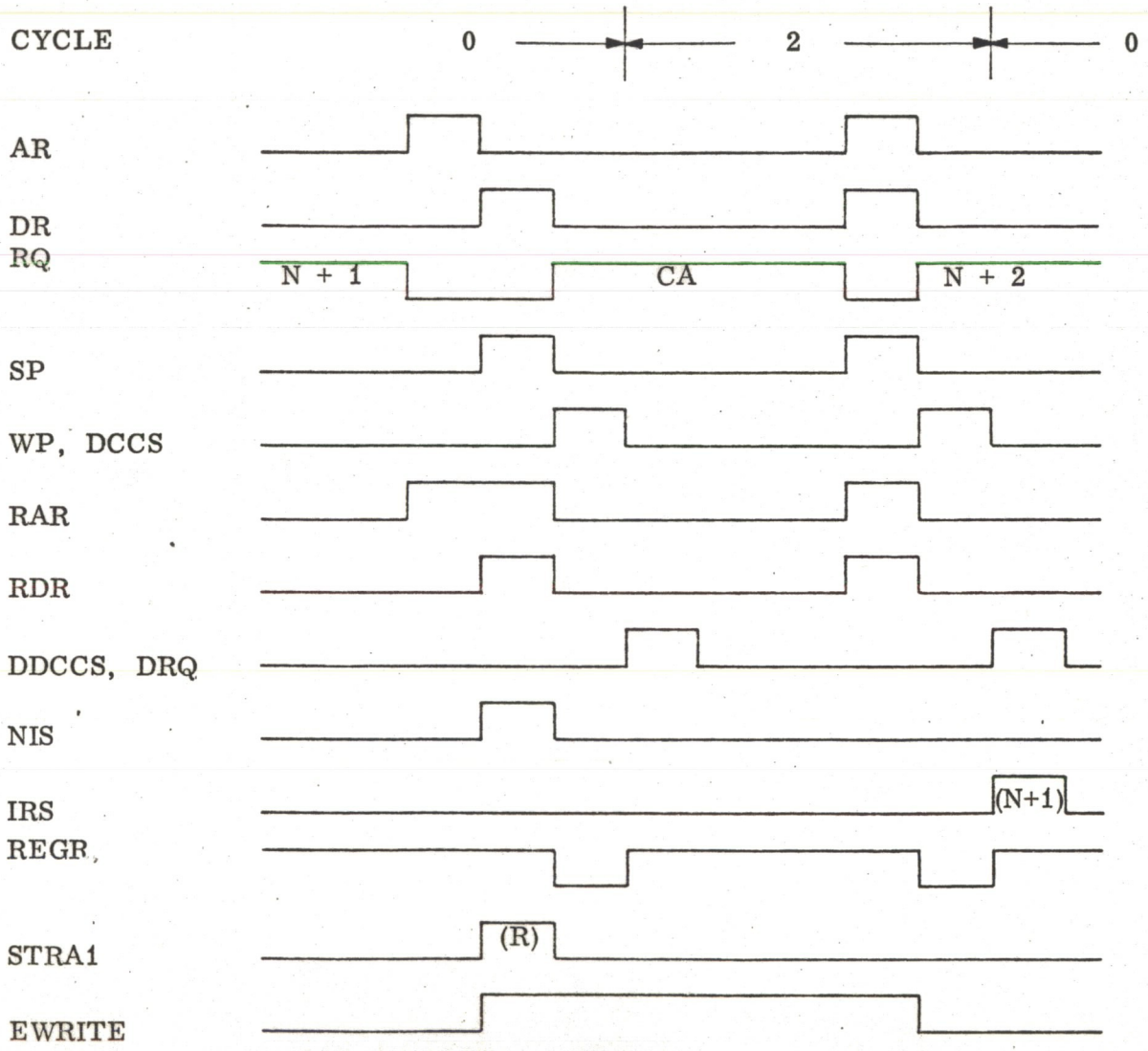
TIMING FOR ADM and XMR. DC0 - DC2 - DC3 - DC0
(WITHOUT PROTECT)



TIMING FOR LDD DC0 - DC2 - DC3 - DC0
(WITHOUT PROTECT)

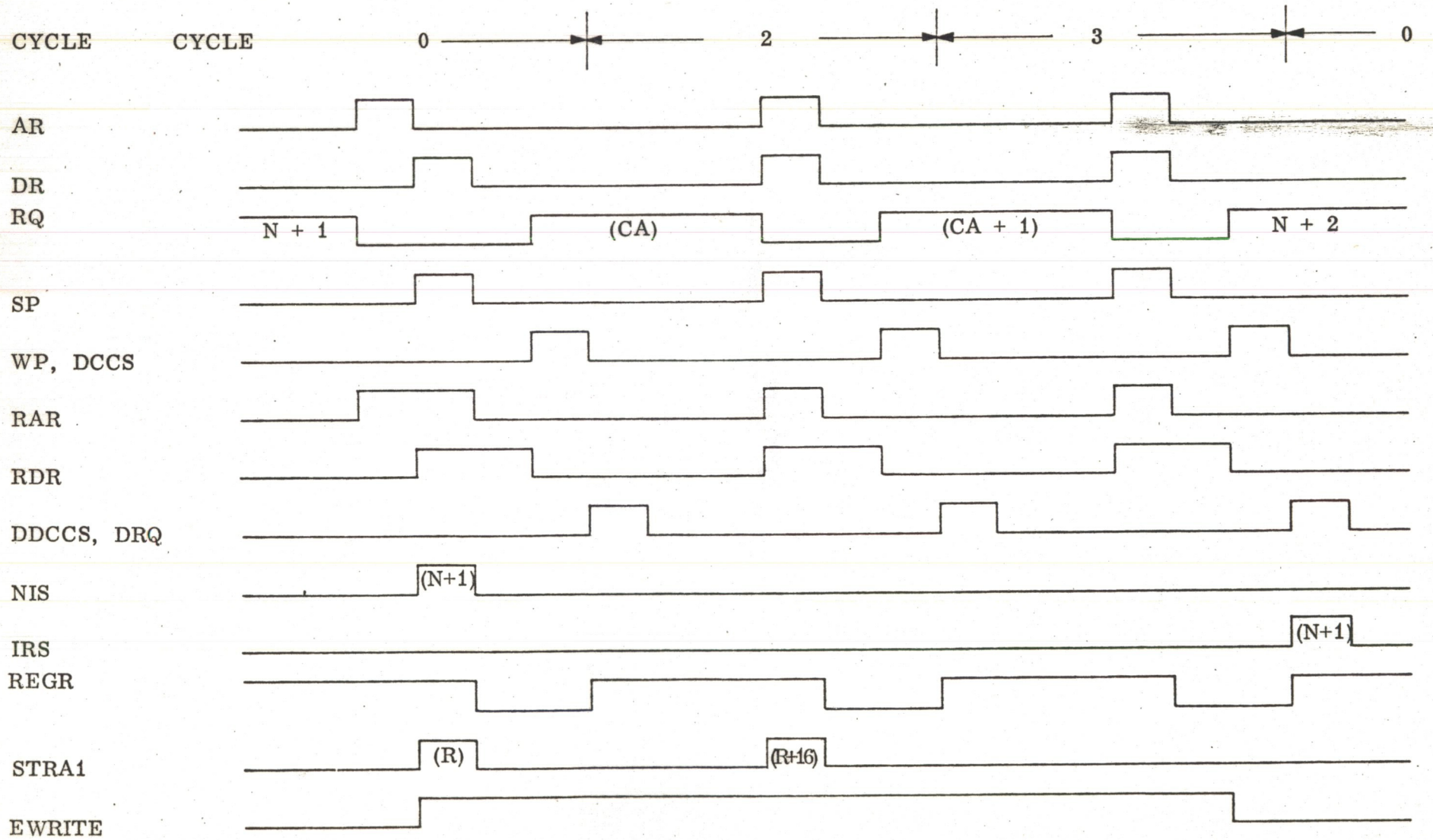


TIMING FOR STR DC0 - DC2 - DC0
(WITHOUT PROTECT)

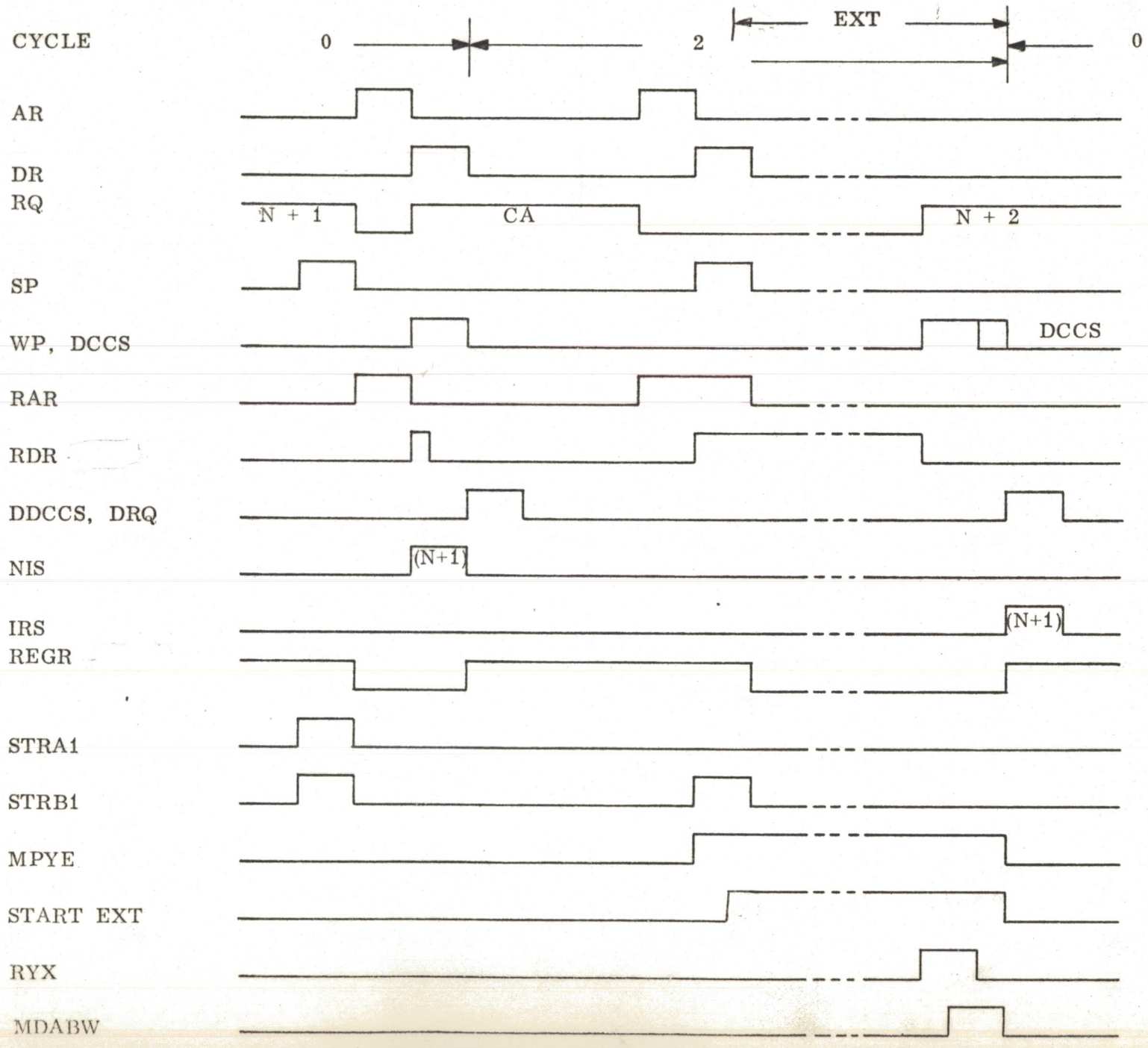


TIMING FOR STD (WITH PROTECT)

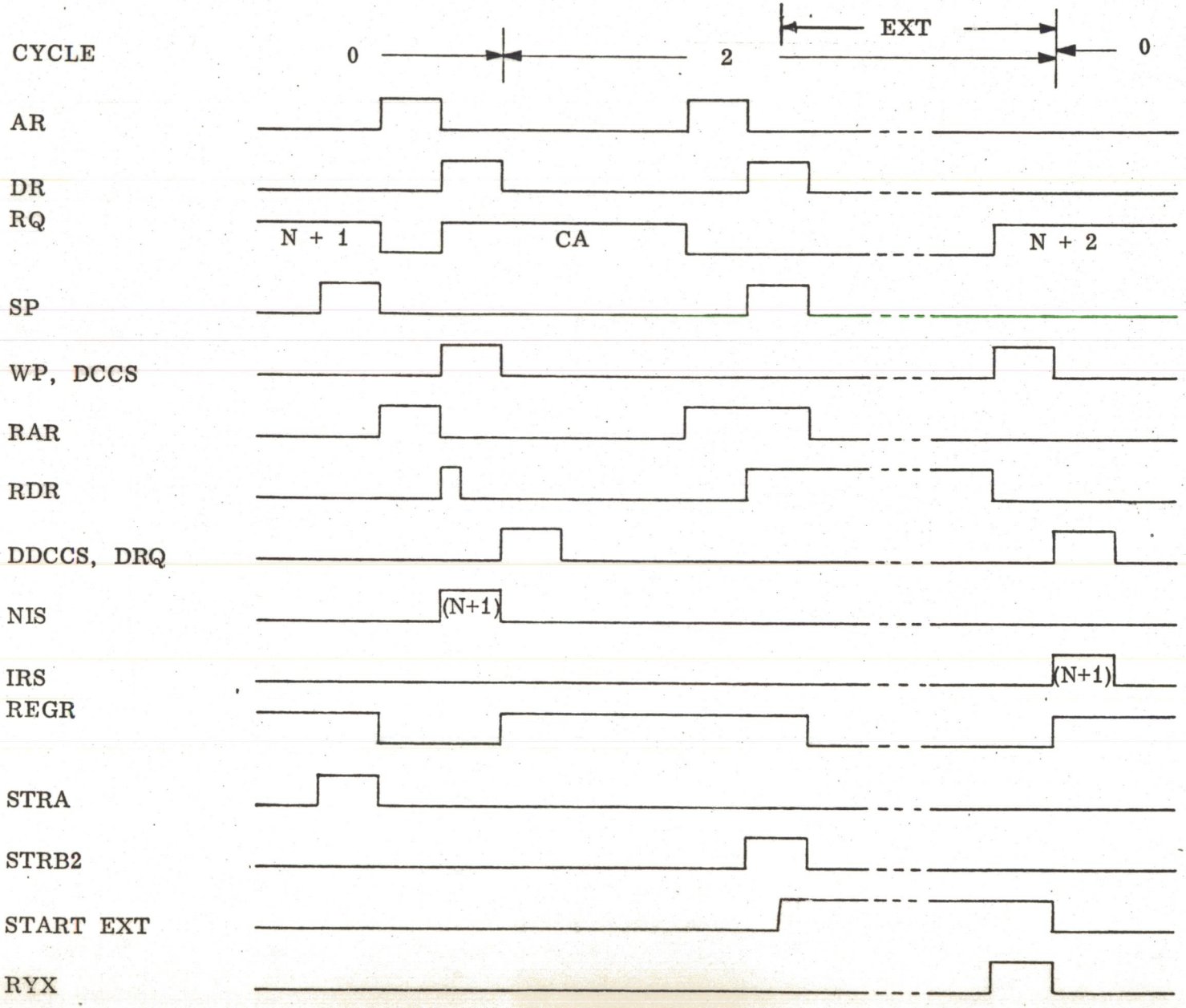
DC0 - DC2 - DC3 - DC0



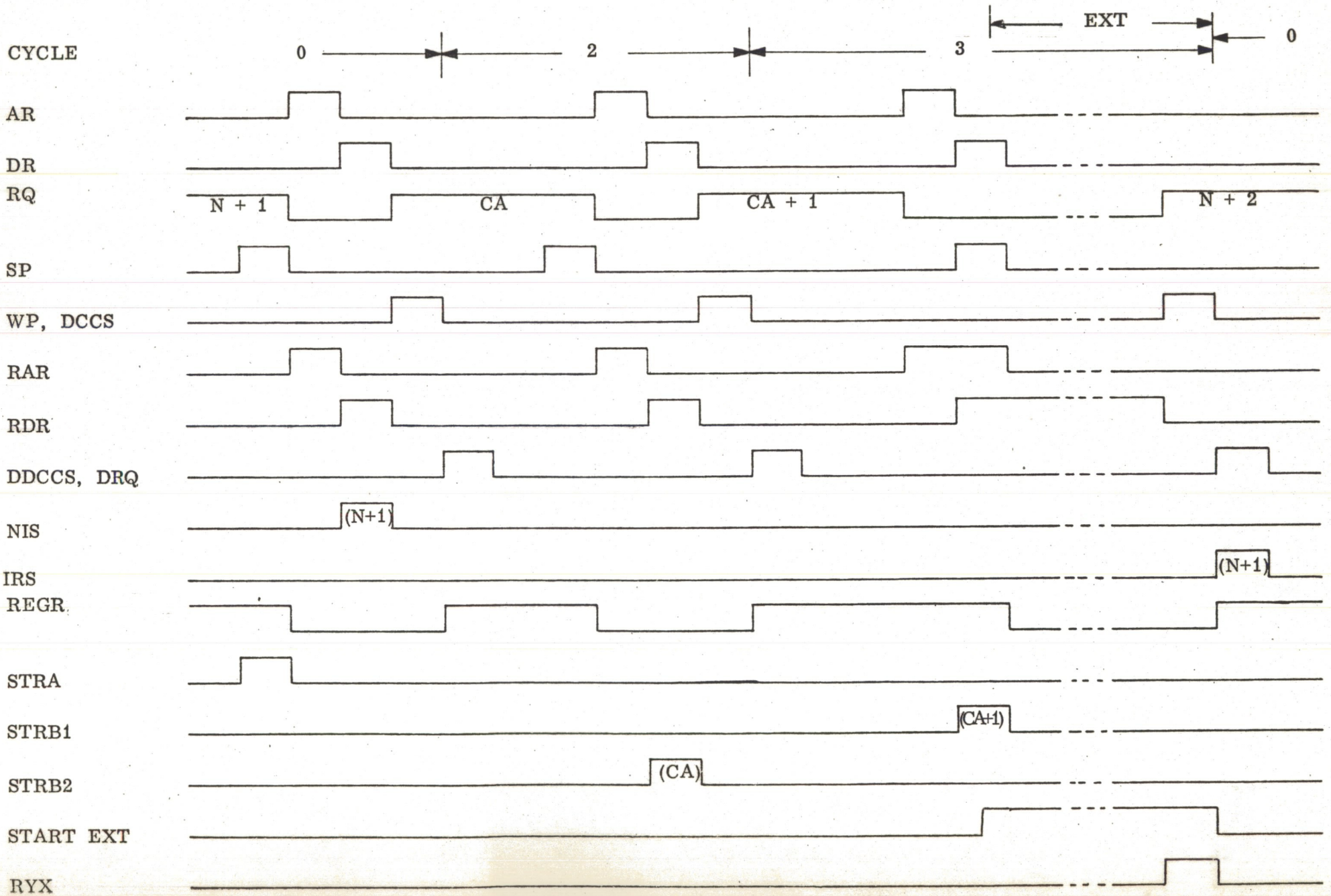
TIMING FOR MPY and DIV DC0 - DC2 - EXT - DC0
(WITHOUT PROTECT)



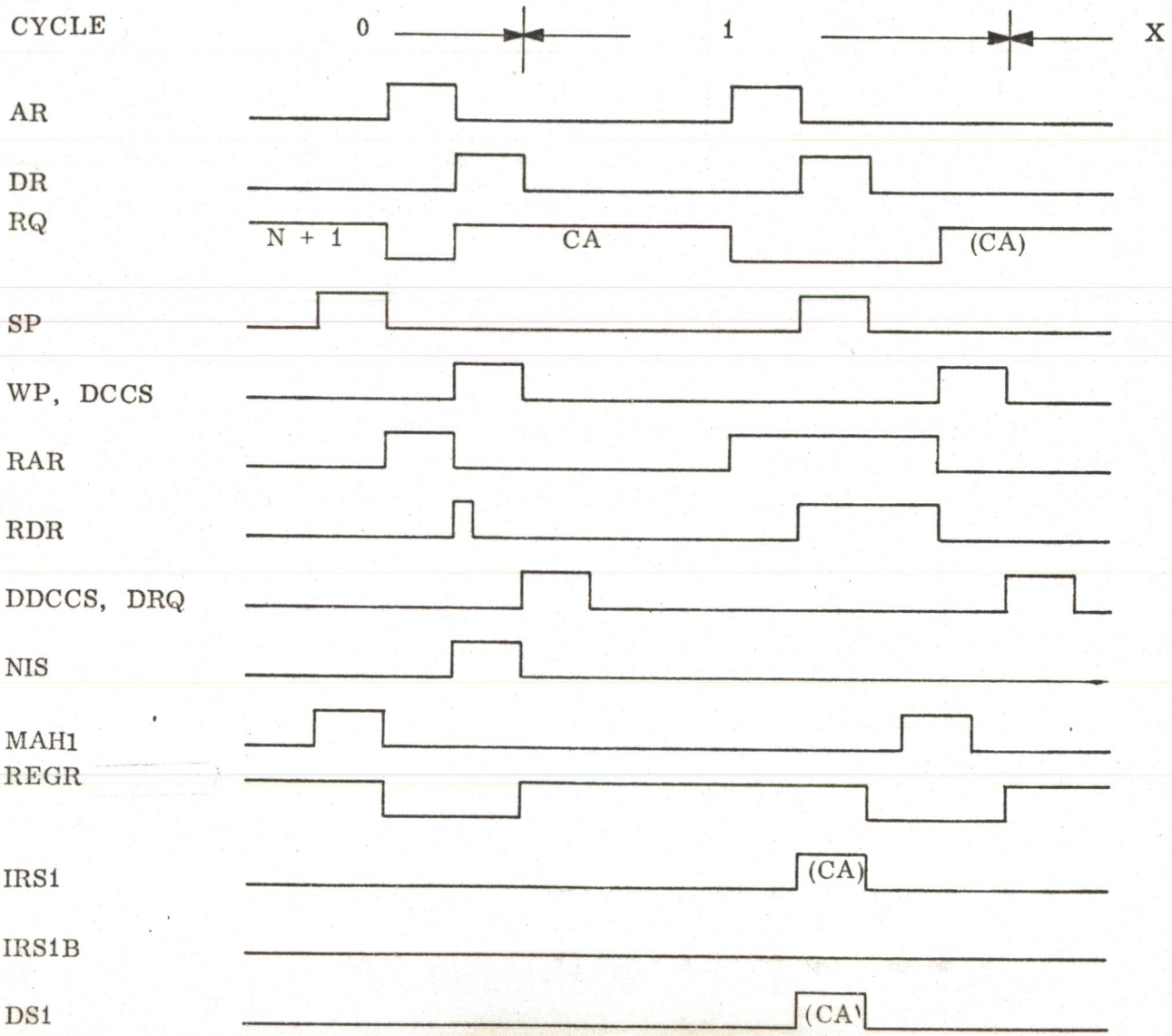
TIMING FOR FAD, FSB, FMU and FDV (SINGLE PRECISION) DC0 - DC2 - EXT - DC0
(WITHOUT PROTECT)



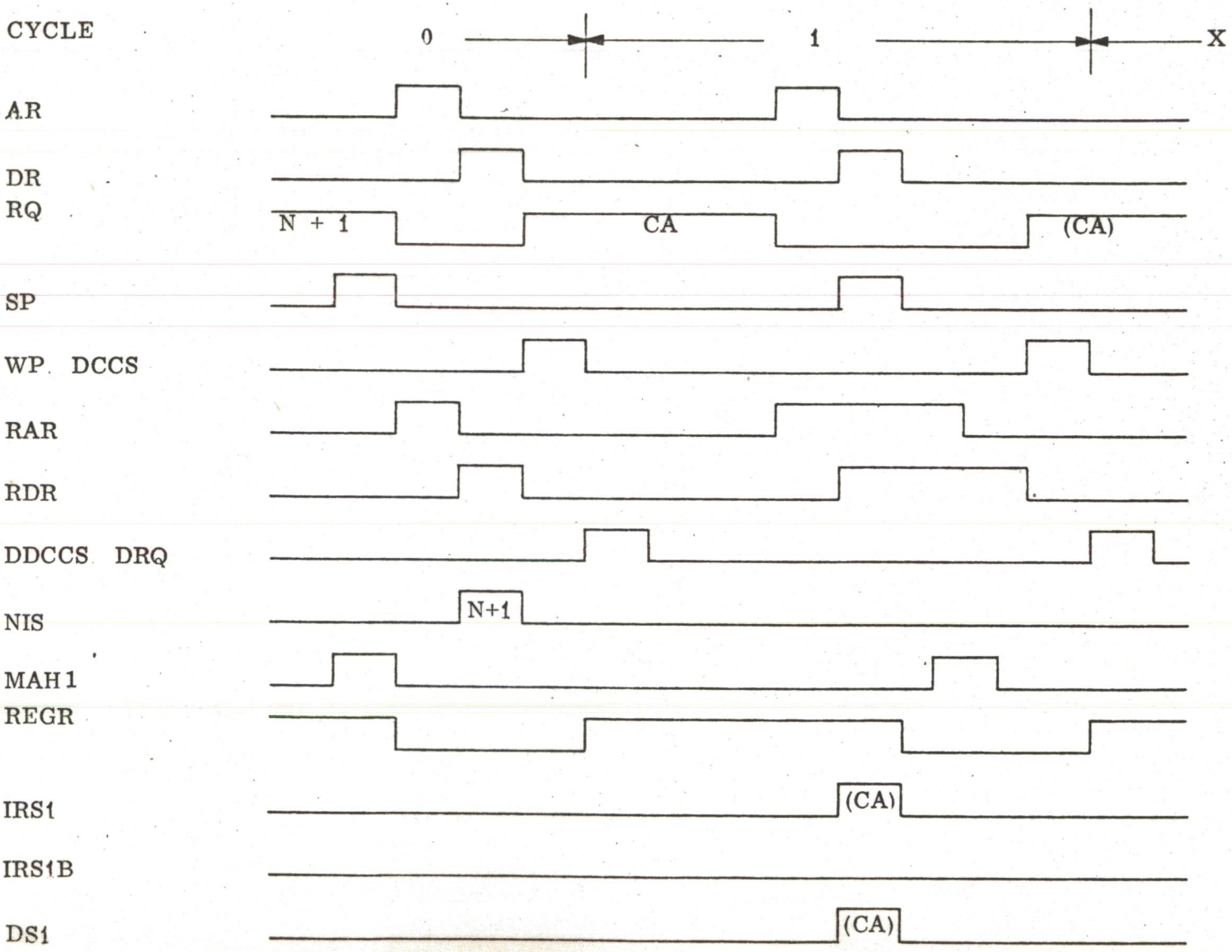
TIMING FOR FADD, PSBD, FMUD and FDVD. (DOUBLE PRECISION). DC0 - DC2 - DC3 - EXT - DC0



TIMING FOR INDIRECT ADDRESS CYCLE DC0 - DC1 -
(WITHOUT PROTECT)



TIMING FOR INDIRECT ADDRESS CYCLE DC0 - DC1 -
(WITH PROTECT)



6 CONTROL MODULE SUMMARY

This chapter contains a short summary of the main functions of each of the control cards 1500, 1504, 1505, 1506, 1507, 1508, 1510 and 1519.

For the meaning of each signal, see the alphabetic list (Chapter 7.)

6.1 NORD-50 I/O Control 1500

The main function of this module is to drive the lamps on the display panel. The line receivers for Address Ready and Data Ready, and the logic for selecting the last of each are also on this module.

In the case of MUL and DIV, the overflow or remainder register must be written into. The write signals and extra delay for write enable are generated on this module.

6.2 NORD-50 Controller 1504

Part of the NORD-10 communication control is on this module, as decoding of I/O instruction and set pulses to status bits (SB). Parity generation and parity checking are done on this module. and also enabling signals for the different memory address sources (MAE2 and MAE5).

Another part of the module is the break point violation logic generating the ABPBQ signal depending on modus bits (Mx) specifying break point conditions.

6.3 Register Address 1505

This module generates register address signals by selecting the appropriate bits from the instruction register. The four sets of four bit register addresses are for register block A (RAAx), for register block B (RABx), for index register block (XAx) and for base register block (BAx).

It also generates chip select signals for register block A (ACSx), register block B (BCSx), index registers (XE1) and base register (BE1).

Parts of the instruction register are buffered and made available for the external arithmetic.

6.4 Cycle Counter 1506

This module contains the cycle counter (DCCx) and logic for deciding the next cycle according to the conditions described in section 4.1. One important signal is the JUMP (or SKIP) EFFECTIVE signal (JEFF) which depends on instruction and arithmetic conditions, and selects cycle 4 as next cycle if true.

6.5 Arithmetic Control 1507

The main function of this module is to generate the five ALU control signals and carry input (CYSX) to main arithmetic (1502). The CFF is the carry flip-flop available to the programmer using interregister arithmetic instruction.

NORD-50 I/O instructions are used for reading and writing Overflow and Remainder registers (PSRS, RGE6, FRE).

6.6 Chip Select 1508

Strobe pulses for A and B bus buffer registers are generated on this module (STRAx, STRBx). Enabling signals for A and B buses (SRAE, SRBE), start and enabling signals for external arithmetic (SFAD, SFSB, SFMU, SFDV, SMPY, SDIV, SOPR, FADE and MPYE) and destination register enabling signals (DREx) are also generated on this module.

6.7 Instruction Control 1510

This module generates various strobe and enabling signals to 1501, 1502 and 1503. The meaning of each signal is best found by checking the alphabetic list of NORD-50 signals.

6.8 Timing Control 1519

Each basic cycle in NORD-50 has two phases, register read and register write. The corresponding timing signals are REGR and REGW. The register read phase is terminated by a buffer strobe pulse (SP) and the write phase by a write pulse (WP). Each of these four basic timing signals are decoded together with the machine cycles to form a set of timing signals.

The length of each phase is more closely described under 5.8.

During "external" arithmetic, i.e. floating point operations and shift the length of the write phase is terminated by the external ready signal (RYX).

7 SIGNAL SOURCE AND DEFINITIONS

SIGNAL	SOURCE	DEFINITION
Axx	1502	Data Bus from register block A.
ABE1	1505	Address bit to data selector for bus A (Axx) bits 0-31.
ABE2	1510	Address bit to data selector for bus A (Axx) bits 32-63.
ABPBQ	1504	Memory address outside specified range, depending on mode (see NORD-10/ NORD-50 communication manual).
ABW1	1510	Register write signal to block A and block B.
ACS1	1505	Chip Select signal to register block A, registers 0-15.
ACS2	1505	Chip Select signal to regisger block A, registers 16-31.
ACS3	1505	Chip Select signal to register block A, registers 32-47.
ACS4	1505	Chip Select signal to register block A, registers 48-63.
ADD1	1510	Control signal to bit 12-19 of address arithmetic adder to add corresponding bits of displacement in indirect addresses.
ADERR	1510	Addressing error. Address outside range (see ABPBQ) or to many levels of indirect addressing. Program is stopped and status bit 1 is set.
ADM	1506	Decoded instruction (add to memory).
AHxx	1503	Data bus A to high-speed multiply unit.
APxx	1502	Data bus A to multiply/divide unit.
AR	1504	Address Ready signal from real memory or simulated memory (NORD-10). AR = ARL + ARS

SIGNAL	SOURCE	DEFINITION
ARG	1506	Decoded instruction (argument set or argument skip).
ARL	1500	Address Ready signal from real memory.
ARS	1519	Simulated Address Ready.
AUxx	1502	Data bus A to add/subtract/shift unit.
Bxx	1502	Data bus from register block B (bits 0-63).
BAx	1505	Address bits to BASE register block.
BBE1	1505	Address bit to data selector for bus B (Bxx) bits 0-31.
BBE2	1505	Address bit to data selector for bus B (Bxx) bits 32-63.
BCSx	1505	Same as corresponding ACSx, but for register block B.
BDxx	1501, 1532	I/O data bus connected to NORD-10 I/O system.
BE1	1505	Chip select signal, BASE register block.
BE2	1510	Chip Select signal, BASE register block.
BHxx	1501	Data bus B to high-speed multiply unit.
BPxx	1501	Break Point register.
BPxx	1502	Data bus B to multiply/divide unit.
BQxx	1501	Break Point register.
BSKP	1507	Decoded instruction (bit skip).

SIGNAL	SOURCE	DEFINITION
BUxx	1502	Data bus B to add/subtract/shift unit.
CF	1519	Clear flags. (Resets NORD-50 status register.)
CGA	1503	Carry generate signal from address arithmetic (X + B).
CGB	1501	Carry generate signal from address arithmetic (XB + D).
CGS	1502	Carry generate signal from main arithmetic (A + B).
CNT15	1510	Level counter in indirect addressing is 15 (limit of permitted levels). The sum of execute or indirect levels in one instruction. Part of ADERR.
CPA	1503	Carry propagate signal from address arithmetic (X + B).
CPB	1501	Carry propagate signal from address arithmetic (XB + D).
CPL	1519	Program completion signal to the CPU cycle counter.
CPS	1502	Carry propagate signal from main arithmetic (A + B).
CYAxx	1503	Carry signal in address arithmetic adder (X + B).
CYBxx	1501	Carry signal in address arithmetic adder (XB + D)
CYGA16	1501	Carry generate signal from address arithmetic second level of look-ahead (X + B).
CYGB	1501	Carry generate signal from address arithmetic second level of look-ahead (XB+D).
CYGS	1501	Carry generate signal from main arithmetic second level of look-ahead (A + B).
CYP	1508	Clock pulse to Carry flip-flop.
CYPA	1501	Carry propagate signal from address arithmetic. Second level (X + B).

SIGNAL	SOURCE	DEFINITION
CYPB	1501	Carry propagate signal from address arithmetic. Second level (XB + D).
CYPS	1501	Main arithmetic. Second level (A + B).
CYSxx	1502	Carry signal in main arithmetic.
Dx	1501	Temporary storage register for Displacement.
DBxx	1501	Selected input to memory (S or SD).
DBPxx	1501	DB parity bit (1 for even parity of the four corresponding DB bits).
DCx	1519	Main CPU cycles. DC0: Instruction readout and execution. DC1: Indirect address cycle. DC2: Memory reference execution , first cycle. DC3: Memory reference execution, second cycle. DC4: Instruction readout to NI only. DC7: Stop/idle cycle.
DC10	1506	DC0+DC1.
DCCx	1506	Cycle counter flip-flop (see DCx).
DCCS	1519	Cycle counter strobe pulse.
DCRx	1519	DCx timed with register read time.
DCSx	1519	DCx timed with register strobe time.
DCWx	1519	DCx timed with register write enabling time.

SIGNAL	SOURCE	DEFINITION
DCWPx	1519	DCx timed with register write set time.
DDCCS	1519	Trailing edge of DCCS shaped to a 100 ns pulse used to change content of IR and D register.
DER	1504	Data error, i.e. underflow or overflow in arithmetic operation and the corresponding flag bits (M1 and 0) is on. Program is stopped and status bit 4 or 3 is set.
DEVC	1519	NORD-50 COMPLETION signal to NORD-10. This completion signal is the result of a STOP instruction in the NORD-50 program, an error stop or data ready from core memory for EXAMINE/DEPOSIT.
DEVS	1532	NORD-50 START signal.
DIV	1508	Decoded instruction. Divide.
DPA	1505	Double precision operation in add/subtract unit.
DPM	1505	Double precision operation in multiply/divide unit.
DR	1519	Data ready signal from real memory or NORD-10 (simulated memory). DR = DRL + DRS.
DRE1	1508	Enable register address bits from destination field of instruction (IR12-17).
DRE2	1508	Enable INDEX and BASE register address from IR12-15, destination address.
DRE3	1508	Determines register address bit 4 in load and store floating instructions.
DRL	1500	Data Ready from real memory.
DRQ	1519	Leading edge of RQ shaped to a 100 ns pulse. Used to generate strobe pulses to TA and TD.
DRS	1519	Simulated Data Ready.

SIGNAL	SOURCE	DEFINITION
DS1	1510	Strobe MDC, MAC or NI into D-register.
Exx	1501	Selected input data to IR and D-registers. Only E23 is used outside 1501-modules because IR23 has to be strobed together with IR24 to IR31 (see IRS1).
ENIS	1510	Enable request for next instruction. (Disabled in case of execute immediate)
EWRITE	1519	Write signal to memory and arithmetic. Generated before the request.
EXC	1506	Decoded instruction (execute).
EXDEP	1504	One of the EXAMINE or DEPOSIT mode bits is on (EXDEP = M12 + M13).
EXOP	1510	Decoded instruction (SHR, SHF, BST, BCL, BSZ, BSO, FIX, FLO).
EXT	1508	The peripheral arithmetic unit is ececuting an instruction (FAD, FSB, SHR, SHF, BST, BCL, BSZ, BSO, FIX, FLO, FRO, FRS, MRY, DIV, FMU, FDV, interregister mulitply/divide).
FADE	1508	Enable line drivers for A and B bus to add/subtract/shift unit.
FIX	1507	Decoded instruction (convert from floating point to fixed point format).
FLOAT	1508	Decoded group of instructions (floating point).
FRE	1507	Address bit to data selector for bus B (Bxx).
FRS	1507	Decoded instruction (floating register skip).
FRSBIT		Selected test result for floating register skip test.
FSx	1507	Function select signals to main arithmetic.

SIGNAL	SOURCE	DEFINITION
Hxx		Result data bus from high-speed multiply unit.
HIGH	1510	Always logical one.
HSME		High speed multiply data bus enable. Not generated.
IN	1504	Data transfer from NORD-50 to NORD-10.
IOAX	1532 II	NORD-10 I/O address bus.
IORE1	1504	IOX read enable for NORD-10 IOX reading bits 0-15 of one of the registers TA, TD, SA or PC.
IORE2	1504	Same as IORE1, but for bits 16-31.
IOSTR1	1504	Decoded device number. Strobe pulse for least significant half (bits 0-15) of register to be loaded from NORD-10.
IOSTR2	1504	Same as IOSTR1 for most significant half (bits 16-31).
IPROT	1510	DC1 + PROT
IRxx	1501	Instruction Register.
IRS	1507	Decoded instruction (interregister skip).
IRS1	1510	Strobe MDC, MAC or NI into IR, bits 0-11 and bits 23-31.
IRS1B	1510	Same as IRS1, but for bits 12-22. These bits are not replaced during an indirect address cycle.
IRS2	1504	IR strobe enabling, i.e. strobe IR on cycle shift.

SIGNAL	SOURCE	DEFINITION
IRXxx	1505	IR signals buffered for use by add/subtract/shift unit.
LBPxx	1501	Effective address less than BP register.
LBQxx	1501	Effective address less than BQ-register.
LCONT	1504	Load Controls bits into NORD-50 modus register.
LDEVC	1519	Device complete signal to NORD-10. (NORD-50 has stopped.)
LDR	1507	Deocded instruction (load register).
Mxx	1531	Mode control signals set by NORD-10 program.
MAxx	1501	Memory Address bus signals.
MAE2	1504	Address bit to memory address register selector (selects SA).
MAE3	1532 II	Address bit to data selector for data transfer to NORD-10 I/O system. Selects one of the registers PC, SA, TA or TD.
MAE4	1532 II	Address bit to data selector (see MAE3).
MAE5	1504	Address bit to memory address register selector (selects computed address CA).
MAH1	1519	Strobe X + B into buffer register.
MAS3	1506	Strobe MA C into PC.
MBxx	1501	Memory Data bus to main arithmetic, equals MDC or instruction address plus one (for RTJ).

SIGNAL	SOURCE	DEFINITION
MCP	1519	Programmed master clear pulse which occurs when mode bit 9 is set. MCP is used to set DC7 and clear a number of control flip-flops.
MDxx	1501	Memory data bus signals, MD= S or MD = SD. Bits 32-35 are found on NORD-50 CONTROLLER 1504.
MDABW1	1500	Register write periode in Multiply and Divide instruction.
MDCxx	1501	Memory Data, TTL-levels.
MDCE1	1510	Enable MDC as input to main arithmetic via MB. Always on except for RTJ when the return address is transferred via the MB bus. Note that PC was strobed into TA on last AR-pulse.
MDCPxx	1501	MDC parity bit (1 for even parity of the four corresponding MDC-bits).
MDE3	1510	Address bit to input selector for IR and D registers.
MDE4	1510	Address bit to input selector for IR and D registers.
MIN	1506	Decoded instruction (memory increment).
MPY	1508	Decoded instruction (multiply).
MPYE	1508	Enable line drivers to multiply/divide unit.
MSIM	1504	Simulated memory. NORD-10 program simulates the NORD-50 memory by examining the requests and address an d returning the proper control signals and data (see ARS, DRS, SD).
NC7	1519	Next cycle is DC7.
NEXT	1506	Go to next instruction. No jump or skip.

SIGNAL	SOURCE	DEFINITION
NIxx	1501	Next Instruction buffer register.
NIS1	1510	Strobe MDCxx (data from memory) into NIxx.
OFX		Floating point overflow signal. Number can not be represented by available format.
OPCZ	1506	Decoded instruction, all operation code bits are zero i.e. interregister or argument.
OPCZ2	1510	Decoded and timed instructions ($OPCZ \cdot IR31_0 \cdot DCO_1$).
OPCZ3	1508	Decoded and timed instructions ($OPCZ \cdot IR31_0 IR29_0 DC0_1$).
OPCZ4	1508	Decoded and timedinstructions ($OPCZ \cdot IR31_0 \cdot IR29_1 \cdot DCO_1$).
ORWE	1500	Overflow or Remainder register write enable.
Pxx		Result data bus from multiply/divide unit.
PCxx	1501	Program Counter.
PCCxx	1501	Count Pulse to next stage of PC.
PCCO	1510	Count Pulse to PC.
PCE2	1506	PC-enable. Sub signal to generate MAE2.
PEBx	1504	Parity error flag, one for each of four bytes.
PROT	1504	The request is stopped if address is within protected area.
PSRS1	1507	Programmed write pulse to overflow register.

SIGNAL	SOURCE	DEFINITION
PSRS2	1507	Programmed write pulse to remainder register.
RAAx	1505	Register address bits to register block A.
RABx	1505	Register address bits to register block B.
RE1	1508	Enable register address bits from fits 23-28 of the instruction (argument instruction).
RE2	1508	Enable INDEX and BASE register address from IR23-30, for effective address computation.
RE4	1510	Generates register address bit 4 equal to one for jump instruction with content modification.
REGW	1519	Register write time. Generates chip select signal during the write phase and overlaps register write pulse WP.
RGE1	1510	Address bit to data selector for bus B (Bxx).
RGE4	1507	ARG·DCO. Subsignal to BBE1, BBE2.
RGE6	1507	Enable remainder register to RG bus.
RQ	1519	Memory request signal.
RQE	1519	Enable memory request at end of cycle.
RQM	1519	Memory request signal to core memory, equals RQ and not simulated memory.
RQS	1519	Set pulse to the memory request flip-flop.

SIGNAL	SOURCE	DEFINITION
RSTAT	1504	Enable NORD-50 status bits to NORD-10.
RTJ	1506	Decoded instruction (return jump).
RYP		Instruction ready signal from add unit.
RYM		Instruction ready signal from multiply/divide unit.
RYX	1504	Instruction ready signal from external arithmetic.
Sxx	1502	Data from main arithmetic or external arithmetic units.
SAxx	1501	Simulated Address or Start Address from NORD-10.
SBxx	1504	Status flip-flop set pulses.
SBM	1506	Decoded instruction, no assignment.
SDxx	1501	Simulated Data from NORD-10.
SDIV	1508	Start divide operation in peripheral arithmetic unit.
SE1	1519	Enable S as input to Memory Data bus driver.
SEB	1508	Address bit to data selector for S bus.
SELBIT		Signal from perihperal arithmetic equal to the selected bit in the bit skip instruction.
SFAD	1508	Start floating point add operation.
SFDV	1508	Start floating point divide operation in multiply/divide unit.

SIGNAL	SOURCE	DEFINITION
SFMU	1508	Start floating point multiply operation in multiply/divide unit.
SFSB	1508	Start floating point subtract operation.
SGL	1510	Single precision data, generated as not double precision. Double precision occurs for SHD, FROD, FADD, FSBD, FMUD, FDVD, register read time for FIXD and register write time for FLOD.
SMPY	1508	Start multiply operation in multiply/divide unit.
SOPR	1508	Start peripheral arithmetic operation (SHR, SHF, BST, BCL, BSZ, BSO, FIX, FLO). (Single or double.)
SP	1519	Timing pulse to go from register read phase to register write phase of instruction.
SRAE	1508	Enable IR6-11 (source register A) as address bits to register block A.
SRBE	1508	Enable IR0-5 (source register B) as address bits to register block B.
SRS1	1508	Strobe signal to overflow register. The overflow register holds the most significant 32 bits of the result of a single precision multiply instruction.
SRS2	1508	Strobe signal to remainder register. The remainder register holds the remainder after a single precision divide instruction.
SSxx	1502	Output from main arithmetic, A+B etc.
STOP	1507	Decoded instruction (stop).
STR	1506	Decoded instruction (store register).

SIGNAL	SOURCE	DEFINITION
STRA1	1508	Strobe pulse to A bus holding register, bits 0-31.
STRA2	1508	Strobe pulse to A bus holding register, bits 32-63
STRB1	1508	Strobe pulse to B bus holding register, bits 0-31
STRB2	1508	Strobe pulse to B bus holding register, bits 32-63
SWLXX	1500	Panel lamp driver signals.
SWX	OPR	Select display of dataref. or fetch-ref. bank in memory on operator panel. (4K banks.)
SZx	1502	All output bits from arithmetic on this card are zero.
TAxx	1501	Memory address register to hold last address on MA bus. Can be read by NORD-10 IOX instruction.
TAS1	1510	Strobe MAC (Memory Address) into TA.
TDxx	1501	Memory Address register to hold last dataword on MD bus. Can be read by NORD-10 IOX instruction.
TDS1	1510	Strobe MDC (Memory Data) into TD.
Uxx		Result data bus from add/subtract/shift unit.
UFX		Floating point underflow signal. Result is less than smallest possible number different from zero.
Wxx	1500	Panel lamp driver signals.
WLX	1500	Panel lamp driver signals.
WP	1519	Timing signal for writing new information into CPU registers and terminate one cycle.

SIGNAL	SOURCE	DEFINITION
WR1	1504	Enable Memory Data line driver.
WRAR	1510	Start register write phase on AR signal from memory.
WRD	1510	True for instruction cycles where a core memory write operation is started. WRD is used to set the WRITE signal.
WRITE	1519	Latch for holding WRD for one complete memory cycle.
WRM	1519	Write control signal to real memory.
Xxx	1503	Data output from INDEX register block.
XAx	1505	Address bits to INDEX register block.
XBxx	1503	Data output from index adder = X + B.
XBW	1510	Write new information into INDEX and BASE register blocks.
XE1	1505	Chip select signal, INDEX register block.
XMR	1506	Decoded instruction (exchange content of register and location in core memory).
XSTOP	1532 II	Stop signal from NORD-10 to NORD-50.
ZROA	1505	Register address is zero or bus A should be made to be zero. Register O is always regarded as containing zero, which is simulated by turning off data selector enabling signal.
ZROB	1505	Same as ZROA for bus B.

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COMMENT AND EVALUATION SHEET

ND-05.004.01 NORD-50 CPU Hardware Manual I

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM: _____

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