NORD

COMPUTER SYSTEMS

CIRCUIT DIAGRAM SYMBOLS

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C I R C U I T D I A G R A M

S Y M B O L S

1. INTRODUCTION

The paragraphs below describe the rules used in obtaining logic expressions and definitions of logic signals and the symbols used to represent logic elements in our circuit diagrams. The system is based on elements of the NAND/NOR family, which is now most common in use. It is also supposed to be NPN elements with positive supply voltage.

2. LOGIC EXPRESSIONS

The two states of the binary variable as represented by a voltage in the circuit system are defined as follows:

State 0 : $V < 0{,}4$ volt or "low"
State 1 : $V > 2{,}4$ volt or "high"
Undefined : $0{,}4$ volt $< V < 2{,}4$ volt

The state of a variable under given conditions is indicated by index 0 or 1 respectively. Index 1 may be omitted, so that A and A_1 are identical.

Example 1

ADD_0: The signal is low when the instruction ADD is present (decoded from the instruction register).

Example 2

$ADD = IR15_0 14_1 13_1 12_0 11_0$

The signal ADD is decoded from the instruction register, IR, bits 11 through 15 and is "true" when IR15=IR12=IR11=0 and IR14=IR13=1.

The symbols used for the logic operations "AND" and "OR" are the standard arithmetic multiplication and addition symbols, including the rule for omitting the multiplication sign.

Example 3

$A \cdot B_0 \cdot C$ or $A_1 \cdot B_0 \cdot C_1$ or $A_1 B_0 C_1$
$D+E+F_0$ or $D_1+E_1+F_0$
$(A_0 B_1 + A_1 B_0)\ (C_0 D_1 + C_1 D_0)$

The "name" of triggering signals should be chosen to reflect the active state of that signal, which means that a signal which is active when it is high should have index 1 and a signal which is quiescent when it is high should have index 0.

Example 4

The clock input to a SN7474 flip-flop is requiring a positive pulse and may be called $AS1$.
The clear input to the same flip-flop requires a negative going pulse and should be labelled $AS2_0$.

3. LOGIC ELEMENTS

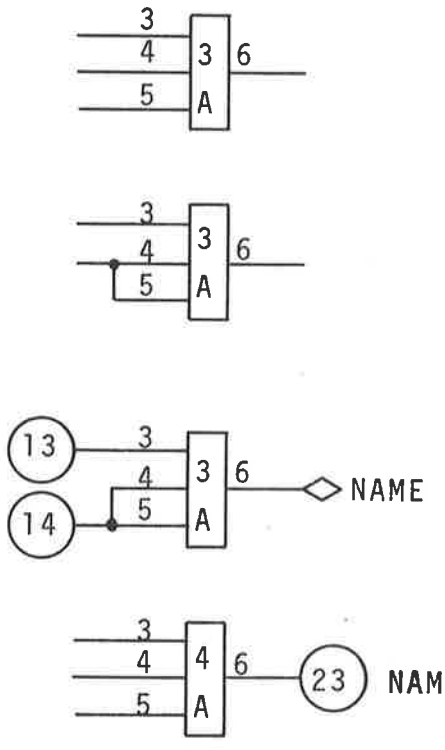
The symbols used for logic elements are a resust from several years of experience in design and manufacture og digital systems. The symbol for a "NAND" gate is shown as such, and no attempt is made to reduce the diagram to a system containing the basic family of AND/OR/INVERT elements. A "NAND" element is a "NAND" element, and one single element is frequently used for both "AND" and "OR" functions simultanously.

3-input NAND 2-input NOR

The selected symbols shown above are used for the basic logic elements, NAND and NOR, which together make a complete logic family. The symbols are chosen for compactness and ease of drawing, and consist of straight lines only. The logic diagrams of course become completely circuit oriented, and corresponds one to one with the actual hardware.

4. CIRCUIT DIAGRAMS

All circuit elements are mounted on printed circuit boards. The position of the circuit on this board is shown by the coordinates of the circuit, column first, identified by a number and then row, identified by one of the letters A, B, C or D. These coordinates together with the pin number of the circuit package are shown in the logic diagrams.



Input terminals are if possible to the left and output to the right. The distance between input lines should be 5 mm. If an unused input terminal is connected to a used terminal this should be shown in the diagram. Circled numbers represent card terminals.

Instead of connecting an output signal to another circuit or an output terminal the signal line may be terminated in a diamond head and given a name. This name usually occurs as input signal other places in the diagram.

Example

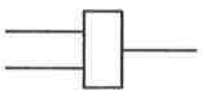
Pin 11 of the circuit in position 2B is referred to as 2B11.

5. SYMBOLS FOR TI SERIES 74N CIRCUITS

The integrated circuit family used by NDE is the Texas Instrument Series 74N, and a complete list of the standard symbol(TI's) and NDE's corresponding symbol is given below.

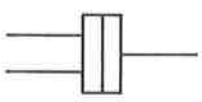
5.1 7400

Quadruple 2-input NAND gate



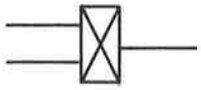
5.2 7401

Quadruple 2-input NAND gate with open collector output



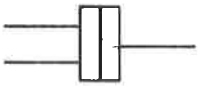
5.3 7402

Quadruple 2-input NOR gate



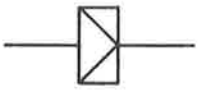
5.4 7403

Quadruple 2-input NAND gate with open collector output



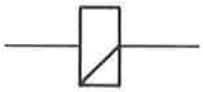
5.5 7404

Hex inverter



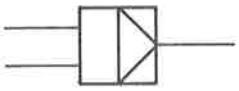
5.6 7405

Hex inverter with open collector output



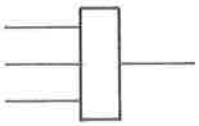
5.7 7408

Quadruple 2-input AND gate



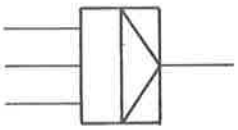
5.8 7410

Triple 3-input NAND gate



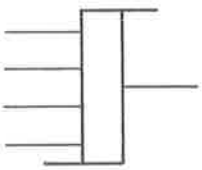
5.9 74H11

Triple 3-input AND gate



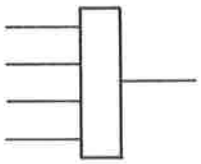
5.10 7413

Dual NAND Schmitt triggers



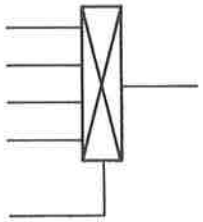
5.11 7420

Dual 4-input NAND gate



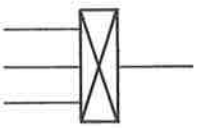
5.12 7425

Dual 4-input NOR gate with strobe



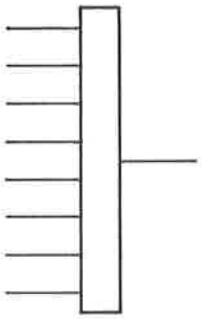
5.13 7427

Triple 3-input NOR gate



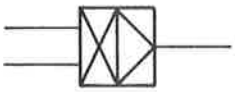
5.14 7430

8-input NAND gate



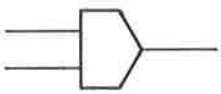
5.15 7432

Quadruple 2-input OR gate



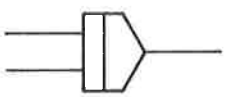
5.16 7437

Quadruple 2-input NAND buffer



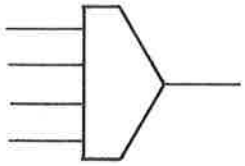
5.17 7438

Quadruple 2-input NAND buffer
(Open collector)



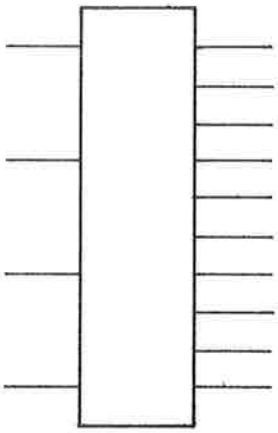
5.18 7440

Dual 4-input NAND buffer



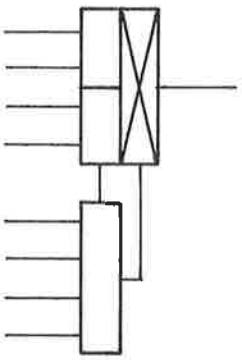
5.19 7442

4-line-to-10-line decoders (1-of-10)



5.20 7450 - 7451 - 7460

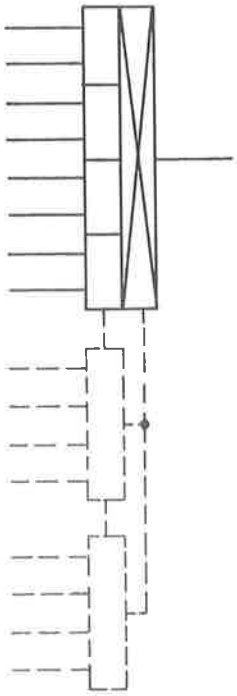
2 x 2 NAND-AND



The four-input gates are 7460 circuits

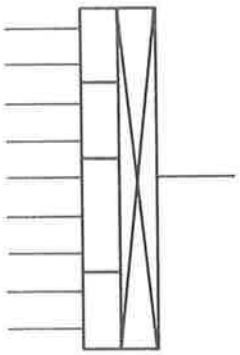
5.21 7453 - 7454

4 x 2 NAND-AND



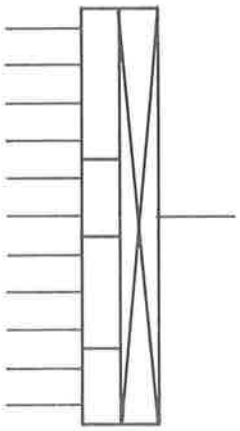
5.22 74H54

Expandable 2-2-2-3 - input AND-OR-invert gates



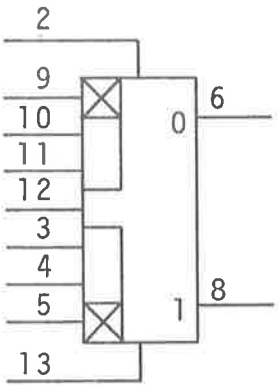
5.23 74S64

4-2-3-2 - input AND-OR-invert gates



5.24 7470

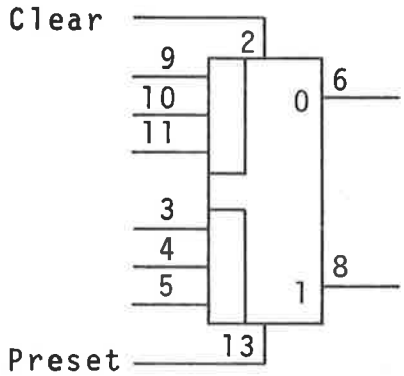
J - K flip-flop



The AND gate oposite the 0 output is equal to K-inputs. The preset and clear input is pointing to that side of the flip-flop which becomes "high" for a corresponding "low" pulse. See 5.21

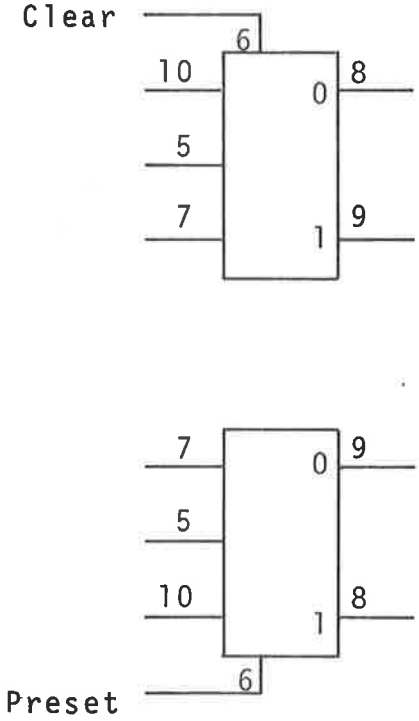
5.25 7472

J - K master-slave flip-flop



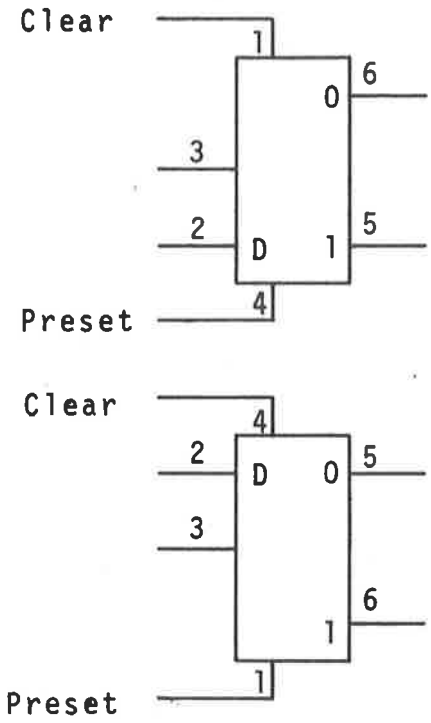
5.26 7473

Dual J - K master-slave flip-flop



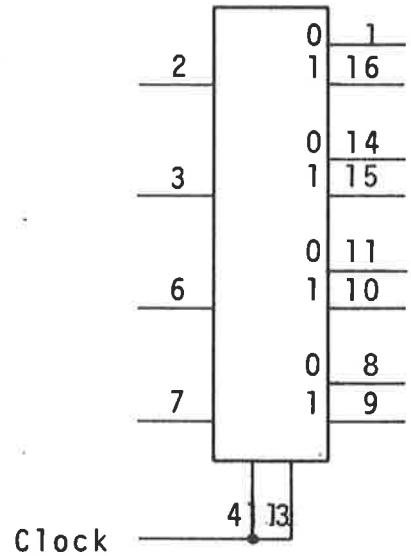
5.27 7474

Dual D-type edge-triggered flip-flop



5.28 7475

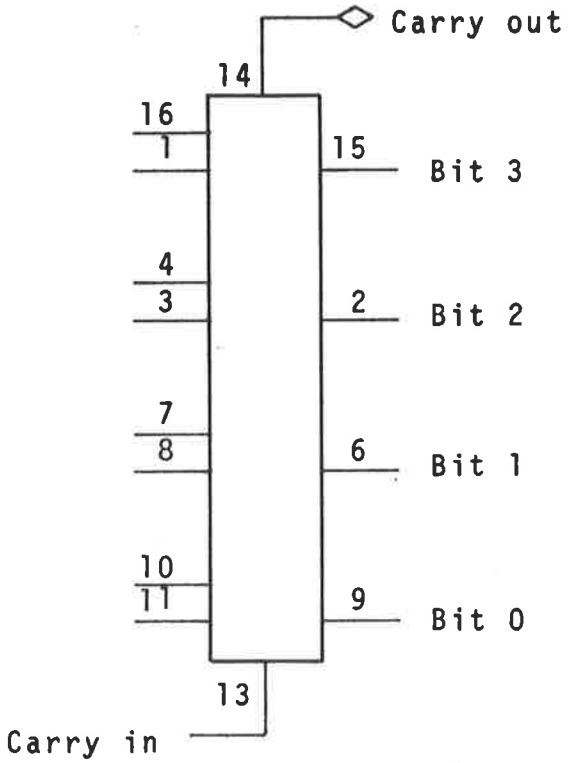
Quadruple bistable latch



The clock input on pins 4 and 13

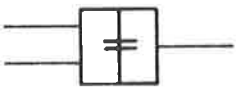
5.29 7483

4-bits binary full-adder



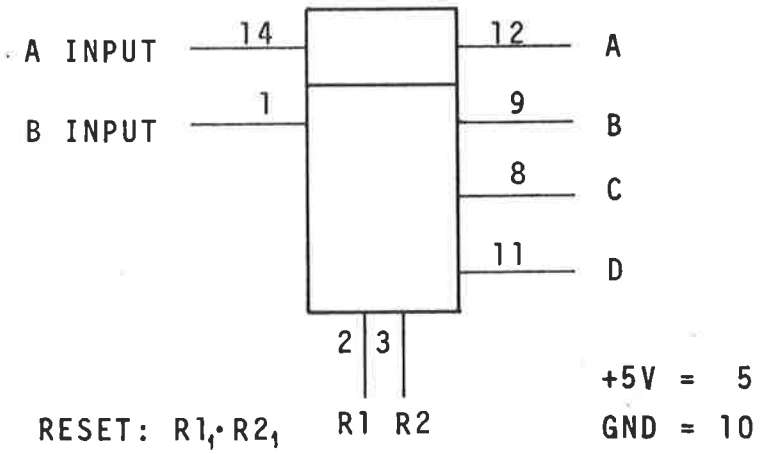
5.30 7486

Quadruple 2-input exclusive-OR element



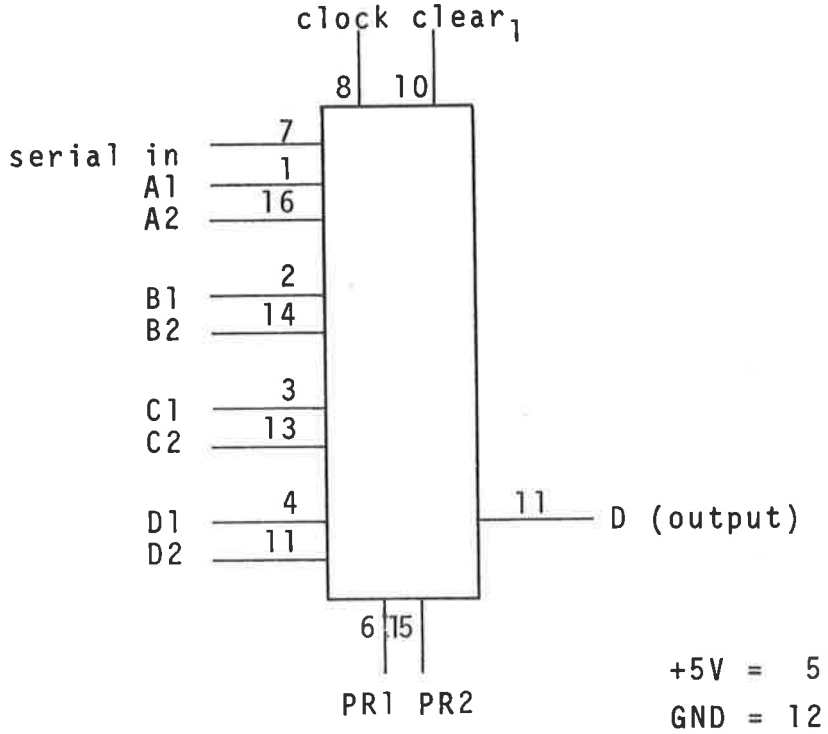
5.31 7493

4-bit binary counter



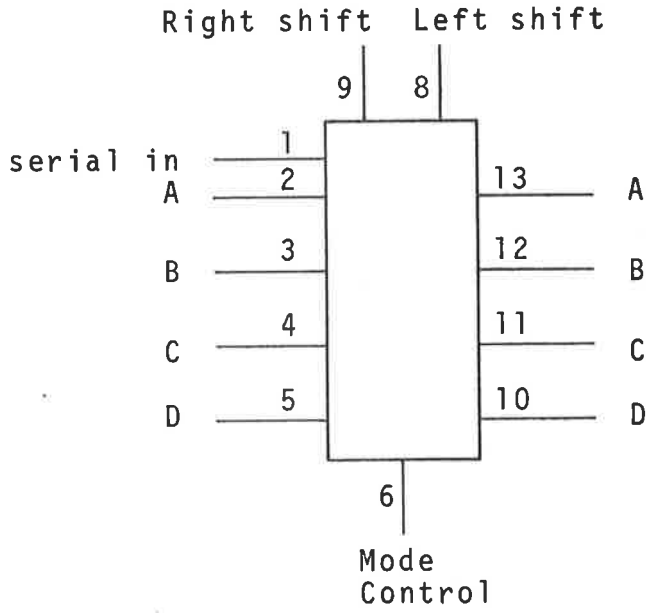
5.32 7494

4-bit shift register



5.33 7495

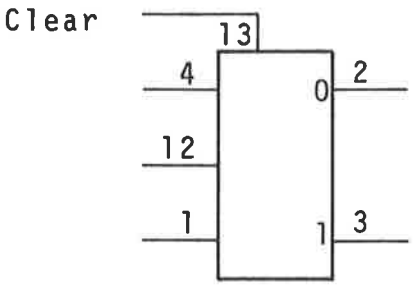
4-bit right-shift, left-shift register



Mode Control: 0 = Shift serial
1 = Shift parallell

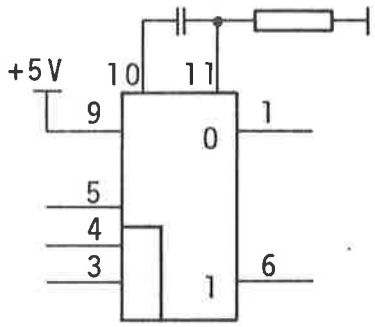
5.34 74107

Dual J-K Master-Slave flip-flop



5.35 74121

Monostable multivibrator



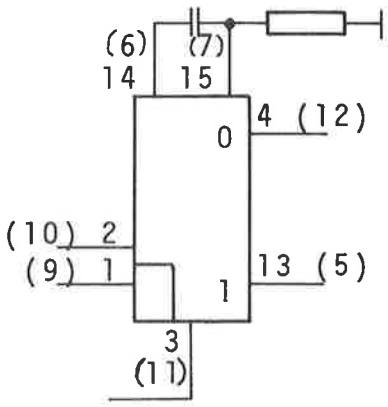
$T \approx 0{,}7 \cdot RC$

Rmin = 1.4 kΩ

Rmax = 40 kΩ

5.36 74123

Retriggerable monostable multivibrator with clear



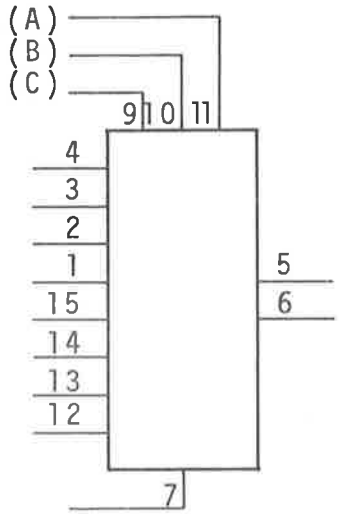
$T \approx 0{,}32 \cdot RC$

Rmin = 5 kΩ

Rmax = 50 kΩ

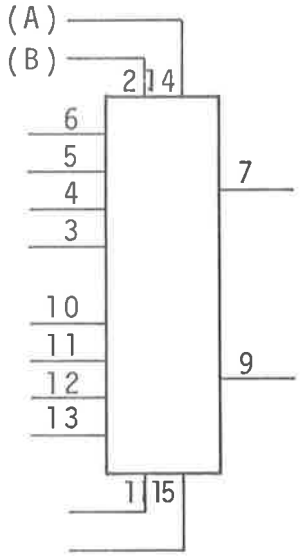
5.37 74151

Data selector/'multiplexer



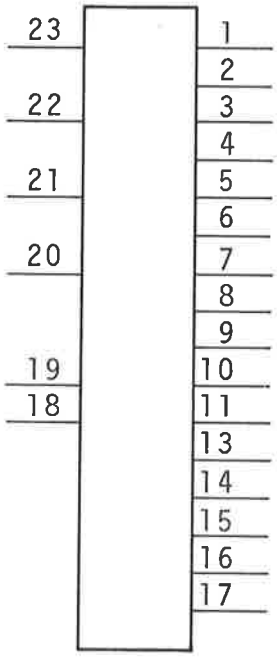
5.38 74153

Dual 4-line-to-1-line data selector/ multiplexer



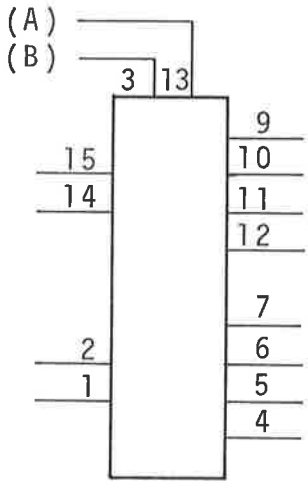
5.39 74154

4-line-to-16-line decoder / demultiplexer



5.40 74155

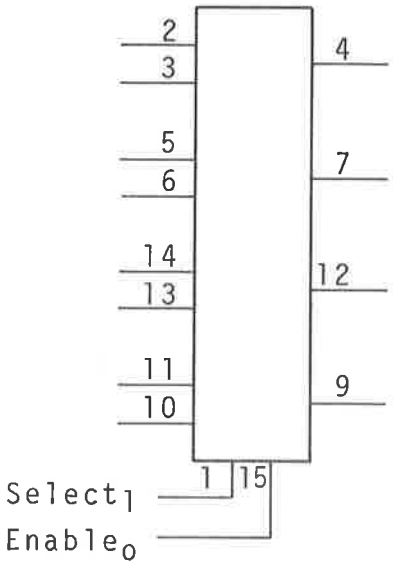
Dual 2-line-to-4-line decoder / demultiplexer



74156 is equal to 74155

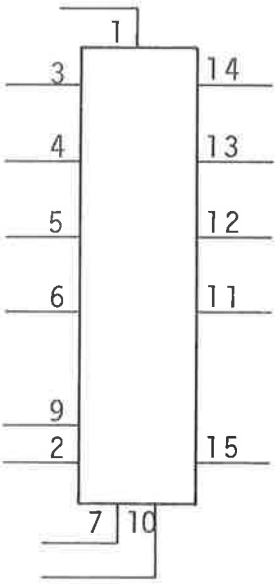
5.41 74157

Quadruple 2-line-to-1-line



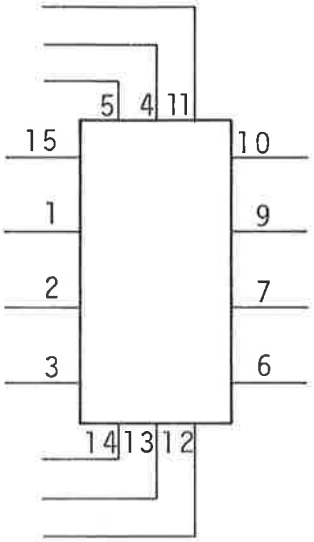
5.42 74161

Synchronous 4-bit counter



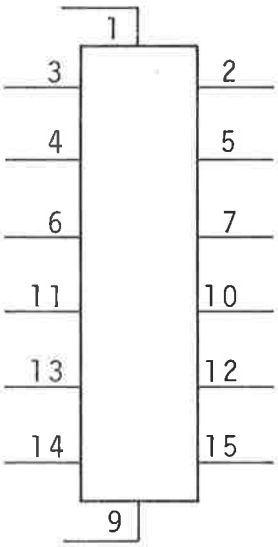
5.43 74170

4-by-4 register file



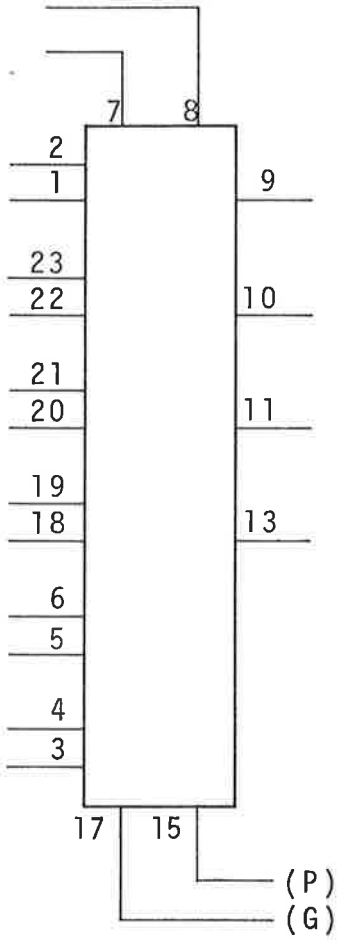
5.44 74174

Hex D-flip-flop



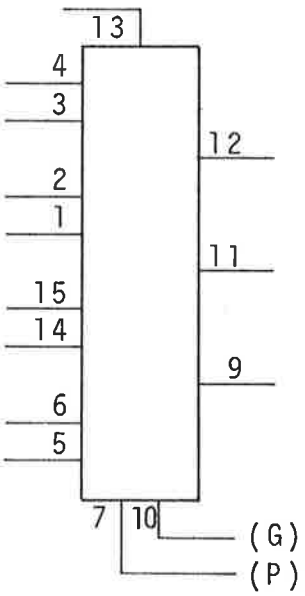
5.45 74181

Arithmetic logic unit/function generator



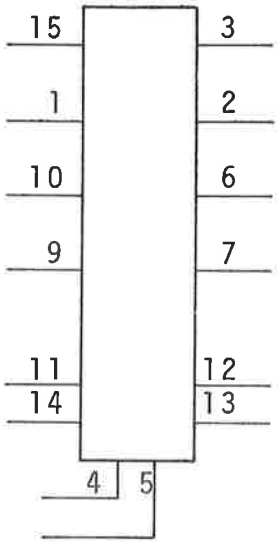
5.46 74182

Look-ahead carry generator



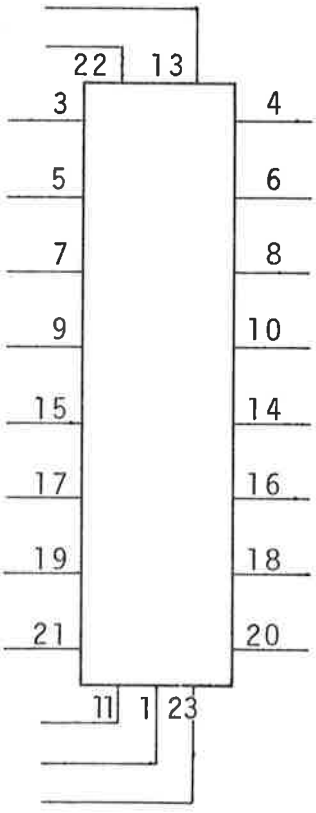
5.47 74191

Synchronous up/down counter



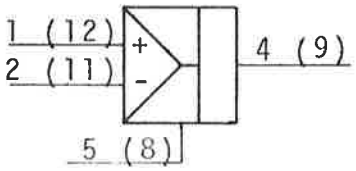
5.48 74198

8-bit shift register

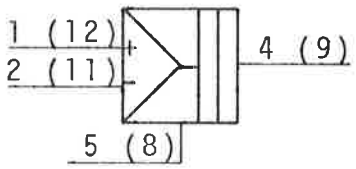


6. DUAL LINE RECEIVERS AND DRIVERS

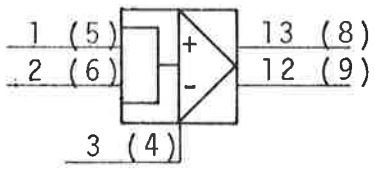
6.1 7507



6.2 7508 (open collector)

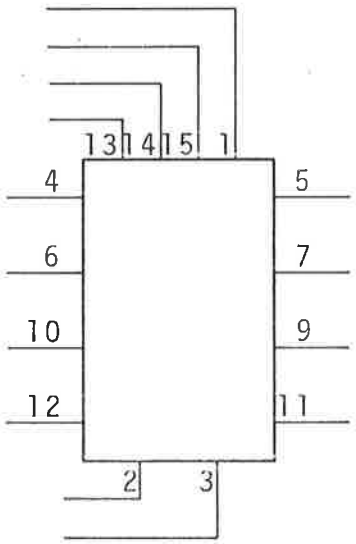


6.3 7509 - 7510



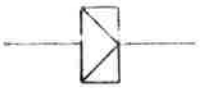
7. INTEL

7.1 3101 (equal to Texas no. 7489)
64-bit read/write memory



8. MOTOROLA MRTL INTERGRATED CIRCUITS WITH POSITIV LOGIC USED:

8.1 MC889P
Hex-inverter



8.2 MC834P
Two-input NOR