OPERATOR'S COMMUNICATION INSTRUCTION SURVEY

CONTROL FUNCTIONS (Does not affect DISPLAY)

System Control

OPCOM ☐		Enter Operator's Communication mode
	ESC key	Leave Operator's Communication mode
MCL ☐	MACL↵	Generate Master Clear
STOP ☐	STOP↵	Stop Program and enter OPCOM Mode
LOAD ☐	& or $	Load according to ALD code (read by I12/)
	xxxxxx& or xxxxxx$	Load from device x

Program Control

!	Continue Program from address of program counter
xxxxxx!	Start Program from address x
Z	Execute a Single Instruction according to program counter
xxxxxxZ	Execute x Instructions from address of program counter
xxxxxx ●	Execute Program until program counter = x and stop
xxxxxx"	Execute Instruction Code x repeatedly
xxxxxxIO/nnnnnn	Execute IOX instruction with device number x
	OPR = Output Data; n = Returned Data

Miscellaneous Functions

xxx#	Do Memory Test in segment x from address of B register to address of X register. P = Fail Address, T = Fail Bits, D = Fail Pattern, L = Test Pattern.
space or @	Delete entry
*nnnnnn	Current Location of memory examine is n (16 least sign. bits)
OPR/nnnnnn zzzzzz↵	Change Operators Panel "Switches" from n to z

DISPLAY FUNCTIONS (Affects only DISPLAY)

uuzzyxF↵	Define Format of Displayed Information (F↵ is default)

    x (3 bits): 0 = Octal   1 = Decoded according to z

                 2 = Binary

    y (3 bits): 0 = Normal   1 = Stretch Zeros

                 2 = Stretch Ones   3 = Stretch Zeros and Ones

    z (6 bits): Decode the 4 bits z to z+3 to a ONE among ZEROS.

    u (4 bits): for Display Processor Maintenance

           1 = Display Year and Month

           2 = Inhibit message

           4 = Initialize panel processor

          10 = Abort message

yxBUS/	Display Memory Accesses on NORD-100 Bus

    x (3 bits): 0 = Undefined   1 = Read Access

                 2 = Write Access   3 = Write or Read Access

    y (3 bits): 0 = CPU Data   1 = DMA Data

                 2 = CPU Address 3 = DMA Address

ACT/	Display Computer Activity (default after MACL)

MONITOR FUNCTIONS (Also shown on DISPLAY)

Memory

E↵	Set Physical Examine mode (default after MACL)
xE↵	Set Virtual Examine mode. Map via page table x.
xxxxxxxx/ nnnnnn zzzzzz↵	Examine and Change Content of memory address x from n to z. x is 24 bits at Physical and 16 bits at Virtual Examine.
xxxxx < yyyyyy↵	Dump Content of memory from address x to address y. Select 64K area of last Examine.

Registers

xxRy/ nnnnnn zzzzzz↵	Examine and Change Content of register Ry on level xx from n to z. Ry may be written as R0=S, R1=D, R2=P, R3=B, R4=L, R5=A, R6=T, R7=X.
xx < yyRD↵	Dump Registers R0 to R7 from level x to level y.
U/ nnnnnn	Content of User Register is n
OPR/nnnnnn zzzzzz ↵	Change Operators Panel "Switches" from n to z

Internal Registers

Ixx/ nnnnnn   Content of Internal Register No. x is n

x (4 bits):

0 = PANS	1 = STS	2 = OPR
3 = PSR	4 = PVL	5 = IIC
6 = PID	7 = PIE	10 = CSR
11 = ACTL	12 = ALD	13 = PES
14 = PCR	15 = PEA	

Iyy/ nnnnnn zzzzzz↵   Deposit z in Internal Registers No. y (n is dummy)

y (4 bits):

0 = PANC	1 = STS	2 = LMP
3 = PCR	5 = IIE	6 = PID
7 = PIE	10 = CCLR	11 = LCIL
12 = UCIL	15 = ECCR	

IRD↵	Dump Internal Registers 0 - 15 (only in STOP)
xx < yyRDE↵	Dump Scratch Registers from level x to level y

Deposit Rules

Content is only changed by zzzzzz↵ in STOP mode and by zzzzzzDEP↵ in STOP or RUN mode.

Content is unchanged by ↵ in STOP or RUN mode and by zzzzzz↵ in RUN mode (? is answered).

Explanations:

☐ = Control Panel Button
↵ = Carriage Return
n = computer answer

All other characters are typed by Operator.

ND-100 INTERNAL REGISTERS AND THEIR BIT ASSIGNMENT:

INTERNAL REGISTER NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
[0] TRA PANS	PAN PRS	PAN FULL	READ	COM RDY	0		PCOM		M	C	U	O	RPAN Q	Z	TG	PTM
[0] TRR PANC	0	0	READ	0	0		PCOM		M	C	U	O	WPAN Q	Z	TG	PTM
[1] TRA STS	ION	PONI	SEXI	N100			PIL									
[1] TRR STS					NOT ASSIGNED											
[2] TRA OPR																
[2] TRR LMP																
[3] TRA PSR	FF	PM		NOT ASSIGNED			PT		PI	APT	PIL		VPN			
[3] TRR PCR			NOT ASSIGNED				PT		APT		1	0	1	0	1	1
[4] TRA PVL											1	0	1	0	1	1
[5] TRA IIC			NOT ASSIGNED								PREV LEVEL		IIC CODE			
[5] TRR IIE			NOT ASSIGNED		POW	MOR	PTY	10X	PI	Z	II	PF	MPV	MC		0
[6] TRA/TRR PID																
[7] TRA/TRR PIE																
[10] TRA CSR					NOT ASSIGNED							MAN DIS	CON DIS	CUP		0
[10] TRR CCLR						DATA LESS										0
[11] TRR LCILR	N.A.		3					LOWER LIMIT PAGE NUMBER								
[11] TRA ACTL								ADDRESS								
[12] TRA ALD	0	0	M	0												
[12] TRR UCILR	N.A.		3					UPPER LIMIT PAGE NUMBER							16	
[13] TRA PES	FETCH	DMA	FATAL		ERROR CODE				UPPER MEMORY ADDRESS		20	21	19	18	17	16
[14] TRA PCR	0	0	0	0			PT		APT		0	0	PIL		RING	
									*							
[15] TRA PEA			NOT ASSIGNED					LOWER MEMORY ADDRESS								
[15] TRR ECCR		TEST 6	DIS	ANY										TEST 15		0

* REQUIRED LEVEL INFORMATION IN THE A-REGISTER BEFORE THE TRA INSTRUCTION

N.A. = NOT ASSIGNED