

**NORD-50 Hardware
Maintenance Manual**

ND-30.010.02

NORSK DATA A.S



NORD-50 Hardware Maintenance Manual

ND-30.010.02

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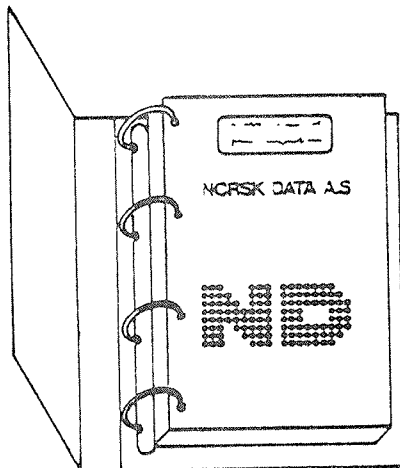
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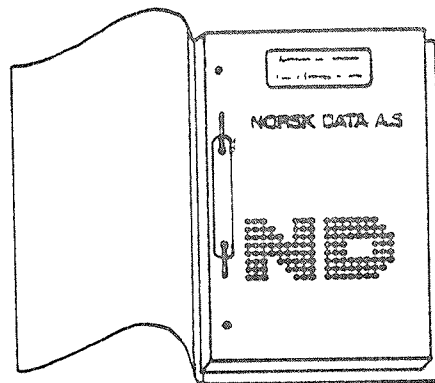
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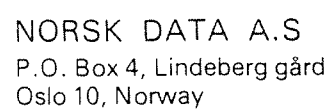
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Preface:THE PRODUCT

This manual covers the:

NORD-50 CPU

The NORD-50 CPU is used in all ND 1400 configurations.

THE READER

This manual has been prepared for Norsk Data Service Department field service engineers and technical personnel directly involved with maintaining the NORD-50 CPU.

PREREQUISITE KNOWLEDGE

A general knowledge of the NORD-10 S hardware including the Input Output and Memory System. A familiarity with the ND Operating System SINTRAN.

THE MANUAL

Maintenance information is provided in eight chapters in this manual. Chapter numbers and a brief description of their contents are listed below:

- Chapter 1 - System architecture and physical layout of the NORD-50 CPU.
- Chapter 2 - NORD-50 hardware summary. Description of the three racks in the NORD-50 CPU and the operators panel.
- Chapter 3 - The NORD-50 Monitor. A NORD-50 Monitor command summary containing the commands needed for hardware maintenance of the NORD-50 CPU.
- Chapter 4 - NORD-50 Error Messages. The error messages are listed with hardware maintenance information.
- Chapter 5 - NORD-50 Test Program Information. Test programs for the external arithmetic and the CPU are overviewed and described.
- Chapter 6 - NORD-50 Memory System. The multiport memory in a NORD-50 configuration is depicted. This section also contains Memory Test Program information.
- Chapter 7 - NORD-50 Memory Expansion. The hardware implementation and the software command SET-MEM is explained in detail.
- Chapter 8 - This section covers the power system.

RELATED MANUALS

Manuals relating to the general and functional description of the NORD-50 are as follows:

Norsk Data Number	Title
ND - 05.003	NORD-50 Reference Manual
ND - 30.007	NORD-50 Test Programs
ND - 05.007	NORD-50 Functional Description
ND - 06.005	NORD-10 NORD-50 Communication System
ND - 60.083	NORD-50 Loader Users Guide
ND - 60.076	NORD-50 MONITOR Users Guide and System Documentation
ND - 60.075	NORD-50 Assembler
ND - 60.095	NORD-50 FORTRAN Reference Manual
ND - 60.098	NORD-50 BRF Editor

The manual that deals with the special systems interfaced with or utilized with the NORD-50 is:

Norsk Data Number	Title
ND - 06.007.01	BIG MULTIPORT MEMORY

These manuals are described in Appendix H, Documentation Review. In addition special hardware and software machine books are prepared for each computer by Norsk Data. These are on site working notebooks containing information about that special computer hardware and software configuration.

The Norsk Data Service Department also utilizes a Hardware Maintenance Notebook that covers the procedures utilized by Norsk Data in Norway.

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1. NORD-50 COMPUTER SYSTEM ARCHITECTURE AND PHYSICAL LAYOUT

This section starts with a short description of the Nord-50 computer system architecture followed by the highlights and the electrical and physical specifications for the Nord-50 cabinet.

The rest of the section deals with schematics of the physical layout inside a Nord-50 cabinet.

To gain access to the interior of a Nord-50 the front and rear doors have to be removed. This door removing procedure is depicted in Figure 1.

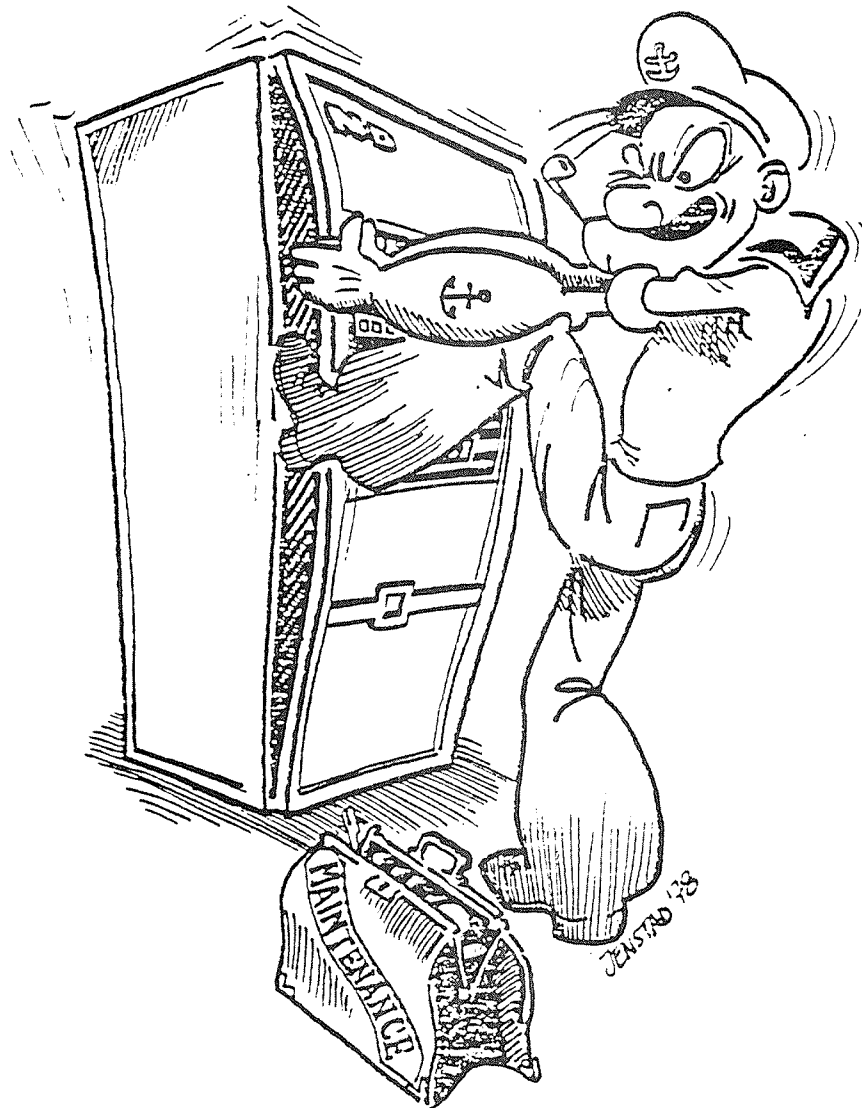


Fig. 1. Door removing procedure

In Figure 2 the physical layout of the main components is shown. The Nord-50 shown in Figure 2 has the multiport memory installed in the rear of the cabinet.

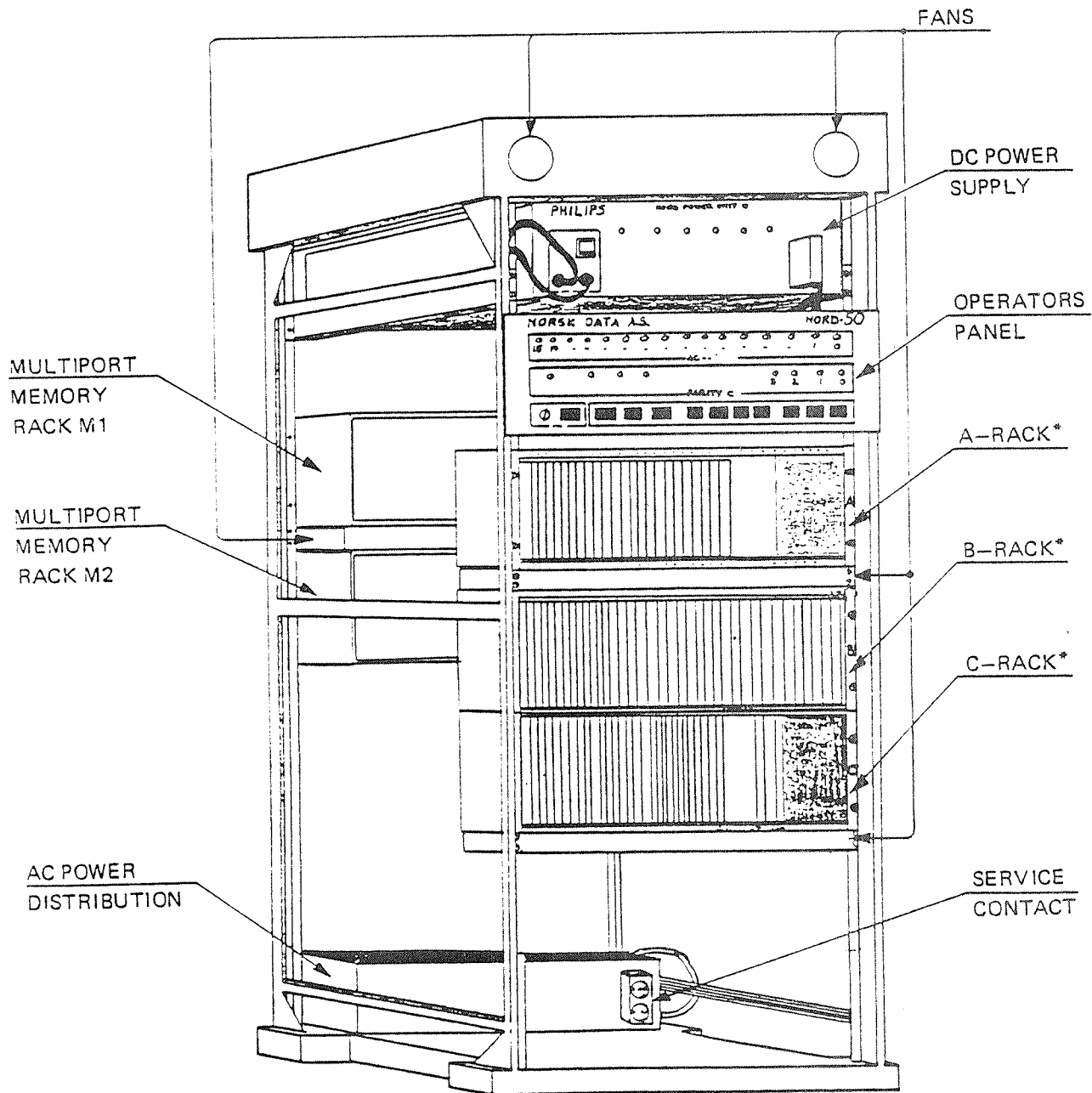


Fig. 2. NORD-50 main component physical layout

More specific information concerning the three racks of the Nord-50 is shown in Figure 3.

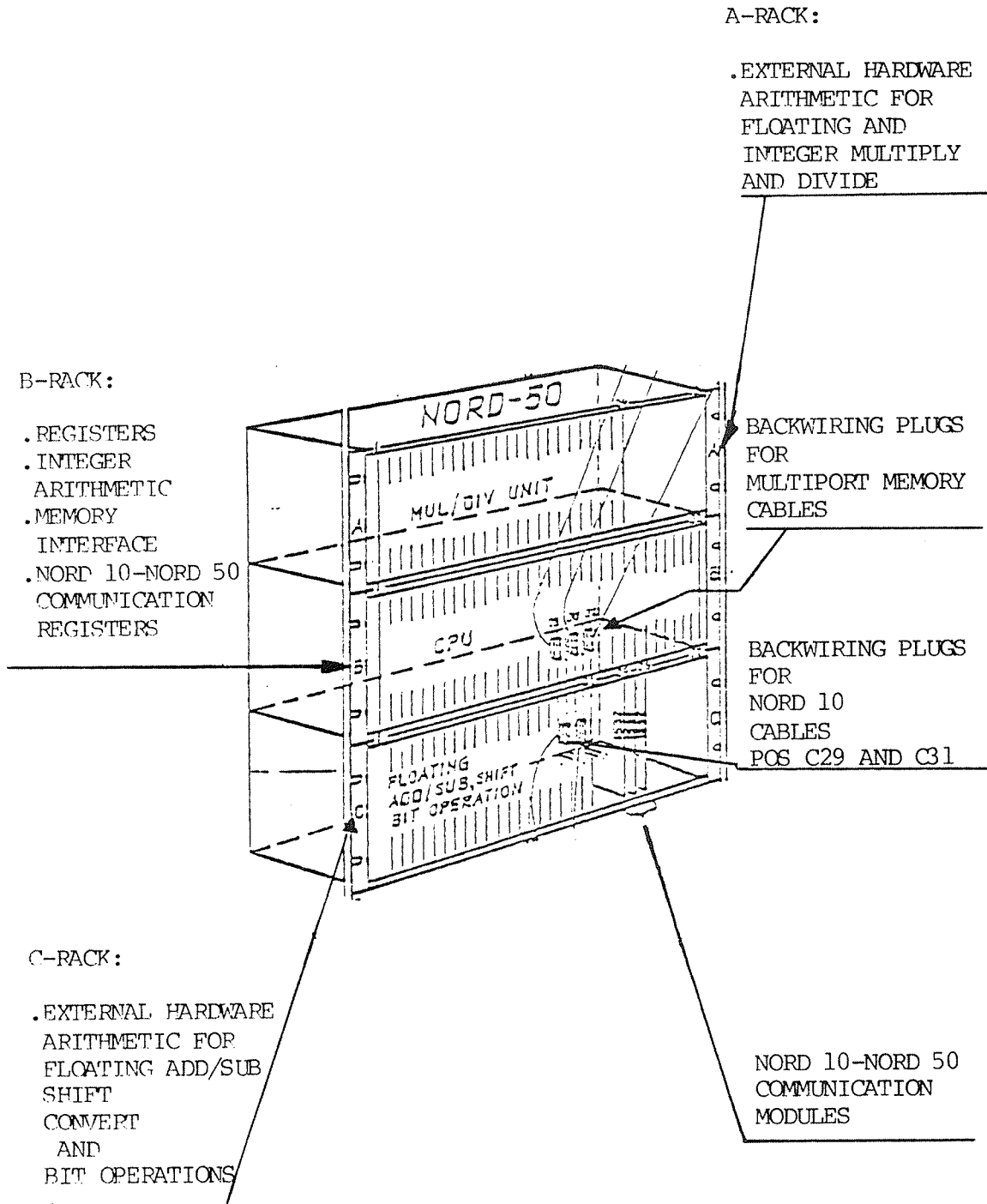


Fig. 3. NORD-50 A B AND C rack physical layout

1.1. Nord-50 Computer System Architecture

The Nord-50 Computer System consists of:

- Nord-10/S CPU
- Nord-10/S I/O System and Peripherals
- Nord-50 CPU
- Multiport Memory System

Figure 4 illustrates a Nord-10/S Computer System configuration in a Nord-50 Computer System. The Nord-10/S has the following functions:

- Acting as the I/O System for the Nord-50 by performing I/O transfer to/from the Nord-50 memory.
- Supervision and synchronization of the Nord-50. See Figure 5.
- Running the operating system, SINTRAN III.
- Generating Nord-50 executable machine code via Nord-50 Assembler or FORTRAN Compiler.

To control the Nord-50, the Nord-10/S has a Nord-10/S - Nord-50 communication interface for starting and stopping the Nord-50. In addition, different control and status information is passed between the processors, such as specified break for overflow, underflow, divide by zero, memory protect error, etc. The communication interface also supports a memory examine/deposit function such that the Nord-10/S may reach all of Nord-50 memory even if this memory is larger than the normal maximum Nord-10/S addressable memory of 512K bytes.

In addition, both processors are connected to the Multiport Memory System and may both use the shared memory. Therefore, this area also provides means of communication between the processors. Each processor may also have its private memory, inaccessible to the other.

Note. With the DMA-ADDRESS-EXTENDER option installed, the disk may access the whole memory, including the Nord-50 private memory.

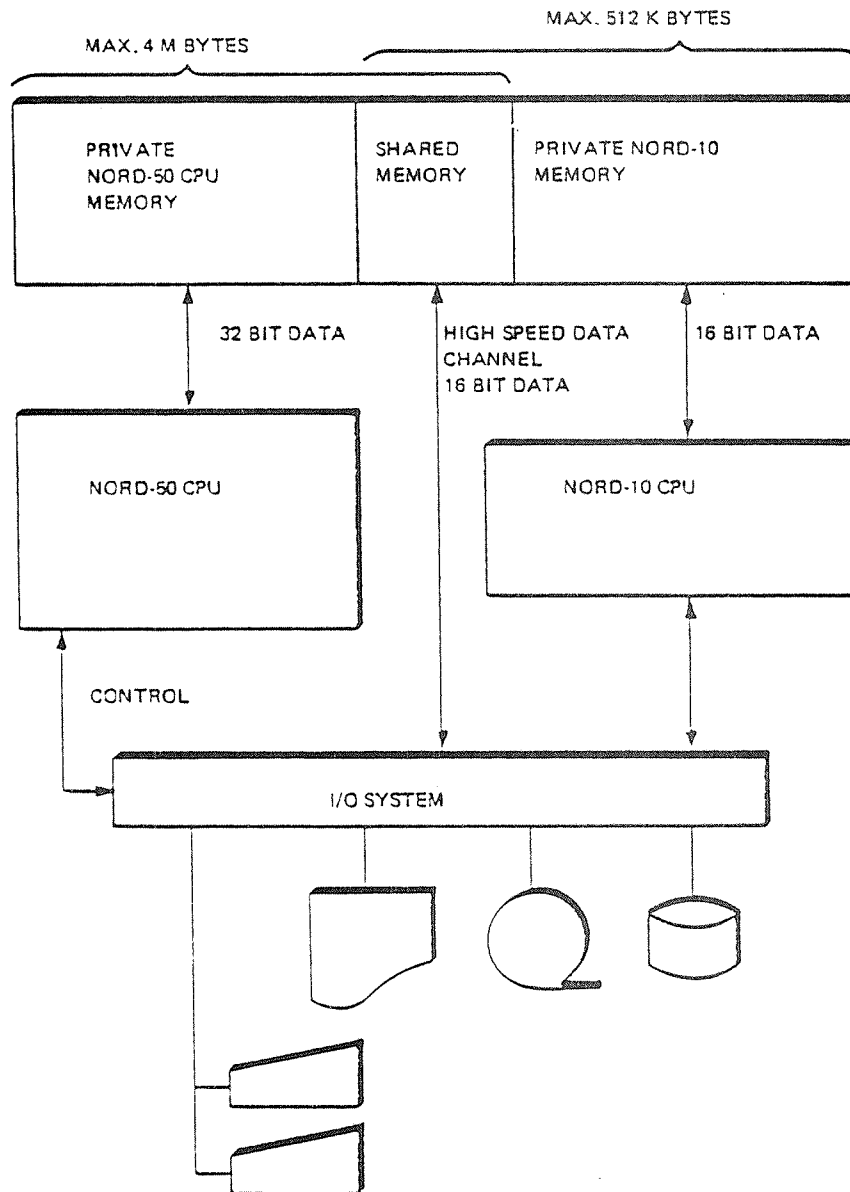
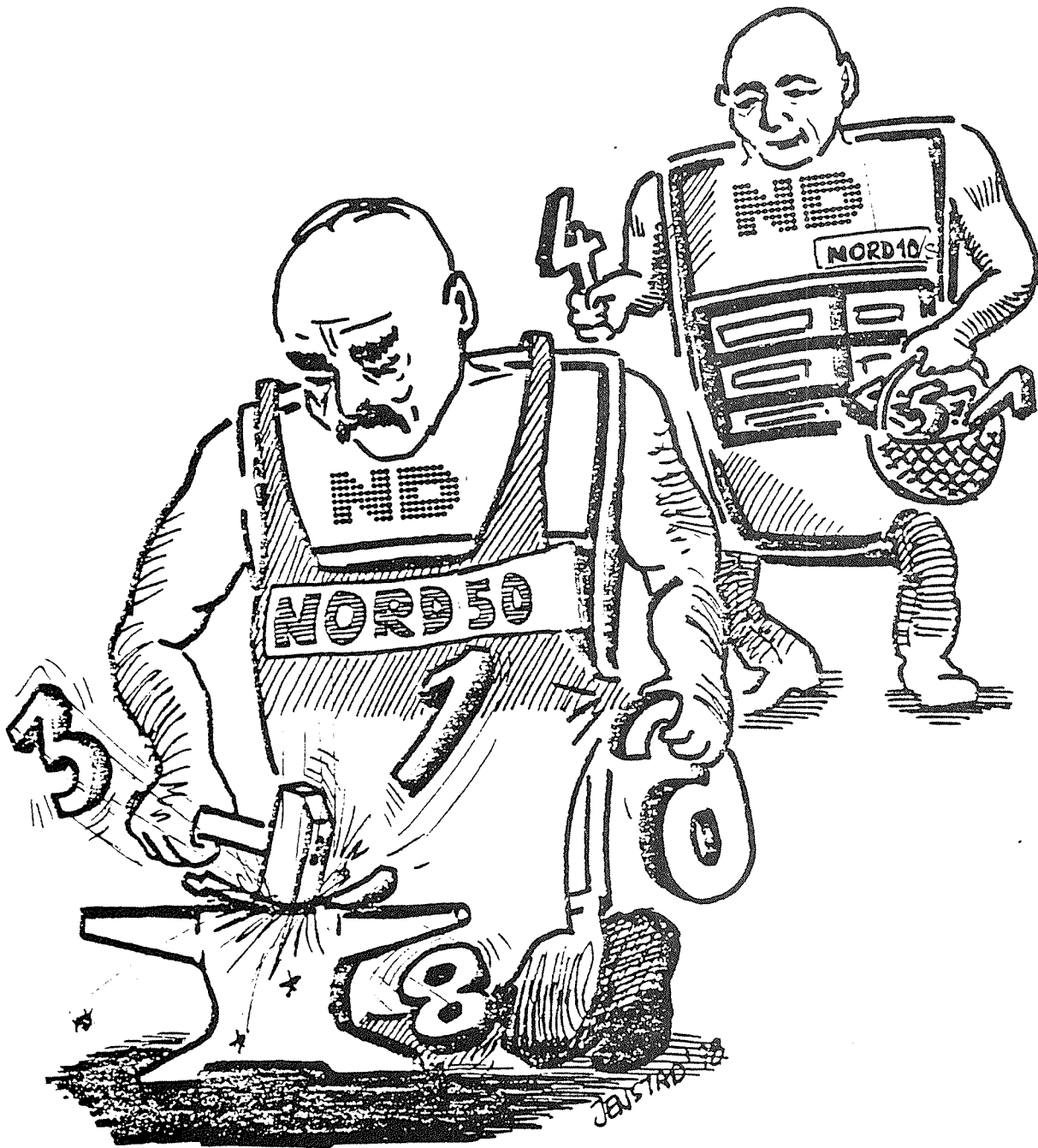


Fig. 4. NORD-50 computer system parts



THE NUMBER CRUNCHER

Fig. 5. Supervision and synchronization of the NORD-50

Some other important attributes of the Nord-50 CPU are as follows:

- 32 bit word length.
- Physical addressing range of 4Mbytes (20 address bits).
- High data precision - Floating point format of 23 or 55 bit mantissa and a 9 bit exponent plus a sign bit.
- Extensive instruction set with single and double precision floating point instructions.
- Multiported shared and private memory.
- Static high speed, private memory for frequently used code and data.
- Instruction look-ahead for increased performance.
- Specialized arithmetic unit for floating multiply/divide and integer multiply/subtract.
- Specialized arithmetic unit for shift, bit operations and floating add/subtract.
- 2 identical blocks of 64 registers, each 32 bits, to obtain increased speed in register operations.

1.2. Electrical and Physical Specifications (Nord-50 Cabinet)

Power consumption 1000W

Power requirements:

ND 1400 220VAC+/- 10%, 50Hz+/-2Hz
ND 2400 110VAC+/- 10%, 60Hz+/-2Hz

Operating temperature + 10 degrees C to + 35 degrees C

Operating relative humidity . . . + 10% to 90% noncondensing

Physical dimensions:

Width 58 cm
Height 160 cm
Depth 68 cm
Weight 100 kg

2.NORD-50 HARDWARE SUMMARY

2.1.General

This section starts with some general comments about debugging the Nord-50. It then continues with an overview of the Nord-50 hardware contained in the three 19-inch racks (also referred to as Rack-A, Rack-B and Rack-C). For each of these three racks the main functions are listed followed by a data flow and a short module description.

Figure 6 shows a Nord-10 - Nord-50 Configuration.

Section:	Describes:
2.3	The B-Rack or the Nord-50 CPU rack.
2.4	The A-Rack* or the multiply/divide unit.
2.5	The C-Rack* or the floating add/subtract and SHIFT UNIT. The C-Rack also contains the Nord-10/Nord-50 communication hardware.
2.6	The Nord-50 Operator's Panel.
	*The A and C-Racks are also referred to as external arithmetic.

2.2.Nord-50 Hardware Maintenance

Of the 79 modules distributed on the A,B and C-Racks, only 27 modules are different. This makes the Nord-50 easy to troubleshoot. All modules with the same number are exchangeable.

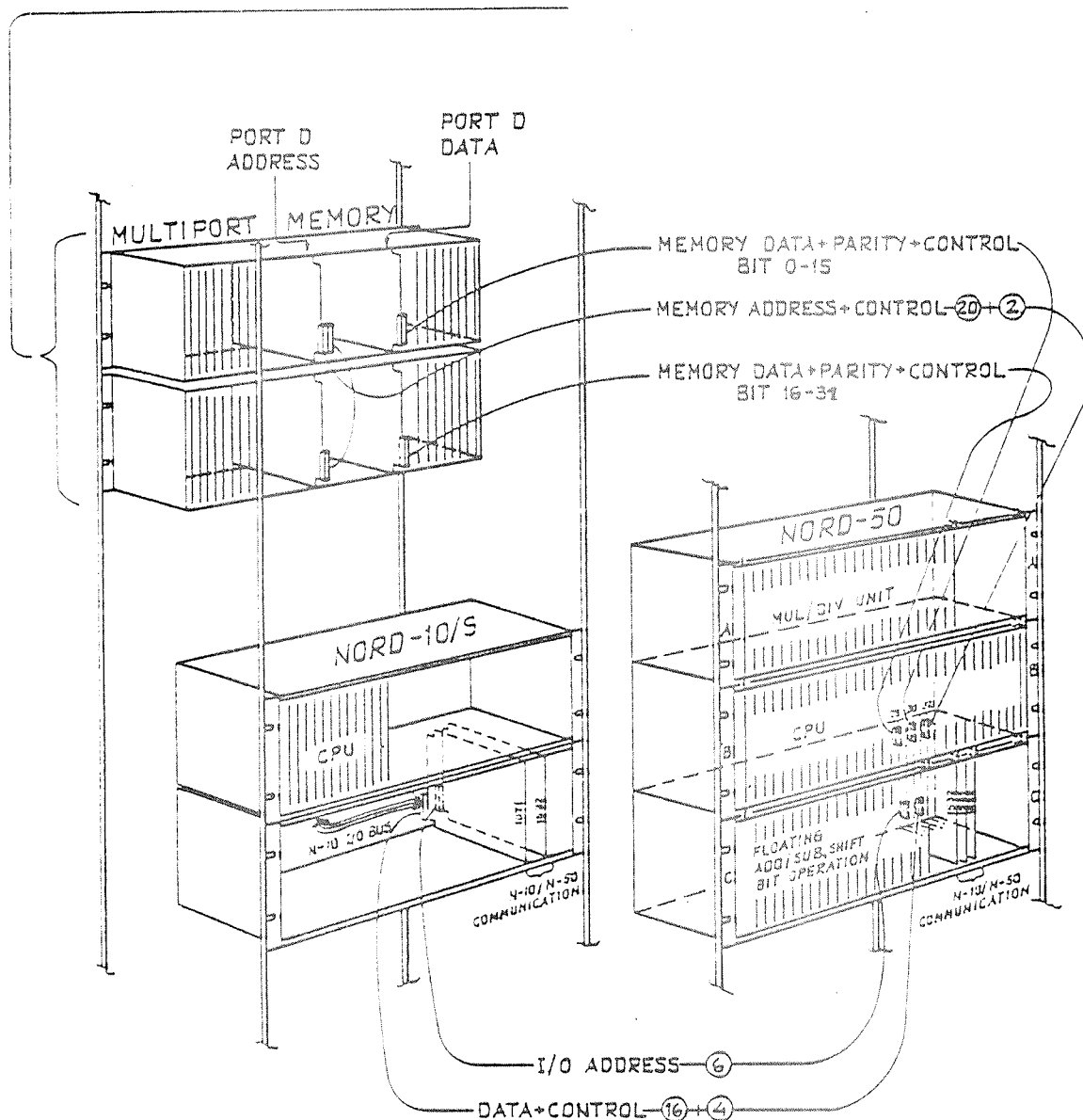
If the test programs indicate a hardware error, swap modules and run the test once more to see if the failing test pattern is changed. Because different parts of the module are used in the different positions, one module may work OK in one position but will fail in another position.

NOTE THESE:

+ THE 5V DC POWER SHOULD NOT BE TURNED OFF
DURING MODULE SUBSTITUTION.

Note.

The Multiport Memory can also be located in the NORD-50 Cabinet.



NORD-10 - NORD-50
CONFIGURATION

Fig. 6. NORD-10 - NORD-50 configuration

+ ERRORS ON INSTRUCTIONS BEING EXECUTED IN THE A-RACK (MUL/DIV) COULD BE CAUSED BY A MALFUNCTION IN THE B-RACK OR IN THE C-RACK*.

+ ERRORS ON INSTRUCTIONS BEING EXECUTED IN THE C-RACK COULD BE CAUSED BY A MALFUNCTION IN THE B-RACK OR IN THE A-RACK*.

* Sections 2.4 and 2.5 contain information about disconnecting the A-Rack and the C-Rack.

2.3.The Nord-50 CPU Rack - Rack-B

The Nord-50 CPU contains the registers, integer arithmetic, the communication registers Nord-10 - Nord-50, memory address and data line drivers/receivers and line drivers/receivers for the external arithmetic, and the C and A-Racks.

Figure 7 shows the data flow to and from external units in the Nord-50 CPU (The B-Rack).

These functions are organized on three different circuit boards, each handling four bits:

Address Arithmetic	1501
Register	1502
Arithmetic Buffer	1503

The 32 bit CPU uses eight of each boards, making a total of 24 boards.

The timing and control section of the CPU uses eight different boards:

Nord-50 I/O Control	1500
Nord-50 Controller	1504
Register Address	1505
Cycle Counter	1506
Arithmetic Control	1507
Chip Select	1508
Instrument Control	1510
Timing Control	1519

Figure 8 is the Nord-50 CPU Module Description.

Figure 9 shows a Nord-50 CPU DATA FLOW.

Figure 10 is a Nord-50 CPU Control Module Description.

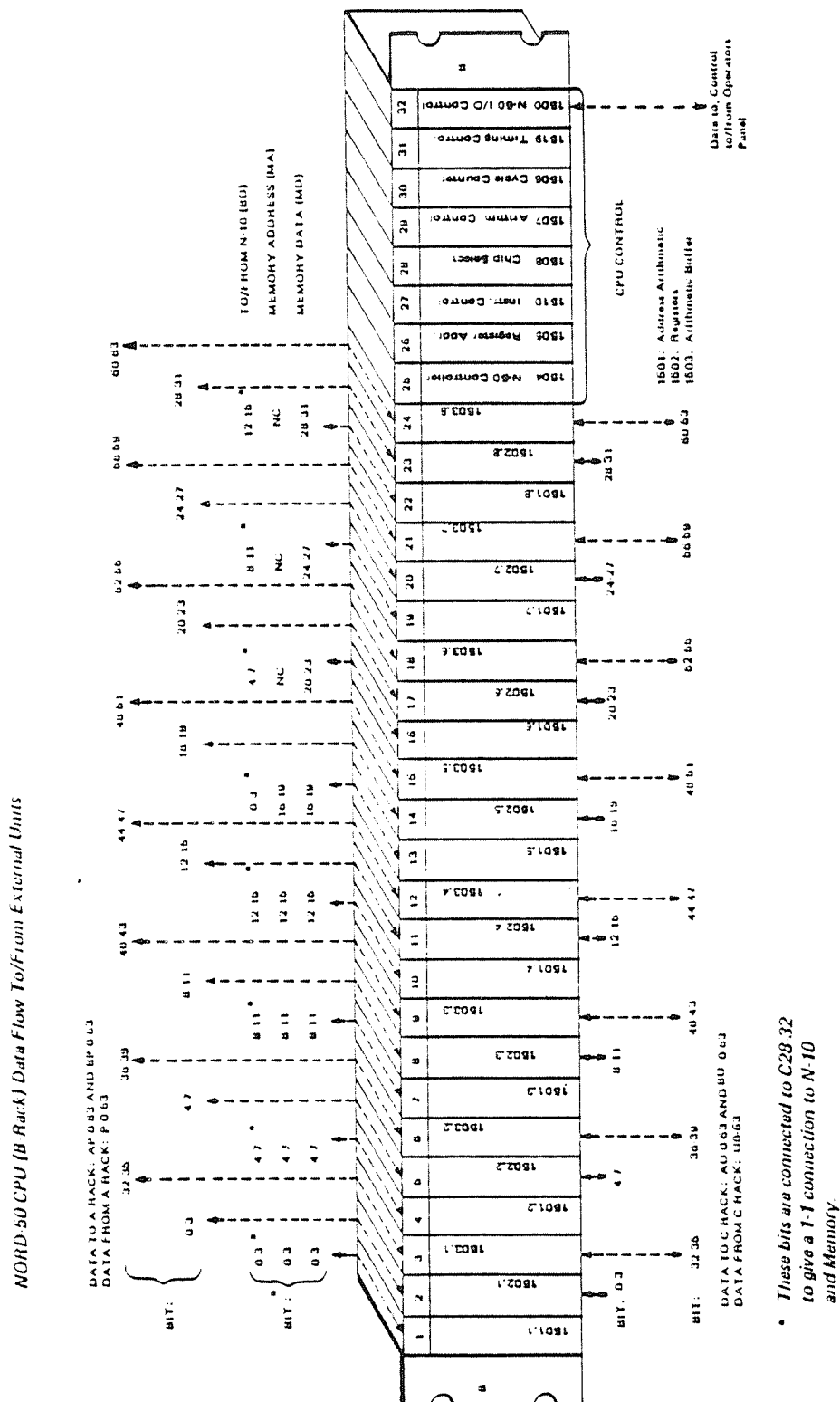


Fig. 7. NORD-50 CPU (B-rack) data flow to/from external units

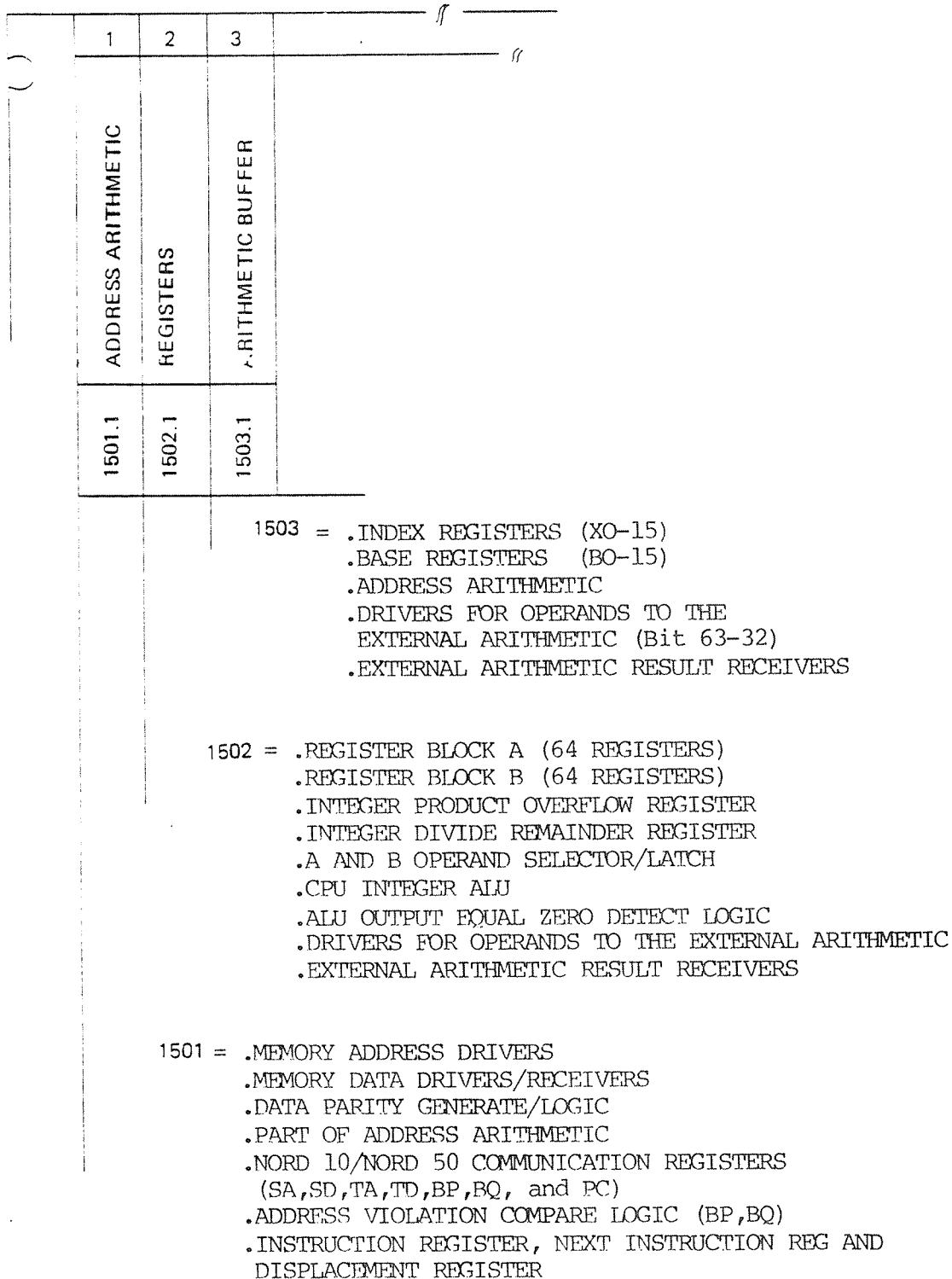


Fig. 8. NORD-50 CPU module description

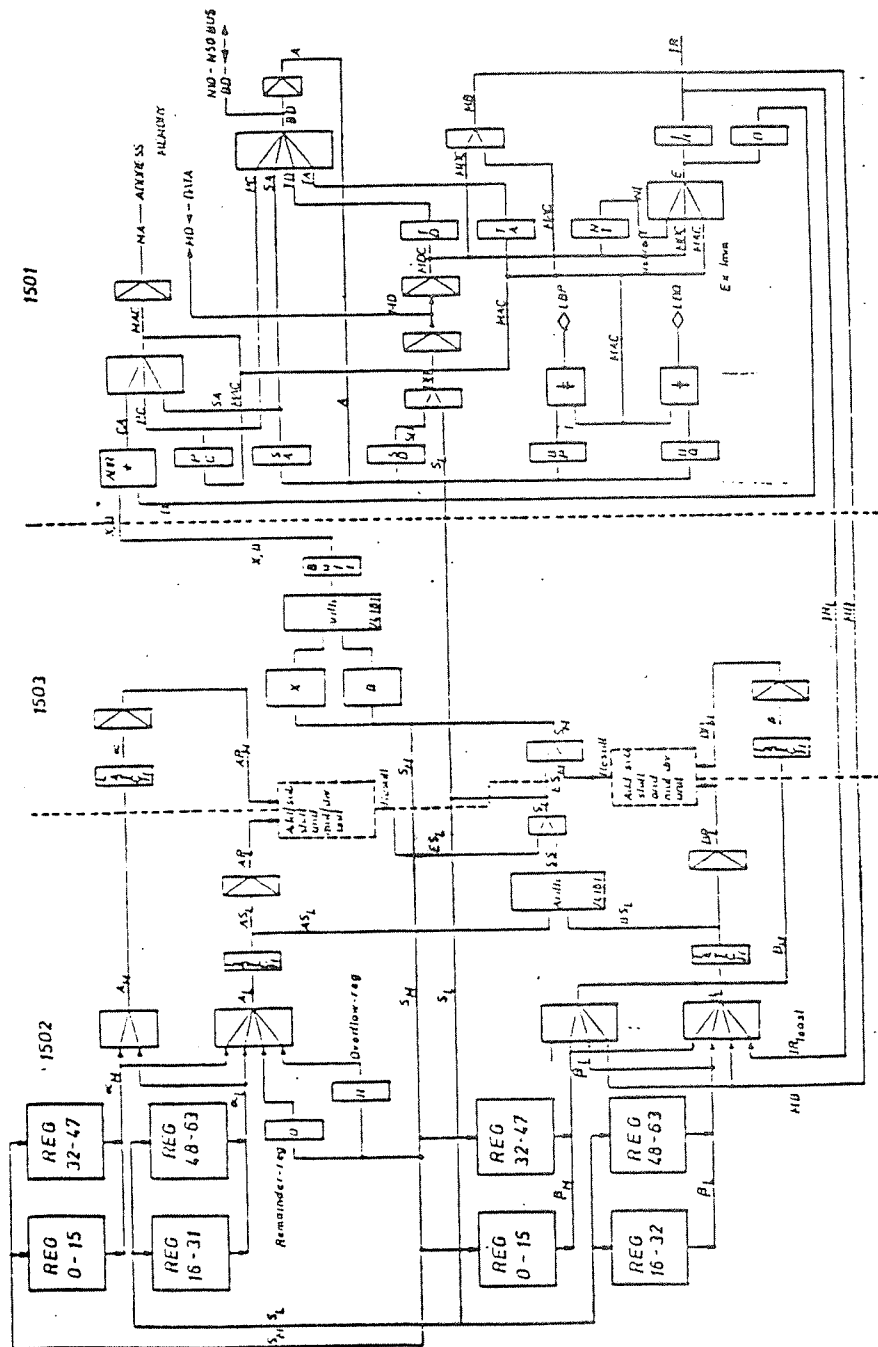


Fig. 9. NORD-50 CPU data flow

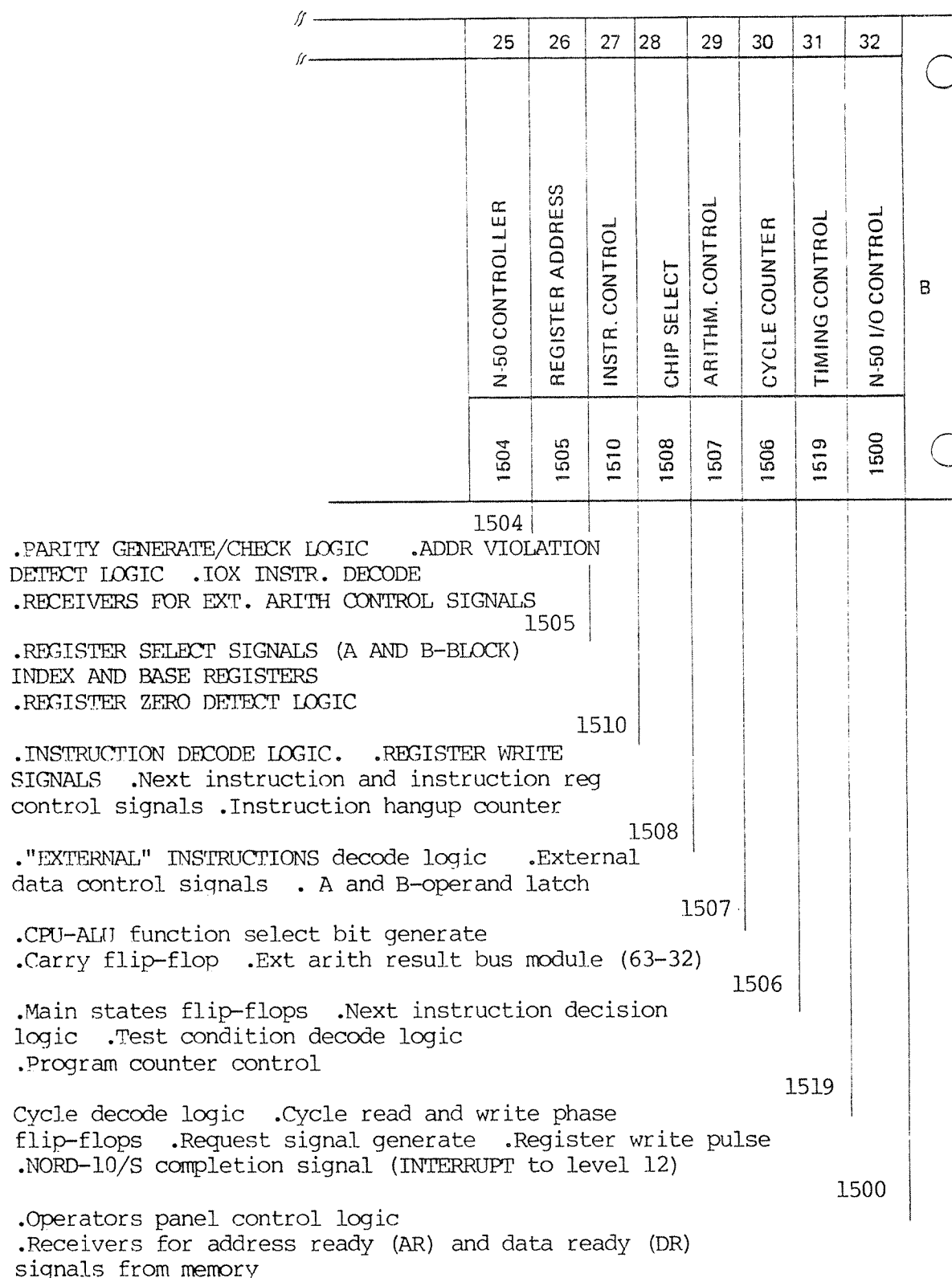


Fig. 10. NORD-50 CPU control module description

2.4. Nord-50 Multiply/Divide Unit (A-Rack)

2.4.1. General

- Integer multiply/divide
and
- Floating multiply/divide
(both single and double precision)

The A-rack can be looked upon a special processor being controlled by the Nord-50 CPU.

The processor is activated when:

- the CPU fetches a floating integer, multiply or divide instruction for execution, and
- the operands are latched in the CPU and presented on the A and B-operand lines to the A-rack.

For a floating double memory reference instruction, this implies that two memory references, each reading a 32 bits operand, have to take place before the processor is activated.

While the processor is active, the CPU waits until a READY signal is received indicating that the SUM-bus to CPU contains an achieved result.

The ready signal triggers a CPU - WRITE - cycle, writing the result back to the register, specified in the destination field of the Instruction Register.

The 64 bits result of a floating double instruction is written back to the register block in parallel.

An integer product of 32 bits is written back to the specified register and in parallel the 32 overflow bits is written into the overflow register.

A quotient of 32 bits, the result of an integer division, is written back to the specified register and in parallel the 32 bits remainder is written into the remainder register.

The A-Rack can easily be disconnected from the CPU (B-Rack) by pulling out all the 1522 modules (1522.1 - 1522.8). This will not influence the execution of instructions in the B-Rack and in the C-Rack.

2.4.2. Maintenance Hints for the A-Rack

- If one or two result bits in the A-Rack are failing, suspect the 1522 modules or the 1502 or 1503 modules in the CPU (B-Rack).
- The exponent arithmetic of floating instructions is handled on a special module, the 1524 module.
- Check the 5V DC power in the A-Rack.

Note! Not less than 4.9 volts.

- Check that the fans underneath the A-Rack are rotating. If the fans are not rotating this could be the cause of sporadic errors.

Figure 11 is a diagram showing the A-Rack (Mul/Div Unit) data flow.

Table 2.1 gives module positional information for Rack-A: A Nord-50 Multiply/Divide Unit.

Figure 12 shows the Nord-50 Multiply/Divide Unit Modules.

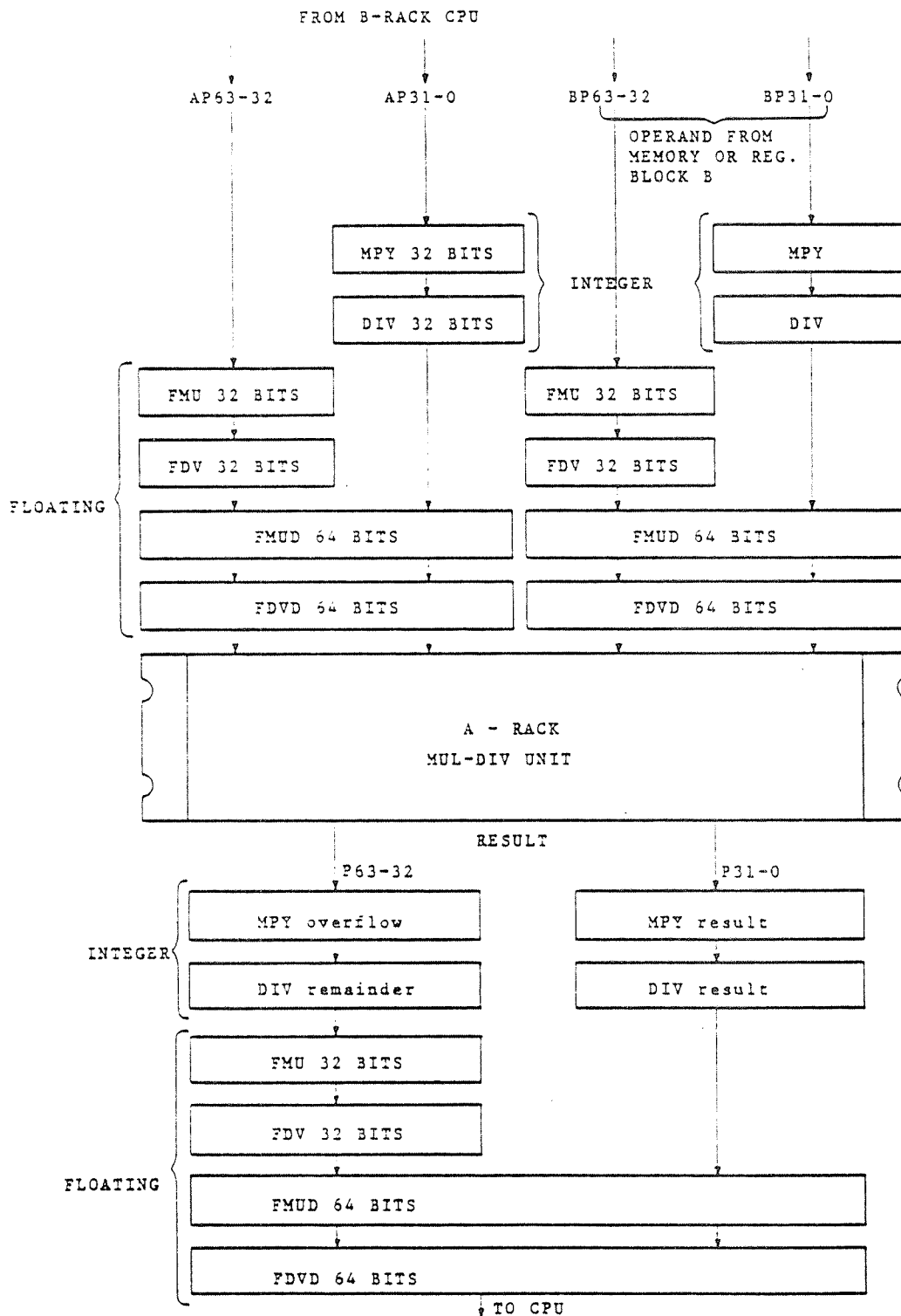


Fig. 11. A-RACK (MULDIV UNIT) data flow

Position:

1	1521.1	MUL-DIV ARITHMETIC
2	1522.1	OUTPUT SELECTOR
3	1521.2	MUL-DIV ARITHMETIC
4	1522.2	OUTPUT SELECTOR
5	1523.4	B-INPUT
6	1521.3	MUL-DIV ARITHMETIC
7	1522.3	OUTPUT SELECTOR
8	1521.4	MUL-DIV ARITHMETIC
9	1522.4	OUTPUT SELECTOR
10	1523.2	B-INPUT
11	1511	SHIFT MATRIX A
12	1512	SHIFT MATRIX B
13	1525	MUL-DIV TIMING
14	1526	MUL-DIV CONTROL
15	1521.5	MUL-DIV ARITHMETIC
16	1522.5	OUTPUT SELECTOR
17	1523.3	B-INPUT
18	1521.6	MUL-DIV ARITHMETIC
19	1522.6	OUTPUT SELECTOR
20	1521.7	MUL-DIV ARITHMETIC
21	1522.7	OUTPUT SELECTOR
22	1523.1	B-INPUT
23	1524	EXPONENT ARITHMETIC
24	1522.8	OUTPUT SELECTOR
25		
26		
27		
28		
29		
30		
31		
32		

Note. Refer to manual Nord-50 General Description and Module Descriptions, ND-05.008.01, for module descriptions.

Table 2.1: RACK-A (MUL/DIV UNIT), POSITIONAL INFORMATION

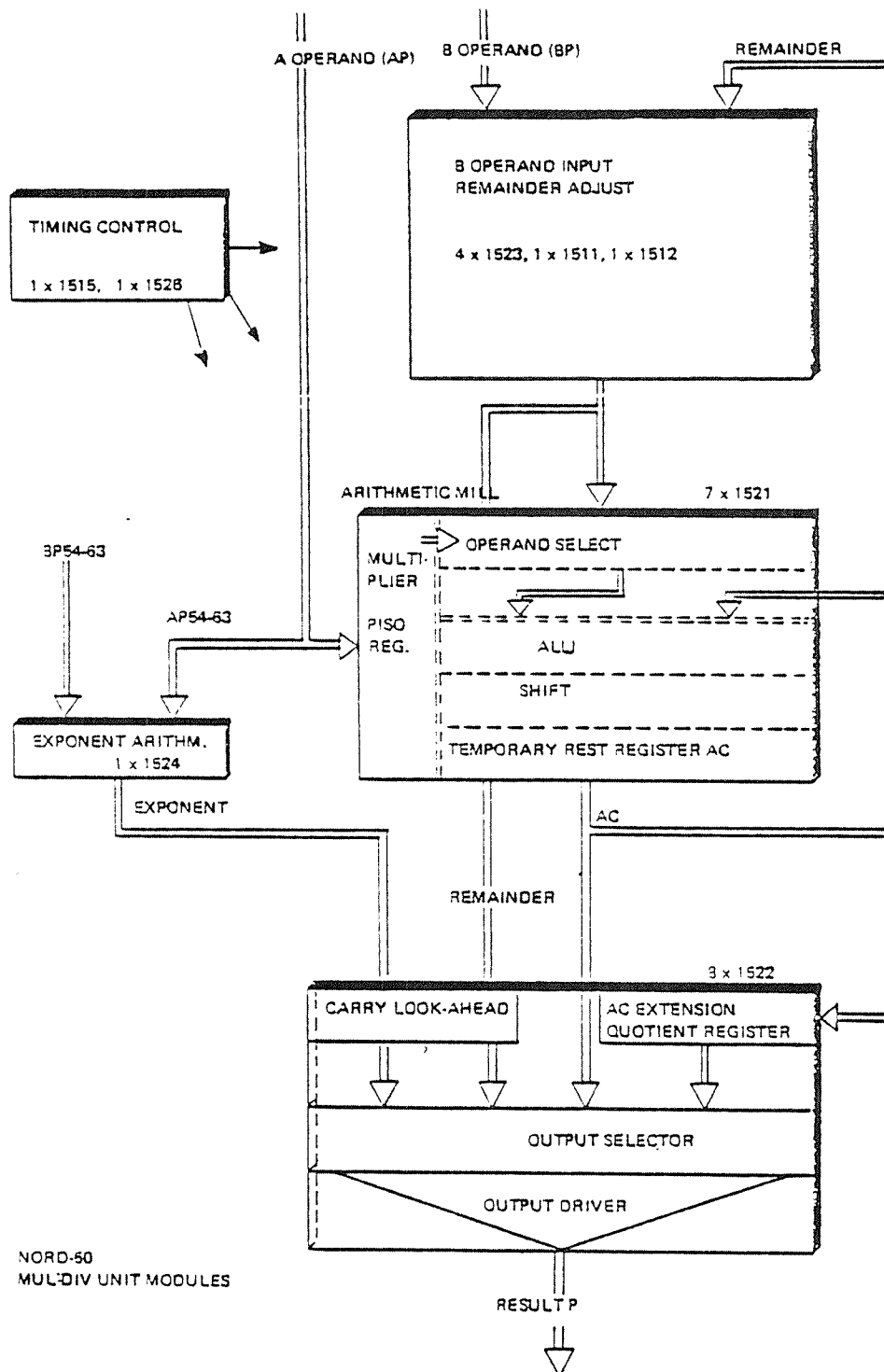


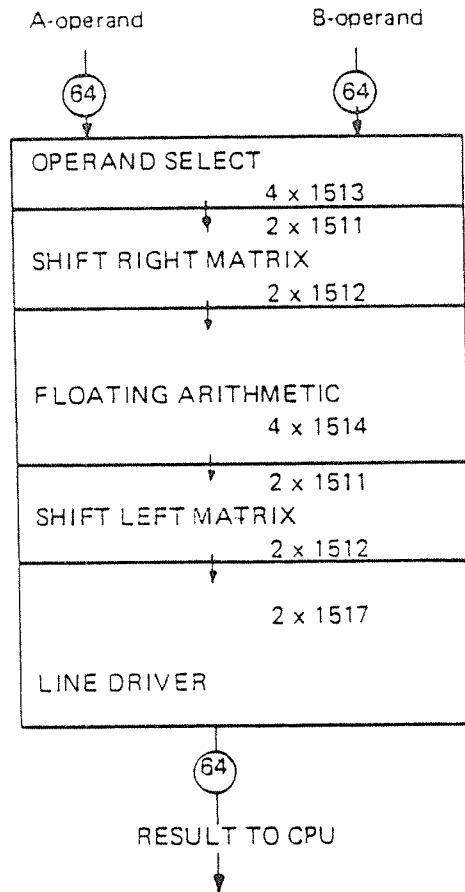
Fig. 12. NORD-50 multiply divide modules

2.5. The Nord-50 C-Rack

In the C-Rack, as part of the external arithmetic, the following instructions are executed:

Mnemonic:	Memory Ref. Inst.	Inter. Register Instr.	Means:	No.of operand bits:
FAD	X		Floating Add F+(EA)	32
FADD	X		Floating DP Add FD+ (Ea, Ea+1)	64
RAF		X	Floating Reg. Add	32
RAFD			Floating DP Reg.Add	64
FSB	X		Floating Subtract F-Ea	32
FSBD			Floating DP Subtract FD-(Ea, Ea+1)	64
FIX		X	Convert floating to Integer	32/32
FIXD		X	Convert DP floating to Integer	64/32
FIR		X	Convert floating to Rounded Integer	32/32
FIRD		X	Convert DP floating to Rounded Integer	64/32
FLO		X	Convert Integer to Floating	32/32
FLOD		X	Convert Integer to DP Floating	32/64
		X	Shift a 32 or 64 bit operand up to 63 places to the right or left with arith- metic, logical or rotational shift	32 or 64
BST		X	Bit set	32
BCL		X	Bit clear	32
BCM		X	Bit complement	32
BSZ		X	Bit skip on zero	32
BSO		X	Bit skip on one	32

As the table indicates, four of the instructions are memory reference instructions (one operand from memory and one from a register) and the rest are inter-register instructions (both operands, if two, are taken from the register block).



DATA FLOW

The C-rack consists of this main card set: OPERAND SELECT 4 x 1513.

Four 1513 cards select the operand to the internal bus.

SHIFT RIGHT MATRIX

Two 1511 cards shift the operand 0, 8, 16, 24, 32, 40, 48 or 56 places. The shift can be rotational or arithmetic.

Two cards shift the operand 0, 1, 2, 3, 4, 5, 6 or 7 places.

FLOATING ARITHMETIC 4 x 1514

The floating mantissas are added or subtracted on these cards (exponent arithmetic on card 1515).

Shift operands go directly through. For bit instructions, the specified bit should now be in 0 and is manipulated and checked on card 1516.

SHIFT LEFT MATRIX

As right shift matrix, but shifted left.

LEFT DRIVER

Drives result on tri-state lines to CPU.

Figure 1.3 shows the C-Rack data flow.

Table 2.2 gives module positional information for Rack-C: A Nord-50 Arithmetic Unit.

2.5.1. Control Modules

1515 SHIFT LEFT

- Right and left shift-matrix control (shift-count)
- Operand to shift-right matrix select
- Priority encoder (most significant "1" bit detect)
- Floating exponent arithmetic

1516 FLOATING CONTROL

- Instruction register bit from CPU decode logic (shift, bit and convert instructions)
- Drivers for control signals back to CPU
- DATA READY decision-logic (One Shot)

The C-Rack may easily be disconnected from the CPU by pulling out the two 1517 modules for DATA and the 1516 module for CONTROL SIGNALS. This will not influence the execution of instructions in the A-Rack and in the B-Rack.

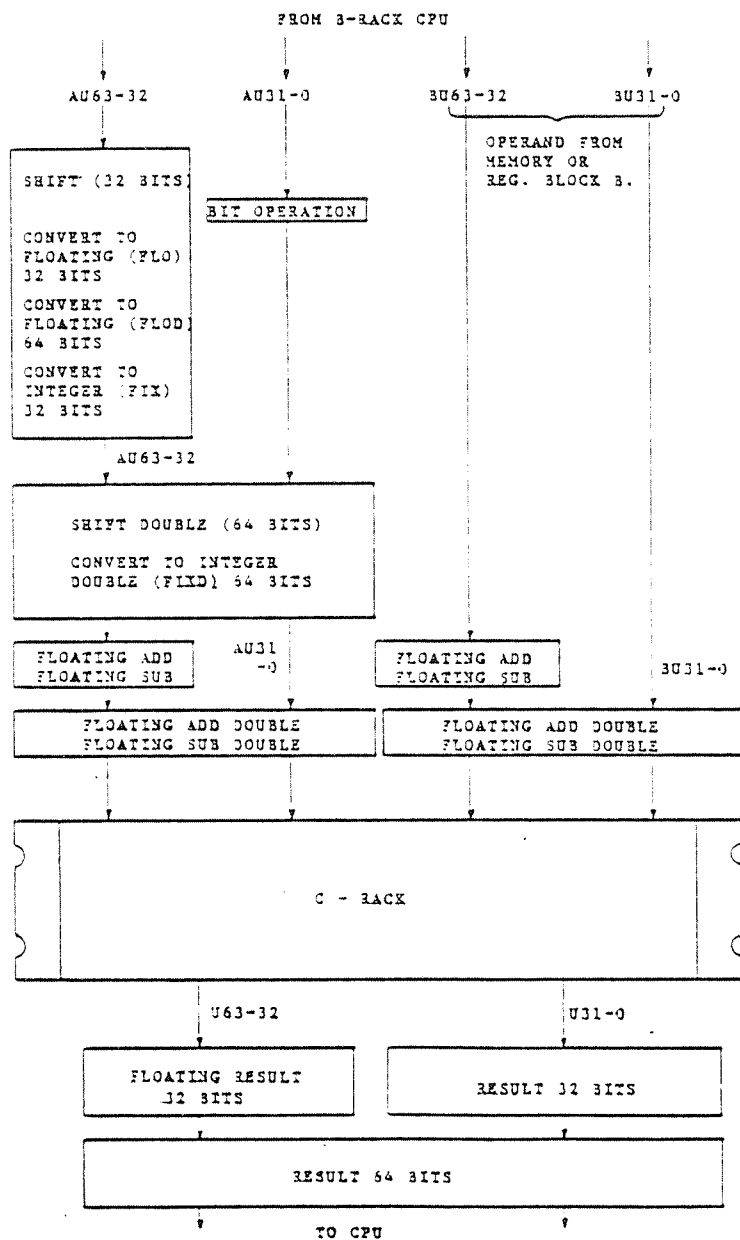


Fig. 13. C-rack data flow

1		
2	1513.1	DATA SELECTOR
3	1513.2	DATA SELECTOR
4	1513.3	DATA SELECTOR
5	1511.1	SHIFT MATRIX A
6	1511.2	SHIFT MATRIX A
7	1512.1	SHIFT MATRIX B
8	1512.2	SHIFT MATRIX B
9	1514.1	FLOATING ARITHMETIC
10	1514.2	FLOATING ARITHMETIC
11	1514.3	FLOATING ARITHMETIC
12	1514.4	FLOATING ARITHMETIC
13	1511.3	SHIFT MATRIX A
14	1511.4	SHIFT MATRIX A
15	1512.3	SHIFT MATRIX B
16	1512.4	SHIFT MATRIX B
17	1517.1**	DATA BUFFER OR 1520
18	1517.2	DATA BUFFER
19	1515	SHIFT CONTROL
20	1518*	FLOATING CONTROL
21	1513.4	DATA SELECTOR
22		
23		
24	1532	DATA & BUS SELECTOR
25	1531	DEVICE REGISTERS
26	1532	ADDRESS BUS SELECTOR
27		
28		
29		
30		
31		
32		

* According to ECO 50-50 this module should be a 1518 module and not a 1516 module.

** In the F-16 configuration, this module is replaced with a compatible 1520 module that also includes a clock.

Note. ECO 50-49 on the 1507 module in the CPU is also necessary.

Table 2.2: RACK-C (ARIT UNIT), POSITIONAL INFORMATION

2.5.2. Nord-10 - Nord-50 Communication Hardware

To control the Nord-50, the Nord-10/S has a Nord-10/S - Nord-50 communication system interface for starting and stopping the Nord-50. In addition, different control and status information is passed between the processors, such as specified break for overflow, underflow, divide by zero, memory protect error, etc. The communication interface also supports a memory examine/deposit function such that the Nord-10/S may reach all of Nord-50 memory even if this memory is larger than the normal maximum Nord-10/S addressable memory of 512K bytes.

Data and instructions may be transmitted to the Nord-50 from the Nord-10 via the communication interface simulating the Nord-50 main memory. 16 bits of data are exchanged at a time. 2 IOX instructions are then needed to transfer a 32 bit word.

The communication hardware consists of 5 modules. 3 are located in the Nord-50 (C-Rack) and 2 in the I/O Rack of the Nord-10/S. Note that 3 of the modules are identical and exchangeable (1532).

2.5.2.1. Modules in the Nord-50

1532 (POSITION C24)

- 16 Bit Differencial Line Drivers/Receivers

1531 (POSITION C25)

- Nord-50 Modus Register (MO-15)
- Nord-50 Status Register (SBO-10)

1532 (POSITION C26)

- Receivers for Nord-10/S IOX Addresses
- Receivers for Nord-10/S Control Signals (START, STOP and STROBE)

2.5.2.2. Modules in the Nord-10/S

1532

- IOX Address Bit Drivers

1071

- 16 Bit Differential Line Drivers/Receivers
- IOX Instruction Decode
- Nord-50 Control Logic
- Nord-10 Interrupt Signal Generate

2.6. Nord-50 Operator's Panel

Figure 14 shows the Active Address portion of the Nord-50 Operator's Panel.

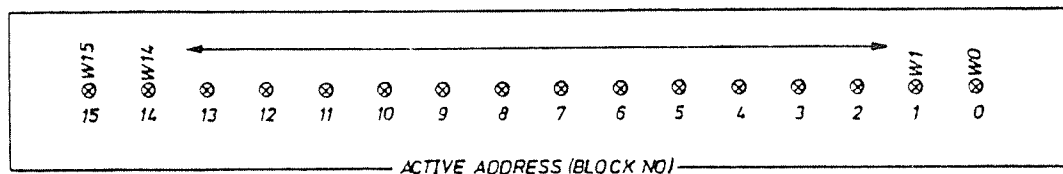


Fig. 14. Active address portion of the operators panel

The program address (PC) and data address are displayed when either DISPLAY PC (switch No. 10) or DISPLAY DATA REF (switch No. 9) is pushed.

The address is displayed in 4K blocks

Address from 0- 4K = Light in 0, etc. -- 60-64K = Light in 15

Address from 64-68K = Light in 0, etc. --

Figure 15 shows the Parity Check portion of the Nord-50 Operator's Panel.

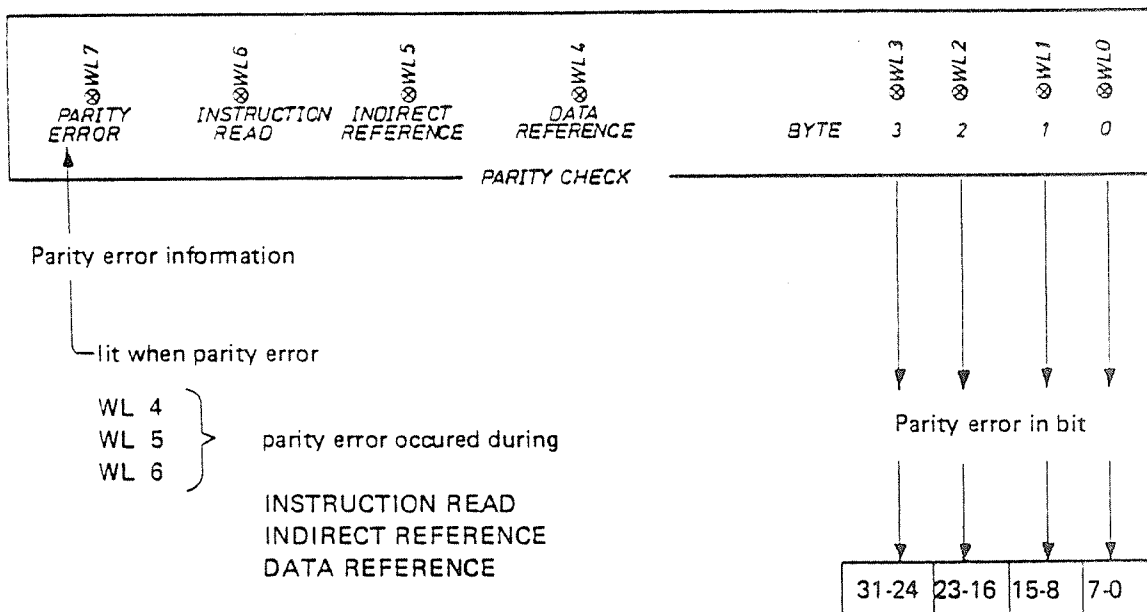


Fig. 15. Parity check portion of the operators panel

Figure 16 shows the Power Switch and the STATUS portions of the Nord-50 Operator's Panel.

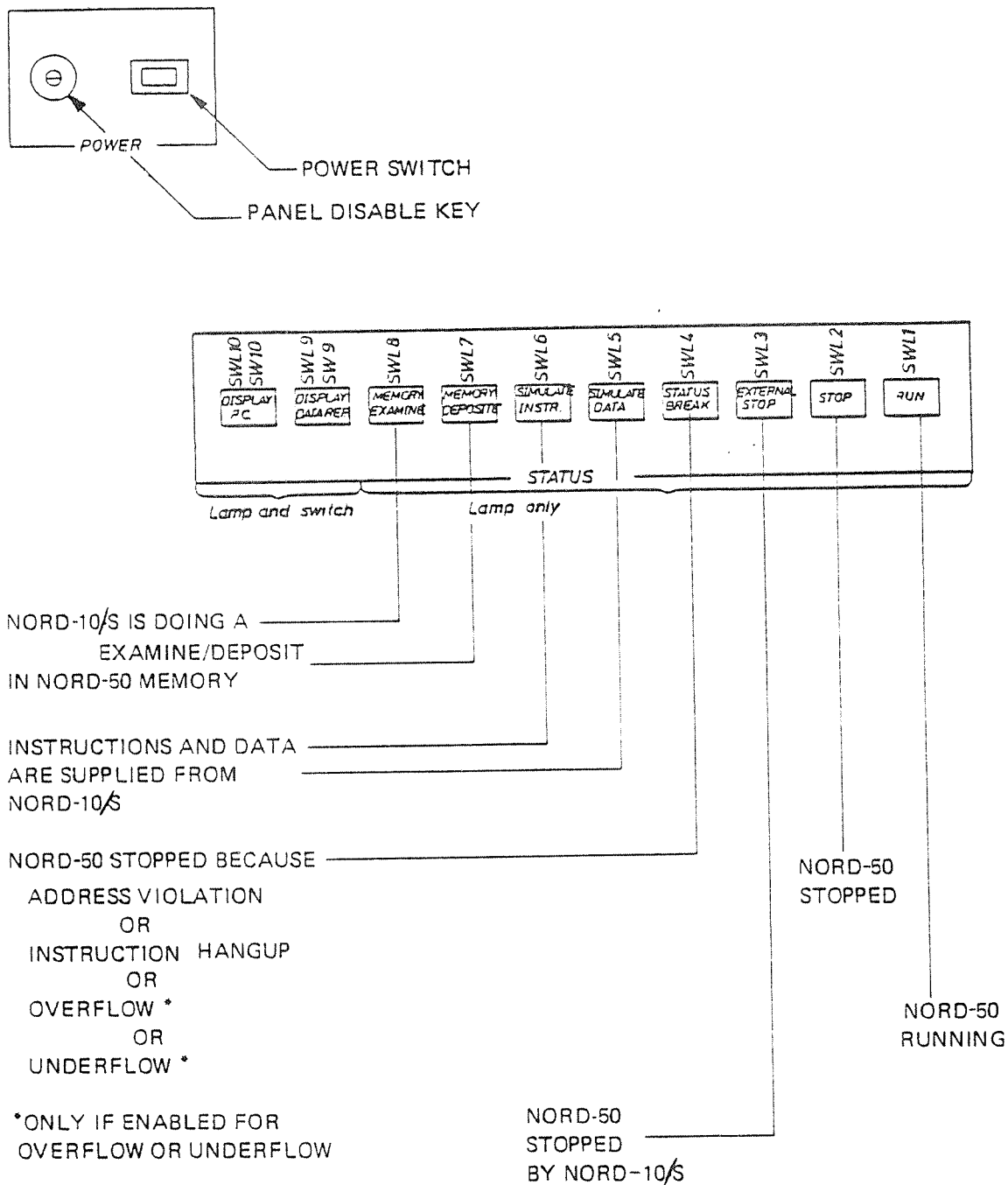


Fig. 16. Power switch and status portions of operators panel

For electrical and mechanical details, refer to the Nord-10/S technical/mechanical drawings:

10S - 48, 49 and 50.

3. NORD-50 MONITOR

3.1. Introduction

The Nord-50 MONITOR is a system program running in the Nord-10/S CPU as an extension of the SINTRAN III/VS Operating System, supervising the execution of programs in the high speed 32 bit Nord-50 CPU.

The functions of the Nord-50 MONITOR can be divided into six groups:

- Performing I/O operations and operating system functions requested from an active program.
- Loading programs into the Nord-50's memory, assigning files, starting execution and providing debugging facilities to the user.
- Reporting errors during program execution.
- Examining the Nord-50 registers/memory after the program has come to a (normal or abnormal) stop.
- System initialization and testing, assigning static, dynamic, sharable and/or local memory to be used by programs.
- The Nord-50 MONITOR also contains a simple assembler. This makes it possible to write small debugging loops in Nord-50 assembly code. Refer to Appendix E for the format.

3.2. Activation of the Nord-50 MONITOR

The Nord-50 MONITOR is activated from an interactive terminal or batch processor using the same commands:

@ N-50 'CR' Note. 'CR' indicates Carriage Return.

In a multi Nord-50 configuration the command:

@ N-50 1 'CR' will enter N-50.1
@ N-50 2 'CR' will enter N-50.2 , etc.

If only the command N-50 is given, the first free Nord-50 is entered.

The commands summarized here are only those necessary for performing hardware maintenance on the Nord-50.

3.3. Nord-50 Monitor Commands

Commands for taking a program in executable format on a file and placing it in Nord-50 Memory and starting it.

PLACE<file name or file number>

Moves the executable Nord-50 program file prepared by the Nord-50 loader into the Nord-50 memory. Default file type: NOR5.

Nord-50 memory is allocated according to the break conditions set from the Nord-50 Loader when the core image file is prepared. See Nord-50 Loader and the command BREAK-CONDITIONS.

RUN

Starts execution of the Nord-50 program in the main program start address. Continues execution after a break. Continues execution after a program is stopped by "escape".

The RUN command will start with the save/unsave routines in location A. Refer to Figure 17.

GOTO<address>

Starts execution of the Nord-50 program in the specified address.

The GOTO command will start with the save/unsave routines in location A. Refer to Figure 17.

LOAD<file name or file number>

Equals the command PLACE and RUN performed in one operation.

Start in location A. Refer to Figure 17.

HARDWARE-GOTO<address>

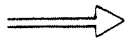
Starts execution of a Nord-50 program in the specified address. The Nord-50 register block is not saved when this command is used and therefore the register contents cannot be examined. This command is usually used when debugging the Nord-50 hardware.

The HARDWARE-GOTO command will start in location B. Refer to Figure 17.

Contains the following information:

- Main program start address
- Break registers (BP and BQ)
- Modus registers (Break conditions)
- Status Registers
- Start address of the save/unsave routines

A



STATUS
INFORMATION

REGISTER
BLOCK

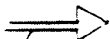
BLOCK 0

- Remainder, Overflow and carry registers
- Register 0-63

SAVE/UNSAVE
ROUTINES
N-50 CODE

- Routines that:
Unsave : Register (Block 0)
to PHYS REG Nord-50
Save : PHYS REG
Nord-50 to Block 0

B



BIT MAP

- Bit map table for program file

NORD-50
PROGRAM
IN
ASSEMBLY
CODE (NOR-5)

BLOCK 1

PROGRAM

Fig. 17. Executable program

BREAK-CONDITIONS <BP address>, <BQ address>, <break conditions>

Set the Nord-50 breakpoint registers and break conditions. <Break conditions> may be A, D, F, S, O, U, P or any combination of these characters.

A stop on any reference in BP<=BQ
D stop on data reference in BP<=BQ
S stop on store reference in BP<=BQ
F stop on fetch reference in BP<=BQ
O stop on overflow
U stop on underflow
P stop on parity error in memory

The BREAK-CONDITIONS command also affects the memory allocation for Nord-50. If BP < BQ and the condition A or S (any or store reference) is on, some of the memory in address interval <BP,BQ> is free and protected from any Nord-50 write operation. Otherwise all of the Nord-50 memory is reserved for Nord-50.

MEMORY EXAMINE/DEPOSIT

The Nord-50 memory is displayed as:

<MEMORY ADDRESS>/ 'CR'	% 20/ will display the content of memory location 20 (octal).
DISPLAYED MEMORY ADDRESS	The output format may be changed with the FORMAT command. Default is: O = Octal and I = instruction disassemble.

By typing Carriage Return the next memory location is displayed.

NORD-50 MEMORY DEPOSIT:

<MEMORY ADDRESS>/ 'CR'	
DISPLAYED MEMORY ADDRESS	xxxxxx 'CR' % the xxxxxx is deposited into the memory address.
@ or .	% return to normal command mode.

REGISTER EXAMINE/DEPOSIT:

R<register number>/ 'CR'	R 10/ 'CR' will display the content of register 10 (Octal).
--------------------------	---

DISPLAYED REGISTER

REGISTER DEPOSIT: The same as for memory.

Note. By typing R<register number>D 'CR' the decimal number is displayed.

FORMAT<formats>

Sets output formats to be used in the commands DUMP-ADDRESS and MEMORY or REGISTER EXAMINE DEPOSIT. Formats may be O, D, F, S, I, A, B, T, C or any combination of these characters.

O	octal
D	decimal
F	floating point (64 bits)
S	floating point (32 bits)
I	instructions (dissassembled)
A	ASCII (one word = 4 ASCII characters)
B	binary
T	two 16 bits octal numbers (Nord-50) compatible output)
C	four 8 bit octal numbers

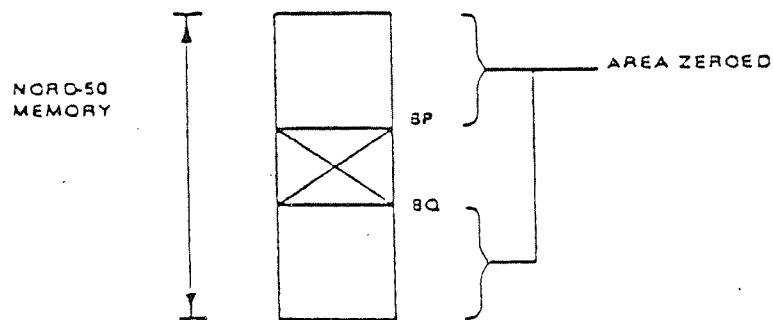
If the FORMAT command is not used formats are defaulted to OI.

STATUS

STATUS prints some information about the Nord-50 status. This command is useful when the Nord-50 stops because of any error condition. Refer to the example below.

ZERO-MEMORY

This command stores zero in the Nord-50 memory in the areas outside the BP, BQ area. If break-conditions O, U or P occur the whole memory is zeroed.



MASTER-CLEAR

Brings the Nord-50 out of any hang-up state.

HARDWARE-STATUS

Prints some information about the Nord-50 hardware status: STATUS, PC, SA, TA, TD (actually read from hardware).

% Status Register Format in Appendix D
 % Program Counter
 % Start Address Register
 % Last Memory Address
 % Last Memory Data

CARRY

Prints the "saved" Nord-50 CARRY-flip-flop.

REMAINDER (Integer Divide Remainder)

The contents of the "saved" Nord-50 remainder register is printed.

OVERFLOW (32 Most Significant Integer Product Bits)

The contents of the "saved" Nord-50 overflow register is printed.

TEST-MEMORY <address>,<number of blocks>

Tests the Nord-50 memory. The number of blocks is decimal default and block size is 1K words.

Refer to Section 6.3 for additional information.

LOOP-ON

Turn on the deposit/examine loop for the TEST-MEMORY command.

LOOP-OFF

Turns OFF the deposit/examine loop for the TEST-MEMORY command.

MEMORY-MAP <output file>

The command lists a map of the Nord-50 memory. The command is especially useful for multiple Nord-50 CPUs with shared memory. In this case a cross-reference of memory addresses as seen from all the CPUs is listed. All addresses are given in octal page numbers (1 page = 512 words). To get the Nord-50 address multiply the octal page number by 1000_8 . The command can only be issued by user system.

4. NORD-50 ERROR MESSAGES

4.1. General

This section covers the error messages given by the Nord-50 MONITOR and also information about Nord-50 FORTRAN error messages. General Nord-50 MONITOR error messages are explained with appropriate illustrations.

Only error messages that could be caused by hardware failures are dwelt with.

Note. The error messages covered are only those error messages from programs that have been tested and accepted as "error free".

Refer to the following manuals for detailed error message information for the Nord-50 LOADER and the Nord-50 FORTRAN COMPILER:

NORD-50 FORTRAN Reference Manual	ND-60.095.02	Appendix F
NORD-50 Loader Users Guide	ND-60.083.01	Appendix B

4.2. Nord-50 Monitor Error Messages

4.2.1. General

When one of the error messages listed below is printed, the Nord-50 STATUS-REGISTER should always be checked. The STATUS-REGISTER is displayed by printing STATUS 'CR'.

The STATUS command will provide the following information:

- The reason for STOP
- The program start address (SA)
- The last memory reference address (TA)
- The last data to or from memory (TD)
- The setting of the address violation break register
(BP = Lower and BQ = Upper)
- The setting of the break conditions

A STATUS command and the resulting STATUS MESSAGE is illustrated in Section 3.3.

A special procedure is necessary to obtain correct information when a PARITY ERROR error message is given. This procedure is described in the PARITY ERROR error message description that follows.

4.2.2.Error Messages With "-NORD-50 ERROR: <Error Message>" Formats

The listed error message will be in the following format:

-NORD-50 ERROR: <Error Message>

The error message will be followed by an "Explanation:" and an "Action:" to be taken as appropriate.

REGISTER SAVE OR UNSAVE ROUTINE FAILED

Explanation:

The "save/unsave" routines, executed in the Nord-50 prior to the program start, are not executed in the correct sequence.

The "save/unsave" routine of 40 Nord-50 instructions is initiated when one of the following commands are given:

- * LOAD <program name>
- * RUN
- * GOTO <address>

At program START:

The "unsave" routine is started when the initial values of all Nord-50 registers are loaded into the registers.

At program STOP:

The "save" routine is started in order to save the Nord-50 register contents in memory.

The "save/unsave" routines may be bypassed by this Nord-50 command:

- * H-G <address> % Hardware GOTO the specified address.

Note. It is not possible to examine/deposit in the Nord-50 registers when the Nord-50 stops.

Action:

Either start a test program such as TINST, TREG or TMEM with the hardware GOTO command,
or

Stop the system and run the Nord-50 TEST SYSTEM. Refer to Section 5.2.1.

ILLEGAL PARAMETER POINTER IN MONITOR CALL

Explanation:

The location, after the STOP or MONITOR CALL instruction, will contain a parameter pointer or parameter address.

This error message is given if one bit from 20-31 is set (specifying an address >4 Mbytes).

A STOP instruction is probably executed as a MONITOR CALL instruction, which was not the intention. This could be caused by:

- Destroyed code
- Execute instructions in the data area

Action:

- Run CPU tests such as:
TINST, TREG
- Run memory tests such as:
TMEM, TEST-MEM

ILLEGAL MEMORY ADDRESS

Explanation:

Examine/deposit in the memory area that is protected by the BP and BQ registers is checked in software before being accessed and the ILLEGAL MEMORY ADDRESS error message is given.

Action:

Check the BP and BQ registers. Also check the break-conditions.

ILLEGAL PARAMETER IN MONITOR CALL

Explanation:

Wrong value of the MONITOR CALL instruction.

Action:

As for ILLEGAL PARAMETER POINTER IN MONITOR CALL error message.

ILLEGAL MONITOR CALL

Explanation:

The Monitor Call Number is >200 .

Action: As for ILLEGAL PARAMETER POINTER IN MONITOR CALL.

MEMORY OUT OF RANGE

Explanation:

No memory reply (memory time-out) when the MONITOR is performing a EXAMINE/DEPOSIT in the Nord-50 memory, or the Nord-50 is addressing nonexisting memory.

Note. Both memory banks have to respond for completing a memory access.

Action:

- Run memory test such as:
TMM, TEST-MEM

Note. See Section 6.

4.2.3. Error Messages With "-<ERROR MESSAGE>-AT:<octal address>" Format

The listed error message will be in the following format:

-<ERROR MESSAGE>-AT:<octal address>

The error message will be followed by an "Explanation:" and an "Action:" to be taken as appropriate.

Error messages with this format will be given if a bit is set in the status-register and the corresponding modus bit is also set (enabled for).

ADDRESS VIOLATION

Explanation:

A Nord-50 memory access was stopped. The access did not match the break-register BP and BQ set up.

Action:

Check the STATUS information given by the STATUS-COMMAND in the MONITOR. Check the BQ and BP setting against the last memory address (TA).

If the address was illegal, the break-registers must be set once more with the B-C command.

If the address was correct, check the hardware. The address violation hardware is located on these modules:

(1501.1 - 1501.5 the 1504 and the 1519 modules)

INSTRUCTION HANG UP

Explanation:

The Nord-50 did more than 16 indirect access operations or executed more than 16 EXECUTE IMMEDIATE instructions.

Action:

- Run TINST instruction test program
- or
- Stop the system and run the Nord-50 TEST-SYSTEM

The "Hang-up" hardware is located on the 1510 and the 1519 modules.

ARITHMETIC OVERFLOW

ARITHMETIC UNDERFLOW

Explanation:

The instruction executed in the external arithmetic gave ARITHMETIC OVERFLOW or UNDERFLOW.

Note. This error message should not appear when the the corresponding bit in the modus register is not set *B-C,,O,U Enable for Overflow and Underflow.

Action:

- Run test programs testing the external arithmetic as follows:

HAMB MET = A and C-Racks
FTEST = C-Rack
DFTEST = C-Rack

Note. The overflow/underflow signals from the external arithmetic are received on the 1504 module in the CPU.

PARITY ERROR

Explanation:

Memory parity error has been detected. With Big multiport memory system, only multiple errors will give this error message.

Action:

Check the address where the parity error was detected by giving the command:

*H-S 'CR' % Hardware status.

The TA-register should contain the failing address.

Note. The registers are not saved during
Parity Error.

The Operator's Panel should give information about the failing byte, but the panel information can be destroyed by the software.

If the parity error was in the Nord-50 local memory and this memory has been idle since last power ON/OFF sequence, do either of the following:

- * A ZERO-MEMORY Command
- or
- * A TEST-MEMORY Command

If not in the Nord-50 private memory, run a Memory test program. Refer to Section 6.3.

Check the memory system, the 1501 modules, or the following CPU control modules:

1504
1519

MEMORY OUT OF RANGE

Explanation:

No reply from one or both multiport memory racks.

Action:

Check the last memory address contained in the TA-Register by giving the STATUS-Command.

- Run memory tests such as:
TMEM, TEST-MEM

and specify the lower and upper address around the non-responding address. If the error is in shared memory, also run a Nord-10/S memory test program, for example, MULTI.

EXTERNAL STOP

Explanation:

This error message is given when the Nord-50 is stopped by a Nord-10. It appears when ESCAPE is printed on the terminal.

Action:

If the Nord-10 did not intend to stop the Nord-50, then:

- Stop the system and run:
TEST-SYSTEM

Note. The first tests will test the Start/Stop sequence of the Nord-50.

- Check the Nord-10 - Nord-50 communication hardware, the 1504 or 1519 modules in the CPU.

4.2.4. Error Message With "*** Nord 50 IS RUNNING" Format

The error message listed below will have this format:

*** NORD 50 IS RUNNING

Explanation:

The Nord-50 was started while in CONTINUE. Bit 3 in the Nord-50 Interface Status Register was ZERO.

Action:

- Give the command:
 - * M-C % Master Clear.
 - or
 - * STOP

If the Nord-50 is still running, do the following:

- Stop the system and run:
TEST-SYSTEM

Note. The first tests will test the Start/Stop sequence on the Nord-50.

4.2.5. Error Messages Caused by the SET-MEMORY Command

The following error messages are caused by the SET-MEMORY command in the Nord-50 MONITOR.

ERROR MESSAGE A:

MEMORY IS OUT OF RANGE ON THE UPPER ALLOCATED ADDRESS

ERROR MESSAGE B:

MAX MEMORY ADDRESS NOT IN ALLOCATED AREA.

Explanation:

This command will specify for the Nord-50 memory the segments that make up the various parts of the memory.

After this command is specified, the Nord-50 MONITOR checks the Nord-50 physical memory to see if the memory is according to the parameters in the SET-MEM command.

The last address, for example AA, is accessed. This address should reply. Then the last address +1, for example AB, is accessed. This address should only give the reply "memory out of range".

- If address AA gives no reply, ERROR MESSAGE A is given.
- If address AB replies, ERROR MESSAGE B is given.

Action:

- Give the command:
*LIST-MEM
- Check to see if the size of the memory given by software matches the size of the physical memory.

Note. The total sum of the size of the segments
x 512 = the number of Nord-50 words in
shared memory.

If the size specified in software looks equal to the physical memory and ERROR MESSAGE A is given, check the memory.

If ERROR MESSAGE B is given, check the CPU (1501, 1519, 1500 modules) and the memory.

The SET-MEM and LIST-MEM commands are specified in Section 7.

4.2.6. FORTRAN RUN-TIME Error Messages

Some examples of FORTRAN RUN-TIME error messages are as indicated below:

- *INTEGER OVERFLOW ON INPUT
- *BAD CHARACTER ON INPUT
- *TOO LARGE ARG.IN
-
-
- etc.

Explanation:

The Nord-50 is in a state such that it is not advisable to run FORTRAN programs.

Action:

- Run assembly programs such as:
TINST, TREG, TMEM
in order to test the Nord-50.

or
- Stop the system and run:
TEST-SYSTEM

5. NORD-50 TEST PROGRAM INFORMATION

This section contains the following test program information for testing the CPU, the external arithmetic, and the communication system:

- Test Program Groups
- Accessing Nord-50 test programs
- FORTRAN programs as test programs
- Test program overview
- The Nord-50 test system
- Nord-50 test program descriptions
- The verification programs

Appendix B contains a step-by-step procedure for the Nord-50 test sequence.

5.1. Nord-50 Test Programs

The general information about Nord-50 test programs includes information about the test program groups, the N50-TEST "user", FORTRAN programs, an overview of test programs and the Nord-50 test system.

5.1.1. Test Program Groups

The test programs for the Nord-50 are divided into two groups:

Group I - Test Programs Running in the Nord-10/S

Test programs in this category are the Nord-50 TEST-SYSTEM and MEMORY TEST PROGRAMS testing the shared memory (MULTI, MOVER, 32K MOS).

Group II - Test Programs Running in the Nord-50

All test programs running in the Nord-50 have to be loaded and started by the Nord-50 MONITOR. These programs are normally available on the disk in a Nord-50 executable format (:NOR5). The Nord-50 assembly programs have been assembled and the FORTRAN programs have been compiled and loaded on the disk by the Nord-50 LOADER during system integration at the factory.

5.1.2. N50-TEST N50-USER

A special "user" has been created and designated N50-TEST, N50-USER. This "user" is often referred to as just TEST.

All Nord-50 test programs running in the Nord-50 are generated under this "user". The "user" normally has no password.

5.1.3. FORTRAN Programs as Test Programs

The following test programs are FORTRAN test programs:

HAMB-MET, ITEST, FTEST, and DFTEST

When one of these programs is loaded with the Nord-50 MONITOR, 16K of Formatted Input/Output (FIO) routines are also loaded into the Nord-50 memory.

These FIO routines are started when the FORTRAN programs require input or output from Nord-10/S I/O devices.

The programs listed above communicate with the Console Terminal.

The FIO routines execute Nord-50 instructions for:

- Converting the ASCII code to an internal representation
- Checking the input format
- Checking the number of characters
- "STORE" the input data to the program area.
The program will test against this location.

The Nord-50 hardware has to be in working condition for exchanging these FIO routines. If the hardware is not in working condition an error message from the FIO system will appear on the terminal and the program will not be started. In event the program will not start it is best to either run assembly test programs or to run the Nord-50 TEST-SYSTEM.

These FORTRAN programs serve the function of verification programs as opposed to test programs.

5.1.4. Module Substitution

Modules (also called cards) are exchangeable during test phases. This module exchange technique is very useful in determining whether or not an error will "follow" the module, thus assisting in fault location. It is important to realize that the TEST SYSTEM can not in fact be destroyed by exchanging or by pulling the modules in and out of the Nord-50 since the test program is actually located in the other computer (normally a Nord-10/S).

Errors or faults are easily isolated by using the module substitution technique. The test is repeated with the failing bit in different combinations so that it is traced to its module.

5.1.5. Test Program Overview

Figure 18 contains an overview of the Nord-50 test programs. In using this data it should be kept in mind that N50 TEST SYSTEM and TEST-MEM are run in the Nord-10/S. The remainder of the programs are run in the Nord-50.

TEST PROGRAM	MAIN TEST AREA					PROGRAM INFORMATION			
	A-RACK	B-RACK	C-RACK	N10-N50	MEMORY	ASSEMBLY PROGRAM	FORTRAN PROGRAM	COMMENTS	
N50 TEST SYSTEM						YES NORD-10		1892	
TINST						YES NORD-50		1840	
TMEM						YES NORD-50		1841	
TREG						YES NORD-50		1842	
HAMB-MET							YES	2464	
ITEST-IRMD							YES	2467	
FTEST							YES	2466	
DFTEST							YES	2465	
TEST MEM						YES NORD-10		Command in the NORD-50 monitor	
SEKUND-JTID								2463	
TCOR-NOG								2462 Verification program	

* Note. The N50 TEST-SYSTEM and TEST-MEM run in the Nord-10/S.
The remainder of the programs run in the Nord-50.

Fig. 18. NORD-50 test program overview

5.2. Nord-50 Test Program Descriptions

The following Nord-50 test programs are described:

- N50-T-SYS-1892
- TINST-50-1840 % Instruction Test
- TMEM-50-1841 % Memory Test
 Note. Described in
 Section 6.
- TREG-50-1842 % Register Test
- SEKUND-2463
- JTID-2468
- ITEST-2467 % Integer Multiply/Divide
 Test
- IRMD-2469
- FTEST-2466 % Floating Test
- DFTEST-2465 % Double Precision Test
- HAMB-MET-2464 % Floating Test
- TCOR-NGO-2462
- TCOR-DATA-2470 % Data file
- N50INITIALIZE-2471 % Example of how to
 initialize the Nord-50
- N50TEST-BATCH-2472 % Mode file to run all
 test programs in sequence
- N50TESTP-ASCOL-2473 % Mode file to assemble,
 compile and load all
 programs

5.2.1. NORD-50 TEST SYSTEM

NORD-50 TEST SYSTEM HAR-1892

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A stand-alone Hardware Test Program to test Nord-50 communication, memory and instructions with simulated memory.
- Function(s) - Tests all instructions.
- Highlights - Instructions and data are exchanged via the Nord-10/S - Nord/50 communication lines.
 - The result of the test is read back to the Nord-10/S and compared with an "Expect Table" located in the memory of the Nord-10/S.
 - Error reports are given on the Nord-10/S Console Terminal.
 - Up to 16384 combinations of data may be used to test one instruction.
 - The number of data combinations for testing each instruction can be specified. The argument in the AAX instruction found in location 1307 will specify the number of data combinations.

:1307/AAX<increment>

The argument in the instruction is used as an index in the test data area. Table 5.1 indicates the number of minutes required to run a complete test for a given number of combinations in Location 1307.

- The B-register of the Nord-10/S is displaying the test being executed.

LOCATION 1307: .	NUMBER OF DATA COMBINATIONS	NUMBER OF MINUTES TO RUN A COMPLETE TEST:
173402	16384	15.
173410	4096	4.15
173420	2048	2.5
173500	512	1.10
173577	256	0.55

Table 5.1: TEST TIMES FOR DATA COMBINATIONS - LOCATION 1307

- Implementation Instructions - Refer to the NORD-50 Test System Manual, ND-62.008.01. Also see PD (Program Description) Sheet in the NORD SOFTWARE LIBRARY.
- LOAD and RUN Procedure -
 1. Stop the Nord-10/S.
 2. Insert the Floppy Diskette with Directory 10112 into the Floppy-Drive. (This is only for a single Nord-50.)
 3. Type 1560& on Terminal No. 1 (Console Terminal).
 4. Write LO N50* on the terminal.
- * In Multi Nord-50 configurations,
Write:


```
LO N51  % For the Test System to Nord-50.1.
LO N52  % " " " " " Nord-50.2.
LO N53  % " " " " " Nord-50.3.
LO N54  % " " " " " Nord-50.4.
```
- Restart address = 1000.
Type: 1000!

Notes:

- 1. Except for the tests: 16, 17, and 50 the Nord-50 memory is not used.
- 2. Temporary errors will not be detected. The execution time in simulated memory is 10 to 15 times longer than normal execution time. The program was designed to detect "hard" errors.
- 3. The TEST SYSTEM responds to the following single letter commands:
 - D Display further information about the current error; failing instruction with mnemonic and code.
 - C Continue; continues the test with the next input data.
 - B Back; restarts the current test with data taken from the beginning of the input data table.
 - N Next test; sometimes the same test is started but with a different type of test data.
 - P Previous test.
 - R Reset; restarts from the first program.
- 4. When an error message is printed on the terminal always print D. A test number is then given followed by failing instruction and code.
- 5. Do not use the test number in the heading of the error message.
- 6. Notes about the error print-out:
 - The test system will print the A-Operand and the B-Operand even if single operand instructions are failing. For INST:SHIFT and bit instructions, only the A-Operand is used.
 - The 32 bit overflow after an integer multiply and the 32 bit remainder after an integer divide will be printed as the least result.

Additional Information:

- 1. Additional information about the Failing Test can be found in:

Nord-50 Test Programs
ND-30.007

- 2. The main test areas of the different tests are listed in Table 5.2.
- 3. The Test System accepts only even parity input. This patch is available to accept odd parity input*

OLD:	NEW:
1122/----	44011
1131/----	175235
	124376
	044004
	124001

- 4. The sequence in which instructions are executed in the Test System is shown in Figure 19.

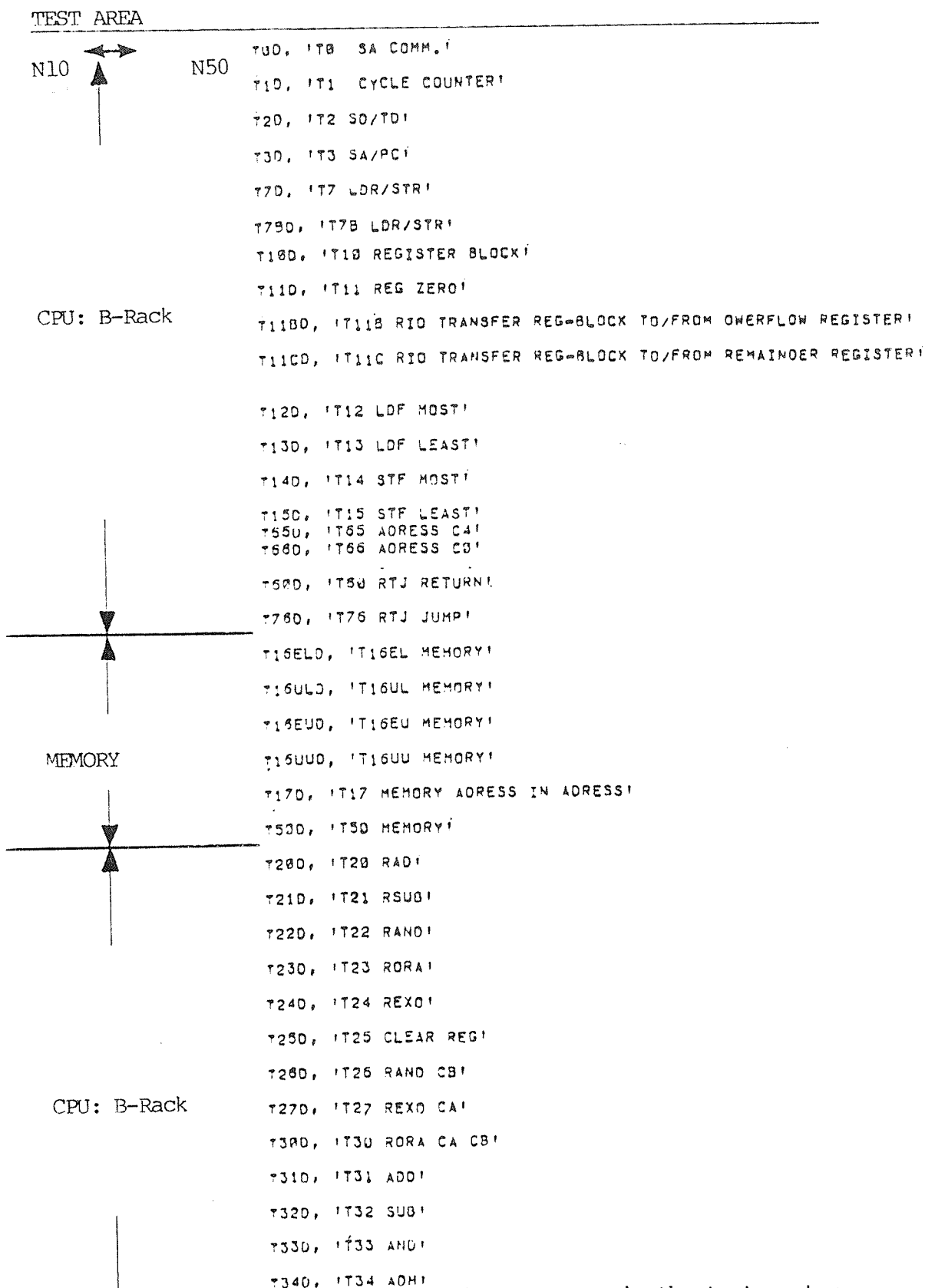
TEST NUMBER (TEST NUMBER APPEARING AFTER D)	TEST AREA:
TO	Nord-10/S - Nord-50 Communication
T16-T17-T50*	Nord-50 Memory EXAMINE-DEPOSIT via Nord-10/S
T 100 - 113 T 144 - 145 T 170 - 171 T 174 - 175 T 215 - 220 T 223 - 224 T 227	} C-Rack and Receivers/Transceivers in the B-Rack
T 164 - 167 T 172 - 173 T 176 - 177 T 221 - 222 T 225 - 226	} A-Rack and Receiver/Transceivers in the B-Rack
ALL OTHER	} B-Rack

* The address area to be tested can be specified in these two memory locations:

6412/--- % Lower Limit
6416/--- % Upper Limit


Only the area between 0-64K can be tested with the test system.

Table 5.2: MAIN TEST AREAS



TEST AREA

CPU: B-Rack



```

T350, 'T35 XMR REGISTER'
T360, 'T36 XMR MEMORY'
T370, 'T37 MIN'
T400, 'T40 SET ARG'
T410, 'T41 SET NEG ARG'
T420, 'T42 ADD ARG'
T430, 'T43 ADD NEG ARG'
T440, 'T44 CLEAR ARG'
T450, 'T45 EXCLUSIVE OR ARG'
T460, 'T46 AND ARG'
T470, 'T47 OR ARG'
T610, 'T61 ADDRESS DISP'
T620, 'T62 ADDRESS X+0'
T630, 'T63 ADDRESS B+0'
T640, 'T64 ADDRESS X+B'
T670, 'T67 ADDRESS I'
T700, 'T70 ADDRESS I DISP'
T710, 'T71 ADDRESS I X+0'
T720, 'T72 ADDRESS I B+0'
T730, 'T73 ADDRESS I X+B'
T740, 'T74 ADDRESS I I'
T750, 'T75 ADDRESS I I I I I I I'
T1500, 'T150 JPH COUNT'
T1510, 'T151 JNH COUNT'
T1520, 'T152 JZH COUNT'
T1530, 'T153 JFH COUNT'
T1540, 'T154 JPH JUMP'
T1550, 'T155 JNH JUMP'
T1560, 'T156 JZH JUMP'
T1570, 'T157 JFH JUMP'

```

Fig. 20. Instruction execution sequence in the test system

TEST AREA

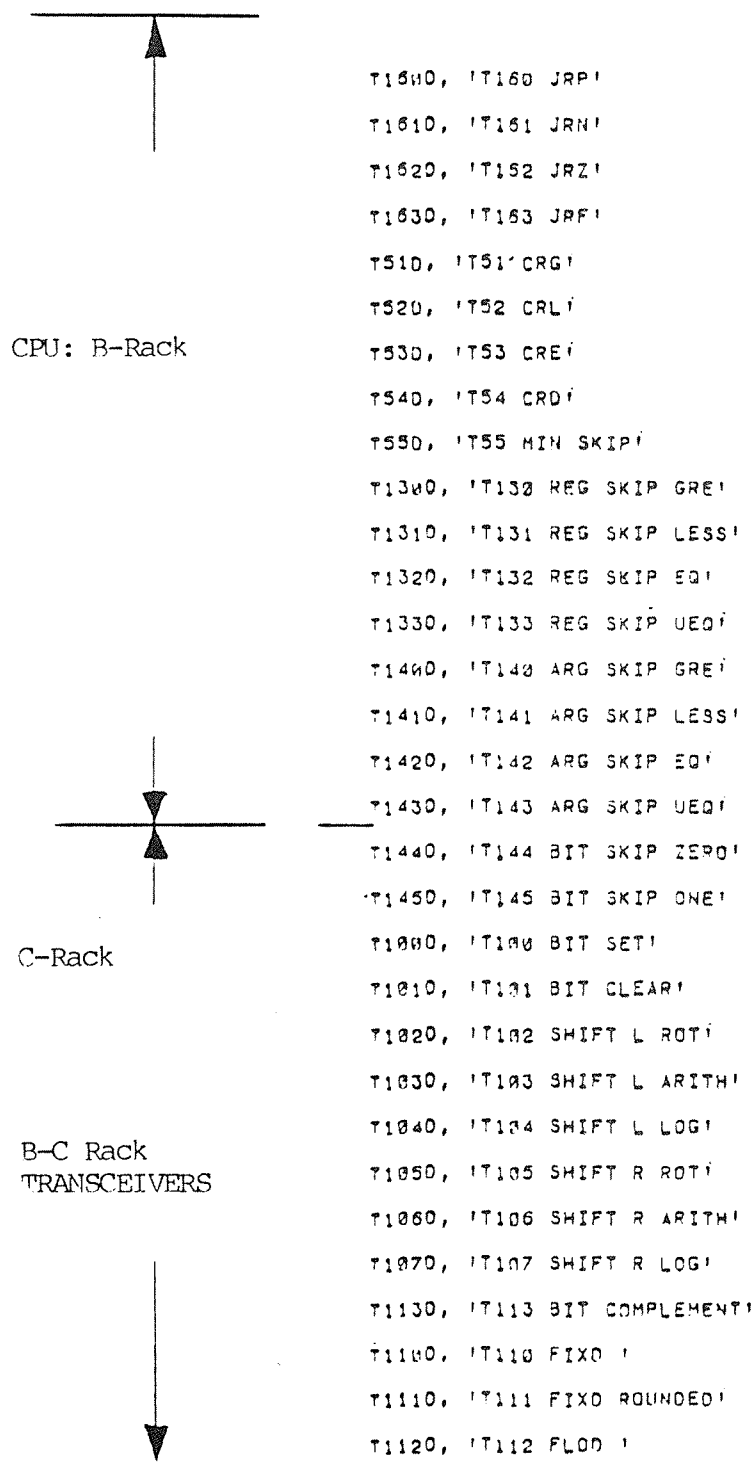


Fig. 21. Instruction execution sequence in the test system

TEST AREA RACK

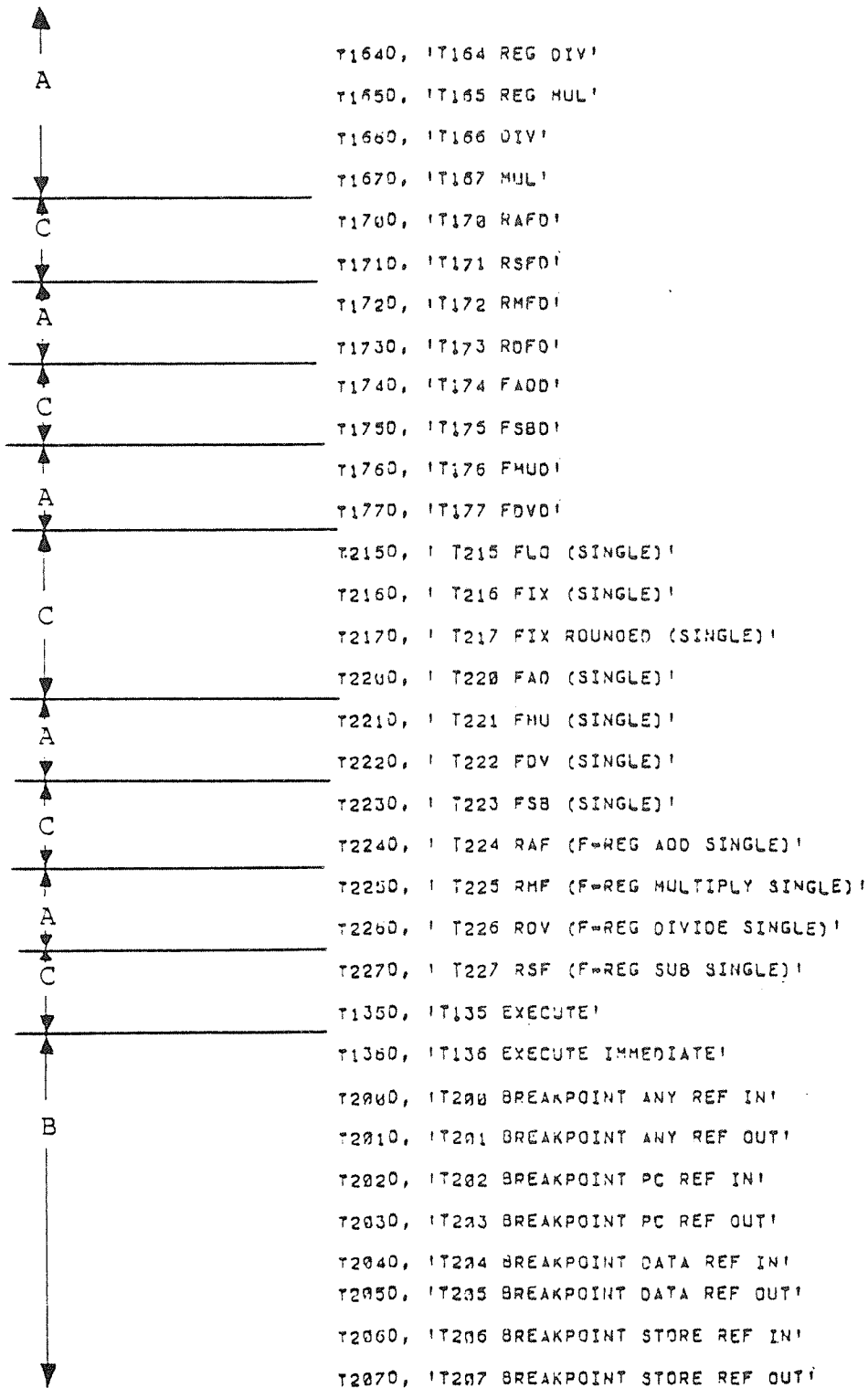


Fig. 22. Instruction execution sequence in the test system

5.2.2. TINST-50

TINST-50 HAR-1840

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A Hardware Test Program for Nord-50 instruction check.
- Highlights - The following instructions are not tested:
EXECUTE, FLOATING, DOUBLE SHIFT, CONVERT
 - Loaded, started and examined via the Nord-50 MONITOR.
 - All of the instructions are fetched from the Nord-50 main memory.
 - This program is equivalent to the Nord-10/S Instruction Check Number One (ONE-CHECK).
 - A "WAIT" Number appears of the terminal as opposed to an extensive printout.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
 - Load procedure when the MONITOR has been entered:
 - * LOAD TINST or
 - * LOAD (N50-TEST) TINST (if not logged on as user TEST).
 - Start address = 27.

Notes:

- 1. The assembly listing is necessary for finding the failing instruction. The program listing is given in Appendix F.

Additional Information:

- 1. The patch for letting the program loop by using the Nord-50 MONITOR is:

1107/RTJ O 27

- 2. Do this if the SAVE/UNSAVE routine is failing:

* PLACE TINST or * PLACE (N50-TEST) TINST
* H-G 27 * H-G 27

Note. The SAVE/UNSAVE routine is bypassed.

- 3. If the Nord-50 is functioning properly, the print-out is:

-xxx END XXX - AT : 1107

- 4. If the Nord-50 is not functioning properly the program contains the following error steps:

- STOP 0 - at:30 RTJ error
- STOP 0 - at:33 RTJ error
- STOP 0 - at:21 Further information about the error can be found in the locations listed below:

22/Content of register 1 (ACC)
23/Content of register 2 (WORK)
24/Content of register 3 (RES)
25/Address plus 1 of the test causing the error
26/Content of register 21 (ACC + 20₈)

Additional information about MPY and DIV (Address 25 = 763 or Address 25 = 1105) can be found in:

767/Multiplier/Dividend (A operand)
770/Multipleir/Divisor (B operand)
771/Expected result - lower 32 bits
772/Expected result - upper 32 bits
773/Actual result - lower 32 bits
774/Actual result - upper 32 bits

5.2.3. (TME-50:SYMB)

TME-50:SYMB HAR-1841

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments: This test program is covered in Section 6.

5.2.4. TREG-50:SYMB

TREG-50:SYMB HAR-1842

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A Hardware Test Program to check the Nord-50 register block.
- Functions - Test program for the 64 registers.
 - All registers are checked with 64 different patterns.
- Highlights - Loaded, started and examined via the Nord-50 MONITOR.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
 - Start address = 0.
 - Load procedure from the MONITOR:
 - * LOAD TREG
 - If the SAVE/UNSAVE routines are failing, use these commands:
 - * PLACE TREG % Hardware GOTO address 0
 - * H-G 0

Additional Information:

- 1. If the registers are operating normally the following message is given on the terminal:

xxx END xxx AT: 136

- 2. If the registers are not operating normally, the following error stops exist in the program:

1 - STOP - at: 1 or: 4 Register 0 is different from 0

2 - STOP - at: 17 Register 3 in error
- STOP - at: 32 Register 2 in error
- STOP - at: 45 Register 1 in error

53/Address to expected pattern
55/Read test pattern

Note. Program listing is necessary for
point 2. The program listing is
given in Appendix G.

3 - STOP - at: 66

54/Expected test pattern
55/Test pattern read
56/Register number (octal)

Examples of Print-outs:

```
*LOAD TREG
- STOP 0 - AT: 000066 -
*54/
000054: 377737777777 STD 77, 7777, 17, 17,I
000055: 377777777777 FDV 77, 7777, 17, 17,I
000056: 00000000052 STOP 000052
```


5.2.4.1. (SEKUND)

SEKUND-JTID HAR-2463

Directory Name: ND-10112
User Name: FLOPPY-USER

Comment: This test program is a part of test program
SEKUND-JTID, HAR-2463. See description for
SEKUND-JTID.

5.2.4.2. (JTID)

SEKUND-JTID HAR-2468

Directory Name: ND-10112
User Name: FLOPPY-USER

Comment: This test program is a part of test program
SEKUND-JTID, HAR-2463. See description for
SEKUND-IRMD.

5.2.5. SEKUND-JTID

SEKUND-JTID HAR-2463

Directory Name: ND-10112
User Name: FLOPPY USER

Comments:

- Purpose - SEKUND-JTID is a hardware test program actually consisting of test program SEKUND used in conjunction with test program JTID. It is (or they are) used to measure execution times for various instructions.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Consideration - Execution times will be dependent upon the type and configuration of the memory.

Additional Information:

Special Note. In the F-16 Flight Simulator application, SEKUND-JTID can be run in both the HIGH-SPEED STATIC memory (EXEC-0) and the MULTIPORT memory (EXEC-10) or in a combination of the two.

The following two sets of instructions were referred from the HIGH SPEED STATIC memory (on the left), from the MULTIPORT Memory (on the right).

*LOAD EXEC-0

LDR 1.02
STR 1.06
ADD 1.02
LDF 1.57
STF 1.56
FAD 1.41
FADD 1.88
RAF 0.86
RAFD 0.86
FMU 3.79
RMF 3.44
RMFD 6.61
FDV 3.99
FDVD 7.63
RDF 3.44
RAD 0.48
ADDA 0.48
MPY 4.97
DIV 2.00
ADM 1.53
SLR 0.86
SLRD 0.87
JFM- 0.54
EXC' 0.95
EXC" 1.43
JFM+ 1.00

- *** END *** - AT: 0000474 -
*

*LOAD (TEST)EXEC-10

LDR 1.45
STR 1.43
ADD 1.45
LDF 2.23
STF 2.04
FAD 1.85
FADD 2.50
RAF 0.88
RAFD 0.88
FMU 4.40
RMF 3.40
RMFD 6.52
FDV 4.40
FDVD 8.16
RDF 3.40
RAD 0.64
ADDA 0.64
MPY 5.34
DIV 2.39
ADM 2.06
SLR 0.89
SLRD 0.89
JFM- 0.64
EXC' 1.12
EXC" 1.93
JFM+ 1.20

- *** END *** - AT: 0100474 -
*

HIGH SPEED STATIC MEMORY

MULTIPORT MEMORY

The Load Procedure for single Nord-50 configurations is as follows:

*LOAD SEKUND SPACE

5.2.5.1. (ITEST)

ITEST-IRMD HAR-2467

Directory Name: ND-10112
User Name: FLOPPY-USER

Comment: This test program is a part of test program ITEST-IRMD,
HAR-2467. See description for ITEST-IRMD.

5.2.5.2. (IRMD)

ITEST-IRMD HAR-2469

Directory Name: ND-10112
User Name: FLOPPY-USER

Comment: This test program is a part of test program ITEST-IRMD,
HAR-2469. See description for ITEST-IRMD.

5.2.6. ITEST-IRMD

ITEST-IRMD HAR-2469

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A special test program for the reliability test of integer multiply and divide arithmetic (A-Rack).
- Highlight - The number of the test patterns is given by the number of bits per group parameter. See Table 5.2.
- Implementation Instructions - See PD Sheet in the NORD Software Library.
- Special Consideration - The Nord-50 must be in operating condition.

Notes:

- 1. Two files must be opened for WRITE prior to running the program. They are:
 - * OPEN TERM 5 W
 - * OPEN TERM 7 W
- 2. Self- documenting.

BITS PER GROUP	NUMBER OF TEST DATA	TIME PER RUN (In Seconds)
1	33	0.191
2	49	0.420
3	71	0.882
4	121	2.562
5	187	6.120
6	316	17.475
7	509	45.339
8	1021	182.427
9	1534	411.802
10	3070	1649.358
11	4095	2934.579
12	8191	11741.182
13	16383	46970.461 % Will give memory out of range with 32K Nord-50 memory.

Table 5.2: BITS PER GROUP PARAMETERS

Additional Information:

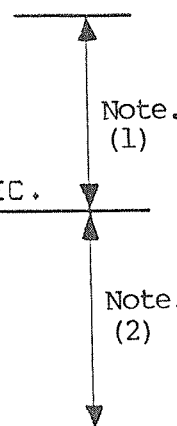
- 1. A print-out example of the running of the ITEST is as shown below:

```

ENTER TEST
PASSWORD:
OK
@-50
NORD-50/1 MONITOR - J
*OPEN TERM 5 W
*OPEN TERM 7 W
*LOAD ITEST

NEW RUN DATA? (0 OR 1): 1
LOOP ON ERROR? (0 OR 1): 1
NO. OF BITS PER GROUP (<14): 1
EXPECTED TIME PER RUN IS 0.191 SEC.
NO. OF RUNS : 1000
TIME NEEDED AFTER DATA READY IS 190.575 SEC.
NEW RUN DATA? (0 OR 1): 0
  33 DATA READY
    1 RUN(S) COMPLETED
    10 RUN(S) COMPLETED
    100 RUN(S) COMPLETED
    1000 RUN(S) COMPLETED
END...DO YOU WANT RESTART? (0 OR 1):0

```



Note. (1) = Data prepare Type 1 to new run data?

Note. (2) = Program run Type 0 to new run data?

- 2. Test Information:

The integer IA multiplied with integer IB form the Product IP 1.

The integer IB multiplied with integer IA form the Product IP 2.

There is an error print-out if IP 1 is not equal to IP 2.

The quotient $IQ1 = IP1/B$.

There is an error print-out if IQ1 is not equal to A.

The quotient $IQ2 = IP2/A$.

There is an error print-out if IQ2 is not equal to B.

Notes. Products IP1 and IP2 are printed with the overflow register first.

Quotients IQ1 and IQ2 are printed with the remainder first.

5.2.7. FTEST

FTEST HAR-2466

Directory Name: ND-10112;
User Name: FLOPPY-USER

Comments:

- Purpose - A Test Program for reliability testing of the single precision floating multiply and divide. Just for SINGLE PRECISION.
- Highlight - The number of test patterns is given by the number of bits per group parameter. See Table 5.3.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Considerations - The Nord-50 must be in operating condition.
 - The program needs more than 32K of Nord-50 memory in order to be loaded.

Notes:

- 1. See the HAMB-MET Test for the floating format.
- 2. See the ITEST Test for the method of running the program and for the preparation of data.

Additional Information:

- Error message Information.

Floating product P1 = Floating A x Floating B
 product P2 = B x A

- Error Print-out 1 - If P1 does not equal P2,

FLOATING QUOTIENT Q1 = P1/B

- Error Print-out 2 - If Q1 does not equal A,

FLOATING QUOTIENT Q2 = P2/A

- Error Print-out 3 - If Q2 does not equal B,

BITS PER GROUP	NUMBER OF TEST DATA	TIME PER RUN (In Seconds)	
1	47	5.660	
2	73	13.138	
3	113	32.793	
4	181	81.531	
5	311	214.585	
6	505	731.456	
7	1017	1901.221	
8	1531	5865.938	% Memory out of range with only 64K Nord-50 Memory.
9	3067	23549.246	
10	6139	69333.359	

Table 5.3: BITS PER GROUP PARAMETERS

5.2.8. DFTEST

DFTEST HAR-2465

Directory Name: ND-10112

User Name: FLOPPY-USER

Comments:

- Purpose - This Test Program is for reliability testing of the double precision floating point multiply and divide arithmetic (A-Rack). Just for DOUBLE PRECISION.
- Highlight - The number of test patterns is given by the number of bits per group parameter. This data is identical to the data for the FTEST Test. See Table 5.3.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Considerations - The Nord-50 must be in operating condition.
 - The program needs more than 32K of Nord-50 memory in order to be loaded.

Notes:

- 1. One file must be opened for WRITE prior to running the program. It is:
 - * OPEN TERM 5 W
- 2. See the HAMB-MET Test for the floating format.

Additional Information:

- The error message information is the same as for the FTEST Test.

5.2.9. HAMB-MET

HAMB-MET HAR-2464

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A Test Program for floating addition and multiplication, both for SINGLE AND DOUBLE PRECISION.
- Highlights - Floating number: X
Result of $X + X$ (C-Rack) compared to result of $2X$ (A-Rack).
 - Failing pattern repeated 10,000 times.
 - Number of errors per 10,000 tries is reported.
 - A random permutation of all possible patterns is used.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Consideration - The Nord-50 must be in working condition.

Additional Information:

- 1. Example of error print-out:

```
*LOAD HAMBURG
FOR HOW MANY MINUTES SHOULD THE TEST RUN ? : 3
```

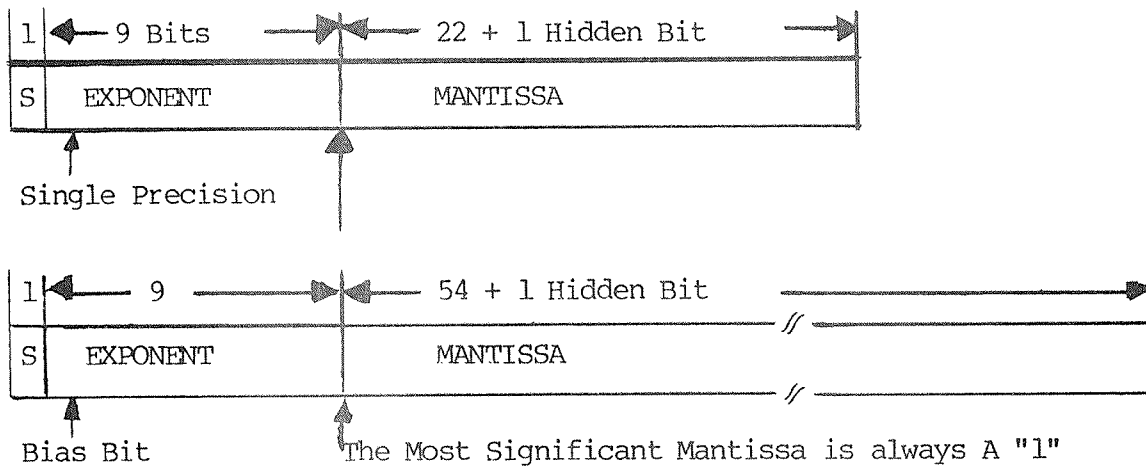
```

X          X+X          2*X          FAILING/10000
10763464416 10763464416 11003464416      1
- *** END *** - AT: 000015 -
```

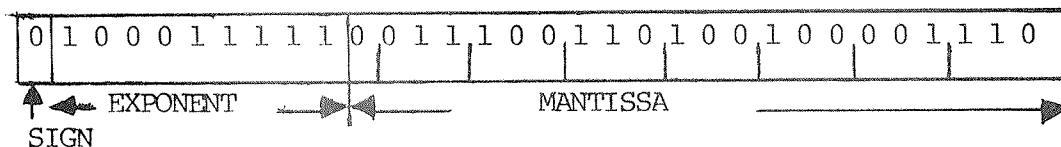
The correct answer to this problem is:
The $X + X$, or the C-Rack failing $2X$ is obtained
by adding one to the exponent.

Note. The number 2 which multiplies the X is
converted to floating point format in
the C-Rack. If both $X + X$ and $2X$ are
failing, check the C-Rack.

- 2. Nord-50 Floating Formats:



THE FLOATING NUMBER X IN THE EXAMPLE WILL THEN APPEAR AS:



5.2.10. TCOR-NGO

TCOR-NGO HAR-2462

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - Verification program to test floating arithmetic.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Consideration - A data file TCOR-DATA:DATA must be present to run this program.

Additional Information:

- Figure 22 shows a TCOR print-out.

*OPEN TCOR-DATA:DATA 5 R																			
*OPEN TERM 6 W																			
*LOAD TCOR-NGO																			
TERRAIN CORRECTION INCREMENT FR. NM RADIUS. CHECK AGAINST UNUSUAL VALUES																			
DISTANCE NM	0	0.002	0.068	0.23	0.59	0.90	1.28	1.75	2.29	2.87	3.52	5.24	8.44	12.4	18.8	28.8	58.8	99.0	166.7
CIRCLE																			
E28I063	0.00	0.00	0.00	1.07	1.07	0.39	0.82	0.47	0.58	0.44	0.451	0.220	0.075	0.037	0.014	0.009	0.011	0.011	0.00
E28I080	0.00	0.00	0.00	1.42	1.30	0.72	0.95	0.59	0.75	0.35	0.091	0.088	0.040	0.032	0.040	0.019	0.014	0.012	0.00
E28I110	0.00	0.00	0.00	0.21	0.89	0.00	0.86	0.75	1.21	0.72	0.244	0.133	0.073	0.035	0.017	0.016	0.012	0.012	0.00
E28I100	0.00	0.00	0.00	7.57	1.11	6.83	2.70	2.00	0.54	0.73	0.438	0.217	0.057	0.023	0.010	0.009	0.009	0.010	5.30
E28I061	0.00	0.00	0.00	3.87	2.94	4.25	3.32	2.59	1.37	0.83	0.538	0.355	0.208	0.125	0.078	0.037	0.022	0.017	9.00
E28N012	0.00	0.00	0.00	0.18	0.03	0.33	0.12	0.08	0.46	0.74	0.417	0.374	0.260	0.132	0.076	0.006	0.001	0.001	0.00
E28I097	0.00	0.00	0.00	7.15	12.30	0.00	3.99	1.39	0.59	0.45	0.143	0.060	0.054	0.062	0.055	0.020	0.013	0.011	13.18
E28I062	0.00	0.00	0.00	2.42	2.24	1.18	0.61	0.57	0.57	0.52	0.432	0.309	0.085	0.037	0.022	0.012	0.011	0.011	2.77
E28I092	0.00	0.00	0.00	1.75	4.85	2.79	4.54	3.57	2.59	1.93	1.627	0.513	0.136	0.058	0.045	0.025	0.016	0.014	0.00
E28I102	0.00	0.00	0.00	9.45	7.42	6.30	3.43	2.66	1.47	0.97	0.674	0.472	0.239	0.113	0.053	0.034	0.020	0.016	7.19
STATION	LATITUDE	LONGITUDE	ELEVATION	LAYER	TERRAIN	FREEAIR	BOUGUER ANOMALY												
E28I063	62 11.23	8 13.33	1414.4	159.58	5.99	436.08	-60.62												
E28I080	62 11.62	7 50.32	1507.1	169.99	6.04	464.65	-64.25												
E28I110	62 13.28	7 58.51	1445.8	163.10	5.96	445.76	-65.30												
E28I100	62 13.43	8 7.69	1315.5	140.47	12.24	405.60	-63.75												
E28I061	62 14.36	7 41.21	1755.9	197.90	19.02	541.33	-59.13												
E28N012	62 15.90	8 11.30	572.0	64.70	6.18	176.39	-61.87												
E28I097	62 16.80	7 46.57	1417.0	159.87	17.08	436.08	-59.00												
E28I062	62 17.45	8 16.37	1401.3	158.11	7.73	432.04	-56.75												
E28I092	62 18.54	8 0.32	1573.2	177.41	17.98	485.02	-59.00												
E28I102	62 18.72	7 52.73	1700.2	191.65	19.56	524.16	-50.38												
02370 STOP																			
- *** END *** - AT: 0000015 -																			
*CC LAST 3 NUMBERS OUT SHOULD BE : 19.56 524.16 -58.38 .																			

FIGURE 22

5.2.11. TCOR-DATA

TCOR-DATA HAP-2470

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - To be used with TCOR-NGO.
- Function - TCOR-DATA is the data file that must be present to run test program TCOR-NGO.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.

5.2.12. N50 INITIALIZE

N50 INITIALIZE HAR-2471

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - This is an example of how to initialize the Nord-50.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.
- Special Consideration - This program must be modified according to the actual system configuration.

5.2.13. N50 TEST-BATCH

N50 TEST-BATCH HAR-2472

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - This is a mode file to run all of the test programs in sequence.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.

5.2.14. N50 TESTP-ASCOL

N50 TESTP-ASCOL HAR-2473

Directory Name: ND-10112
User Name: FLOPPY-USER

Comments:

- Purpose - A mode file to assemble, compile, and load all of the test programs.
- Implementation Instructions - See PD Sheet in the NORD SOFTWARE LIBRARY.

6.NORD-50 MEMORY SYSTEM

6.1. Introduction

This section contains:

- General information on the Nord-50 memory.
- The multiport memory as seen from the Nord-50.
- The test possibilities for the Nord-50 memory.
- The identification of failing memory modules.

Notes. - Sections 6.2 and 6.4 will only deal with the multiport memory system as it is found in the "European" version of the Nord-50. The "F-16" memory configuration is not covered in these sections.

- Appendix B contains a step-by-step procedure for the Nord-50 test sequence.

6.2. General Nord-50 Memory Information

The Nord-50 may be physically connected to the same memory as the Nord-10/S via one port in the multiport memory system (a shared memory) or to a separate multiport memory system as a private memory. This is shown in Figure 24.

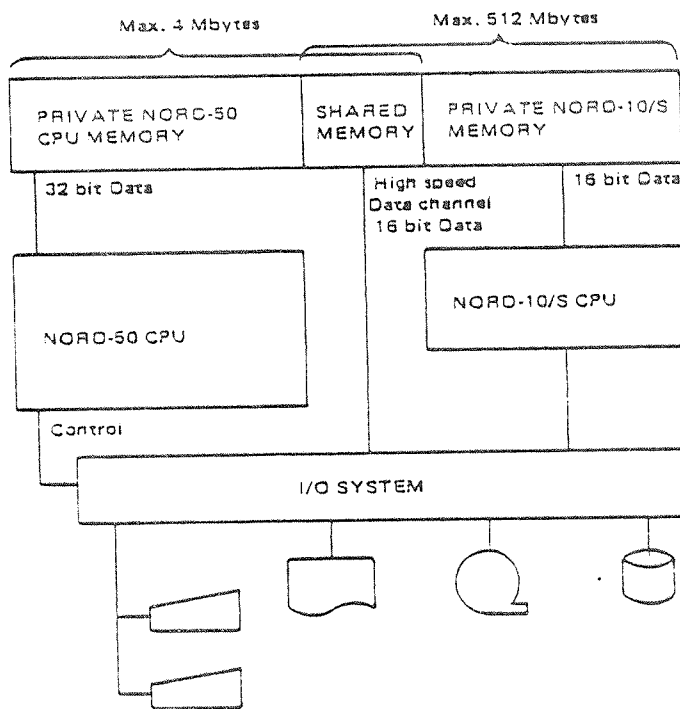


Fig. 24. The NORD-50 computer system

The Nord-50 supplies differential address lines of 20 bits + 2 control signals to the port via a one-to-one cable.

Two cables with differential lines are used for carrying the 32 bit data word. One cable is for bits 0-15 plus 2 parity bits. The other cable is for bits 16-31 plus 2 parity bits.

In memory (the multiport memory system), the Nord-50 occupies one port out of four. The remaining three ports are used by the DMA mass storage devices of the Nord-10/S. The third may be used by a second Nord-50.

The address area each port can utilize is set by the lower and upper limit switches on the address module in the multiport system. This provides for private and shared memory locations for both the Nord-50 and for the Nord-10/S.

The priority for the requests of both the Nord-50 and the Nord-10/S is fixed. The priority is determined by the physical position of the data receiver/driver module and the address receiver module in the multiport rack.

The 32 bit memory word is divided between two 18 bit memory banks with identical memory addresses. The bank in the upper multiport rack takes care of bits 0-15, while the bank in the lower rack handles bits 16-31.

The Nord-50 receives two sets of data ready/address ready signals from the memory modules in the two banks. These signals are supplied to the Nord-50 via the data module in the multiport where the signals are latched - waiting for the last signal to appear.

In a typical Nord-50 configuration, there are two 16 bit multiport channels (i.e., one for the CPU and the other for the DISK) and one 32 bit channel (i.e., for the Nord-50). The address cable of the 16 bit channels are shifted (i.e., interleaved). In this way, all odd addresses are routed to the upper multiport rack and all even addresses are routed to the lower multiport rack. Two 16 bit words, stored in memory into two sequential addresses, are read by the Nord-50 in one read operation.

Figure 25 shows an example of a memory layout in a Nord-10/S - Nord-50 configuration.

6.3. General Precautions for Swapping Nord-50 Multiport Modules

When error messages such as:

MEMORY OUT OF RANGE

or

MEMORY PARITY ERROR

appear on the terminal screen, do not swap modules in the M1 rack with the corresponding module in the M2-rack. The reason for this is that the Nord-50 must have both racks responding when supplying a 32 bit word.

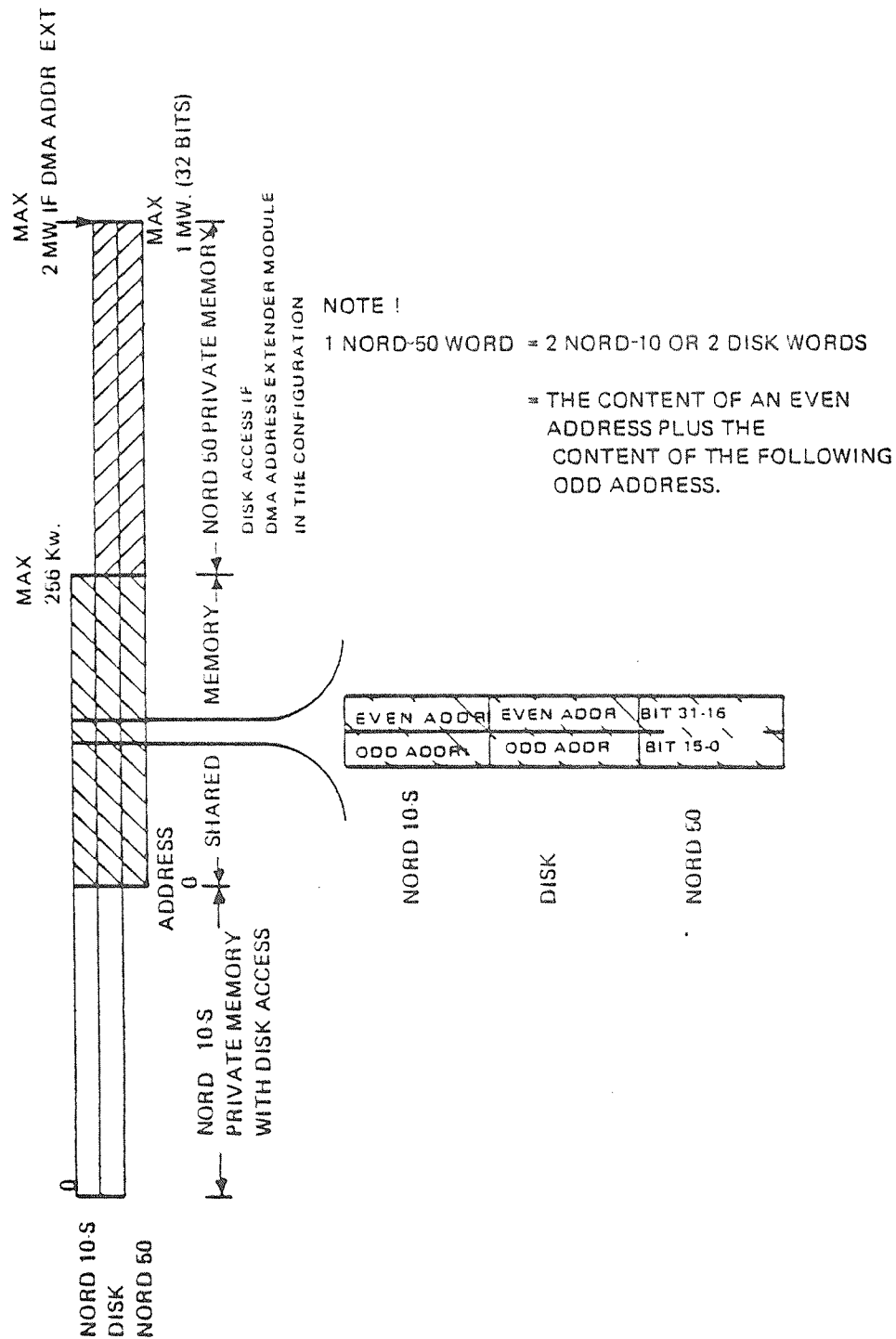
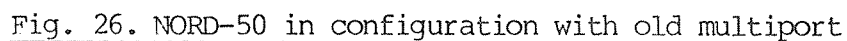


Fig. 25. Memory layout in a NORD-10S - NORD-50 configuration

Figure 26 illustrates the Nord-50 configuration with old multiport.



General information about the Old Multiport is found in the Nord-10/S Hardware Maintenance Manual.

Figure 27 illustrates the Nord-50 configuration with big multiport.

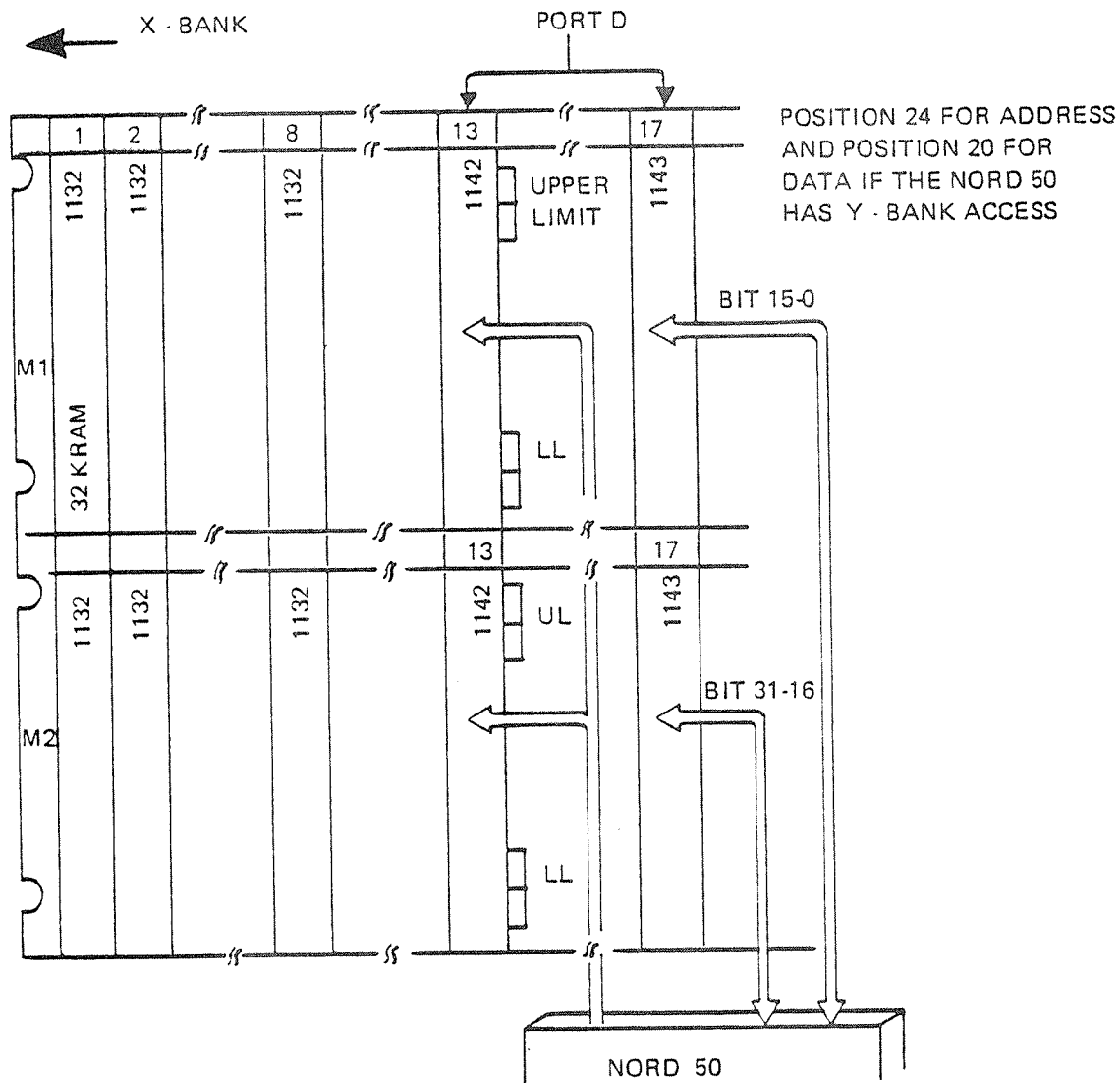


Fig. 27. NORD-50 in configurations with big multiport

Notes ! - Rack-M1 and rack-M2 receive the same Nord-50 address.

- Nord-50 data bit 15-0 to/from rack M1.

- Nord-50 data bit 31-16 to/from rack M2.

- Parity bits 0 and 1 on the Nord-50 operator's panel are referring to rack-M1, bits 2 and 3 are referring to rack-M2.

General information about the Big Multiport is found in the Nord-10/S Hardware Maintenance Manual.

6.5. Types of Tests for the Nord-50 Memory

The types of tests used for the Nord-50 memory are covered in this section.

6.5.1. SHARED MEMORY TESTED FROM THE NORD-10/S

The shared memory (i.e., a memory where both the Nord-10/S and the Nord-50 have access) can be tested by all available Nord-10/S memory test programs (i.e., MOVER, MULTI, T8KMOS, and T32KMOS). Nord-10/S test programs are found in the Test Program Description Manual for the Nord-10/S and the Nord-100.

A Nord-50 address can be converted to a Nord-10/S address in shared memory by using this formula:

$$\begin{array}{r}
 \text{NORD 10 ADDRESS FOR} \\
 \text{NORD 50 ADDRESS 0} \\
 + \\
 (\text{NORD 50 ADDRESS}) * 2 \\
 + \\
 \begin{array}{l}
 0 \text{ if bit 31-16} \\
 \text{or} \\
 1 \text{ if bit 15-0}
 \end{array} \\
 \hline
 \text{NORD 10 ADDRESS} = \hline
 \end{array}$$

6.5.2. SHARED AND NORD-50 PRIVATE MEMORY TESTED FROM THE NORD-50

They are:

1. TEST-MEM : command in the Nord-50 MONITOR
2. TMEM : Nord-50 test program
3. Additional test possibilities

6.5.2.1. TEST-MEM

The command for TEST-MEM is built into the Nord-50 MONITOR. When the command:

*TEST-MEM

is given, the Nord-50 is set in MEMORY EXAMINE/DEPOSIT MODE by the monitor. Data and addresses are then supplied from the Nord-10/S via the I/O system in the Nord-10/S and the Nord-50 CPU to the Nord-50 memory, private and shared.

The test is performed by reversing the data flow and checking the received data.

The following are the highlights of this program:

- This memory test program is in the Nord-50 MONITOR. The command is also in the monitor.
- The Nord-50 memory is tested by depositing/examining the memory via the Nord-10/S Input/Output System.
- The Nord-50 memory is tested in decimal increments of 1K.
- Patterns: 0
 -1

252525252
125252525
37700177400
37777600000
00000177777

Address in address test (2 x 16 bits address)

- See Figure 28 for an example of an Address in Address Test.
- Error print-outs:

Pattern test failing

Address test failing

- Looping is possible if this command is given before program start

*LOOP-ON

Program will loop, and if there is an error, the failing pattern will be repeated

*LOOP-OFF

Note. The address protect registers BP and BQ must be reset prior to the start of the test. Reset BP and BQ with this command:

*B-C , ,P

Examples of this print-out:

@ N-50

NORD-50 MONITOR - K

*B-C , *P

*TEST-MEM

START ADDRESS: 0

NUMBER OF 1K BLOCKS TO BE TESTED : 32

OK!

*

The Address in Address Test, indicated in the highlights is used both in TEST MEM and IMEM.

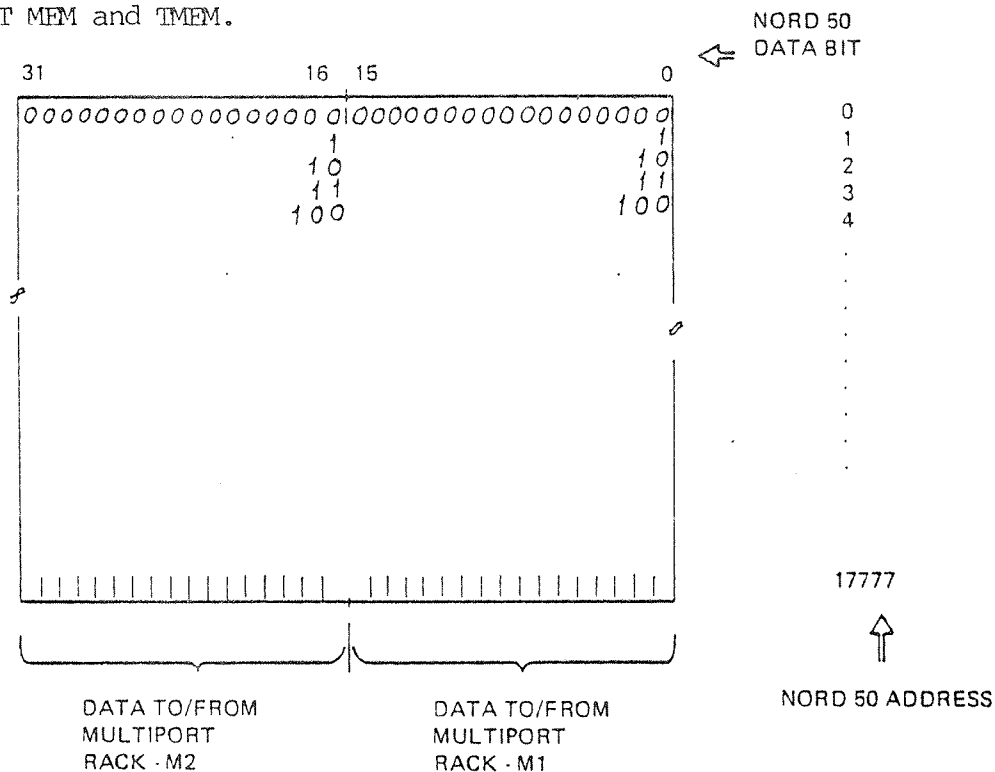


Fig. 28. Address in address test

The two racks in the multiport memory receive the same Nord-50 address. Data bit 15-0 is for the upper rack while data bet 31-16 is for the lower rack.

The Address in Address Test is built up of two blocks of 16 bits each. By using this method it is possible to detect address error both in the M1 and M2 racks. If both racks are failing, suspect the source = Nord-50.

6.5.2.2. TMEM

The Nord-50 memory is tested with the program TMEM. This program is loaded and started with the *LOAD command in the Nord-50 MONITOR. Addresses are specified so that all or any part of the shared memory, the high speed static memory or the Nord-50 private memory can be tested.

The highlights of this test are:

- The test program is used to test and run the Nord-50 memory.
- The program is loaded and started via the Nord-50 MONITOR.
- The following tests may be specified:

Test1*:Store/Read 0

Test2*:Store/Read - 1

Test3*:Address in Address Test (2x16 bits address)

Test4*:Address in Address Test with inverse address

Test5**:Walking tests

- a) writes a pattern in the test area
- b) writes the pattern inverted in the first location
- c) checks that no locations are changed
- d) resets inverted pattern

* = Fast Tests

** = Overnight Test

- Start address = 0
- Examples of Print-out:

```

@N-5 1
NORD-50/1 MONITOR - J
*B-C , ,P
*LOAD TMEM

```

```

THIS IS YOUR N-50 MOS MEMORY TEST PROGRAM
THE PROGRAM OCCUPIES LOCATIONS: 0000000 TO 0001227
LOWER TEST ADDRESS(OCTAL): 100000
UPPER TEST ADDRESS(OCTAL): 117777
SPECIFY TESTS TO BE RUN BY OCTAL
NUMBERS TERM. BY CR.STOPS WHEN 0 IS TYPED
77 MEANS ALL TESTS
77

```

```

WANT TESTS TO LOOP? 0:NO 1:YES

```

```

1
ERRORS WILL BE REPORTED IN THE FOLLOWING FORMAT
TEST1,2,3&4: <FAILING ADDR.>, <FOUND DATA>, <EXP. DATA>, <TEST NO>
TEST5: <WALK PATT. ADDR.>, <SAME AS ABOVE>, <READ/WRITE>

```

6.5.2.3. Additional Testing Possibilities

The stand-alone test program

MEM-TEST-2304

is available for testing the memory shared between the universal DMA interface and the Nord-50.

The stand-alone test program

MEMORY-MAP-2317

is used to examine memory configurations. The program will determine the parts of memory that are shared and indicated the manner of program division.

6.6. Failing Memory Module(s) Identification

Figures 28 and 29 will assist in identifying failing modules.

Figure 28 should be used in conjunction with Section 6.4.

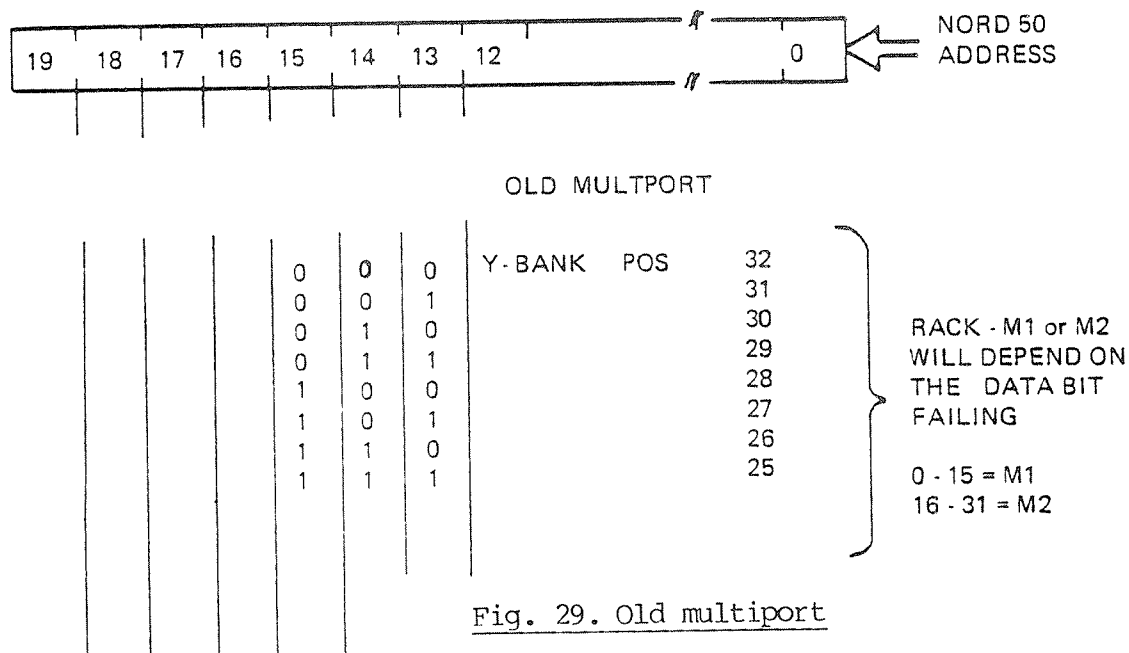


Fig. 29. Old multiport

Figure 27 should be used in conjunction with Section 6.5.

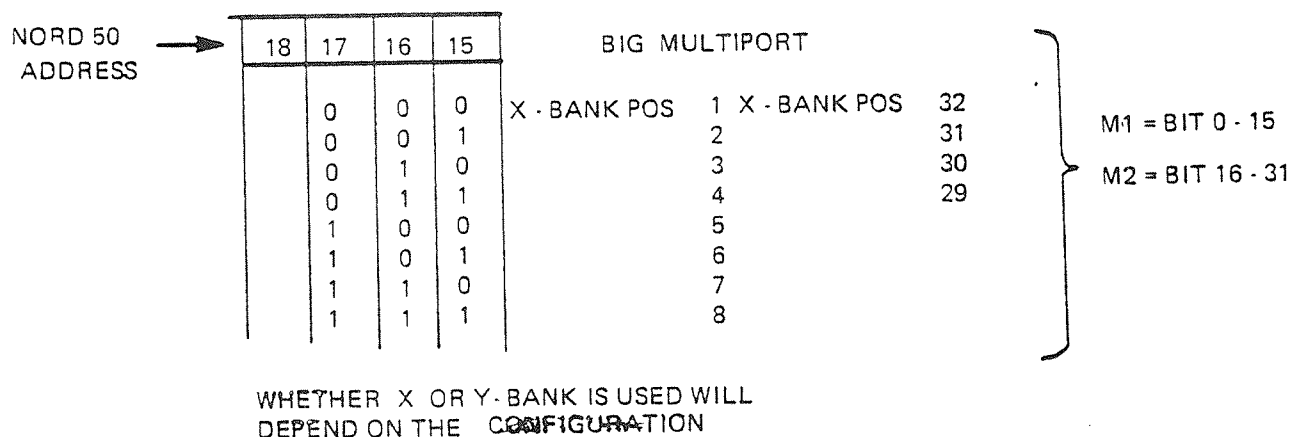


Fig. 30. Big multiport

7.NORD-50 MEMORY EXPANSION

7.1. Introduction

This section is divided into three parts. The first part contains a description of the hardware implementation. The second part contains a description of the software implementation. This part also gives some general remarks about the memory in a Nord-10/S - Nord-50 configuration. In the third part the software commands for changing the memory are covered in detail.

7.2. Memory Expansion Hardware

In configurations with the BIG-MULTIPORT memory, the memory is expanded in 32k x 32 bit increments (2 memory modules). This equals 64k x 16 bit increments or 100 octal pages seen from the disk or the Nord-10/S. In the "old" multiport with 8k (1094) memory modules, the memory can be expanded in 8k x 32 bit or 16k x 16 bit increments.

Note. The memory expansion must always be symmetrical in the M1 and M2 memory racks. Remember to update the address-range switches in the address module of the Nord-50 port of Nord-50 private memory - or all the ports (Nord-50, DMA and Nord-10/S) if expanding the SHARED memory.

7.3.Memory Expansion Software

7.3.1.Nord-50 Memory - General

The absence of a memory management system in the Nord-50 disallows a dynamic swapping of Nord-50 memory during program execution. Therefore, all parts of a program must be in memory prior to its execution, and it must remain there throughout the execution. This also applies to the pages in shared memory. Being a part of the Nord-10/S memory, the pages in shared memory are normally subject to swapping outside the programmer's control.

A way to prevent SINTRAN from swapping a specified physical area is to load a segment and "fix" it in memory using the FIXC monitor call. This is performed automatically by the Nord-50 MONITOR when preparing for the execution of a program. In Figure 31 the Nord-50 program resides in the shaded region.

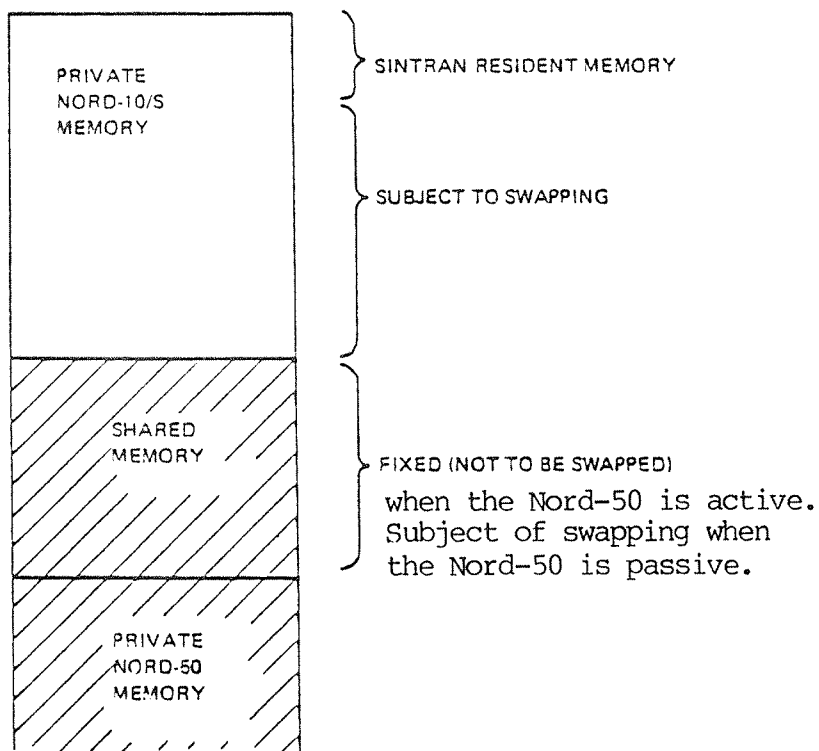


Fig. 31. Physical memory organization

Some Nord-50 programs will not occupy the entire shared memory. In such cases it is uneconomical to fix it all. A better utilization of shared memory is obtained by splitting it into partitions, where each partition is represented by a segment. See Figure 31.

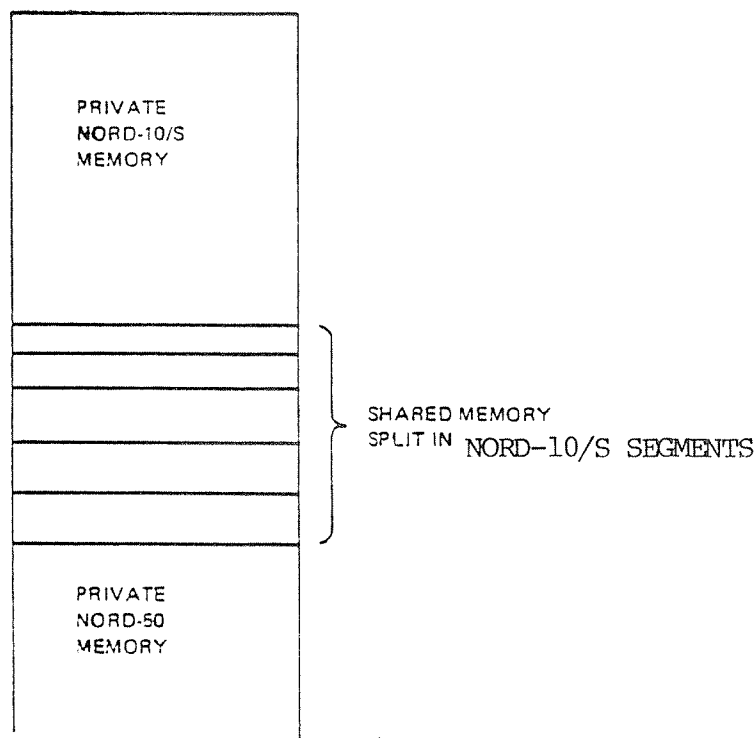


Fig. 32. Shared memory split in segments

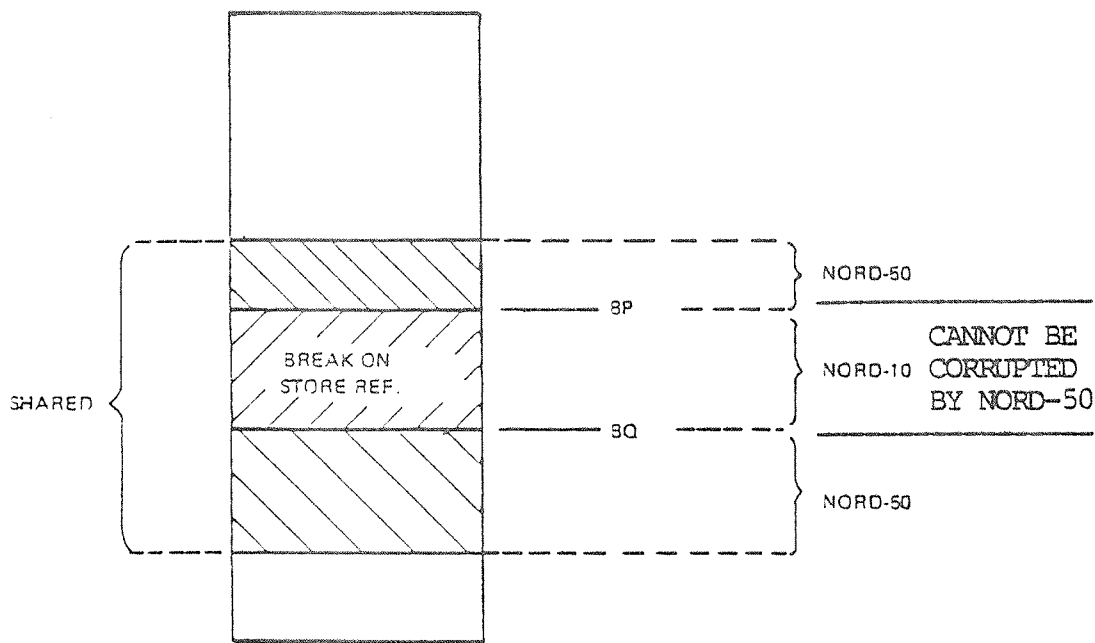
When a part of memory is allocated for the Nord-50, the **SEGMENT TABLE** is used to place the segments in the correct place in the physical memory.

The segments may be of different sizes. Each segment is fixed separately if the corresponding memory space is required by a Nord-50 program.

Important

Note. The finer the partition (i.e., the smaller the segments), the better the utilization of shared memory will be. However, increased administrative overhead is the price we have to pay.* Figure 31 illustrates how shared memory should be utilized.

* Typical size is 16k (16 bits) when 128k of shared memory.



BP and BQ define break area set by:

NORD-50 Loader

- *EXIT (stored in block 0 of program)
- *BREAK-CONDITIONS

NORD-50 Monitor

- *BREAK-CONDITIONS

Fig. 33. Shared memory allocation

In the discussion above, we have assumed all segments in shared memory to be **dynamic** segments. A dynamic segment has the quality that it will only be fixed when required. A **static** segment, however, will be fixed the first time it is required, and will remain fixed whatever program is being run.

An RT common area may also be a part of shared memory. This area is not subject to swapping and allocates no segment for this part of memory. The organization of physical memory is mapped by the Nord-50 Memory Segment Table. This table is illustrated in Figure 34.

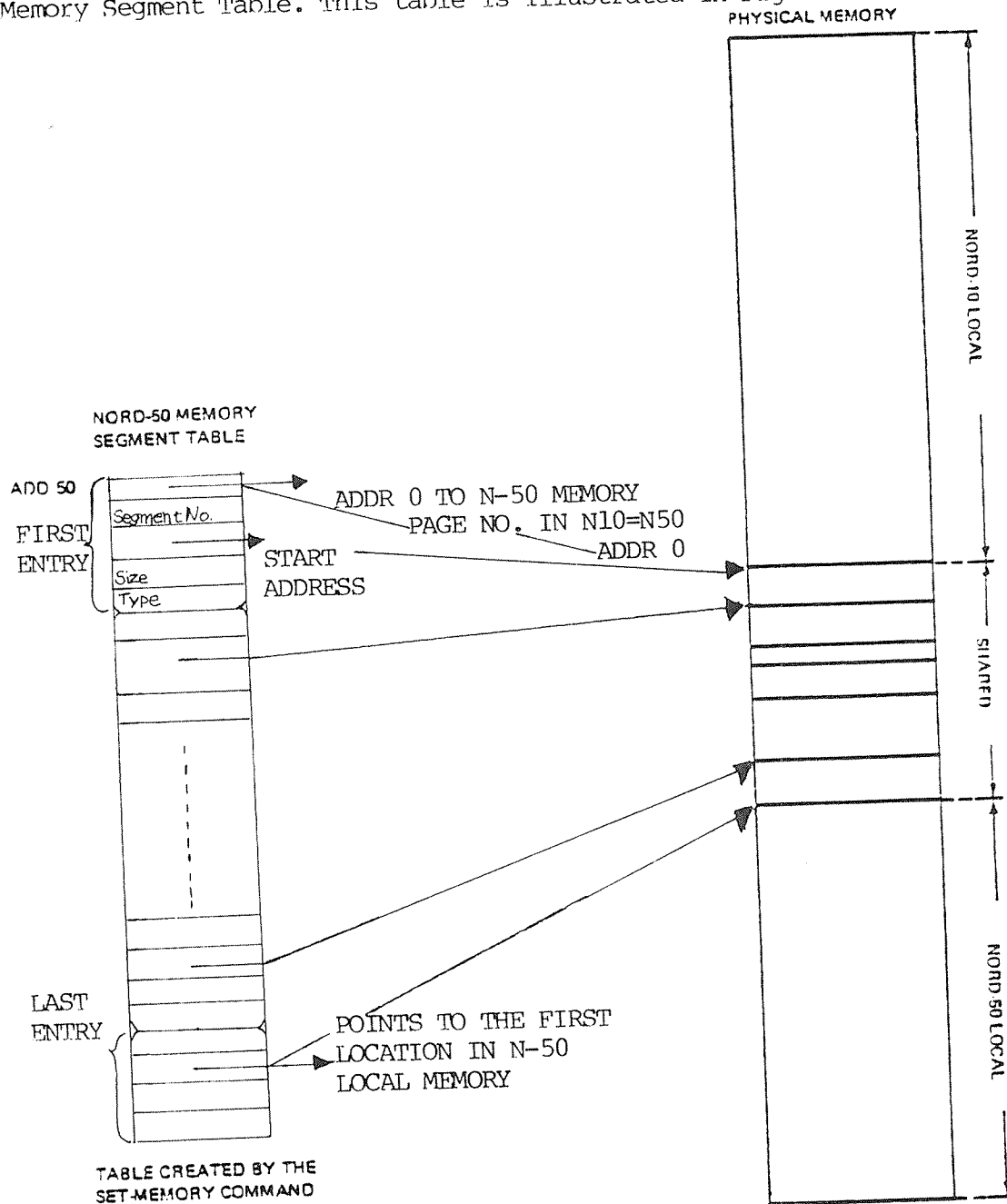
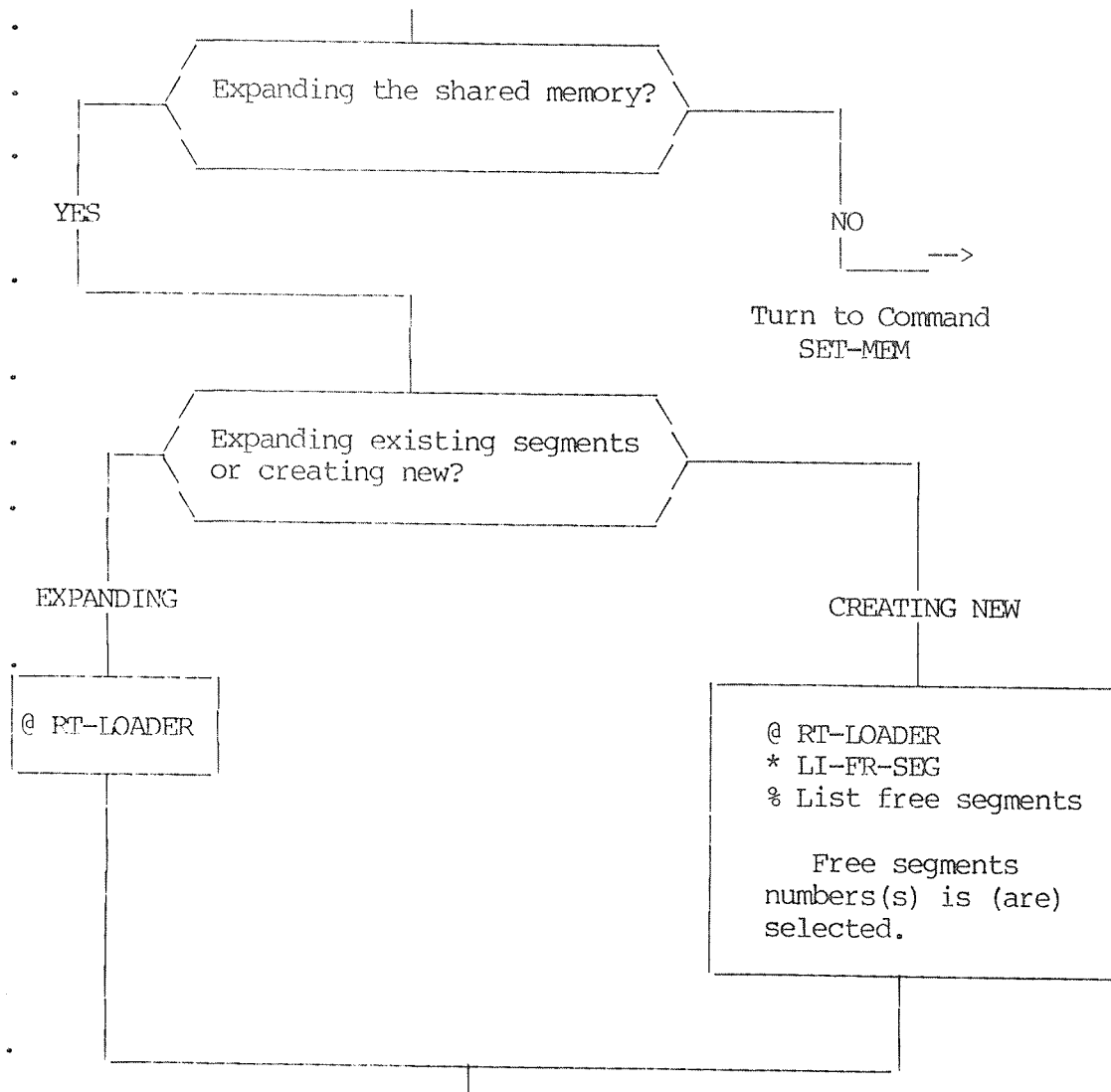


Fig. 34. NORD-50 memory segment table

7.3.2. Memory Expansion7.3.2.1. Software Commands

1

Check if RT-core common area
by this command:

* WRITE-SEGMENT 0,,,

Then specify these commands:

*

* N-S % New segments
 % Only in creating
 a new segment

* SET-P-T 1

*

* A-A % Allocate area

* FORMAT NEXT PAGE

7.3.2.2. RT-Loader Commands

* NEW-SEGMENT % SPECIFY A NEW SEGMENT

<segment w> Number of the segment(s) to
 be expanded or segment number(s)
 from LI-FRI-SEG

<ring> Protect ring 0,1,2 or 3
 Default = 0

<segment type> ND = Non demand
 DM = Demand

<protect bits> Permit bits:

 F = fetch permitted
 R = read permitted
 W = write permitted or
 any combination

 Default = RFW

<WP/NP> Written in page bit set

 WP = SET
 NP = Not SET (default)

Example:

N-S 204 2 ND RW WP

A-A % ALLOCATE AREA

<segment numbers> Segment number of the
 segment currently being built

<area size> Number of 16 bit words
 in Octal

 8 K = 20 000
 16 K = 40 000
 24 K = 60 000
 32 K = 100 000

<lower address> First address of the area
 to be allocated.

Note. - 2 pages in Nord-10 = 1 page in Nord-50

- The area size in RT-LOADER is converted to
SET-MEM size in N50 MONITOR as indicated
below:

RT-LOADER = SET-MEM in N50 MONITOR
area size size

$\text{<AREA SIZE>/2.1000} = \text{<SIZE>}$

Example:

AREA SIZE :	40 000	=	SET-MEM SIZE :	20
	60 000	=	" "	: 30
	100 000	=	" "	: 40

The RT common area is not specified here.

7.3.2.3. Nord-50 MONITOR Commands

SET-MEM

Command for generating the Nord-50 Segment Table. It indicates which segment should make which part of physical memory.

<N-10 page no.)

Nord-10 page number for Nord-50 address 0

40	=	32K
100	=	64K
200	=	128K
300	=	192K
400	=	256K

This parameter is found by the CONFIGURATION-INVESTIGATOR test program.

<segment No.>*

Allocated segment number with A-A command in RT-loader

-1 = no segment defined in this part of memory

Used when:

1. RT-common
2. Nord-50 private memory

0 = Denotes end of table

<size>*

Size in Nord-50 pages

10	=	4K N50	=	8K N10
20	=	8K N50	=	16K N10
40	=	16K N50	=	32K N10
100	=	32K N50	=	64K N10
200	=	64K N50	=	128K N10
400	=	128K N50	=	256K N10

<type>*	0	=	DYNAMIC	
	1	=	STATIC	
	2	=	RT-COMMON	
	3	=	LOCAL N50 MEMORY	
	4	=	" " " with DMA	
				access
	5	=	HOLE	

Note. * means repeated until segment number is zero.

When the SET-MEM command is given, the size parameters are added together and tested against the physical memory. If a mismatch, the error messages listed in Section 4 are given. Figure 35 shows an example of a SET-MEM command.

```

KN
QNDRO-50 3
KU
KN
SET-MEM 100 -1 100 3 70 40 1 71 40 1 -1 400 5 -1 100 4 -1 100 4 0
KU
KN
EX

```

Type	Size in Pages	Segment No.	
N50 PRIVATE WITH DMA ACCESS	100	- 1	256K
	100	- 1	
HOLE	400	- 1	196K
			128K
SHARED	40	71	64K
	40	70	
N50 PRIVATE	10	- 1	32K
64K N-10			<-- Nord-50 Address 0 = Nord-10 Page No. 100 Octal
- - - - -			<-- Nord-10 Address 0

Fig. 35. Example of SET-MEM command

LIST-MEMORY <output file>

This command lists the segment table.

Example:

```
*LIST-MEMORY 1 ✓
SEGMENT NO.  FIRST ADDR.  SIZE  IN USE  TYPE
061          000000      0020      X  DYNAMIC
046          020000      0020      DYNAMIC
047          040000      0020      DYNAMIC
050          060000      0020      DYNAMIC
051          100000      0020      DYNAMIC
052          120000      0020      DYNAMIC
053          140000      0020      DYNAMIC
054          160000      0020      DYNAMIC
055          200000      0020      X  DYNAMIC
056          220000      0020      X  DYNAMIC
057          240000      0020      X  DYNAMIC
050          260000      0020      X  DYNAMIC
NONE         300000      0020      X  LOCAL MEMORY
                                FOR NORD-50
```

NORD-10 PAGE NO. FOR NORD-50 ADDRESS 0:

0100

8.NORD-50 POWER SYSTEM

8.1. Introduction

This section covers three topics:

- AC distribution (an example)
- DC distribution (an example)
- DC voltage measurement

For a description of the power supplies in use, refer to the Nord-10/S Hardware Maintenance Manual.

For details of the AC and DC power distribution in the Nord-50, refer to the Nord-10/S technical/mechanical drawings numbers 10/S-26-29 and 10/S 44-65.

8.2. AC Distrubution

8.2.1. Nord-50 Power Sequence

To turn ON the Nord-50, the following conditions should be fulfilled:

- The Nord-10/S must be turned on. (220 V AC to solid state relay for AC sequence control.)
- The power in the Nord-50 operators panel must be pushed. (The key must be released.)
- The main switch in the Nord-50 power supply must be ON.

Note. The additional multiport memory supply , in some configurations is located in the bottom of the Nord-10/S cabinet.

The Nord-50 is automatically turned OFF when powered down.

Turning OFF the Nord-50 will not affect the Nord-10/S, but the multiport memory power will be turned OFF.

8.2.2.AC Distribution in the Nord-50

Figure 36 illustrates the AC power distribution in the Nord-50.

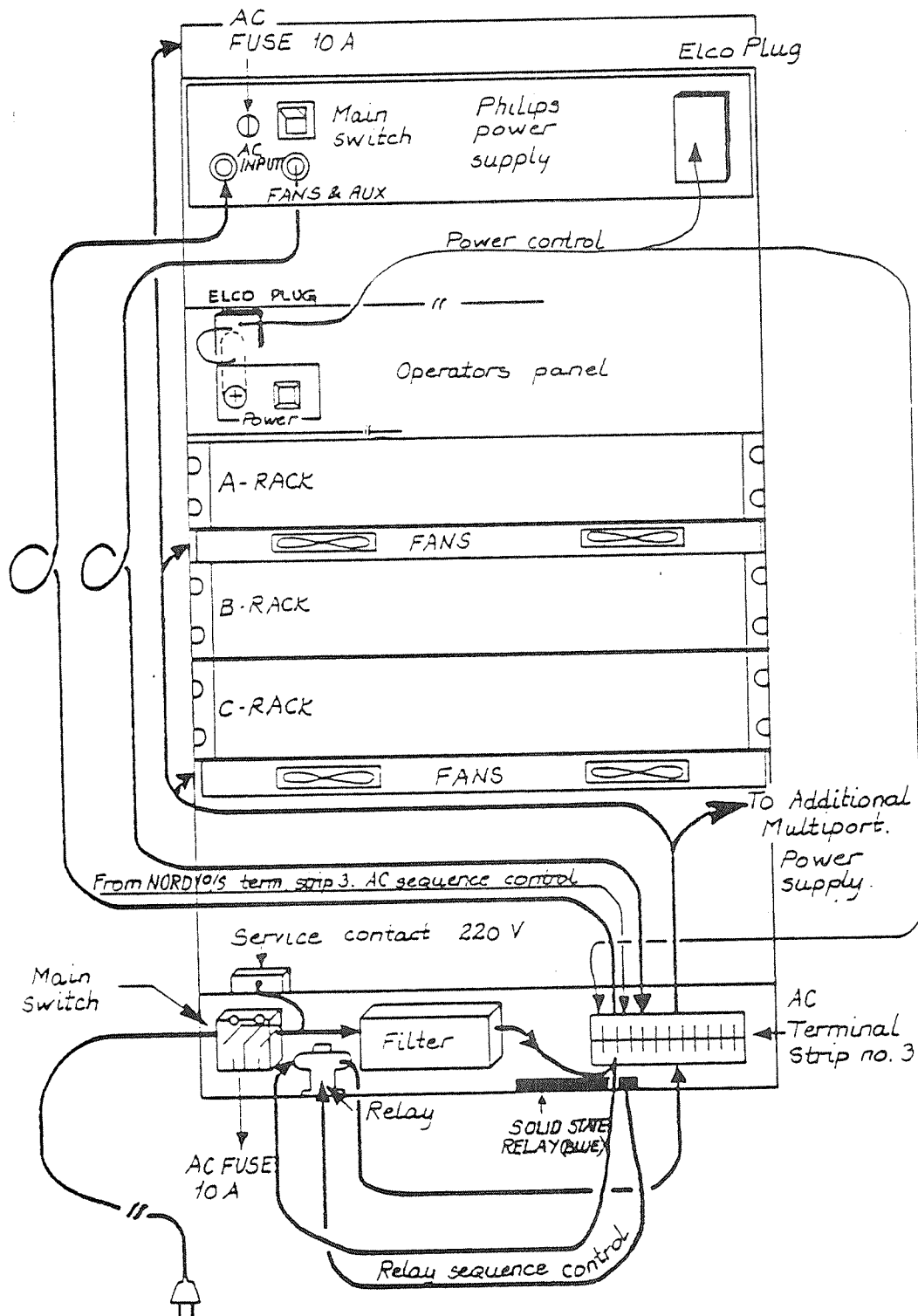


Fig. 36. AC power distribution in the NORD-50

8.3.DC Power Distribution

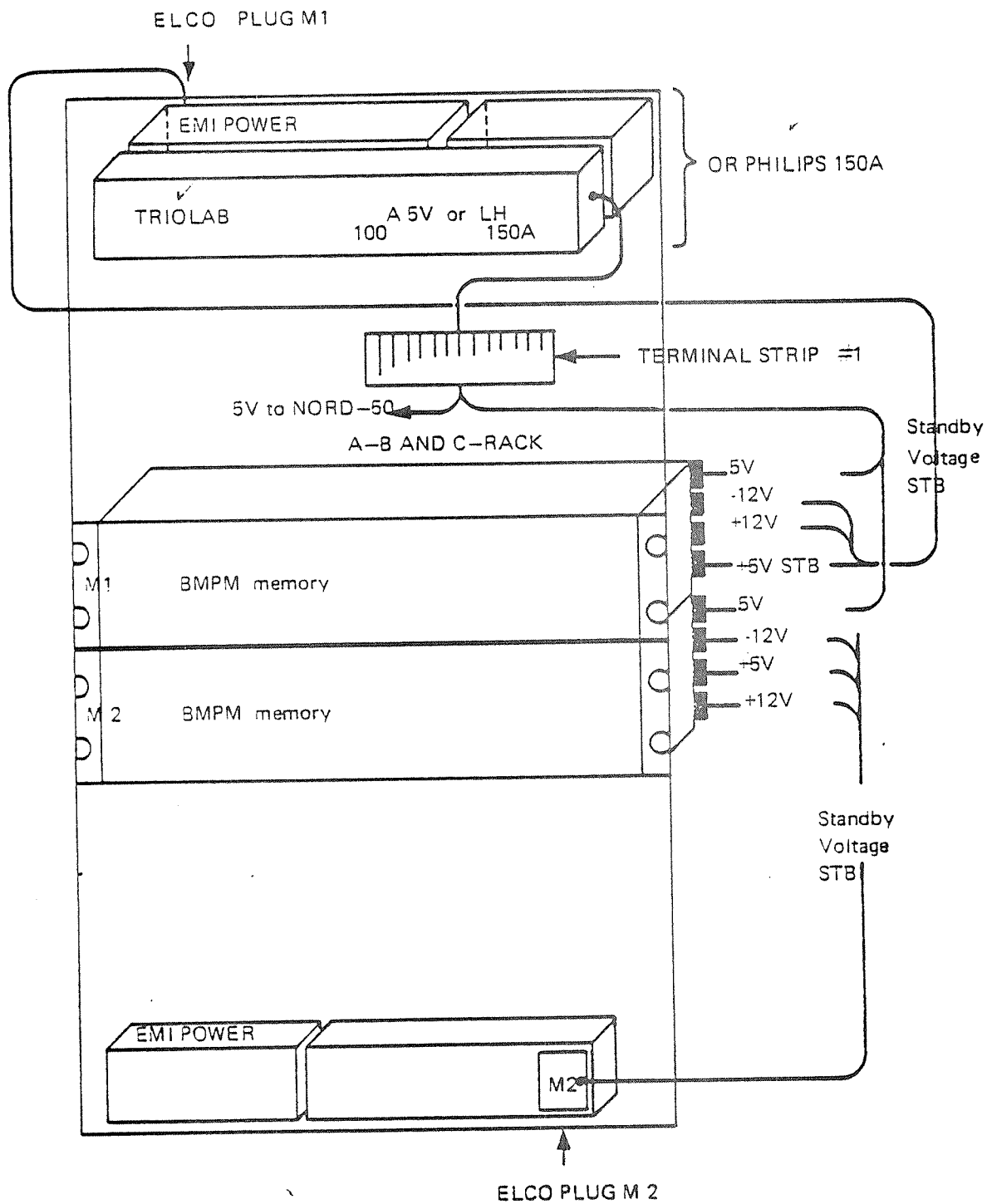
8.3.1.DC Power Distribution General

Standby voltage to the second multiport rack-M2 is supplied from a second multipower supply unit. This may be located in the Nord-50 or in the Nord-10/S cabinet.

In configurations with TRIOLAB 100A 5V power supply this supply is duplicated. One supply distributes 5V to the Nord-50 A and B-racks, while the other supplies the C-rack, and the multiport racks-M1 and M2.

8.3.2.DC Power Distribution in the Nord-50

Figure 37 illustrates the DC power distribution in the Nord-50.



(Nord-50, rear view.)

Fig. 37. DC power distribution in the NORD-50

8.4.DC Voltage Measurements

All DC voltages should be verified on a board extender module.

- Only 5 volts DC is connected to the Nord-50 racks.
- All modules in use in the Nord-50 should be inserted.
- The voltage should be checked in the middle of the rack.
- Check the multiport memory voltage in position 8. If Old multiport and if Big with the X-bank, use position 29 if Big multiport with only Y-bank.

Table 8.1 indicates the various voltages and voltage tolerances.

VOLTAGE	TERMINAL	GROUND TERM	TOLERANCE
+5V	0,1,98,99	2,3,96,97	4.95 - 5.05 VOLT
-5V	58,59	56,57	-4.9 - -5.1 VOLT
+12V * (Standby)	90,91,92,93	96,97	8k modules = 11.8 VOLT 32k modules = 12.0 VOLT
-12V * (Standby)	94,95	96,97	Not Critical
+5V * (Standby)	88,89	96,97	4.95-5.05 VOLT

* The STANDBY voltage is used by the MOS memory systems (local, multiport, and Big multiport) to "refresh" the memory.

Note. Should also be present during normal operation.
 Lasts for approximately 20 minutes after the
 AC input drops.

Table 8.1: Voltage Locations and Tolerances

APPENDICES

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Note. See Section 2.5 for a MNEMONIC List.
This list contains the Mnemonics and
their meanings associated with the
Nord-50 C-Rack.

Definitions

COMPUTER TERMS AS USED IN THIS MANUAL

ASC code: ASCII code

assembly test programs: Test programs in Nord-50 assembly language

Block: (As in B-Block.) A group of information units handled as a single group.

board: Circuit board.

board extender module: For extending modules

card: A module.

Central Processing Unit: (CPU) The part of the computer that controls the interpretation and execution of the processing instructions.

Console Terminal: Terminal connected to Nord-10/S

debugging: The removing of a mistake, malfunction, or a fault; for example, removing a mistake in a program, removing a malfunction in a computer, or removing a fault in a power line. disk: A revolving plate upon which data and programs are stored.

dynamic segment: Swapable segment

ELCO Plug: Plug connection in power supply

"European" version of Nord-50: All Nord-50 except F16 Nord-50's

fetch: Same as retrieve.

flip-flop: A circuit or device, usually containing active elements,
capable of assuming either one of two stable states.

"hard" error: Repeatable hardware error

high speed static memory: Memory made of flip-flops

latch: As in "to latch" or "the operands are latched in the
CPU . . .")

memory, private: A memory in which only one CPU has access.

memory, shared: A memory where both the Nord-10/S and, the DMA and the
Nord-50 have access.

Monitor, Nord-50: Program in Nord-10/S, supervising Nord-50

multiport memory: Memory system with 4 access ports

port: (As in PORT D ADDRESS) Communication modules between source and
memory modules

RT common area: Area in memory where RT-programs can exchange data

shared memory: See memory, shared.

SINTRAN III Operating System:

static segment: Segments permanent in memory during execution

TRIOLAB: Power supply name (type)

X-Bank: Part of multiport memory

Y-Bank: Part of multiport memory

Acronyms

A	A register.
AAX	AAX instruction. See Section 5.2.1.
AC	Alternating current.
ALU	Arithmetic Logic Unit
AR	Address Ready.
BD	Data Bus.
BMPM	(As in "BMPM memory".)
BP	A communication register. (As in <BP address>) (As in BP area.) BP = Lower. BP register.
BQ	A Communication register. (As in <BQ address>) (As in BQ area.) BQ = Upper. BQ register.
CA	Calculated memory address.
CPU	Central Processing Unit.
CR	Carriage Return.

DC	Direct Current.
DIV	Divide.
DMA	Direct Memory Access.
DR	Data Ready.
ECO	Engineering Change Order
EMI	(As in "EMI power".)
FDV	Floating Divide.
FDVD	Floating Divide Double Precision
FIO	Formatted Input/Output. A routine.
FMU	Floating Multiply.
FMUD	Floating Multiply Double Precision.
HAR	Hardware Test Programs
I/O	Input/Output.
IOX	Input/Output Execute.
IR _{least}	Least Significant Bit of Instruction Register.
LBP	Breakpoint Register.
LBO	Breakpoint Register.
LL	Lower Limit.

MA	Memory Address
MAC	Machine Assembly Code.
MD	Memory Data
MILL	(As in ARITHMETIC MILL.) Instruction Processing.
MPY	Multiply.
NC	Not Connected.
ND	Norsk Data, A.S
P	(As in RESULT P.) Result from A-rack.
PC	A communication register. (Program address ???)
PD	Program Description.
PISO	(As in PISO REG.) Parallel input, serial output
POS	Position
RAM	Random Access Memory.
RT	(As in "RT common area".) Real-time.
SA	A communication register. Start address.
SD	A communication register.
SINTRAN	Name of operating system.
STB	Standby. (As in "Standby Voltage STB".)
SUM	(As in "SUM-bus".) Result bus.

TA	A communication register. The last memory reference address. Last memory address.
TD	A communication register. The last data to or from memory.
UL	Upper Limit.
V	Volt.
VS	(As in SINTRAN III/VS.) Virtual Storage.

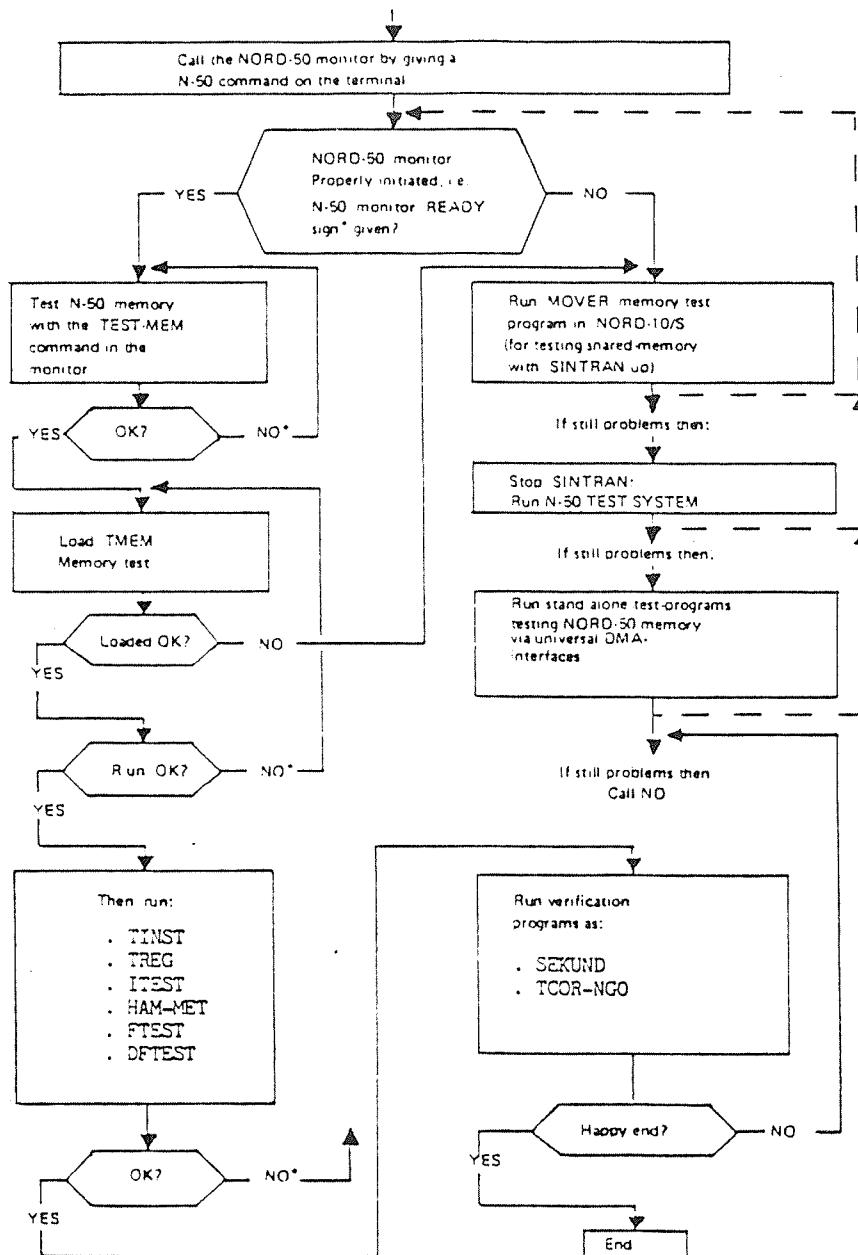
Abbreviations

%	"That means."
ADD/SUB	Add/Subtract
ADR	Address (Also ADDR.)
arith	arithmetic (Also ARITHM., ARIT)
AUX	auxiliary
BD	Bus Data
C	Centigrade
CA	Calculated Address
cm	centimeter
ext.	extension
FIXD	fixed
FLOD	floating
Hz	Hertz
instr.	instruction (also INSTR.)
Kg	Kilogram
Kw	Kilowatt

MA	Memory Address
MAX.	maximum
MD	Memory Data Bus
MUL/DIV	Multiply/Divide
Mw	(As in "MAX 2 Mw if ADDR. EXT.") Megaword
PC	Program Counter
PHYS	(As in PHYS REG N-50.) Physical
REF	Reference
REG	(Also reg.) Register.
SD	Simulated Data Register
SW	(As in SE10, SW9)
SWL	(As in SWL10, SWL9, . . . SWL2, SWL 1)
W	watt
W	(As in W15, W14, . . . W1, W0) LED Indicator
WL	(As in WL5, WL4, . . . WL1, WL0) Operator panel light number indicator

A P P E N D I X B

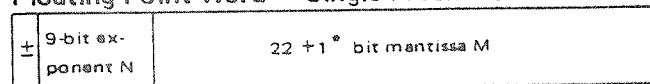
NORD-50 TEST SEQUENCE



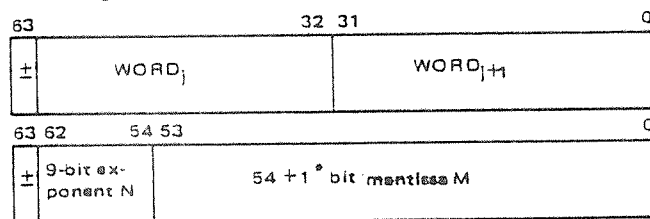
NO* = CALL NO or CHANGE FAILING MODULE IF NEW MODULE AVAILABLE
AND REPEAT THE TEST

A P P E N D I X C

DATA FORMAT SUMMARY

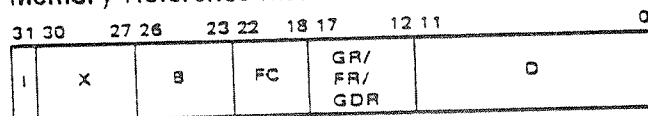
Integer WordRange: -2^{31} to $2^{31}-1$ **Floating Point Word — Single Precision**Range: 10^{-76} to $10^{76} = 7$ decimal digits.Bit 31 is sign of mantissa. Bias is 400_g.

- * The extra bit in the mantissa is the most significant bit and is set to one unless all bits in the exponent are zero. The bit is only used in the arithmetic and is removed in the result.

Floating Point Word — Double PrecisionRange: 10^{-76} to $10^{76} = 16.3$ decimal digits.Bit 63 is sign of mantissa. Bias is 400_g.

- * The extra bit in the mantissa is the most significant bit and is set to one unless all bits in the exponent are zero. The bit is only used in the arithmetic and is removed in the result.

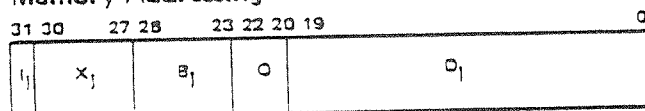
Memory Reference Instruction Word



where

- 1 — Indirect addressing flag
- X — Index register — 1 of 16
- B — Base register — 1 of 16
- FC — Function code — 1 of 32 instructions
- GR — General register number
- FR — Single precision, floating register number
- FDR — Double precision, floating register number
- D — Displacement $0 \leq D < 4096$

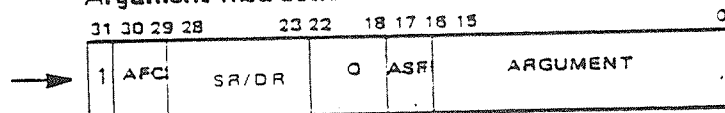
Memory Addressing



Indirect address word — IAW_j at level j .

- 1_j — Indirect addressing flag at level j
- X_j — Index register for IAW_j
- B_j — Base register for IAW_j
- D_j — Displacement for IAW_j $0 \leq D < 1048576$

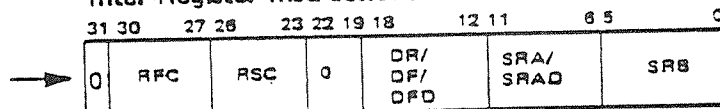
Argument Instructions



where

- AFC/ — Argument function and subfunction code —
- ASF — direct logical/arithmetical operations, direct test and direct skip
- SR/DR — Source register/Destination register

Inter-Register Instructions



where

- RFC/ — Inter-register instruction and subfunction code
- RSC — shift, arithmetic, test and skip, logical operations, miscellaneous operations
- DR — Destination register
- DF — Destination floating register
- DFD — Destination double precision floating register
- SRA — Source register A
- SRAD — Double precision source register A
- SRB — Source register B

3130	2726	2322	1817	12,11	6,5	0	
0	0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 0	MONITOR CODE			STOP (monitor call)
0	0 0 0 0 1	0 0 0 0 W	0 0 0 0 0 0	DR	SRA	EXT. REG. NO.	RIO
0	0 0 1 0 0	L R SM	0 0 0 0 0 0	DR	SRA	SHIFT COUNT	SHR
0	0 0 1 1 1	L R SM	0 0 0 0 0 0	DFD	SRAD	SHIFT COUNT	SHD
0	0 1 0 0 0	1 1 0 C	0 0 0 0 0 0	DR	SRA	BITNO	BST, BCM
0	0 1 0 1 1	1 1 0 0	0 0 0 0 0 0	DR	SRA	BITNO	BCL
0	0 1 1 0 0	1 1 0 0	0 0 0 0 0 0	DR	SRA	BITNO	BSZ
0	0 1 1 1 1	1 1 0 0	0 0 0 0 0 0	DR	SRA	BITNO	BSO
0	1 0 0 0 0	R 0 0 0 0	0 0 0 0 0 0	DR	SRA/SRAD	0 0 0 0 0 0	FIX, RIR FIXD, FIRD
0	1 0 0 1 0	0 0 1 0	0 0 0 0 0 0	DF/DFD	SRA	0 0 0 0 0 0	FLO, FLOD
0	1 0 1 0 0		LO 0 0 0 0 0 0	DR	SRA	SRB	LRO
0	1 0 1 1 0		0 0 0 0 0 0				Not used
0	1 1 0 0 0		AF 0 0 0 0 0 0	DR	SRA	SRB	IRO
0	1 1 0 1 0 0	AF	0 0 0 0 0 0	DF/DFD	SRA/SRAD	SRB/SRBD	FRO
0	1 1 1 0 0	RL AF	0 0 0 0 0 0	DR	SRA	SRB	IRS
0	1 1 1 1 0	RL AF	0 0 0 0 0 0	DF/DFD	SRA/SRAD	SRB/SRBD	FRS
I	X	B	0 0 0 0 0 1	R		D	RTJ
I	X	B	0 0 0 1 0	R		D	EXC
I	X	B	0 0 0 1 1	R		D	MIN
I	X	B	0 0 1 0 0	R		D	CRG
I	X	B	0 0 1 0 1	R		D	CRL
I	X	B	0 0 1 1 0	R		D	CRE
I	X	B	0 0 1 1 1	R		D	CRD
I	X	B	0 1 0 0 0	R		D	JRP
I	X	B	0 1 0 0 1	R		D	JRN
I	X	B	0 1 0 1 0	R		D	JRZ
I	X	B	0 1 0 1 1	R		D	JRF

Appendix C
DATA FORMAT SUMMARY

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	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1		X				B				0	1	1	0	0		R																	JPM
I		X				B				0	1	1	0	1		R																	JNM
I		X				B				0	1	1	1	0		R																	JZM
I		X				B				0	1	1	1	1		R																	JFM
I		X				B				1	0	0	0	0		R																	ADD
I		X				B				1	0	0	0	1		R																	SUB
I		X				B				1	0	0	1	0		R																	AND
I		X				B				1	0	0	1	1		R																	LDR
I		X				B				1	0	1	0	0		R																	ADM
I		X				B				1	0	1	0	1		R																	Not used
I		X				B				1	0	1	1	0		R																	XMR
I		X				B				1	0	1	1	1		R																	STR
I		X				B				1	1	0	0	0		R																	MPY
I		X				B				1	1	0	0	1		R																	DIV
I		X				B				1	1	0	1	0		FD																	LDD
I		X				B				1	1	0	1	1		FD																	STD
I		X				B				1	1	1	0	0		F/FD																	FAD/FADD
I		X				B				1	1	1	0	1		F/FD																	FSE/FSBD
I		X				B				1	1	1	1	0		F/FD																	FMU/FMUD
I		X				B				1	1	1	1	1		F/FD																	FDV/FDVD
I _i		X _j				B _j				0	0	0																					Ind. addr. word
I		0	0			DR				0	0	0	0	0		LF																	DLR
1		0	1			DR				0	0	0	0	0		AF																	DAR
1		1	CM			DR				0	0	0	0	0		RL																	DSK

A P P E N D I X D

NORD-50 STATUS REGISTER FORMAT

Status Register Bit Number	Meaning	
0	Program STOP	
1	Address Violation	
2	Instruction hang-up	

3	Overflow	
4	Underflow	
5	Memory Request	Only valid when running in simulated memory mode (used by the TEST SYSTEM).

6	Memory WRITE/READ	
7	Parity Error	
8	Memory hang-up	

A P P E N D I X E

NORD - 50 INSTRUCTIONS

The NORD-50 Assembler is documented in a separate manual (ND-60.075.01).
The NORD-50 Reference Manual (ND-05.003.01) may also be helpful when
writing assembly programs.

The same format is used in the assembler in the Nord-50-MONITOR.

A summary of all instructions, with the relevant operands for each of them
follows.

Summary of Instructions

Memory Reference Instructions:

Mnemonic:		Action:
RTJ	R, D, B, X, I	Return jump
EXC	R, D, B, X, I	Remote execute
MIN	R, D, B, X, I	Memory increment
CRG	R, D, B, X, I	Skip if (R) \geq (Ea)
CRL	R, D, B, X, I	Skip if (R) $<$ (Ea)
CRE	R, D, B, X, I	Skip if (R) = (Ea)
CRO	R, D, B, X, I	Skip if (R) \neq (Ea)
JRP	R, D, B, X, I	Jump if (R) \geq 0
JRN	R, D, B, X, I	Jump if (R) $<$ 0
JRZ	R, D, B, X, I	Jump if (R) = 0
JRF	R, D, B, X, I	Jump if (R) \neq 0
JPM	R, D, B, X, I	Modify (R) and jump if (R) \geq 0
JNM	R, D, B, X, I	Modify (R) and jump if (R) $<$ 0
JZM	R, D, B, X, I	Modify (R) and jump if (R) = 0
JFM	R, D, B, X, I	Modify (R) and jump if (R) \neq 0
ADD	R, D, B, X, I	Add (Ea) to (R)
SUB	R, D, B, X, I	Subtract (Ea) from (R)
AND	R, D, B, X, I	Logical AND between (Ea) and (R)
LDR	R, D, B, X, I	Load (R) with (Ea)
ADM	R, D, B, X, I	Add (R) to (Ea)
XMR	R, D, B, X, I	Exchange (Ea) and (R)
STR	R, D, B, X, I	Store (R) in (Ea)
MPY	R, D, B, X, I	Multiply (R) by (Ea)
DIV	R, D, B, X, I	Divide (R) by (Ea)
LDD	R, D, B, X, I	Load (FD) with (Ea, Ea + 1)
FTD	R, D, B, X, I	Store (FD) in (Ea, Ea + 1)
FAD	R, D, B, X, I	Add (Ea) to (F)
FADD	R, D, B, X, I	Add (Ea, Ea + 1) to (FD)
FSB	R, D, B, X, I	Subtract (Ea) from (F)
FSBD	R, D, B, X, I	Subtract (Ea, Ea + 1) from (FD)
FMU	R, D, B, X, I	Multiply (F) by (Ea)
FMUD	R, D, B, X, I	Multiply (FD) by (Ea, Ea + 1)
FDV	R, D, B, X, I	Divide (F) by (Ea)
FDVD	R, D, B, X, I	Divide (FD) by (Ea, Ea + 1)

R = register
D = displacement
B = base register
X = index register
I = indirect addressing

Memory Reference Instructions Format:

	INSTR	REG NR	DISPLACEMENT	B	X	I
ASSEMBLER:	0-63 ₁₀	0-4 K	0-15	0-15	0 or 1	
MONITOR :	0-77 ₈	0-4 K	0-17	0-17	0 or 1	

NORD-50 address calculation:

$$Ca = (X) + (B) + D$$

Calculated address	=	Content of reg. 0-15 X-field	+	Content of reg. 0-15 B-field	+	Displacement
--------------------	---	------------------------------	---	------------------------------	---	--------------

Inter Register Operations

Shift Instructions:

Mnemonic:		Action:
SLR	DR, SR, SC	Left rotational shift
SRR	DR, SR, SC	Right rotational shift
SLA	DR, SR, SC	Left arithmetical shift
SRA	DR, SR, SC	Right arithmetical shift
SLL	DR, SR, SC	Left logical shift
SRL	DR, SR, SC	Right logical shift
SLRD	DR, SR, SC	Left rotational double register shift
SRRD	DR, SR, SC	Right rotational double register shift
SLAD	DR, SR, SC	Left arithmetical double register shift
SRAD	DR, SR, SC	Right arithmetical double register shift
SLLD	DR, SR, SC	Left logical double register shift
SRLD	DR, SR, SC	Right logical double register shift

DR = destination register

SR = source register

SC = shift count

0 ≤ SC ≤ 31 for single register operations

0 ≤ SC ≤ 63 for double register operations

Miscellaneous Operations:

Mnemonic:		Action:
BST	DR, SR, BN	Bit set
BCM	DR, SR, BN	Bit complement
BCL	DR, SR, BN	Bit clear
BSZ	DR, SR, BN	Bit skip on zero
BSO	DR, SR, BN	Bit skip in one
FIX	DR, SR	Convert floating to integer
FIR	DR, SR	Convert floating to rounded integer
FIXD	DR, SR	Convert double precision floating to integer
FIRD	DR, SR	Convert double precision floating to rounded integer
FLO	DR, SR	Convert integer to floating
FLOD	DR, SR	Convert integer to double precision floating
RIN	DR,, ER	Register input
ROUT	,SR, ER	Register output

BN = bit number
 $0 \leq BN \leq 31$
 ER = external register
 2 — OR (overflow register)
 3 — RR (remainder register)

Arithmetic Operations:

Mnemonic:		Action:
RAD	DR, SRA, SRB	Register add
RSB	DR, SRA, SRB	Register subtract
RMU	DR, SRA, SRB	Register multiply
RDV	DR, SRA, SRB	Register divide
RAF	DR, SRA, SRB	Floating register add
RSF	DR, SRA, SRB	Floating register subtract
RMF	DR, SRA, SRB	Floating register multiply
RDF	DR, SRA, SRB	Floating register divide
RAFD	DR, SRA, SRB	Double precision floating register add
RSFD	DR, SRA, SRB	Double precision floating register subtract
RMFD	DR, SRA, SRB	Double precision floating register multiply
RDFD	DR, SRA, SRB	Double precision floating register divide
RAS	DR, SRA, SRB	Register add set carry
RAA	DR, SRA, SRB	Register add add carry
RASA	DR, SRA, SRB	Register add add and set carry
RSS	DR, SRA, SRB	Register subtract set carry
RSA	DR, SRA, SRB	Register subtract add carry
RSSA	DR, SRA, SRB	Register subtract add and set carry

SRA = source register A
 SRB = source register B

Test and Skip:

Mnemonic:		Action:
SGR	DR, SRA, SRB	Subtract registers and skip if result ≥ 0
ASG	DR, SRA, SRB	Add registers and skip if result ≥ 0
SLE	DR, SRA, SRB	Subtract registers and skip if result < 0
ASL	DR, SRA, SRB	Add registers and skip if result < 0
SEQ	DR, SRA, SRB	Subtract registers and skip if result $= 0$
ASE	DR, SRA, SRB	Add registers and skip if result $= 0$
SUE	DR, SRA, SRB	Subtract registers and skip if result $\neq 0$
ASU	DR, SRA, SRB	Add registers and skip if result $\neq 0$
SGF	DR, SRA, SRB	Subtract floating registers and skip if result ≥ 0
ASGF	DR, SRA, SRB	Add floating registers and skip if result ≥ 0
SLF	DR, SRA, SRB	Subtract floating registers and skip if result < 0
ASLF	DR, SRA, SRB	Add floating registers and skip if result < 0
SEF	DR, SRA, SRB	Subtract floating registers and skip if result $= 0$
ASEF	DR, SRA, SRB	Add floating registers and skip if result $\neq 0$
SUF	DR, SRA, SRB	Subtract floating registers and skip if result $\neq 0$
ASUF	DR, SRA, SRB	Add floating registers and skip if result $\neq 0$
SGD	DR, SRA, SRB	Subtract double precision and skip if result ≥ 0
AGFD	DR, SRA, SRB	Add double precision and skip if result ≥ 0
SLD	DR, SRA, SRB	Subtract double precision and skip if result < 0
ALFD	DR, SRA, SRB	Add double precision and skip if result < 0
SED	DR, SRA, SRB	Subtract double precision and skip if result $= 0$
AEFD	DR, SRA, SRB	Add double precision and skip if result $= 0$
SUD	DR, SRA, SRB	Subtract double precision and skip if result $\neq 0$
AUFD	DR, SRA, SRB	Add double precision and skip if result $\neq 0$

Logical Operations:

Mnemonic:		Action:
RND	DR, SRA, SRB	Register AND
RNDA	DR, SRA, SRB	Register AND, use complement of (SRA)
RNDB	DR, SRA, SRB	Register AND, use complement of (SRB)
RXO	DR, SRA, SRB	Register exclusive OR
RXOA	DR, SRA, SRB	Register exclusive OR, use complement of (SRA)
RXOB	DR, SRA, SRB	Register exclusive OR, use complement of (SRB)
ROR	DR, SRA, SRB	Register OR
RORA	DR, SRA, SRB	Register OR, use complement of (SRA)
RORB	DR, SRA, SRB	Register OR, use complement of (SRB)
SZR	DR, SRA, SRB	Set all zeros
RNAB	DR, SRA, SRB	Register AND, use complement of SRA and SRB
ROAB	DR, SRA, SRB	Register OR, use complement of SRA and SRB
RXAB	DR, SRA, SRB	Register exclusive OR, use complement of SRA and SRB

Argument Instructions:

Mnemonic:		Action:
XORA	DR, ARG	Exclusive OR
ANDA	DR, ARG	AND
ORA	DR, ARG	OR
SETA	DR, ARG	Set register
SECA	DR, ARG	Set register to complement
ADDA	DR, ARG	Add
ADCA	DR, ARG	Add complement
DDP	DR, ARG	Skip if (DR) \geq ARG
DDN	DR, ARG	Skip if (DR) $<$ ARG
DDZ	DR, ARG	Skip if (DR) = ARG
DDF	DR, ARG	Skip if (DR) \neq ARG
DSP	DR, ARG	Skip if (DR) \geq -ARG
DSN	DR, ARG	Skip if (DR) $<$ -ARG
DSZ	DR, ARG	Skip if (DR) = -ARG
DSF	DR, ARG	Skip if (DR) \neq -ARG

ARG = argument

A P P E N D I X F

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

(TINST HAR 1840)

ND-30.010.02

Appendix F
ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

161

00004 000010000000 0 00 00 01 00	0066	RTJ	0,++2	
00005 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	JRZ JUMP ACC>0
00006 00001000000 0 00 00 01 00	0070	JRF	ACC,++2	
00007 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	JRF NO JUMP ACC>0
00008 00001000000 0 00 00 01 00	0072	JRN	ACC,++2	
00009 00001000000 0 00 00 01 00	0073	RTJ	0,++2	
00010 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	JRN JUMP ACC>0
00011 00001000000 0 00 00 01 00	0001	CRE	ACC,POS	CRE NO SKIP ACC==(EA)
00012 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00013 00001000000 0 00 00 01 00	0001	CRG	ACC,POS	CRG NO SKIP ACC=(EA)
00014 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00015 00001000000 0 00 00 01 00	0005	CRL	ACC,ONE	
00016 00001040014 0 00 00 01 04	0102	RTJ	0,++2	
00017 00001000000 0 00 00 01 00	0014	RTJ	LINK,ERROR	CRL SKIP ACC>(EA)
00018 00001040014 0 00 00 01 04	0002	LDR	ACC,NEG	
00019 00001000000 0 00 00 01 00	0105	JRN	ACC,++2	JRN NO JUMP ACC<0
00020 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	JRF NO JUMP ACC<0
00021 00001000000 0 00 00 01 00	0111	JRP	ACC,++2	
00022 00001040014 0 00 00 01 04	0112	RTJ	0,++2	JRP JUMP ACC<0
00023 00001000000 0 00 00 01 00	0014	RTJ	LINK,ERROR	
00024 00001040014 0 00 00 01 04	0115	RTJ	0,++2	JRZ JUMP ACC<0
00025 00001000000 0 00 00 01 00	0014	RTJ	LINK,ERROR	
00026 00001040014 0 00 00 01 04	0004	CRL	ACC,ONES	CRL NO SKIP ACC<(EA)
00027 00001000000 0 00 00 01 00	0014	RTJ	LINK,ERROR	
00028 00001040014 0 00 00 01 04	0002	CRD	ACC,NEG	CRD SKIP ACC=(EA)
00029 00001000000 0 00 00 01 00	0122	RTJ	0,++2	
00030 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	CRG SKIP ACC<(EA)
00031 00001000000 0 00 00 01 00	0125	CRG	ACC,ONE	
00032 00001040014 0 00 00 01 04	0014	RTJ	0,++2	
00033 00001000000 0 00 00 01 00	0004	LDR	ACC,ONES	
00034 00001040014 0 00 00 01 04	0006	STR	ACC,STORE	STR ERROR
00035 00001000000 0 00 00 01 00	0006	CRE	ACC,STORE	
00036 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	STR ERROR
00037 00001000000 0 00 00 01 00	0001	LDR	ACC,POS	
00038 00001040014 0 00 00 01 04	0006	STR	ACC,STORE	STR ERROR
00039 00001000000 0 00 00 01 00	0006	CRE	ACC,STORE	
00040 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	STR ERROR
00041 00001000000 0 00 00 01 00	0003	LDR	ACC,ZRO	
00042 00001040014 0 00 00 01 04	0006	STR	ACC,STORE	
00043 00001000000 0 00 00 01 00	0006	CRE	ACC,STORE	
00044 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	STR ERROR
00045 00001000000 0 00 00 01 00	0005	LDR	ACC,ONE	
00046 00001040014 0 00 00 01 04	0004	ADD	ACC,ONES	ADD ERROR 1+(-1)
00047 00001000000 0 00 00 01 00	0151	JRZ	ACC,++2	
00048 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00049 00001000000 0 00 00 01 00	0001	LDR	ACC,POS	SUB ERROR POS=POS
00050 00001040014 0 00 00 01 04	0001	SUB	ACC,POS	
00051 00001000000 0 00 00 01 00	0155	JRZ	ACC,++2	
00052 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00053 00001000000 0 00 00 01 00	0001	LDR	ACC,POS	
00054 00001040014 0 00 00 01 04	0001	AND	ACC,POS	AND ERROR POS AND POS
00055 00001000000 0 00 00 01 00	0001	CRE	ACC,POS	
00056 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00057 00001000000 0 00 00 01 00	0002	LDR	ACC,NEG	
00058 00001040014 0 00 00 01 04	0001	AND	ACC,POS	AND ERROR POS AND NEG
00059 00001000000 0 00 00 01 00	0165	JRZ	ACC,++2	
00060 00001040014 0 00 00 01 04	0014	RTJ	LINK,ERROR	
00061 00001000000 0 00 00 01 00	0005	LDR	ACC,ONE	
00062 00001040014 0 00 00 01 04	0003	LDR	WORK,ZRO	
00063 00001000000 0 00 00 01 00	0004	ADM	ACC,ONES	

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

00170	00006320304	0	00	00	06	32	0024	CRE	WORK,ONES	
00171	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	AOM ERROR 1*(-1)
00172	00023011027	0	00	00	23	01	1027	LDR	ACC,=-1	
00173	00027010004	0	00	00	27	01	0004	STR	ACC,ONES	
00174	00023010003	0	00	00	23	01	0003	LDR	ACC,ZRO	
00175	00027010007	0	00	00	27	01	0007	STR	ACC,INCR	
00176	00023011030	0	00	00	23	01	1030	LDR	ACC,=-1	
00177	00023021031	0	00	00	23	02	1031	LDR	WORK,=-1	
00200	00026010007	0	00	00	26	01	0007	XMR	ACC,INCR	
00201	00012010203	0	00	00	12	01	0203	JNZ	ACC,=-2	
00202	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	IXMR ERROR REG FAILED
00203	00006020007	0	00	00	06	02	0007	CRE	WORK,INCR	
00204	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	XMR ERROR (EA) FAILED
00205	00023011032	0	00	00	23	01	1032	LDR	ACC,=-4	
00206	00027010007	0	00	00	27	01	0007	STR	ACC,INCR	
00207	00023010005	0	00	00	23	01	0005	LDR	ACC,ONE	
00210	00003010007	0	00	00	03	01	0007	MIN	ACC,INCR	
00211	000010000213	0	00	00	01	00	0213	RTJ	0,=-2	
00212	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	MIN SKIPPED (EA)=-2
00213	00003010007	0	00	00	03	01	0007	MIN	ACC,INCR	
00214	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	MIN NO SKIP (EA)=0
00215	00002000010	0	00	00	02	00	0010	EXEC	EXC	
00216	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00217	00023010011	0	00	00	23	01	0011	LDR	ACC,CORTJ	
00220	00042010222	0	00	01	02	01	0222	EXC	1,=-2,ACC	
00221	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00222	00023010004	0	00	00	23	21	0004	LDR	ACC+120,ONES	
00223	00023010005	0	00	00	23	01	0005	LDR	ACC,ONE	
00224	00015010225	0	00	00	15	01	0225	JNM	ACC,=-2	
00225	000010000227	0	00	00	01	00	0227	RTJ	0,=-2	JNM JUMP ACC=0
00226	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00227	00015010231	0	00	00	15	01	0231	JNM	ACC,=-2	JNM NO JUMP ACC<0
00228	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00231	00015010233	0	00	00	15	01	0233	JZM	ACC,=-2	
00232	000010000234	0	00	00	01	00	0234	RTJ	0,=-2	JZM JUMP ACC<0
00233	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00234	00023010005	0	00	00	23	01	0005	ADD	ACC,ONE	
00235	00023010005	0	00	00	23	21	0005	LDR	ACC+120,ONE	
00236	00015010240	0	00	00	15	01	0240	JZM	ACC,=-2	JZM NO JUMP ACC=0
00237	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00240	00015010242	0	00	00	15	01	0242	JZM	ACC,=-2	
00241	000010000243	0	00	00	01	00	0243	RTJ	0,=-2	JZM JUMP ACC>0
00242	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00243	00015010245	0	00	00	15	01	0245	JNM	ACC,=-2	
00244	000010000246	0	00	00	01	00	0246	RTJ	0,=-2	JNM JUMP ACC>0
00245	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00246	00014010250	0	00	00	14	01	0250	JPM	ACC,=-2	JPM NO JUMP ACC>0
00247	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00250	00021011033	0	00	00	21	01	1033	SUB	ACC,=2	
00251	00023010004	0	00	00	23	21	0004	LDR	ACC+120,ONES	
00252	00014010254	0	00	00	14	01	0254	JPM	ACC,=-2	JPM NO JUMP ACC=0
00253	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00254	00014010256	0	00	00	14	01	0256	JPM	ACC,=-2	
00255	000010000257	0	00	00	01	00	0257	RTJ	0,=-2	JPM JUMP ACC<0
00256	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00257	00017010261	0	00	00	17	01	0261	JFM	ACC,=-2	JFM NO JUMP ACC<0
00258	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00261	00028010005	0	00	00	20	01	0005	ADD	ACC,ONE	
00262	00023010005	0	00	00	23	21	0005	LDR	ACC+120,ONE	
00263	00017010265	0	00	00	17	01	0265	JFM	ACC,=-2	
00264	000010000266	0	00	00	01	00	0266	RTJ	0,=-2	JFM JUMP ACC=0
00265	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00266	00017010270	0	00	00	17	01	0270	JFM	ACC,=-2	JFM NO JUMP ACC>0
00267	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	
00270	00023010001	0	00	00	23	01	0001	LDR	ACC,POS	
00271	14000010001	0	14	00	00	01	0001	RAD	ACC,0,ACC	

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00272	00000010001	0	00	00	06	01	0001	CRE	ACC,POS	
00273	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	RAD ERROR POS+0<>POS
00274	00023010000	0	00	00	23	01	0002	LDR	ACC,NEG	
00275	10040010101	0	14	01	00	01	01 01	RSB	ACC,ACC,ACC	
00276	00012000000	0	00	00	12	00	0300	JRZ	0,++2	
00277	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	RSB ERROR NEG-NEG<>0
00300	00023010001	0	00	00	23	01	0001	LDR	ACC,POS	
00301	10040000010	0	16	01	00	00	01 01	SGR	0,ACC,ACC	
00302	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SGR NO SKIP RESULT=0
00303	00023020004	0	00	00	23	02	0004	LDR	WORK,ONES	
00304	10040000000	0	16	01	00	00	00 02	SGR	0,0,WORK	
00305	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SGR NO SKIP RESULT>0
00306	10040000000	0	16	01	00	00	00 01	SGR	0,0,ACC	
00307	00001000311	0	00	00	01	00	0311	RTJ	0,++2	
00310	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SGR SKIP RESULT<0
00311	10000000010	0	16	00	00	00	01 02	ASG	0,ACC,WORK	
00312	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASG NO SKIP RESULT>0
00313	00023010005	0	00	00	23	01	0005	LDR	ACC,ONE	
00314	10000000010	0	16	00	00	00	01 02	ASG	0,ACC,WORK	
00315	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASG NO SKIP RESULT=0
00316	10000000020	0	16	00	00	00	02 00	ASG	0,WORK,0	
00317	00001000321	0	00	00	01	00	0321	RTJ	0,++2	
00320	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASG SKIP RESULT<0
00321	10240000000	0	16	05	00	00	00 02	SLE	0,0,WORK	
00322	00001000324	0	00	00	01	00	0324	RTJ	0,++2	
00323	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SLE SKIP RESULT>0
00324	10240000020	0	16	05	00	00	02 00	SLE	0,WORK,0	
00325	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SLE NO SKIP RESULT<0
00326	10240000010	0	16	05	00	00	01 01	SLE	0,ACC,ACC	
00327	00001000331	0	00	00	01	00	0331	RTJ	0,++2	
00330	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SLE SKIP RESULT=0
00331	10200000010	0	16	04	00	00	01 02	ASL	0,ACC,WORK	
00332	00001000334	0	00	00	01	00	0334	RTJ	0,++2	
00333	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASL SKIP RESULT=0
00334	10200000000	0	16	04	00	00	00 01	ASL	0,0,ACC	
00335	00001000337	0	00	00	01	00	0337	RTJ	0,++2	
00336	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASL SKIP RESULT>0
00337	10200000020	0	16	04	00	00	02 00	ASL	0,WORK,0	
00340	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASL NO SKIP RESULT<0
00341	00023010002	0	00	00	23	01	0002	LDR	ACC,NEG	
00342	10440000010	0	16	11	00	00	01 01	SEQ	0,ACC,ACC	
00343	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SEQ NO SKIP RESULT=0
00344	10440000000	0	16	11	00	00	00 01	SEQ	0,0,ACC	
00345	00001000347	0	00	00	01	00	0347	RTJ	0,++2	
00346	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SEQ SKIP RESULT>0
00347	10440000010	0	16	11	00	00	01 00	SEQ	0,ACC,0	
00350	00001000352	0	00	00	01	00	0352	RTJ	0,++2	
00351	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SEQ SKIP RESULT<0
00352	00023010001	0	00	00	23	01	0001	LDR	ACC,POS	
00353	00023020000	0	00	00	23	02	0000	LDR	WORK,MIP0S	
00354	10400000010	0	16	10	00	00	01 02	ASE	0,ACC,WORK	
00355	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASE NO SKIP RESULT=0
00356	10400000010	0	16	10	00	00	01 00	ASE	0,ACC,0	
00357	00001000361	0	00	00	01	00	0361	RTJ	0,++2	
00360	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASE SKIP RESULT>0
00361	10400000020	0	16	10	00	00	02 00	ASE	0,WORK,0	
00362	00001000364	0	00	00	01	00	0364	RTJ	0,++2	
00363	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASE SKIP RESULT<0
00364	10640000020	0	16	15	00	00	02 02	SUE	0,WORK,WORK	
00365	00001000367	0	00	00	01	00	0367	RTJ	0,++2	
00366	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SUE SKIP RESULT=0
00367	10640000020	0	16	15	00	00	02 00	SUE	0,WORK,0	
00370	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SUE NO SKIP RESULT<0
00371	10640000010	0	16	15	00	00	01 00	SUE	0,ACC,0	
00372	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	SUE NO SKIP RESULT>0
00373	10600000010	0	16	14	00	00	01 02	ASU	0,ACC,WORK	
00374	00001000376	0	00	00	01	00	0376	RTJ	0,++2	
00375	00001040014	0	00	00	01	04	0014	RTJ	LINK,ERROR	ASU SKIP RESULT=0

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

00376	10600000100	2	16	14	03	00	31	00	ASU	0,ACC,0	
00377	0001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00400	15600300200	0	16	14	00	00	02	00	ASU	0,WORK,0	
00401	00001340014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ASU NO SKIP RESULT<0
00402	00023010001	0	00	00	23	01	0001		LDR	ACC,POS	
00403	00023020002	0	00	00	23	02	0002		LDR	WORK,NEG	
00404	12040030102	0	12	01	00	03	01	02	RND	RES,ACC,WORK	
00405	00006030003	0	00	00	06	03	0003		CRE	RES,ZRO	
00406	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RND ERROR POS AND NEG<>0
00407	12440030102	0	12	11	00	03	01	02	RNOA	RES,ACC,WORK	
00408	00006030002	0	00	00	06	03	0002		CRE	RES,NEG	
00409	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOA ERROR NEG AND POS!<>NEG
00410	12240030102	0	12	05	00	03	21	02	RNOB	RES,ACC,WORK	
00411	00006030003	0	00	00	06	03	0001		CRE	RES,POS	
00412	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOB ERROR POS AND NEG!<>POS
00413	12100030102	0	12	02	00	03	01	02	RNOB	RES,ACC,WORK	
00414	00006030004	0	00	00	06	03	0004		CRE	RES,ONES	
00415	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOB ERROR POS EXOR NEG<>ONES
00416	12100030101	0	12	02	00	03	21	01	RNOB	RES,ACC,ACC	
00417	00006030003	0	00	00	06	03	0003		CRE	RES,ZRO	
00418	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOB ERROR POS EXOR POS<>ZRO
00419	12500030202	0	12	12	00	03	02	02	RNOA	RES,ACC,WORK	
00420	00006030004	0	00	00	06	03	0004		CRE	RES,ONES	
00421	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOA ERROR NEG! EXOR NEG<>ONES
00422	12300030102	0	12	06	00	03	21	02	RNOB	RES,ACC,WORK	
00423	00006030003	0	00	00	06	03	0003		CRE	RES,ZRO	
00424	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RNOB ERROR POS EXOR NEG!<>ZRO
00425	12140030102	0	12	03	00	03	01	02	ROR	RES,ACC,WORK	
00426	00006030004	0	00	00	06	03	0004		CRE	RES,ONES	
00427	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ROR ERROR POS OR NEG <>ONES
00428	12140030202	0	12	03	00	03	02	02	ROR	RES,ACC,WORK	
00429	00006030002	0	00	00	06	03	0002		CRE	RES,NEG	
00430	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ROR ERROR NEG OR NEG <>NEG
00431	12540030201	0	12	13	00	03	02	01	RORA	RES,WORK,ACC	
00432	00006030001	0	00	00	06	03	0001		CRE	RES,POS	
00433	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RORA ERROR NEG! OR POS<>POS
00434	12340030201	0	12	07	00	03	02	01	RORB	RES,WORK,ACC	
00435	00006030002	0	00	00	06	03	0002		CRE	RES,NEG	
00436	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	RORB ERROR NEG OR POS!<>NEG
00437	12340030201	0	12	07	00	03	02	01	RORB	RES,WORK,ACC	
00438	00006030001	0	00	00	06	03	0001		CRE	RES,POS	
00439	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00440	12340030201	0	12	07	00	03	02	01	RORB	RES,WORK,ACC	
00441	00006030002	0	00	00	06	03	0002		CRE	RES,NEG	
00442	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00443	12300030102	0	12	06	00	03	00	00	SZR	ACC	
00444	00006030003	0	00	00	06	03	0003		CRE	ACC,ZRO	
00445	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SZR ERROR
00446	12000030000	0	12	00	00	01	00	00	LDR	ACC,POS	
00447	00006030004	0	00	00	06	03	0004		CRE	ACC,0	
00448	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	XORA ERROR POS EXOR 0<>POS
00449	12000030000	0	12	00	00	01	00	00	XORA	ACC,0	
00450	00006030001	0	00	00	06	03	0001		CRE	ACC,POS	
00451	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00452	12000030000	0	12	00	00	01	00	00	LDR	ACC,NEG	
00453	00006030002	0	00	00	06	03	0002		CRE	ACC,1125252	
00454	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ANOA ERROR NEG AND 1125252
00455	12000030000	0	12	00	00	01	00	00	ANOA	ACC,1125252	
00456	00006030001	0	00	00	06	03	0001		CRE	ACC,1125252	
00457	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00458	12000030000	0	12	00	00	01	00	00	LDR	ACC,POS	
00459	00006030002	0	00	00	06	03	0002		CRE	ACC,POS	
00460	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ORA ERROR POS ORA 152525<>POS
00461	12000030000	0	12	00	00	01	00	00	ORA	ACC,152525	
00462	00006030001	0	00	00	06	03	0001		CRE	ACC,POS	
00463	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00464	12000030000	0	12	00	00	01	00	00	SECA	ACC,1	
00465	00006030002	0	00	00	06	03	0002		CRE	ACC,ZRO	
00466	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SECA ERROR ACC<>0
00467	12000030000	0	12	00	00	01	00	00	SECA	ACC,1	
00468	00006030001	0	00	00	06	03	0001		CRE	ACC,ONES	
00469	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SECA ERROR ACC<>=1
00470	12000030000	0	12	00	00	01	00	00	ADDA	ACC,2	
00471	00006030002	0	00	00	06	03	0002		CRE	ACC,ONE	
00472	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ADDA ERROR ACC<>1
00473	12000030000	0	12	00	00	01	00	00	ADCA	ACC,2	
00474	00006030001	0	00	00	06	03	0001		CRE	ACC,ONES	
00475	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	ADCA ERROR ACC<>=1
00476	12000030000	0	12	00	00	01	00	00	LDR	ACC,1376	
00477	00006030002	0	00	00	06	03	0002		CRE	ACC,1377	
00478	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	
00479	12000030000	0	12	00	00	01	00	00	DOP	ACC,1377	
00480	00006030001	0	00	00	06	03	0001				

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00502 00001000504 0 00 00 01 00 0014	RTJ 0,++2	
00503 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDP SKIP ACC<ARG
00504 00040000376 1 02 00 00 01 000376	DDP ACC,'1376	
00505 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDP NO SKIP ACC=ARG
00506 00040000376 1 02 00 00 01 000376	DDP ACC,'1376	
00507 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDP NO SKIP ACC>ARG
00508 00040000377 1 02 01 00 01 000377	DDN ACC,'1377	
00509 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDN NO SKIP ACC<ARG
00510 00040000376 1 02 01 00 01 000376	DDN ACC,'1376	
00511 00001040014 0 00 00 01 04 0014	RTJ 0,++2	
00512 00040000376 1 02 01 00 01 000376	RTJ LINK,ERROR	DDN SKP ACC=ARG
00513 00001000515 0 00 00 01 00 0015	DDN ACC,'1376	
00514 00001040014 0 00 00 01 04 0014	RTJ 0,++2	
00515 00040000376 1 02 01 00 01 000376	DDN ACC,'1375	DDN SKIP ACC=ARG
00516 00001000520 0 00 00 01 00 0020	RTJ 0,++2	
00517 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDN SKIP ACC>ARG
00518 00040000376 1 02 02 00 01 000376	DDZ ACC,'1376	
00519 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDZ NO SKIP ACC=ARG
00520 00040000377 1 02 02 00 01 000377	DDZ ACC,'1377	
00521 00001000525 0 00 00 01 00 0025	RTJ 0,++2	
00522 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDZ SKIP ACC<ARG
00523 00040000376 1 02 02 00 01 000376	DDZ ACC,'1375	
00524 00001000530 0 00 00 01 00 0030	RTJ 0,++2	DDZ SKIP ACC>ARG
00525 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00526 00040000376 1 02 03 00 01 000376	DDF ACC,'1376	DDF SKIP ACC=ARG
00527 00001000533 0 00 00 01 00 0033	RTJ 0,++2	
00528 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDF SKIP ACC>ARG
00529 00040000377 1 02 03 00 01 000377	DDF ACC,'1377	
00530 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DDF NO SKIP ACC<ARG
00531 00040000376 1 02 03 00 01 000376	DDF ACC,'1375	DDF NO SKIP ACC>ARG
00532 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00533 00040000377 1 02 03 00 01 000377	LDR ACC,==1776	
00534 00001040014 0 00 00 01 04 0014	DSP ACC,'1776	DSP NO SKIP ACC==ARG
00535 00040000376 1 02 03 00 01 000376	RTJ LINK,ERROR	
00536 00001040014 0 00 00 01 04 0014	DSP ACC,'1777	DSP NO SKIP ACC>=ARG
00537 00023011036 0 00 00 23 01 1036	RTJ 0,++2	
00538 000400001776 1 03 00 00 01 001776	RTJ LINK,ERROR	DSP SKIP ACC<=ARG
00539 00001040014 0 00 00 01 04 0014	DSN ACC,'1776	
00540 000400001777 1 03 00 00 01 001777	RTJ 0,++2	DSN SKIP ACC==ARG
00541 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00542 000400001777 1 03 00 00 01 001777	DSN ACC,'1777	DSN SKIP ACC>=ARG
00543 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00544 000400001775 1 03 00 00 01 001775	DSN 0,++2	DSN NO SKIP ACC<=ARG
00545 00001000547 0 00 00 01 00 0047	RTJ 0,++2	DSZ NO SKIP ACC==ARG
00546 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00547 000400001776 1 03 01 00 01 001776	DSN ACC,'1776	DSP SKIP ACC<=ARG
00548 00001000552 0 00 00 01 00 0052	RTJ 0,++2	
00549 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DSN SKIP ACC==ARG
00550 000400001777 1 03 01 00 01 001777	DSN ACC,'1777	
00551 00001000555 0 00 00 01 00 0055	RTJ 0,++2	DSN SKIP ACC>=ARG
00552 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00553 000400001775 1 03 01 00 01 001775	DSN ACC,'1775	DSN NO SKIP ACC<=ARG
00554 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00555 000400001776 1 03 01 00 01 001776	DSZ ACC,'1776	DSZ NO SKIP ACC==ARG
00556 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00557 000400001775 1 03 02 00 01 001775	DSZ ACC,'1777	DSZ SKIP ACC>=ARG
00558 00001000564 0 00 00 01 00 0064	RTJ 0,++2	
00559 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DSZ SKIP ACC<=ARG
00560 000400001776 1 03 02 00 01 001776	DSF ACC,'1776	
00561 00001040014 0 00 00 01 04 0014	RTJ 0,++2	DSF SKIP ACC==ARG
00562 000400001775 1 03 02 00 01 001775	RTJ LINK,ERROR	
00563 00001000567 0 00 00 01 00 0067	DSF ACC,'1775	DSF NO SKIP ACC>=ARG
00564 00001040014 0 00 00 01 04 0014	RTJ 0,++2	
00565 000400001776 1 03 03 00 01 001776	RTJ LINK,ERROR	DSF SKIP ACC<=ARG
00566 00001000572 0 00 00 01 00 0072	RTJ 0,++2	
00567 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DSF NO SKIP ACC>=ARG
00568 000400001777 1 03 03 00 01 001777	DSF ACC,'1775	
00569 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	DSF NO SKIP ACC<=ARG
00570 000400001775 1 03 03 00 01 001775	RTJ 0,++2	
00571 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00572 00001000575 0 00 00 01 00 0075	LDR ACC,ONE	
00573 000400001776 1 03 04 00 01 001776	BZ ACC,ACC,31	BZ NO SKIP BIT=0
00574 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	
00575 000400001775 1 03 04 00 01 001775	BZ ACC,ACC,0	BZ SKIP BIT=1
00576 00001000580 0 00 00 01 00 0080	RTJ 0,++2	
00577 000400001776 1 03 04 00 01 001776	RTJ LINK,ERROR	
00578 00001040014 0 00 00 01 04 0014	BZ ACC,ACC,0	
00579 000400001775 1 03 04 00 01 001775	RTJ 0,++2	
00580 00001040014 0 00 00 01 04 0014	RTJ LINK,ERROR	

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

00004	07600010100	0	07	14	00	01	01	00	BSO	ACC,ACC,0	
00005	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BSO NO SKIP BIT=1
00006	07600010107	0	07	14	00	01	01	37	BSO	ACC,ACC,31	
00007	00001000011	0	00	00	01	00	0011		RTJ	0,002	
00008	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BSO SKIP BIT=0
00009	00023011037	0	00	00	23	01	1037		LDR	ACC,#7	
00010	04600010103	0	04	14	00	01	01	03	BST	ACC,ACC,3	
00011	00000011040	0	00	00	00	01	1040		CRE	ACC,#15	
00012	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BST ERROR
00013	00023011041	0	00	00	23	01	1041		LDR	ACC,#7	
00014	04600010100	0	04	15	00	01	01	00	BSM	ACC,ACC,0	
00015	00000011042	0	00	00	00	01	1042		CRE	ACC,#0	
00016	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BSM ERROR
00017	04600010100	0	04	15	00	01	01	00	BSM	ACC,ACC,0	
00018	00000011043	0	00	00	00	01	1043		CRE	ACC,#7	
00019	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BSM ERROR
00020	00023011044	0	00	00	23	01	1044		LDR	ACC,#17777	
00021	05600010114	0	05	14	00	01	01	14	BCL	ACC,ACC,12	
00022	00000011045	0	00	00	00	01	1045		CRE	ACC,#17777	
00023	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	BCL ERROR
00024	00023010001	0	00	00	23	01	0001		LDR	ACC,POS	
00025	02400010101	0	02	10	00	01	01	01	SLR	ACC,ACC,1	
00026	00000010002	0	00	00	00	01	0002		CRE	ACC,NEG	
00027	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SLR ERROR
00028	02400010107	0	02	10	00	01	01	37	SLR	ACC,ACC,31	
00029	00000010001	0	00	00	00	01	0001		CRE	ACC,POS	
00030	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SLR ERROR
00031	00023010012	0	00	00	23	01	0012		LDR	ACC,HALF1	
00032	02400010120	0	02	10	00	01	01	20	SLR	ACC,ACC,16	
00033	00000010013	0	00	00	00	01	0013		CRE	ACC,HALF2	
00034	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SLR ERROR
00035	00023010002	0	00	00	23	01	0002		LDR	ACC,NEG	
00036	02200010101	0	02	04	00	01	01	01	SRR	ACC,ACC,1	
00037	00000010001	0	00	00	00	01	0001		CRE	ACC,POS	
00038	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SRR ERROR
00039	02200010107	0	02	04	00	01	01	37	SRR	ACC,ACC,31	
00040	00000010002	0	00	00	00	01	0002		CRE	ACC,NEG	
00041	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SRR ERROR
00042	00023010013	0	00	00	23	01	0013		LDR	ACC,HALF2	
00043	02200010120	0	02	04	00	01	01	20	SRR	ACC,ACC,16	
00044	00000010012	0	00	00	00	01	0012		CRE	ACC,HALF1	
00045	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SRR ERROR
00046	00023010012	0	00	00	23	01	0012		LDR	ACC,HALF1	
00047	02500010120	0	02	12	00	01	01	20	SLA	ACC,ACC,16	
00048	00000010013	0	00	00	00	01	0013		CRE	ACC,HALF2	
00049	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SLA ERROR
00050	00023010013	0	00	00	23	01	0013		LDR	ACC,HALF2	
00051	02300010120	0	02	06	00	01	01	20	SRA	ACC,ACC,16	
00052	00000010004	0	00	00	00	01	0004		CRE	ACC,ONES	
00053	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SRA ERROR
00054	00023010013	0	00	00	23	01	0013		LDR	ACC,HALF2	
00055	02500010120	0	02	13	00	01	01	20	SLL	ACC,ACC,16	
00056	00000010003	0	00	00	00	01	0003		CRE	ACC,ZRO	
00057	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SLL ERROR
00058	00023010013	0	00	00	23	01	0013		LDR	ACC,HALF2	
00059	02300010120	0	02	07	00	01	01	20	SRL	ACC,ACC,16	
00060	00000010012	0	00	00	00	01	0012		CRE	ACC,HALF1	
00061	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	SRL ERROR
00062	00032010001	0	00	00	32	01	0001		LDF	ACC,POS	
00063	00000010001	0	00	00	00	01	0001		CRE	ACC,POS	
00064	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	LDD ERROR
00065	00000010002	0	00	00	00	01	0002		CRE	ACC+120,NEG	
00066	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	LDD ERROR
00067	00032010003	0	00	00	32	01	0003		LDF	ACC,ZRO	
00068	00000010003	0	00	00	00	01	0003		CRE	ACC,ZRO	
00069	00001040014	0	00	00	01	04	0014		RTJ	LINK,ERROR	LDD ERROR
00070	00000010004	0	00	00	00	01	0004		CRE	ACC+120,ONES	

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

```

00707 00001040014 0 00 00 01 04 0014
00708 00023010001 0 00 00 23 01 0001
00709 00023010002 0 00 00 23 01 0002
00710 00033010006 0 00 00 33 01 0006
00711 00006010006 0 00 00 06 01 0006
00712 00001040014 0 00 00 01 04 0014
00713 00006010006 0 00 00 06 01 0006
00714 00001040014 0 00 00 01 04 0014
00715 00006010006 0 00 00 06 01 0006
00716 00001040014 0 00 00 01 04 0014
00717 00023010003 0 00 00 23 01 0003
00718 00023010004 0 00 00 23 01 0004
00719 00033010006 0 00 00 33 01 0006
00720 00006010006 0 00 00 06 01 0006
00721 00001040014 0 00 00 01 04 0014
00722 00006010006 0 00 00 06 01 0006
00723 00001040014 0 00 00 01 04 0014
00724 00006010006 0 00 00 06 01 0006
00725 00001040014 0 00 00 01 04 0014
00726 00023010006 0 00 00 23 01 0006
00727 00025021047 0 00 00 05 02 1047
00728 00001000765 0 00 00 01 00 0765
00729 00023010004 0 00 00 23 01 0004
00730 00027010766 0 00 00 27 01 0766
00731 00123010000 0 00 02 23 01 0000
00732 00027010766 0 00 00 27 01 0766
00733 00123010000 0 00 02 23 01 0000
00734 00027010767 0 00 00 27 01 0767
00735 24100400001 1 01 02 00 02 000001
00736 00123010000 0 00 02 23 01 0000
00737 00027010772 0 00 00 27 01 0772
00738 24100400001 1 01 02 00 02 000001
00739 00123010000 0 00 02 23 01 0000
00740 00027010771 0 00 00 27 01 0771
00741 24100400001 1 01 02 00 02 000001
00742 00123010000 0 00 02 23 01 0000
00743 00027010772 0 00 00 27 01 0772
00744 24100400001 1 01 02 00 02 000001
00745 00123010000 0 00 02 23 01 0000
00746 00027010772 0 00 00 27 01 0772
00747 24100400001 1 01 02 00 02 000001
00748 00123010000 0 00 02 23 01 0000
00749 24100400001 1 01 02 00 02 000001
00750 00123010000 0 00 02 23 01 0000
00751 00027010773 0 00 00 27 01 0773
00752 00006010771 0 00 00 06 01 0771
00753 00027010766 0 00 00 27 00 0766
00754 00001000002 0 01 00 00 01 00 00
00755 00027010774 0 00 00 27 01 0774
00756 00006010772 0 00 00 06 01 0772
00757 00027010766 0 00 00 27 00 0766
00758 00001040014 0 00 00 01 04 0014
00759 24100400001 1 01 02 00 02 000001
00760 00001000727 0 00 00 01 00 0727
00761 00001001050 0 00 00 01 00 1050
00762 37777777777

```

```

RTJ LINK,ERROR LDO ERROR
LDR ACC,POS
LDX ACC+120,NEG
STF ACC,STORE
CRE ACC,STORE
RTJ LINK,ERROR STD ERROR
CRE ACC+120,INCR
RTJ LINK,ERROR STD ERROR
LDR ACC,ZRO
LDX ACC+120,ONES
STF ACC,STORE
CRE ACC,STORE
RTJ LINK,ERROR STD ERROR
CRE ACC+120,INCR
RTJ LINK,ERROR STD ERROR
LDX WORK,MUDAT
CRL WORK,MFINDA
RTJ 0,MFIN
LDR ACC,ONES
STR ACC,ERRFL
LDR ACC,0,WORK
STR ACC,DATA
ADDA WORK,1
LDR ACC,0,WORK
STR ACC,DATA+1
ADDA WORK,1
LDR ACC,0,WORK
STR ACC,EXP
ADDA WORK,1
LDR ACC,0,WORK
STR ACC,EXP+1
ADCA WORK,3
LDR ACC,0,WORK
ADDA WORK,1
MPY ACC,0,WORK

```

```

00752 00027010773 0 00 00 27 01 0773
00753 00006010771 0 00 00 06 01 0771
00754 00027010766 0 00 00 27 00 0766
00755 00001000002 0 01 00 00 01 00 00
00756 00027010774 0 00 00 27 01 0774
00757 00006010772 0 00 00 06 01 0772
00758 00027010766 0 00 00 27 00 0766
00759 00001040014 0 00 00 01 04 0014
00760 24100400001 1 01 02 00 02 000001
00761 00001000727 0 00 00 01 00 0727
00762 00001001050 0 00 00 01 00 1050
00763 37777777777

```

```

STR ACC,RESUL
CRE ACC,EXP
STR 0,ERRFL
RIO ACC,0,2
STR ACC,RESUL+1
CRE ACC,EXP+1
STR 0,ERRFL
MIN 0,ERRFL
RTJ LINK,ERROR MULTIPLY ERROR
ADDA WORK,3
RTJ 0,LOUP1
MPFIN RTJ 0,DIVID
ERRFL GCN -1

```

```

00767 00000000000
00768 00000000000
00769 00000000000
00770 00000000000
00771 00000000000
00772 00000000000
00773 00000000000
00774 00000000000

```

```

DATA GCN 0 TWO WORDS
EXP GCN 0 TO BE MULTIPLIED
RESUL GCN 0 EXPECTED RESULT LEAST SIG.
GCN 0 EXPECTED RESULT MOST SIG.
GCN 0 ACTUAL RESULT LEAST SIG.
GCN 0 ACTUAL RESULT MOST SIG.

```

```

00775 00000000001
00776 00000000001
00777 00000000001
01000 00000000000

```

```

MUDAT GCN 1
GCN 1
GCN 1
GCN 0

```

```

01001 37777777777
01002 00000000001
01003 37777777777
01004 37777777777

```

```

GCN -1
GCN 1
GCN -1
GCN -1

```

```

01005 37777777777

```

```

GCN -1

```

ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

01006 0000000000	GCN	0
01007 0000000000	GCN	0
01010 0000000000	GCN	0
01011 1777777777	GCN	1777777777
01012 1000000000	GCN	1000000000
01013 3000000000	GCN	3000000000
01014 0377777777	GCN	0377777777
01015 1777777777	GCN	1777777777
01016 3000000000	GCN	3000000000
01017 1000000000	GCN	1000000000
01020 3400000000	GCN	3400000000
01021 2000000000	GCN	2000000000
01022 3000000000	GCN	3000000000
01023 0000000000	GCN	0000000000
01024 0377777777	GCN	0377777777
01025 0000000000	GCN	0000000000
01026 0000000000	GCN	0000000000
01027 3777777777	GCN	3777777777
01030 3777777777	GCN	3777777777
01031 3777777777	GCN	3777777777
01032 3777777777	GCN	3777777777
01033 0000000000	GCN	0000000000
01034 00000125252	GCN	00000125252
01035 0000000000	GCN	0000000000
01036 3777777777	GCN	3777777777
01037 0000000000	GCN	0000000000
01040 0000000000	GCN	0000000000
01041 0000000000	GCN	0000000000
01042 0000000000	GCN	0000000000
01043 0000000000	GCN	0000000000
01044 00000017777	GCN	00000017777
01045 00000007777	GCN	00000007777
01046 00000007777	GCN	00000007777
01047 00000001025	GCN	00000001025
01050 00023021135 0 00 00 23 02 1135	DIVIO LOR	WORK, 0 DIVIO
01051 00005021135 0 00 00 05 02 1136	LOOP2 CRL	WORK, 0 OAFIN
01052 00001001107 0 00 00 01 00 1107	RTJ	0, OIFIN
01053 00023010004 0 00 00 23 01 0004	LOR	ACC, ONES
01054 00027010766 0 00 00 27 01 0766	STR	ACC, ERRFL
01055 00123010000 0 00 02 23 01 0000	LOR	ACC, 0, WORK
01056 00027010767 0 00 00 27 01 0767	STR	ACC, DATA
01057 24100400001 1 01 02 00 02 000001	ADDA	WORK, 1
01060 00123010000 0 00 02 23 01 0000	LOR	ACC, 0, WORK
01061 00027010770 0 00 00 27 01 0770	STR	ACC, DATA+1
01062 24100400001 1 01 02 00 02 000001	ADDA	WORK, 1
01063 00123010000 0 00 02 23 01 0000	LOR	ACC, 0, WORK
01064 00027010771 0 00 00 27 01 0771	STR	ACC, EXP
01065 24100400001 1 01 02 00 02 000001	ADDA	WORK, 1
01066 00123010000 0 00 02 23 01 0000	LOR	ACC, 0, WORK
01067 00027010772 0 00 00 27 01 0772	STR	ACC, EXP+1
01070 24100400003 1 01 03 00 02 000003	ADCA	WORK, 3
01071 00123010000 0 00 02 23 01 0000	LOR	ACC, 0, WORK
01072 24100400001 1 01 02 00 02 000001	ADDA	WORK, 1
01073 00131010000 0 00 02 31 01 0000	DIV	ACC, 0, WORK
01074 00027010773 0 00 00 27 01 0773	STR	ACC, RESULT
01075 00006010771 0 00 00 06 01 0771	CRL	ACC, EXP
01076 00027000766 0 00 00 27 00 0766	STR	0, ERRFL
01077 01000010003 0 01 00 00 01 00 03	RID	ACC, 0, 3
01100 00027010774 0 00 00 27 01 0774	STR	ACC, RESULT+1
01101 00006010772 0 00 00 06 01 0772	CRL	ACC, EXP+1
01102 00027000766 0 00 00 27 00 0766	STR	0, ERRFL
01103 00003000766 0 00 00 03 00 0766	MIN	0, ERRFL
01104 00001040014 0 00 00 01 04 0014	RTJ	LINK, ERROR
01105 24100400003 1 01 02 00 02 000003	ADDA	WORK, 3
01106 00001001051 0 00 00 01 00 1051	RTJ	0, LOOP2

DIVIDE ERROR

Appendix F
ASSEMBLY LISTING FOR INSTRUCTION CHECK PROGRAM (TINST HAR 1840)

169

```

21137 00000000134 0 00 00 00 00 000134      OIFIN  STOP  '134

21112 00000000000      DIVDA  GCN   0
21111 37777777777      GCN   -1
21112 00000000000      GCN   0
21113 00000000000      GCN   0

21114 37777777777      GCN   -1
21115 00000000001      GCN   1
21116 37777777777      GCN   -1
21117 00000000000      GCN   0

21120 37777777777      GCN   -1
21121 37777777777      GCN   -1
21122 00000000001      GCN   1
21123 00000000000      GCN   0

21124 10000000000      GCN   '10000000000
21125 17777777777      GCN   '17777777777
21126 00000000000      GCN   0
21127 10000000000      GCN   '10000000000

21130 00000000005      GCN   5
21131 00000000002      GCN   2
21132 00000000002      GCN   2
21133 00000000001      GCN   1
21134 00000000000      OAFIN  GCN   0

21135 00000001110      LDR
21136 00000001134      END
                        EOF

```


A P P E N D I X G

ASSEMBLY LISTING FOR NORD-50 REGISTER TEST PROGRAM (TREG -HAR1842)

ASSEMBLY LISTING FOR NORD-50 REGISTER TEST PROGRAM (TREG -HAR1842)

```

MAIN TREG
*
*
* CHECKS GR0
*
TREG CRE 0,ZRO
STOP 0 GR0 NONZERO
STR 0,STORE
CRE 0,STORE
STOP 0 STR <GR0> NONZERO (EA)
RTJ 0,TST
STORE GCN -1
ZRO GCN 0
*
* GR 1,2&3 ARE USED AS WORKING REGISTERS IN THE TEST
* AND SHOULD BE TESTED FIRST
*
*
TST LDR 3,IPATTS
STR 3,IPATT
LDR 3,PCNT1
STR 3,PCNT1

LOOPA LDR 3,IPATT,0,0,1
STR 3,FOUND
CRE 3,IPATT,0,0,1
STOP 0 GR 3 ERROR
MIN 0,IPATT
MIN 0,PCNT1
RTJ 0,LOOPA
LDR 3,IPATTS
STR 3,IPATT
LDR 3,PCNT1
STR 3,PCNT1

LOOPB LDR 2,IPATT,0,0,1
STR 2,FOUND
CRE 2,IPATT,0,0,1
STOP 0 GR2 ERROR
MIN 0,IPATT
MIN 0,PCNT1
RTJ 0,LOOPB
LDR 2,IPATTS
STR 2,IPATT
LDR 2,PCNT1
STR 2,PCNT1

LOOPC LDR 1,IPATT,0,0,1
STR 1,FOUND
CRE 1,IPATT,0,0,1
STOP 0 GR 1 ERROR
MIN 0,IPATT
MIN 0,PCNT1
RTJ 0,LOOPC
RTJ 0,TSTRG

FIN ACN PATTS*00
IPATT ACN PATTS
EXP GCN 0
FOUND GCN 0
RCOUN GCN 0
PCNT1 GCN 0
SAVE GCN 0

00000 0000000007 0 00 00 06 00 0007
00001 0000000000 0 00 00 00 00 000000
00002 00027000006 0 00 00 27 00 0006
00003 00000000000 0 00 00 00 00 0000
00004 00000000000 0 00 00 00 00 000000
00005 00001000010 0 00 00 01 00 0010
00006 37777777777
00007 00000000000

00010 00023000145 0 00 00 23 03 0145
00011 00027000053 0 00 00 27 03 0053
00012 00023000146 0 00 00 23 03 0146
00013 00027000057 0 00 00 27 03 0057

00014 00023000053 1 00 00 23 03 0053
00015 00027000055 0 00 00 27 03 0055
00016 00006000053 1 00 00 06 03 0053
00017 00000000000 0 00 00 00 00 000000
00020 00003000053 0 00 00 03 00 0053
00021 00003000057 0 00 00 03 00 0057
00022 00001000014 0 00 00 01 00 0014
00023 00023000147 0 00 00 23 03 0147
00024 00027000053 0 00 00 27 03 0053
00025 00023000150 0 00 00 23 03 0150
00026 00027000057 0 00 00 27 03 0057
00027 00023000053 1 00 00 23 02 0053
00030 00027000055 0 00 00 27 02 0055
00031 00006000053 1 00 00 06 02 0053
00032 00000000000 0 00 00 00 00 000000
00033 00003000053 0 00 00 03 00 0053
00034 00003000057 0 00 00 03 00 0057
00035 00001000027 0 00 00 01 00 0027
00036 00023000151 0 00 00 23 02 0151
00037 00027000053 0 00 00 27 02 0053
00040 00023000152 0 00 00 23 02 0152
00041 00027000057 0 00 00 27 02 0057
00042 00023000053 1 00 00 23 01 0053
00043 00027000055 0 00 00 27 01 0055
00044 00006000053 1 00 00 06 01 0053
00045 00000000000 0 00 00 00 00 000000
00046 00003000053 0 00 00 03 00 0053
00047 00003000057 0 00 00 03 00 0057
00050 00001000042 0 00 00 01 00 0042
00051 00001000076 0 00 00 01 00 0076

00052 000000000254 0 00 00 00000254
00053 000000000160 0 00 00 00000160
00054 000000000000
00055 000000000000
00056 000000000000
00057 000000000000
00060 000000000000

```

ASSEMBLY LISTING FOR NORD-50 REGISTER TEST PROGRAM (TREG -HAR1842)

```

00061 000270100000 0 00 00 27 01 0000
00062 000270100000 1 00 00 27 01 0000
00063 000270100000 0 00 01 23 01 0000
00064 000270100000 0 00 00 27 01 0000
00065 000270100000 0 00 00 23 01 0000
00066 000270100000 0 00 00 00 00 000000

```

```

ERROR STR 1,SAVE
ANOA 1,17777
LDR 1,0,1
STR 1,EXP
LDR 1,SAVE
STOP 0

```

```

00067 000270100000 0000000000
00068 000270100000 0000000000
00069 000270100000 0000000000
00070 000270100000 0000000000
00071 000270100000 0000000000
00072 000270100000 0000000000
00073 000270100000 0000000000
00074 000270100000 0000000000
00075 000270100000 0000000000

```

```

FORM 20,12
FINI FOAT 12304,PATTS*60
LDREG FOAT 12304,PATTS
STREG FOAT 12304,FOUND
CHREG FOAT 12304,PATTS
INCR1 GCN 110001
INCR2 GCN 110000
ROUND GCN 0

```

```

00076 000270100000 0 00 00 23 03 0153
00077 000270100000 0 00 00 27 03 0057
00078 000270100000 0 00 00 23 03 0154
00079 000270100000 0 00 00 27 03 0056
00080 000270100000 0 00 00 27 00 0075
00081 000270100000 0 00 00 23 03 0070
00082 000270100000 0 00 00 23 02 0071
00083 000270100000 0 00 00 23 01 0072
00084 000270100000 0 00 00 21 03 0073
00085 000270100000 0 00 00 20 03 0073
00086 000270100000 0 00 00 02 01 0080
00087 000270100000 0 00 00 03 00 0057
00088 000270100000 0 00 00 01 00 0107
00089 000270100000 0 00 00 23 03 0155
00090 000270100000 0 00 00 27 03 0057
00091 000270100000 0 00 00 23 03 0156
00092 000270100000 0 00 00 27 03 0056
00093 000270100000 0 00 00 21 02 0074
00094 000270100000 0 00 00 21 01 0073
00095 000270100000 0 00 00 20 02 0074
00096 000270100000 0 00 00 02 02 01 0000
00097 000270100000 0 00 00 03 00 0056
00098 000270100000 0 00 00 20 01 0073
00099 000270100000 0 00 01 02 01 0000
00100 000270100000 0 00 00 01 00 0061
00101 000270100000 0 00 00 03 00 0057
00102 000270100000 0 00 00 01 00 0121
00103 000270100000 0 00 00 03 00 0075
00104 000270100000 0 00 00 23 03 0070
00105 000270100000 0 00 00 20 03 0075
00106 000270100000 0 00 00 06 03 0067
00107 000270100000 0 00 00 01 00 0137
00108 000270100000 0 00 00 00 00 000134
00109 000270100000 0 00 00 23 01 0072
00110 000270100000 0 00 00 20 01 0075
00111 000270100000 0 00 00 23 02 0157
00112 000270100000 0 00 00 27 02 0057
00113 000270100000 0 00 00 23 02 0071
00114 000270100000 0 00 00 01 00 0106

```

```

TSTRG LDR 3,0000
STR 3,PCNT1
LDR 3,03
STR 3,RCOUN
STR 0,ROUND
LDR 3,LDREG
LDR 2,STREG
LDR 1,CHREG
LOOP SUB 3,INCR1
LOOP1 ADD 3,INCR1
EXC 1,0,3
MIN 0,PCNT1
RTJ 0,LOOP1
LDR 3,0000
STR 3,PCNT1
LDR 3,03
STR 3,RCOUN
SUB 2,INCR2
SUB 1,INCR1
LOOP2 ADD 2,INCR2
EXC 1,0,2
MIN 0,RCOUN
ADD 1,INCR1
EXC 1,0,1
RTJ 0,ERROR
MIN 0,PCNT1
RTJ 0,LOOP2
MIN 0,ROUND
LDR 3,LDREG
ADD 3,ROUND
CRE 3,FINI
RTJ 0,002
STOP 1134
LDR 1,CHREG
ADD 1,ROUND
LDR 2,0000
STR 2,PCNT1
LDR 2,STREG
RTJ 0,LOOP

```

```

00145 0000000000
00146 37777777701
00147 0000000000
00148 37777777701
00149 0000000000

```

```

LDR

```

```

00152 37777777701
00153 37777777704
00154 00000000003
00155 37777777704
00156 00000000003
00157 37777777704

```

00160 00000000000	00000000000	PATTS	FORM	4,4,4,4,4,4,4
00161 02104210421	00000000001		FDAT	0,0,0,0,0,0,0
00162 04210421042	00000000002		FDAT	1,1,1,1,1,1,1
00163 06314631463	00000000003		FDAT	2,2,2,2,2,2,2
00164 10421042104	00000000004		FDAT	3,3,3,3,3,3,3
00165 12525252525	00000000005		FDAT	4,4,4,4,4,4,4
00166 14631463146	00000000006		FDAT	5,5,5,5,5,5,5
00167 10735673567	00000000007		FDAT	6,6,6,6,6,6,6
00170 21042104210	00000000010		FDAT	7,7,7,7,7,7,7
00171 23146314631	00000000011		FDAT	8,8,8,8,8,8,8
00172 25252525252	00000000012		FDAT	9,9,9,9,9,9,9
00173 27356735673	00000000013		FDAT	10,10,10,10,10,10,10
00174 31463146314	00000000014		FDAT	11,11,11,11,11,11,11
00175 33567356735	00000000015		FDAT	12,12,12,12,12,12,12
00176 35673567356	00000000016		FDAT	13,13,13,13,13,13,13
00177 37777777777	00000000017		FDAT	14,14,14,14,14,14,14
00200 37777777777	00000000016		FDAT	15,15,15,15,15,15,15
00201 37777777775	00000000015		FDAT	15,15,15,15,15,15,14
00202 37777777773	00000000013		FDAT	15,15,15,15,15,15,13
00203 37777777767	00000000007		FDAT	15,15,15,15,15,15,7
00204 37777777757	00000000017		FDAT	15,15,15,15,15,15,15
00205 37777777737	00000000017		FDAT	15,15,15,15,15,15,13
00206 37777777677	00000000017		FDAT	15,15,15,15,15,15,11
00207 37777777757	00000000017		FDAT	15,15,15,15,15,15,15
00210 37777777737	00000000017		FDAT	15,15,15,15,15,15,13
00211 37777777577	00000000017		FDAT	15,15,15,15,15,15,7
00212 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00213 37777777677	00000000017		FDAT	15,15,15,15,15,15,13
00214 37777777577	00000000017		FDAT	15,15,15,15,15,15,11
00215 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00216 37777777677	00000000017		FDAT	15,15,15,15,15,15,14
00217 37777777577	00000000017		FDAT	15,15,15,15,15,15,13
00220 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00221 37777777677	00000000017		FDAT	15,15,15,15,15,15,11
00222 37777777577	00000000017		FDAT	15,15,15,15,15,15,15
00223 37777777377	00000000017		FDAT	15,15,15,15,15,15,13
00224 37777777677	00000000017		FDAT	15,15,15,15,15,15,15
00225 37777777577	00000000017		FDAT	15,15,15,15,15,15,7
00226 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00227 37777777677	00000000017		FDAT	15,15,15,15,15,15,13
00230 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00231 37777777677	00000000017		FDAT	15,15,15,15,15,15,15
00232 37777777577	00000000017		FDAT	15,15,15,15,15,15,15
00233 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00234 37777777677	00000000017		FDAT	15,15,15,15,15,15,15
00235 37777777577	00000000017		FDAT	15,15,15,15,15,15,15
00236 37777777377	00000000017		FDAT	15,15,15,15,15,15,15
00237 37777777677	00000000017		FDAT	15,15,15,15,15,15,15
00240 17777777377	00000000017		FDAT	15,15,15,15,15,15,15
00241 00000000017	00000000017		FDAT	15,15,15,15,15,15,15
00242 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00243 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00244 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00245 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00246 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00247 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00250 00000000000	00000000000		FDAT	15,15,15,15,15,15,15
00251 00000000001	00000000001		FDAT	15,15,15,15,15,15,15
00252 00000000000	00000000000		FDAT	15,15,15,15,15,15,15

FOAT	3, 3, 0, 0, 0, 1, 0, 3
FOAT	0, 0, 0, 0, 1, 0, 0, 3
FOAT	3, 3, 0, 1, 0, 0, 0, 0
FOAT	0, 0, 1, 0, 0, 0, 0, 0
FOAT	3, 1, 0, 0, 0, 0, 0, 0
FOAT	1, 0, 0, 0, 0, 0, 0, 0

[illegible]

20355 00000010000	0000000000	FOAT 0,0,0,0,1,0,0,0
20356 00000200000	0000001000	FOAT 0,0,0,1,0,0,0,0
20357 00000000000	0000000000	FOAT 0,0,1,0,0,0,0,0
20358 00100000000	0000000000	FOAT 0,1,0,0,0,0,0,0
20359 02000000000	0000000000	FOAT 1,0,0,0,0,0,0,0
		END
		EOF

ASSEMBLY LISTING FOR NORD-50 REGISTER TEST PROGRAM (TREG -HAR1842)

A P P E N D I X H

DOCUMENTATION REVIEW

Descriptions of manual content within functional groups are as follows:

NORD-50 RELATED MANUALS

1. NORD-50 FUNCTIONAL DESCRIPTION ND-05.007

This manual describes the main building blocks of the Nord-50 and their functions, from a hardware point of view.

It is written for technical and maintenance personnel requiring detailed information about the Nord-50, and should also be of be of interest to software personnel.

Some knowledge of digital techniques and computer systems in general is recommended. Knowledge of the Nord-50 instruction set found in the Nord-50 Reference Manual is necessary.

2. NORD-50 TEST PROGRAMS ND-30.007

This manual contains the descriptions of the test programs used with the Nord-50.

It is written for field service engineers and technical personnel directly involved with testing or maintaining the Nord-50 CPU. It contains detailed information on the contents and structure of each test program and the procedure for their implementation. The manual is the centralized reference document on these test programs.

In-depth knowledge of the functioning of the Nord-50 CPU is required.

3. NORD-10/NORD-50 COMMUNICATION SYSTEM ND-06.005

This manual describes the operation of the communication hardware in the Nord-10/Nord-50 system. It gives a general description of memory communication, and describes communication instructions and simulated memory programming. It is written for technical and maintenance personnel and communication system programmers.

Familiarity with the Nord-10/S and the Nord-50 at the level described in the Nord-10/S and Nord-50 Functional Descriptions is required, also knowledge of the Nord-10/S and Nord-50 instruction sets, which can be found in the Nord-10/S and Nord-50 Reference Manuals.

4. NORD-50 REFERENCE MANUAL ND-05.003

This manual gives a detailed description of the Nord-50 registers and instructions set. It is intended for programmers and operators. The part concerning registers should be of interest to technical and maintenance personnel.

5. NORD-50 LOADER USER'S GUIDE ND-60.083

This manual gives a brief introduction to the loading process. It describes how to use the Nord-50 Loader, how to load an overlaid program, and how to define the communication between the Nord-50 and the Nord-10. The relocatable code (BRF5) format and the error messages produced by the loader are also described.

It is written for all programmers using the Nord-50. It is also recommended for system supervisors who maintain a library of relocatable modules for the Nord-50 with the Nord-50 BRF Editor. No previous knowledge of loaders is required. Familiarity with the Nord-10/S-Nord-50 system is of great advantage for understanding the more advanced use of the Loader.

6. NORD-50 MONITOR USER'S GUIDE AND SYSTEM DOCUMENTATION ND-60.076

The first three chapters of this manual describe the method to be used to run Nord-50 programs. All available commands are explained, including those reserved for the system supervisor. File access and the use of monitor calls from the Nord-50 are described.

Chapters four to six contain the Monitor system architecture and describe how to implement monitor and system documentation.

This manual should be read by all Nord-50 users. The first three chapters are intended for users who execute programs on the Nord-50. A working knowledge of SINTRAN III and with Nord-50 Fortran are required. These can be obtained from the SINTRAN III Timesharing/Batch Guide, ND-60.132 and the Nord-50 Fortran Reference Manual, ND-60.095.

Chapters four to six are not required reading in order to use the Monitor, but should be read by system programmers and analysts and by system supervisors installing the Monitor. Thorough knowledge of the internal operation of SINTRAN III and/or the underlying hardware is required. Less detailed information is required by users reading these chapters as a general description of the Monitor.

7. NORD-50 ASSEMBLER ND-60.075

This manual describes the Nord-50 assembler operating procedure, the assembler directives, macro usage and external program representation. The appendices contain tables of instructions, BRF directives generated by the assembler and numeric opcodes. It is written for any user of the Nord-50 assembler. Familiarity with assembler programming and sufficient SINTRAN III experience to run the assembler is required. Details of the instruction set are given in the Nord-50 Reference Manual, ND-05.003.

8. NORD-50 BRF Editor ND-60.098

This manual describes the commands available in the NORD-50 BRF editor to maintain and modify NORD-50 BRF files and to disassemble the BRF directives and machine instructions. It is written for those maintaining libraries of relocatable NORD-50 modules, including system supervisors, advanced programmers and system programmers. Some knowledge of the internal BRF format (BRF5) is required. This can be found in the NORD-50 Loader User's Guide, ND-60.083, which also gives the required background information about loading NORD-50 segments.

9. NORD-50 FORTRAN REFERENCE MANUAL

ND-60.095

This is a reference manual describing the Nord-50 implementation of Fortran. It also describes external program representation, compiler operating procedure and file access under the SINTRAN III Operating System. Appendices include error message explanations, summaries of loader and monitor commands and a short description of internal data representation and procedure call conventions for interfacing to other languages.

The manual is written for Fortran programmers of the Nord-50. Familiarity with elementary Fortran and SINTRAN III usage are recommended, but the manual contains all the information required to write, compile, load and execute a Fortran program on the Nord-50.

MANUALS FOR THE SPECIAL SYSTEMS INTERFACED OR USED WITH THE NORD-50

1. BIG MULTIPOINT MEMORY SYSTEM

ND-06.007

This manual gives a general and detailed description of the Big Multipoint Memory System architecture, including memory, service and control channel specifications, and installation.

It is written for technical and maintenance personnel requiring a good understanding of this system, and also for installation personnel. Familiarity with the Nord-10/S and the Nord-50 and the Nord-100 CPUs at the level described in their respective functional descriptions is required.

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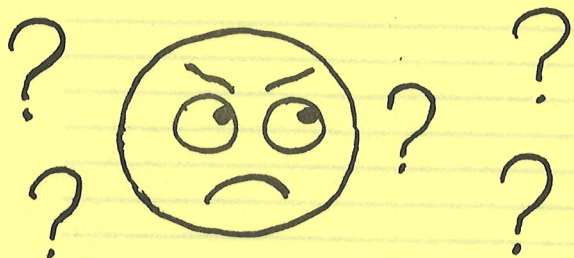
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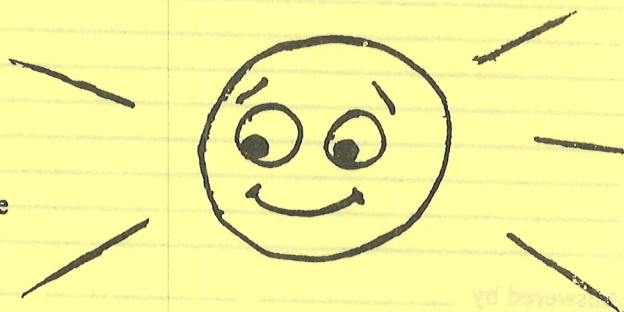


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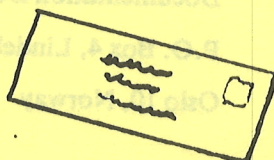
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