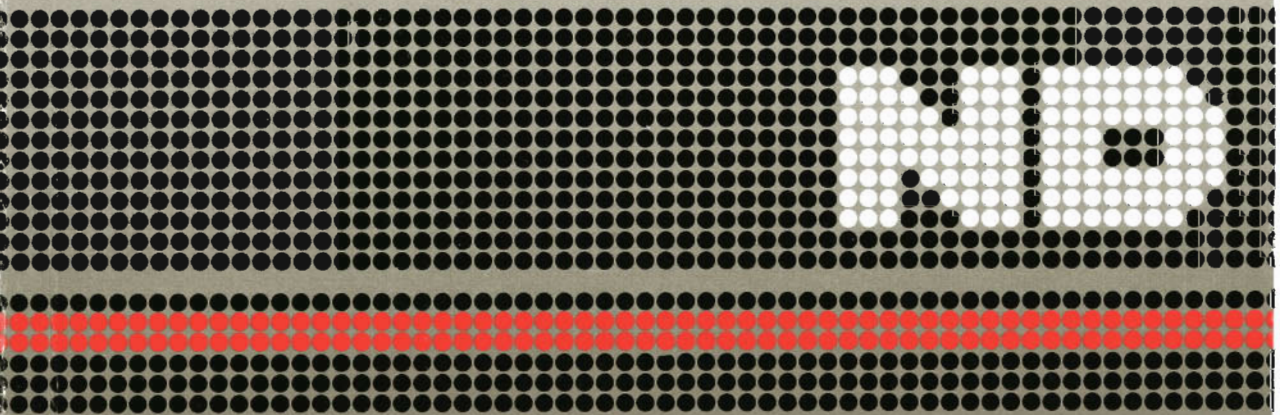# Ethernet II Controller

ND-12.055.1 EN

# Ethernet II Controller

ND-12.055.1 EN

( ii )

**The product**        The Ethernet* II controller (ND number 110063).

**The reader**         This manual is intended for all personnel who
                       require information about the Ethernet II
                       Controller.

**Assumed**            The reader is assumed to have a general
**background**         knowledge of digital hardware design.

**The manual**         This manual outlines the main features of the
                       Ethernet controller and its installation.
                       It is divided into the following three sections:

- 1. Introduction - a general overview,
  including an outline of the Ethernet
  protocol

- 2. The Controller - what it does and how

- 3. Installation - what you need to use and
  how to install the Controller

The appendices include a glossary of terms,
Ethernet protocol details and an ND Ethernet
product guide.

**Related manuals**    The following manuals may be useful:

ECMA 57/TC12/83/51 Technical Report TR19 - Local
Area Networks Safety Requirements.

IEEE Std 802.3-1985 (ISO/DIS 8802/3) Carrier
Sense Multiple Access with Collision Detection
(CSMA/CD).

Data sheets for:
LANCE (Am7990) - AMD reference number 05698
SIA (Am7992B) - AMD reference number 03378
MFP (68901) - various vendors (Motorola, Mostek)

* Ethernet is a trade mark of the Xerox
Corporation.

( iv )

## Notation

| | |
|---|---|
| **hex** | Where possible hexadecimal notation of numbers has been used. |
| **octal** | Octal numbers, commonly used by ND-100 users, are denoted by the subscript: $_8$. |
| **binary** | Binary numbers have the subscript: $_2$. |
| **bits** | Bits within registers are also described using subscripts e.g. Ethernet control register$_2$ is bit 2 of this register. |

In the COSMOS Monitor example (pages 45-9), the following notation is used:

| | |
|---|---|
| **highlight** | Highlighted text will be displayed by the computer. |
| underline | Where underlined text is shown, information is to be entered by the user. ↵ denotes carriage return. |

( vi )

Table of appendices

( x )

( xii )

# CHAPTER 1    INTRODUCTION

2

The Ethernet II controller is implemented on a
single-card for ND-100 based systems. The
controller conforms to the IEEE 802.3 and
ISO/DIS 8802/3 standards.

Systems using the two-card Ethernet I from
Norsk Data can be upgraded to this single card
option (see Section 3.4). ND-100 based systems
can drive a maximum of four Ethernet II
controllers.

This chapter outlines the basic features of the
controller and of the protocol required for
communicating on an Ethernet.

## Architecture

The Ethernet controller implements the three lowest layers of the OSI seven layer model for system communication. The network layer (level 3) is implemented by software running on the Ethernet controller with the controller's hardware and external transceiver implementing the data link and physical layers (levels 2 and 1).

A complete overview of the seven layers is given in Appendix C.

```
   ┌──────────────────────────────┐
   │ COSMOS    Network Service     │
 3 │ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─    │      software
   │ Ethernet Network Service      │
   ├──────────────────────────────┤
   │    IEEE 802.2    LLC          │
 2 │ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─      │   ─ ─ ─ ─ ─ ─
   │    IEEE 802.3    MAC          │
   ├──────────────────────────────┤
   │                               │      hardware
 1 │     Physical   Layer          │
   └──────────────────────────────┘
```
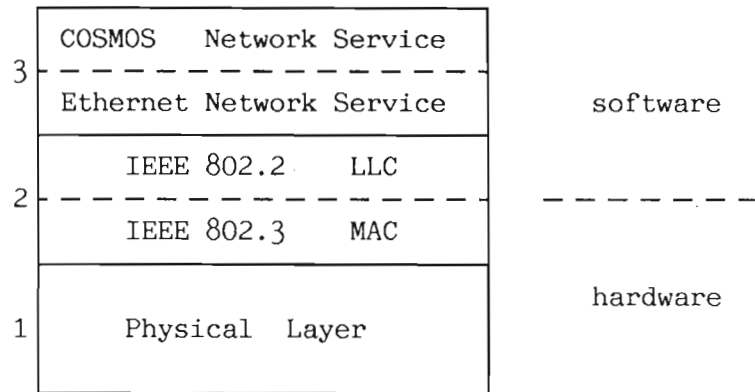
LLC    : Logical Link Layer
MAC    : Medium Access Layer
COSMOS: proprietary software

*Figure 1. The implementation of Ethernet II –*
*OSI standard*

The Ethernet II controller has the following
hardware architecture:

to ND-100

```
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
│  ┌──────────┐   ┌──────────┐  ┌────────┐ ┌─────────┐ │
│  │ ND-100   │   │ 68000    │  │ local  │ │ parity  │ │
│  │ interface│───│ local    │  │ memory │ │ check   │ │
│  └──────────┘   │ processor│  │ 512    │ │ and     │ │
│       │         └──────────┘  │ Kbytes │ │ error log│ │
│       │              │        └────────┘ └─────────┘ │
│       └──────────────┴──────────────┬─────────┘      │
│              │                       │               │
│          ┌────────┐          ┌───────────────────┐   │
│          │ LANCE  │          │ Multi-Function    │   │
│          └────────┘          │ Peripheral (MFP)  │   │
│              │               └───────────────────┘   │
│          ┌────────┐                                  │
│          │ SIA    │                                  │
│          └────────┘                                  │
│              │                                       │
│          ┌────────────┐                              │
│          │ isolation  │                              │
│          │ circuitry  │                              │
│          └────────────┘                              │
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
                transceiver cable
          ┌────────────┐
          │ transceiver│
          └────────────┘
                coaxial cable
            to Ethernet
```

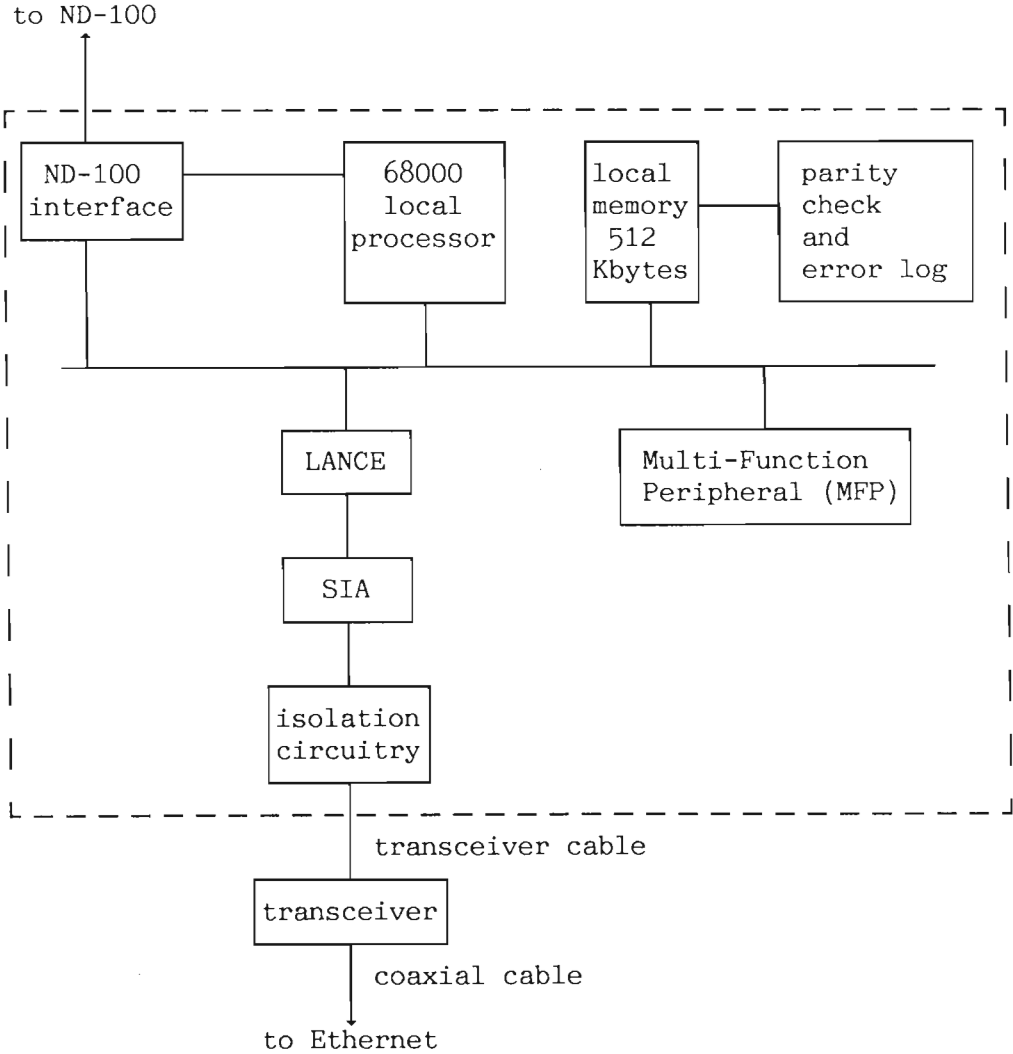*Figure 2. Block diagram of Ethernet II*

## Ethernet protocol

Ethernet is a protocol designed for baseband local area networks (LANs). The network has a bus topology using an algorithm for bus access known as CSMA/CD (Carrier Sense Multiple Access with Collision Detection).

**CSMA/CD**

Access to the network is as follows:

All stations on the Ethernet continually listen to network activity.

A controller wishing to transmit waits for a quiet period (i.e. no activity on the network - none of the stations are transmitting) and begins to transmit.

**collision**

If another station begins to transmit at almost the same time, the transmitted signals will collide and the data on the network becomes garbled.

The transmitting nodes detect this collision and continue to transmit for a predetermined length of time. This ensures that all the nodes on the network recognize that a collision has occurred. The nodes transmit a **jam** pattern of any pattern except that of the CRC. If the collision occured during the preamble, the preamble is still sent followed by the jam pattern.

The action taken by a receiving controller during collision depends upon the time taken to detect the collision.

- If within 4.8μs, an address mismatch has occurred, the packet will be rejected and the Silo pointer reset.

- If within 51.2μs, the packet will be rejected as a **runt packet**.

- After 51.2μs, a **late collision** has occured and the packet written into the Silo (the FIFO on the LANCE - see Section 2.2) but with the CRC error bit set.

The transmitting nodes then **backoff**, each delaying a random period of time before retransmitting. Sixteen attempts, with increasing timeout range, can be made by the controller before an error message is given due to excessive collisions on the network.

The frame formats of packets transmitted and received by the controller are given in Appendix B.

The Ethernet II controller conforms to the following protocol standards:

- IEEE 802.3

- ECMA 80/81/82

- ISO/DIS 8802/3

8

CHAPTER 2    THE CONTROLLER

The controller is implemented on a single card featuring:

- a 68000 local processor

- a LANCE (Local Area Network Controller for Ethernet)

- a SIA (Serial Interface Adapter)

- local memory

- Ethernet transceiver power control

- a MFP (Multi-Function Peripheral controller)

- ND-100 bus interface

## 2.1 68000 local processor

The 68000 is a 10 MHz, 16-bit processor dedicated to the I/O processing required by the Ethernet controller. Its basic control signals - HALT and RESET - are directly set by the ND-100.

## 68000 interrupt levels

These are assigned as follows:

| level | interrupt source |
|-------|------------------|
| 7 | ND-100 power low |
| 6 | ND-100 OPCOM |
| 5 | parity error |
| 4 | test console (PTC) |
| 3 | MFP (and ND-100) * |
| 2 | LANCE interrupt |
| 1 | not used |
| 0 | indicates no interrupt |

* see Section 2.4.5

Interrupt priority is assigned such that level 7 has highest priority and level 0 the lowest.

Detailed and introductory descriptions of the 68000 can be found in the vendors' manuals.

## 2.2 LANCE

The LANCE (Local Area Network Controller for Ethernet - Am7990) is a single integrated circuit featuring:

- on-board DMA and buffer management (48 byte FIFO known as a Silo)

- network and packet error reporting

- back-to-back packet reception

- network diagnostics (see page 46):
  - internal/external loopback
  - CRC logic check
  - time domain reflectometer

to the 68000                                                    to the SIA
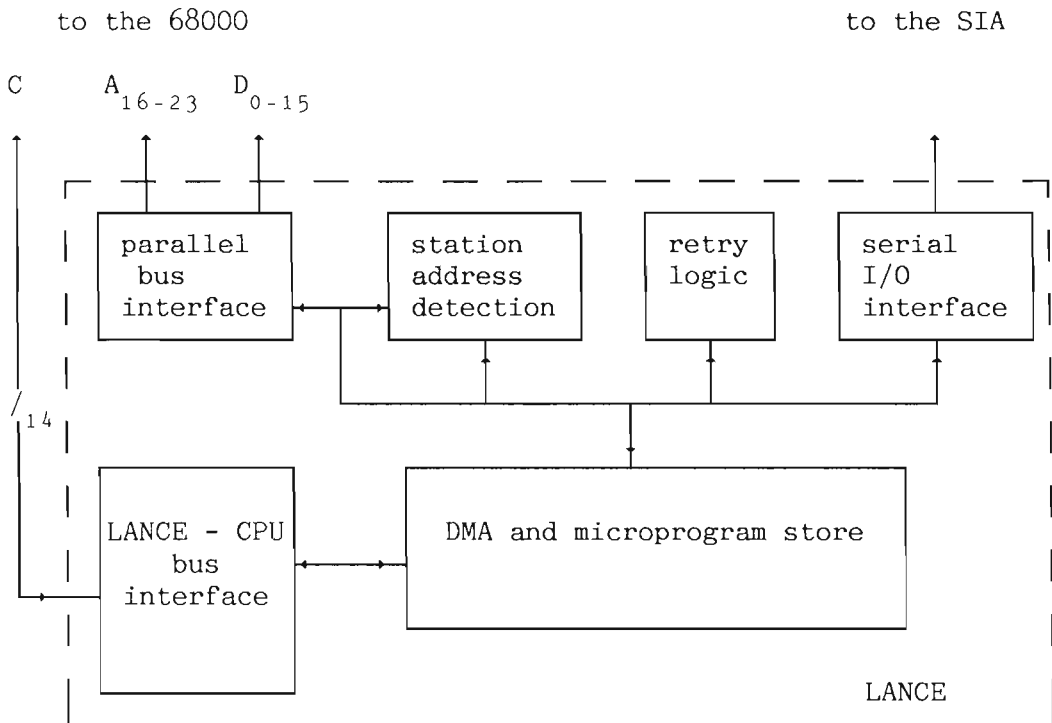


C: control signals

*Figure 3. Block diagram of the LANCE*

The LANCE operates in two modes:

- transmit

- receive

**In transmit mode,** the LANCE directly accesses data in memory and formats it into a **packet** for transmission (see Appendix B). The packet consists of:

- preamble

- sync pattern

- data

- 32-bit CRC

The LANCE transmits the packet to the SIA. It loads the first byte of data into its Silo. Then, as the LANCE transmits the preamble to the SIA, it simultaneously loads the Silo with the remaining data.

**In receive mode,** packets are loaded into the Silo via the SIA. The CRC of the received data is calculated and compared and appended to CRC field given by the packet. If the CRCs do not match, an error bit is set.

## Error reporting

System errors reported by the LANCE include:

- babbling transmitter (the transmitter is attempting to send more than 1518 data bytes)

- collision (collision detection malfunctions)

- missed packet (insufficient buffer space)

- memory timeout (25.6µs)

Packet errors include:

- CRC (data invalid)

- framing (the end of the packet was not on a byte boundary). This is also known as octet or alignment error.

- overflow/underflow (slow response to a DMA request)

- buffer (insufficient buffer space)

Detailed information on LANCE operation can be found in the vendors' manuals.

## 2.3 SIA

The SIA (Serial Interface Adapter - Am7992B) is a single integrated circuit featuring:

- a Manchester encoder/decoder

- collision detection

**For transmission** the SIA encodes the separate clock and NRZ data packet into a standard Manchester II serial bit stream (see Appendix B for a description of Manchester encoding).

**For reception** the SIA indicates to the LANCE that data is being received and separates the incoming Manchester-encoded data stream into clock and NRZ data.

Any collisions on the network are detected and signalled to the LANCE.

## 2.4 Local memory

The local memory consists of:

- 512 Kbyte DRAM (dynamic RAM)

- 1 Kbit SRAM (static RAM)

- 128 Kbyte EPROM (future option)

## 2.4.1 Local DRAM

The local DRAM is accessible from the ND-100 as
if it were any other ND-100 memory bank. The
location of the DRAM in the ND-100 address space
can be set by two thumbwheels located on the
card edge (see section 3.2). The bank number of
the card can be read back to the ND-100 using
the IOXT instruction.

Messages between the controller and ND-100 can
be transferred via special mailbox areas in the
DRAM.

To pass messages, the Ethernet controller can
interrupt the ND-100 and vice versa. The
controller's control and status registers are
under the direct control of the ND-100 (see
section 2.4.6 for their description).

## DRAM access priority

The priority of access to the DRAM is:

- ND-100 (highest)

- LANCE

- 68000  (lowest)

## Byte parity on memory

The DRAM includes a byte parity DRAM of 256K by
18 bits.

## Parity errors

The Ethernet II has two parity error tests:

- external

- internal

**external parity
test**

Here, the ND-100 generates an error which is
reported.

> ┌─ Note ─────────────────────────────────┐
> This test should only be used by ND-100
> stand-alone programs. Tests under SINTRAN
> should only run after the memory has been
> tested.
> └────────────────────────────────────────┘

The ND-100 executes the test as follows:

- it disables the parity write by using an
  IOXT instruction to set the **disable check
  bit** in the Ethernet control register
  (bit 8). (See page 29.)

- it then looks for the parity error signal on
  the bus when the error is detected

- and sets the LED marked 'PERR' on (see
  Section 3.2). The LED is turned off by a
  RESET.

**internal parity
test**

Here the 68000 generates parity errors and
initiates an interrupt.

- the 68000 writes a one to PARITYDIS, the
  parity disable register (address: EF0022) to
  disable parity write

- any parity error is reported by a level 5
  interrupt to the 68000

- the contents of PARITYDIS are read

If PARITYDIS is set together with BREAKMODE
(address: EF0024), forced parity errors are used
to set the breakpoint without changing the code.
The parity error routine should read the
BREAKMODE address to determine whether the
parity error was a breakpoint or not.

## Power failure

The DRAM and its refresh system are connected to
the stand-by power supply so that the memory
contents are preserved.

The ND-100 activates its **Master Clear**, a power
failure sequence, on detecting the failure of
its main power supply. This includes a **power-low
interrupt** to the controller which resets the
controller within approximately 50µs. The
interrupt service routine for power-low saves
all registers in the 68000 and drives the HALT
and RESET signals low.

At the end of the Master Clear pulse, bus
arbitration is reset and the 68000 becomes bus
master. The SCIP (Status Change in PIOC)
register on the Ethernet controller (see
Section 2.4.3) is reset 200µs after power low by
the **Delayed Clear** pulse.

The ND-100 restarts the controller by using an
IOXT instruction, which results in the 68000
fetching the system stack pointer and restart
address (held in the first eight bytes of DRAM).
SINTRAN (the operating system) and PIOCOS cannot
restart the controller in this manner.

## Local SRAM - DRAM protection

The SRAM protects the DRAM from being written to:

- by input DMA.

- by the 68000 user

The SRAM is a **protect table** for the controller's DRAM.

The DRAM is divided into memory segments of 512 bytes. Each segment has a corresponding bit in the SRAM which is either set or cleared to select memory protection or not.

Read and write access to a memory segment is gained by writing a one to the address of the segment concerned plus an offset address of 15360K. A zero protects the segment from access.
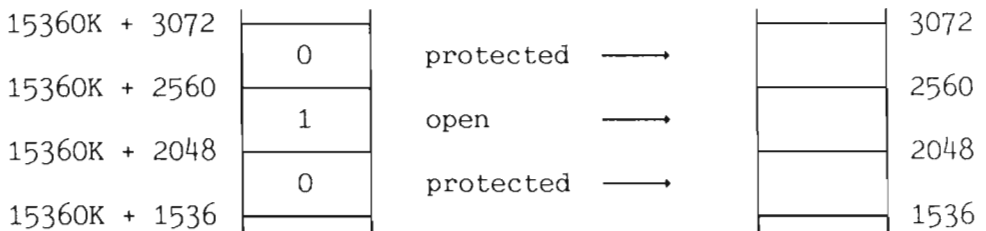


*Figure 4. Memory protection*

Attempting to access a protected area results in a bus error which will interrupt the 68000 with a write protect violation.
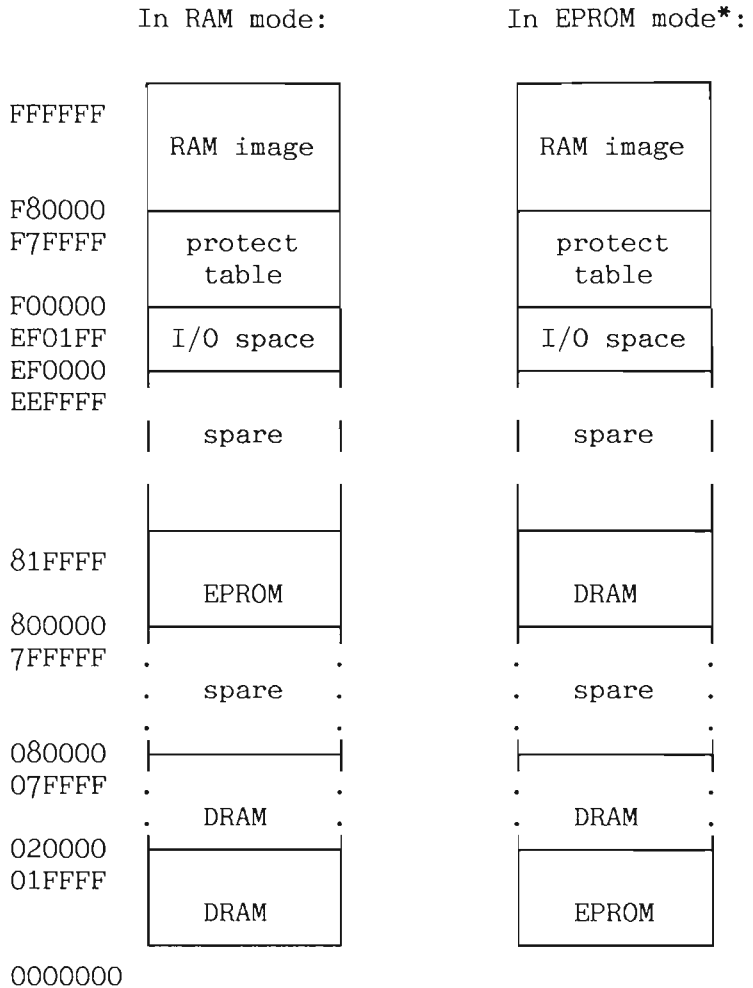
The protect table is established at system start-up. Programs running in 68000 Supervisor mode can access protected DRAM areas.

## 2.4.2 EPROM

The 128K by 16 bit EPROM can only be accessed by
the 68000. The EPROM is currently not used by
the controller, so the boards are delivered with
empty EPROM sockets. Future developments may
implement EPROM.

## 2.4.3 Address decoding

In RAM mode:                    In EPROM mode*:

```
FFFFFF   ┌──────────────┐        ┌──────────────┐
         │  RAM image   │        │  RAM image   │
F80000   ├──────────────┤        ├──────────────┤
F7FFFF   │   protect    │        │   protect    │
         │    table     │        │    table     │
F00000   ├──────────────┤        ├──────────────┤
EF01FF   │  I/O space   │        │  I/O space   │
EF0000   ├──────────────┤        ├──────────────┤
EEFFFF   |    spare     |        |    spare     |
                                 
         ┌──────────────┐        ┌──────────────┐
81FFFF   │              │        │              │
         │    EPROM     │        │    DRAM      │
800000   ├──────────────┤        ├──────────────┤
7FFFFF   .    spare     .        .    spare     .
080000   ├──────────────┤        ├──────────────┤
07FFFF   .    DRAM      .        .    DRAM      .
020000   ├──────────────┤        ├──────────────┤
01FFFF   │    DRAM      │        │    EPROM     │
0000000  └──────────────┘        └──────────────┘
```

* see previous section

RAM image          This area is always used by the ND-100. The
                   LANCE and 68000 do have access.

## Addresses of other devices in the I/O address space

The I/O addresses within this region are decoded twice i.e. EF00XX = EF01XX, so that PIOC and Ethernet I software can be used.

| address range | used by/as: | R/W |
|---|---|---|
| EF00C0 - EF00FF | MFP | R/W |
| EF00B8 - EF00BF | ETHSTAT | R |
| EF00B0 - EF00B7 | LANRESET | W |
| EF00A8 - EF00AF | XCVPW | W |
| EF00A0 - EF00A7 | LANCE | R/W |
| EF0080 - EF009F | SCIP | W |
| EF0060 - EF007F | EAREN | R |
| EF0040 - EF005F | MERRSTAT | R |
| EF0020 - EF003F | MODCR | R/W |
| EF0010 - EF001F | PROFF | W |
| EF0000 - EF000F | not used | - |

R:   read
W:   write

*Table 1. Addresses used in the I/O address space*

MFP

**Multi-Function Peripheral**
The MFP uses the base address of EF00C0 plus a displacement of 1-55 (1-37 hex) to address all the registers within the MFP. ONLY ODD addresses are used to access the MFP.

ETHSTAT

**Ethernet hardware status**
These addresses read the current hardware status of the controller. Only two of the bits read are significant when ZERO:

| bit | meaning |
|---|---|
| 2 | power enable |
| 0 | LAN interrupt |

LANRESET            **LANCE hardware reset**
                    Using an address in this range will initiate a
                    hardware reset.


XCVPW               **Transceiver 12 Volt power switch**
                    Writing a one to this single-bit register will
                    enable the 12 Volt power switch on the
                    transceiver. Writing a zero, turns the power
                    off.


LANCE               **LANCE address space**
                    Only two addresses are needed to address the
                    LANCE. They are:

| address | name |
|---------|------|
| EF00A0 | Register Data Port (RDP) |
| EF00A2 | Register Address Port (RAP) |

                    All accesses to the LANCE are 16-bit using even-
                    byte addresses.


SCIP                **Status Change In PIOC**
                    Using this address range results in an interrupt
                    on level 12 to the ND-100.


EAREN               **Error Address Enable**
                    Using this address range returns the address
                    ($A_{1-16}$) of a memory error on the 68000 data bus.

MERRSTAT                **Parity Error Enable**
The information returned by these addresses has
the format:

```
15         11 10        5 4 3      0
┌─┬─┬─┬─┬─┬──────────┬─┬─┬──────┐
│0│1│0│0│0│  parity  │0│0│ info │
└─┴─┴─┴─┴─┴──────────┴─┴─┴──────┘
```
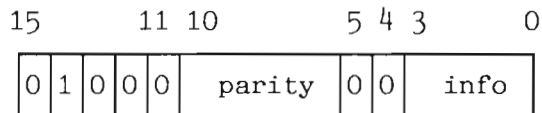
| bit | description |
|-----|-------------|
| 10 | write to parity |
| 9 | address bit 18 |
| 8 | address bit 17 |
| 7 | NGACK ) error detected in      * |
| 6 | BGACK ) read access            * |
| 3 | parity error in high byte |
| 2 | parity error in low byte |
| 1 | parity bit read with high byte |
| 0 | parity bit read with low byte |

**Write to parity** is enabled when the bit is zero;
disabled when set.

* The logic state of the following bits/signals
determine which device detected an error in read
access:

| NGACK bit 7 | BGACK bit 6 | device |
|-------------|-------------|--------|
| 0 | 0 | ND-100 |
| 0 | 1 | none |
| 1 | 0 | LANCE |
| 1 | 1 | 68000 |

MODCR                    **Mode control register**
                         This is addressed by:

| address | description |
|---------|-------------|
| EF0020  | EPROMMODE   |
| EF0022  | PARITYDIS   |
| EF0024  | BREAKMODE   |
| EF0026  | SPARE       |

All four single-bit registers are cleared after
RESET. Each register can be cleared by writing a
zero or set by writing a one to its address.

PROFF                    **Protection Off**
                         Writing a one into this address by a 68000
                         routine means the protect table contents are
                         ignored.


## 2.4.4 Ethernet transceiver power control

A current switch monitors the D.C. current
supplied to the transceiver from the ND-100 via
the controller card. The current switch will
disconnect the supply on controller command or
when the current level could harm hardware or
data integrity.

## 2.4.5 Multifunction Peripheral (MFP)

The 68901 Multifunction Peripheral (MFP)
combines many of the peripheral functions into
one integrated circuit:

- eight parallel I/O lines

- interrupt controller for 16 sources

- four timers

- one full-duplex serial port for Asynchronous
  or Synchronous communication channel (USART)

A functional block diagram of the MFP is given
below:
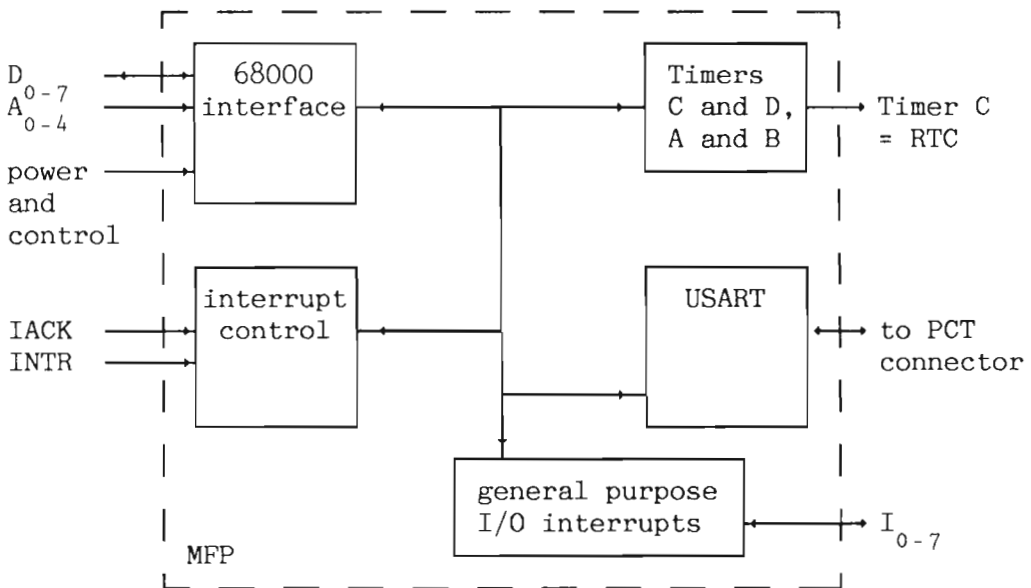


PCT: PIOC console terminal
RTC: real time clock

*Figure 5. The Multifunction Peripheral (MFP) block diagram*

The MFP is used as follows:

**USART**            The USART is connected to a 10-pin PCT (PIOC console terminal) connector. When activated, the PCT interrupts the 68000 on interrupt level 5 via the MFP.

**Timers A-D**       Timer C is used as a real time clock (RTC). Timers A,B and D are not used.

**Interrupts**       The interrupts $(I_0 - I_7)$ are assigned as follows:

| interrupt | use |
|-----------|-----|
| 7         | write violation |
| 6         | ND-100 interrupt |
| 5         | LANCE error * |
| 4-0       | not used |

\* A LANCE error is generated when a memory cycle is stopped by any of the following:

● protect violation

● bus error

● address out of range

## MFP after RESET and initialization

After RESET, all the MFP's registers except for timer registers are cleared. Software then re-initializes the registers. The interrupt vectors from the MFP to the 68000 are:

| vector address | indicates: |
|---|---|
| 117 | write violation by 68000 * |
| 116 | ND-100 requesting interrupt * |
| 114 | receive buffer full |
| 113 | receive error |
| 112 | transmit buffer empty |
| 111 | transmit error |
| 107 | LANCE memory access error |
| 105 | RTC (real time clock) |

* the ND-100 is the source

## 2.4.6 ND-100 interface

Messages between the controller and ND-100 can be transferred via mailbox areas in the DRAM.

To pass messages, the Ethernet controller can interrupt the ND-100 on interrupt level 12 and the ND-100 can interrupt the controller by setting the **ND interrupt** bit (Ethernet control register$_2$ - see following description).

The ND-100 will interrupt the controller on level 6 when the normal Ethernet/ND-100 communication path cannot be used.

The control and status registers are under the direct control of the ND-100.

## Ethernet control register

This is a 16-bit register controlling the
following functions:

| bit | function |
|-----|----------|
| 15-9 | not used |
| 8 | disable check bit |
| 7 | not used |
| 6 | power low |
| 5 | halt |
| 4 | reset |
| 3 | start OPCOM |
| 2 | ND interrupt |
| 1 | not used |
| 0 | enable SCIP interrupt |

A **Master Clear** pulse from the ND-100 (or
power-on) will set the controller's RESET and
HALT signals and reset any local I/O activity.

The ND-100 starts controller activity by writing
to the control register with the halt and reset
bits cleared (zero).

The ND-100 writes to this register using an IOXT
instruction. The Ethernet address of the
controller plus 1 or 3 must be loaded into the
T register before an IOXT is executed (see
Section 3 - Thumbwheel selection of Ethernet
address).

**Ethernet status register**

This has the format:

| bit | function |
|------|----------|
| 15-8 | bank number |
| 6 | memory is 512 Kbytes * |
| 5 | halt |
| 4 | reset active |
| 2 | interrupt set for ND-100 on level 12 |
| 0 | interrupt enabled onto ND-100 bus |

* always zero

**bank number**  Bits 8 and 9 are ALWAYS zero as the controller must start on a half-megabyte boundary i.e. the bank number is **always** a multiple of four.

The ND-100 reads this register using an IOXT instruction. The Ethernet address of the controller plus 0 or 2 must be loaded into the T register before an IOXT is executed (see Section 3 - Thumbwheel selection of Ethernet address).

**CHAPTER 3    INSTALLATION**

CHAPTER 3    INSTALLATION

This section outlines how to install your
Ethernet II card. It also offers some guidelines
on network configuration and equipment
requirements.

```
┌ Note ─────────────────────────────────
│ All equipment using the Ethernet II
│ controller must be to IEEE 802.3,
│ ISO/DIS 8802/3 standards.
└───────────────────────────────────────
```

## 3.1 What you need

Controller to ND-100:

- Ethernet II Controller

- Ethernet/GPIB plug panel

- internal cable between controller and plug
  panel

To establish an Ethernet network:

- Ethernet transceiver(s)

- fan-out unit(s)*

- transceiver cable(s)

- coaxial cable(s)

- coaxial accessories

- repeater(s)*

- point-to-point cable(s)*

    * depends upon network size

**Ethernet transceiver**

The transceiver is powered by the ND-100's
12 Volt D.C. supply via the Ethernet controller.
A current switch will disconnect the power to
the transceiver in the case of:

- short circuit or excessive transceiver
  current consumption

- low 5 Volt supply

- a power off command from the controller

A **power-off command** is issued:

- after jabber (data transmitted to jam the
  network)

- as a result of a hanging transmitter

- if the heartbeat is missing

**Fan-out unit**

A fan-out unit acts as a transceiver
multiplexer, providing eight transceiver-type
connections for DTEs (Data Terminal Equipment).

**Transceiver cable**

This cable links the transceiver to the Ethernet
controller card via the ND-100's plug panel. The
maximum cable length, i.e. distance between
transceiver and controller, is 50m. It is a
four-pair shielded cable, 75Ω impedance.

> Note
> The transceiver cable is called an AUI
> (Attachment Unit Interface) cable in
> IEEE 802.3 terminology.

connectors            **cable to transceiver:**

- 15 pin D-type sub-miniature female with slide
  lock assembly

- Cinch type DA 51220-1 or equivalent

The transceiver must have a mating male
connector with locking posts.

**cable to controller:**

- male with locking posts

- Cinch type DA 53018 or equivalent

This connector must mate with the female
connector in the ND-100 plug panel.

## Coaxial cable

The maximum segment length of coaxial cable is
500m. The cable is marked every 2.5m for correct
transceiver installation. It has the following
characteristics:

- 4 shields

- foamed dielectric

- 50Ω impedance

- 10.3mm thick

- propogation velocity: 0.77c

- supplied by one vendor only

**Cable recommendations:**

The following lists, in order of preference,
steps that can be taken to reduce signal
reflections caused by cable discontinuities.

- The cable segment should be made from one
  continuous cable.

- If segments are built up from smaller
  sections, cable from the same manufacturer
  and preferably the same batch should be
  used.

- If cable sections from different
  manufacturers are used, then standard
  lengths (23.4m, 70.2m, 117m) should be used.

- An arbitary configuration of the cable
  should only be used if the worst-case signal
  reflection at any point on the cable is less
  than 7% of the initial signal.

## Coaxial accessories

The following accessories are required:

- male n-type coaxial connector at the end of
  every cable segment

- female jack with a 50$\Omega$ terminator at each
  end of the (composite) segment

- a cable splice - female-female coaxial
  barrel connector - to join segments

All of these connectors must be electrically
isolated from the building ground (rubber
isolators are available for the Ethernet
terminator and cable splice accessories).

## Repeaters

---

A repeater must be used when more than one 500m cable segment is used. Two types of repeaters are available:

- local repeater

- remote repeater

A repeater ensures that valid data is transferred over a long distance on the Ethernet. It does this by:

- regenerating preamble

- extending collision fragments

- carrying out automatic partitioning and reconnection in the event of a segment failure

- allowing manual partitioning for segment servicing or reconfiguration

A **local repeater** is used for point-to-point links between cable segments within the same building.

A **remote repeater** is used for connections between buildings.

A maximum of two repeaters can be used in the path between any two stations connected to the Ethernet. However, more than two repeaters can be used providing the **round-trip delay** (51µs) is not exceeded.

## Point-to-point cable

Coaxial segments in the same building can be joined by using a link segment of up to 1 km.

The link can be greater than 1 km providing the **round-trip delay** (51µs) is not exceeded.

The point-to-point cable consists of a double fibre optic cable terminated by 9mm SMA connectors at each end.

```
                  fibre   cable
       ┌────(▯===========▯)───┐
       █                      █
      │coaxial              │coaxial
      │cable                │cable
```

(▯   half repeater (BICC 1150)
▯)   half repeater (BICC 1150)
=    double fibre optic cable
█    transceiver
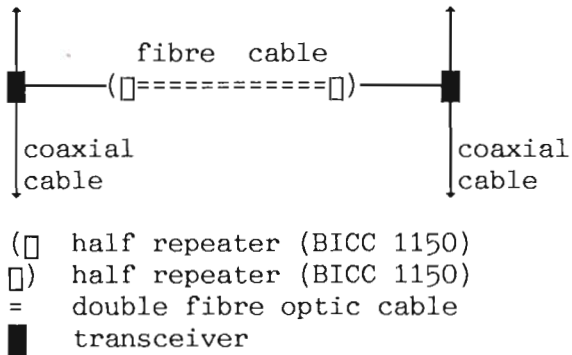
*Figure 6. A point-to-point link*

## 3.2 What to set

```
┌─────────────────────────────────────────┐
│              *  *  *  *        *         │    Ethernet II
│   ≣  ≣  ≣                                │    card
│   7J 9J 12J   5 3 1 2        8          │
│                                         │    (component
│                                         │       side)
│   ┌────┐     ┌──────┐    ┌──────┐       │
│   └────┘     └──────┘    └──────┘       │
└─────────────────────────────────────────┘
      C            B           A
```
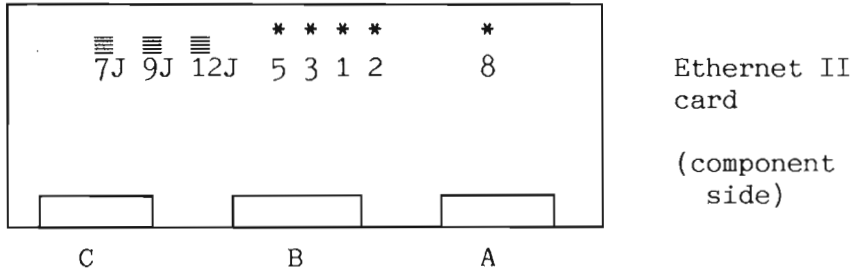
key:

*

| LED | colour | denotes |
|-----|--------|---------|
| 8 | yellow | external 12V transceiver |
| 5 | red | memory parity error |
| 3 | yellow | active memory cycle |
| 2 | red | 68000 halt |
| 1 | red | 68000 reset |

≣

| thumbwheel | selects | page ref: |
|------------|---------|-----------|
| 7J,9J | memory bank number | 40 |
| 12J | Ethernet number | 41 |

A,B,C   edge connectors

*Figure 7. LED activity and thumbwheel selection on an Ethernet II card*

## Thumbwheel selection of memory bank

The thumbwheels numbered 7J and 9J select the
memory bank accessible to the controller. The
thumbwheel numbers correspond to the memory
segments as follows:

| thumbwheel 7J | 9J | bank number | PIOC address space (Kbytes) | Physical page (hex) | |
|---|---|---|---|---|---|
| 0 | 0-3 | 0 | 0 - 512 | 0 - FF | |
| 0 | 4-7 | 4 | 512 - 1024 | 100 - 1FF | |
| 0 | 8-11 | 8 | 1024 - 1536 | 200 - 2FF | |
| 0 | 12-15 | 12 | 1536 - 2048 | 300 - 3FF | |
| 1 | 0 | 16 | 2048 - 2560 | 400 - 4FF | |
| . | . | . | . | . | . |
| . | . | . | . | . | . |
| ↓ | ↓ | ↓ | ↓ | ↓ | ↓ |
| etc. | etc. | etc. | etc. | etc. | etc. |

*Table 2. Thumbwheel selection of memory banks*

## Thumbwheel selection of Ethernet number

An ND-100 can control four Ethernet controllers. The Ethernet address of a controller in the system must be set by thumbwheel 12J.

| thumbwheel 12J | Ethernet number | Ethernet address (device number) | Ident Code |
|---|---|---|---|
| 0 | 1 | $140360_8$ | $140034_8$ |
| 1 | 2 | $140364_8$ | $140035_8$ |
| 2 | 3 | $140370_8$ | $140036_8$ |
| 3 | 4 | $140374_8$ | $140037_8$ |

*Table 3. Thumbwheel selection of Ethernet address*

The Ethernet address (device number) given above is the base address, each controller is assigned four addresses, two for reading from and two for writing to the ND-100 (see Section 2.4.6).

## 3.3 How to connect to the network

```
                        ┌─────────────────────────┐
                        │         ND-100          │
                        │                         │
                        │    ┌──────────────┐     │
                        │    │ Ethernet II  │     │
                        │    │ controller   │     │
                        │    └──────────────┘     │
                        └─────────────────────────┘

                          │
                          ↑
        transceiver       │
           cable          │
         50m max.         │
                          ↓
     x────────────●───────────────────■──────────────────────x

     ←──────────────x──────────────────x──────────────────────→
              cable segment   500m max.
```
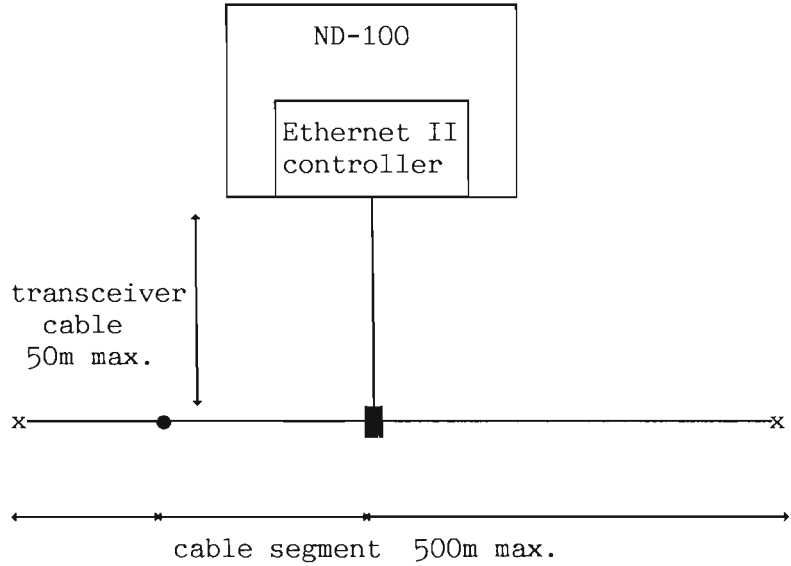
x :      50Ω terminator with insulator

■ :      transceiver

● :      cable splice with insulator

↔:       standard lengths of coaxial cable
         (to a maximum of 500m)

*Figure 8. Connecting to the Ethernet*

Configuration:
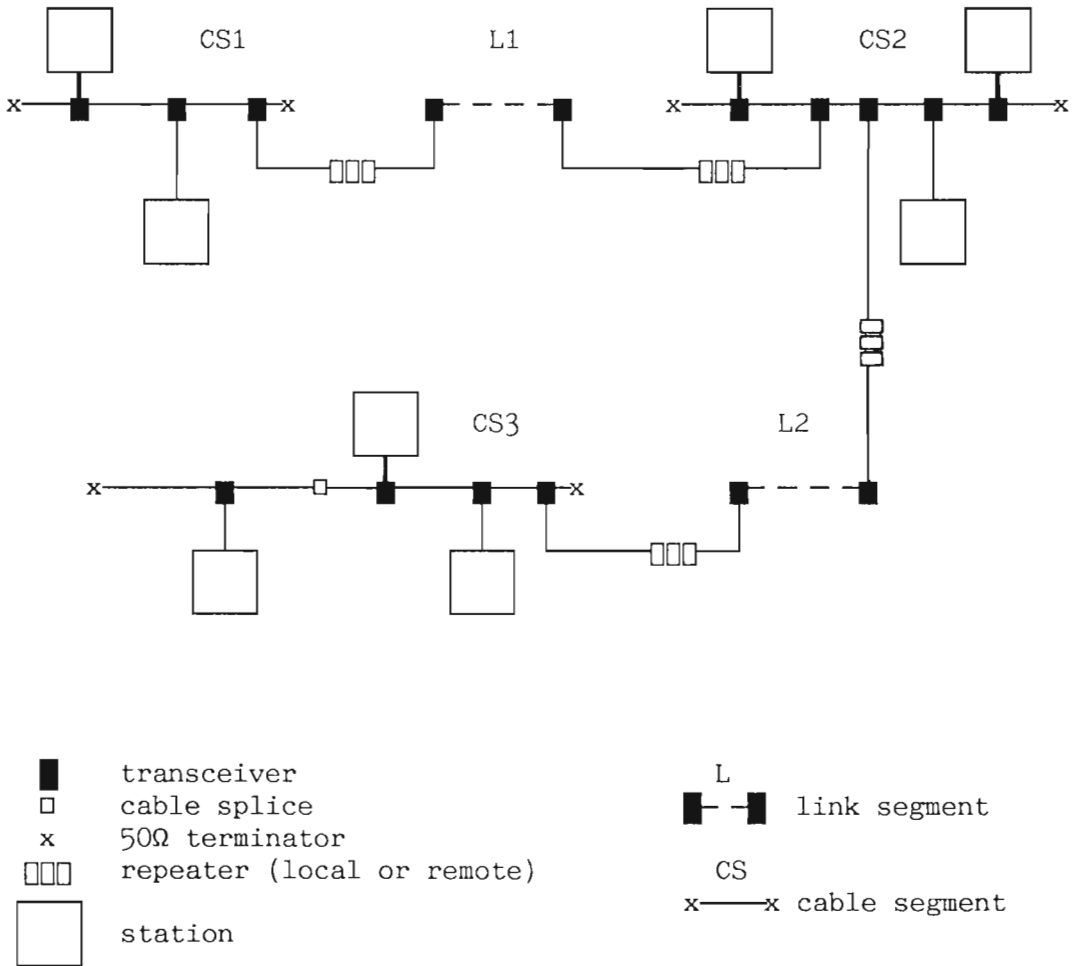


Figure 9. A typical multi-station, multi-segment Ethernet

## 3.4 How to upgrade to an Ethernet II
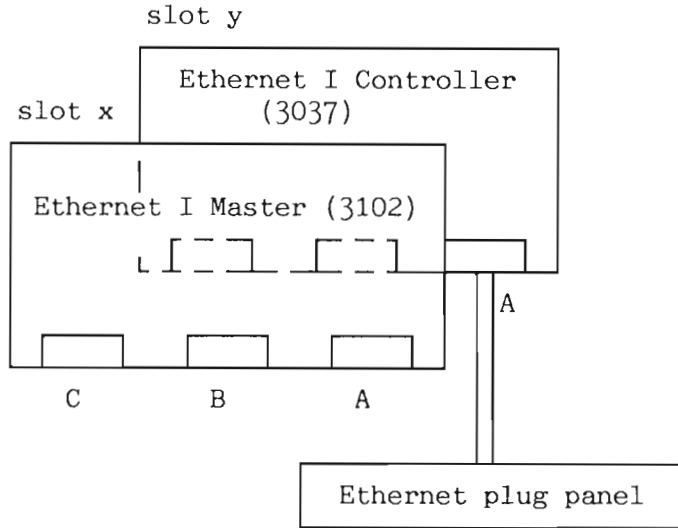


*Figure 10. Upgrading from an Ethernet I*

1. Remove the Ethernet I Master and Controller cards.

2. Remove the cable linking the B-connectors.

3. Insert the Ethernet II card in the slot that was occupied by the Ethernet I Controller card (slot y).

4. Reset the thumbwheel settings of any I/O cards above the Ethernet memory space.

5. IF any DMA request sources are installed at slot numbers greater than the Ethernet controller, insert a dummy plug linking the following connector signals in the slot once occupied by the Ethernet I Master (slot x):

        INGRANT   to   OUTGRANT
        INIDENT   to   OUTIDENT

6. Run configuration test.

7. Reinstall COSMOS Ethernet option.

## 3.5 Ethernet statistics

A monitor program can be run as follows:

```
@(UTI)ENCOS-MON↵

-----------------------------------------------------------------
                    COSMOS ETHERNET MONITOR
                        VERSION xxx
                 FOR ND-110063 ETHERNET II
           (type HELP for list of available commands)

-----------------------------------------------------------------
ENTER COMMAND:STAT↵
  get statistics
 server number (0/1/2/3):0
 system name:name of system
 source of statistics is specified by integer code as follows:
 0  => MA Logical Address statistics
 N  => Network Server Statistics for connection to system N
 specify statistics source (0/N):0
MA stats
 via physical copy (Y/N):N
```

*Figure 11. Calling Ethernet statistics from the COSMOS Monitor*

where xxx represents the current version number
of the COSMOS Monitor

This will return the statistics for Ethernet server 0. The following is an example of statistics reported to the terminal. The text which is not highlighted is a cross-reference to the relevant registers in the LANCE (it is NOT reported to the terminal).

| ETHERNET MA STATISTICS FOR LOCAL SYSTEM | | $CSR_0$ | TMD | RMD |
|---|---|---|---|---|
| frames transmitted successfully | 263 | TINT | | |
| including after one collision | 0 | TINT | ONE | |
| and after multiple collisions | 0 | TINT | MORE | |
| frames aborted(excess collisions) | 0 | TINT | RTRY | |
| frames received and given to user | 263 | RINT | | |
| received and dropped | 0 | * RINT | | |
| missed | 0 | MISS | | |
| CRC errors | 0 | | | CRC |
| alignment errors | 0 | | | FRAM |
| FIFO overflows | 0 | | | OFLO |
| buffer overflows | 0 | | | BUFF |
| bad MA length field | 0 | * | | |
| loss of carrier during transmit | 0 | | LCAR | |
| transmit underflow | 0 | | UFLO | |
| late collision | 0 | | LCOL | |
| bad length received | 0 | * | | |
| bad address received | 0 | * | | |
| missing transceiver heartbeat | 0 | CERR | | |
| jabber detected | 1 | BABL | | |
| memory error | 0 | MERR | | |
| hung transmit state | 0 | * | | |
| restarts | 0 | * | | |

CSR:   Control and Status Register
RMD:   Receive Message Descriptor
TMD:   Transmit Message Descriptor
*:     statistic determined by the 68000

*Figure 12. Typical Ethernet statistics returned by the COSMOS Monitor*

## Description of COSMOS Monitor statistics

**frames transmitted successfully**
This is the number of successfully transmitted
frames.

**frames transmitted successfully after one
collision**
This the number of frames that required one
retry to transmit the packet.

**frames transmitted successfully after multiple
collisions**
This the number of frames that required more
than one retry to transmit the packet.

**frames aborted**
This is the number of frames aborted. The
transmitter has failed after sixteen retries to
transmit the frame.

**frames received and given to the user**
This is the number of successfully received
frames.

**frames received and dropped**
The number of frames dropped after reception if
the ENNS buffer space is full.

**frames missed**
This is the number of times the receiver lost a
packet.

**CRC errors**
This is the number of CRC errors detected by the
receiver.

**alignment errors**
This is the number of alignment or framing
errors received. The error is flagged when a
received packet contains a non-integer multiple
of eight bits and a CRC error.

**FIFO overflows**
This is the number of times the Silo overflowed

resulting in all or part of the incoming packet
being lost.

**Buffer overflows**
A buffer overflow is detected when either the
Silo overflow occurred before the LANCE received
the next status information or the LANCE does
not own the next buffer whilst data-chaining a
received packet.

**bad MA length field**
This is the number of received frames with a
field length inconsistent to that in the DMA
command byte.

**loss of carrier during transmit**
This is the number of times the carrier input
signal to the LANCE (RENA) has been lost whilst
the LANCE was transmitting. The LANCE continues
to transmit the packet but will not retry if
transmission fails.

**transmit underflows**
This is the number of times the transmitter has
truncated a message due to late data being
received from memory. In this case, the Silo is
emptied before the end of the packet was
reached.

**late collision**
The number of collisions that occurred after the
slot time.

**bad length received**
The number of incorrect length fields received.

**bad address received**
The number of incorrect addresses received.

**missing transceiver heartbeat**
This is the number of times a collision occuring
after LANCE transmission fails to activate the
LANCE within 2μs.

**jabber detected**
This is the number of times a transmitter
timeout error has occurred. This timeout occurs

when the transmitter has been on the channel
longer that the time required to send the
maximum packet length.

**memory error**
This error is set when the LANCE, as a Bus
Master, has not received a READY signal in
response to an address. This error turns the
LANCE transmitter and receiver off.

**hung transmit state**
The number of one second software timeouts on
awaiting transmit commands.

**restarts**
The number of restarts given by the ND-100 to
the 68000.

**APPENDIX A    GLOSSARY**

| | |
|---|---|
| backoff | The time a transmitting node waits before retransmitting after a collision. |
| 68000 | 16-bit microprocessor |
| c | speed of light in a vacuum ($3 \times 10^8$ ms$^{-1}$) |
| CPU | Central Processing Unit |
| CRC | Cyclic Redundancy Checksum |
| CSMA/CD | Carrier Sense Multiple Access/Collision Detect |
| DMA | Direct Memory Access |
| Ethernet | A protocol for communicating between devices on a Local Area Network. |
| Ethernet I | An Ethernet controller for ND-100 systems based on a two card solution (Ethernet master and a controller). |
| frame | packet + preamble |
| FIFO | First-In, First-Out (called Silo as implemented within the LANCE). |
| heartbeat | A signal generated by a transceiver to indicate it is operative. This is also known as SQE. |
| IEEE | Institute of Electrical and Electronic Engineers (U.S.A.) |
| ISO | International Standards Organisation |
| jam | Nodes jam the network by transmitting simultaneously to ensure all nodes know a collision has occured on the network. |
| LAN | Local Area Network |

LANCE            Local Area Network Controller for Ethernet

LED              Light Emitting Diode

ND-100 series    The family of 16-bit general purpose computers
                 from Norsk Data consisting of the following:

                     ND-100
                     ND-100/CE
                     ND-100/CX
                     ND-100 Compact
                     ND-100 Satellite
                     ND-110/CE
                     ND-110/CX

node             An access point to (or a device on) the Ethernet.

NRZ              Non-Return-to-Zero...a type of data encoding.

OPCOM            OPerator COMmunication...direct communication
                 with the ND-100 CPU.

OSI              Open Systems Interconnection

packet           Significant information within the Ethernet
                 frame (destination address to FCS fields).

PIOC             Programmable Input/Output Controller

preamble         preamble + sync (or SFD)

segment          in memory...512K of contiguous memory
                 of a cable...fixed length of cable.

SIA              Serial Interface Adapter

SQE              Signal Quality Error (see heartbeat)

**APPENDIX B    ETHERNET PROTOCOL DETAILS**

## Frame format

| IEEE 802.3 | | Ethernet |
|---|---|---|
| preamble | | preamble |
| SFD $10101011_2$ | 64 bits | sync $11_2$ |
| destination address | 6 bytes | destination address |
| source address | 6 bytes | source address |
| length | 2 bytes | type |
| data | 46-1500 bytes | data |
| pad | | FCS |
| FCS | | |

## IEEE 802.3 - Ethernet differences

### Frame terminology

An IEEE 802.3 and Ethernet frame should be identical. Each protocol divides the frame into fields with different names. A short description of the field terminology is given below.

Each octet (byte) in the frame is transmitted/received low-order bit first (see FCS). Transmission/reception begins with the preamble field.

**preamble**       A sequence of bits transmitted to synchronize clocks and other devices on the network. The bit pattern is alternate ones and zeros (1010...10). An Ethernet frame transmits a further six bits as preamble compared to the IEEE 802.3 (equivalent to the first six bits of the SFD).

**SFD - IEEE 802.3**  **Start Frame Delimiter.** This is a byte of data indicating the start of a frame (information) after the preamble. The byte is always $10101011_2$ (IEEE 802.3 only).

**sync - Ethernet**  An Ethernet sync field consists of two bits both set to one.

> Note ─────────
> The actual bit pattern of the preamble and SFD (IEEE 802.3) will be the same as the preamble and sync (Ethernet).

**source**
**address**

This six byte field specifies the station
sending the frame. It has the format:

| byte | 1 | 2 | 3 | 4 | 5 | 6 |
|------|----|----|----|----|----|----|
| hex value | 08 | 00 | 26 | LB | HB | 00 |

The first three bytes are the **global ND address**.
A number unique to ND Ethernet equipment and
registered with the IEEE and ISO.

The next two bytes are the high and low bytes
(HB and LB) of an ND system.

The last byte is zero.

**destination**
**address**

This six byte field specifies the station(s)
for which the frame is intended.

The first two bits have the following
significance:

| bit | value | type of address |
|-----|-------|-----------------|
| 0 | 0<br>1 | individual<br>group * |
| 1 | 0<br>1 | global<br>local/broadcast |

* a group address can select none, one, more
than one or all stations.

**length -**
**IEEE 802.3**

This two byte field gives the number of data
bytes in the frame. If the number of data bytes
is less than 64 bytes a pad field is added to
allow the shorter data field to be received.

**type - Ethernet**

This two byte field specifies the type of
packet. Packet length is supplied by the LANCE
during reception.

**data**              This is Manchester-encoded data (see next
                      section).

FCS                   **Frame Check Sequence** A cyclic redundancy check
                      (CRC) is used by the transmit and receive
                      algorithms to monitor any corruption of
                      information received/transmitted on the
                      Ethernet. The FCS (Frame Check Sequence) field
                      of the frame will contain the frame's CRC value.

                      The CRC is calculated from the following frame
                      fields:

                      ● source address

                      ● destination address

                      ● length (type)

                      ● data

                      ● pad

                      Note: The low-order bit transmitted/received
                      first of the FCS is the most significant term of
                      the CRC polynomial and the high-order bit the
                      least significant.

**Manchester encoding**

---

The separate data and clock signals are encoded by making, at the centre of a bit cell:

- a positive-going transition for a logical ONE

- a negative-going transition for a logical ZERO

and

- a transition at each cell boundary between consecutive bit cells of the same value.

Three examples of a Manchester-encoded bit stream are given below:

bit  cell
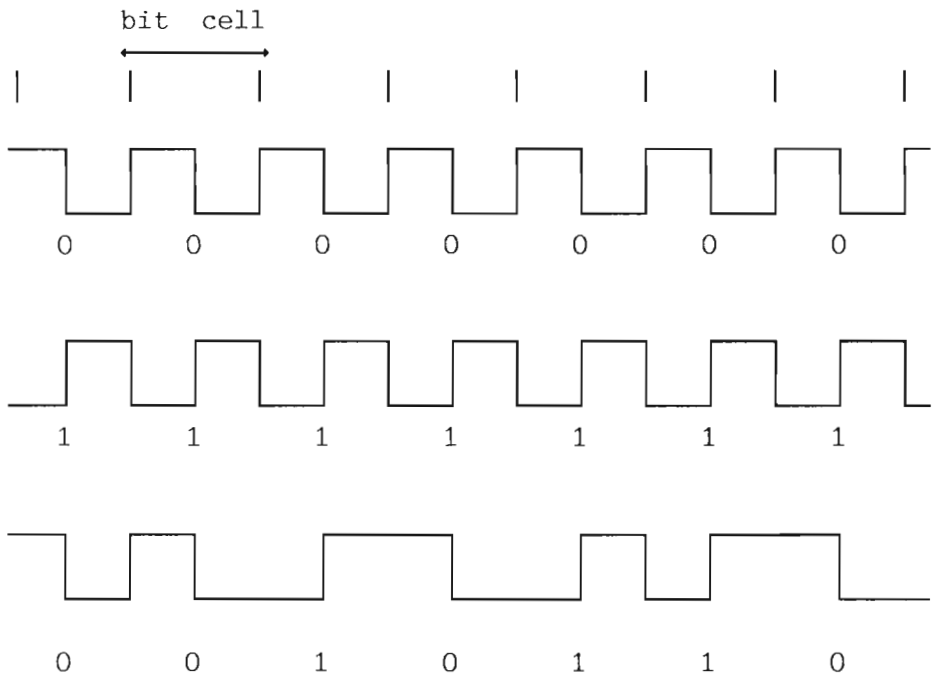
Figure 13. Examples of Manchester-encoded signals

# APPENDIX C    ND ETHERNET PRODUCT GUIDE

## Ethernet accessories

| ND Number | Product Name | |
|-----------|--------------|---|
| 107700 | Transceiver cable, 5m | |
| 107710 | Transceiver cable, 15m | |
| 107720 | Ethernet 50Ω terminator | |
| 107730 | Ethernet cable splice | |
| 107740 | Ethernet transceiver | |
| 107750 | Local repeater package | A |
| 107760 | Ethernet coaxial cable, 23.4m | |
| 107770 | Ethernet coaxial cable, 70.2m | |
| 107780 | Ethernet coaxial cable, 117m | |
| 107790 | Remote repeater package | B |
| 107830 | Fan out unit package | |

A includes 1 repeater, 2 transceivers and two transceiver cables
B includes 2 repeaters, 2 transceivers and two 15m transceiver cables

## OSI model and ND's implementation

| Layer | | | | |
|---|---|---|---|---|
| 7 | COSMOS | ISO Applications | FTP Telnet | ⎫ |
| 6 | | | nil | |
| 5 | XMSG | | nil | host (ND-100 series) |
| 4 | | ISO TC.4 | ARPA TCP* | |
| 3 | LNCN | ISO CNLSNL (inactive subset) | ARPA IP | |
| 2 | LLC1 | LLC1 / MAC | DIX | Ethernet II |
| 1 | Physical | | | ⎭ |
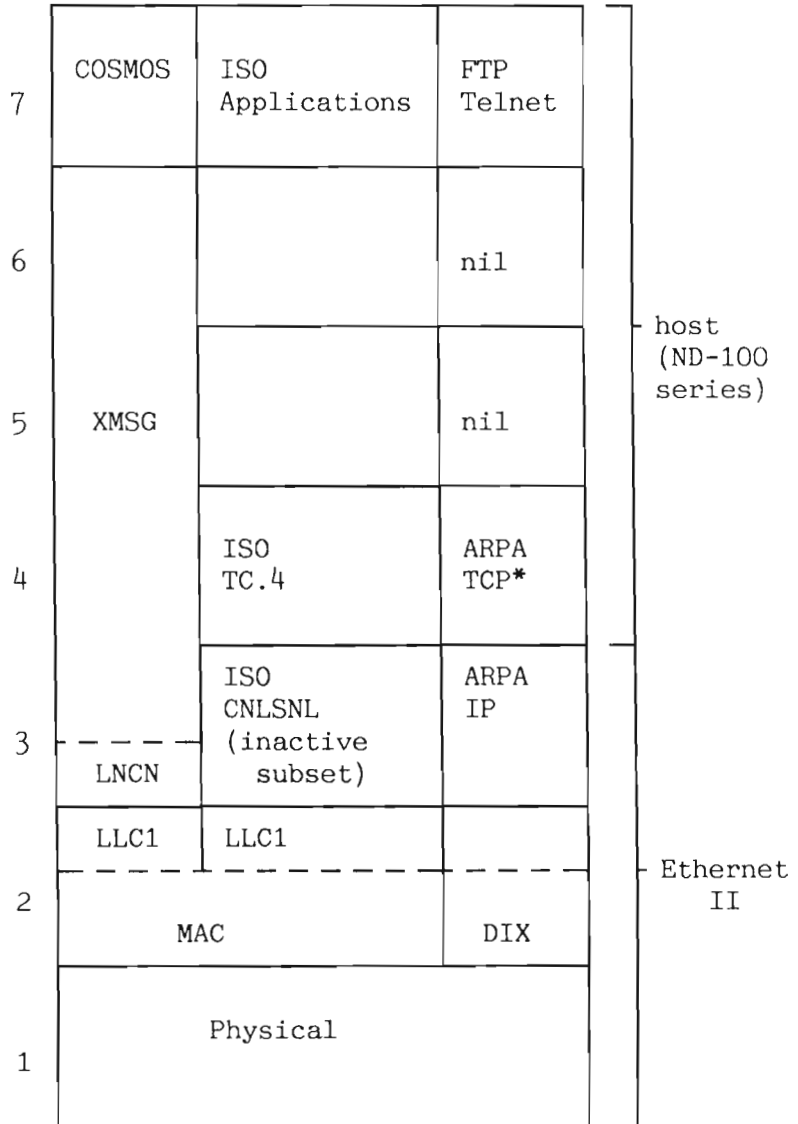
\* to be implemented late 1987 by Ethernet II

```
DIX    : Digital-Intel-Xerox specified protocol
ARPA   : Advanced Research Projects Agency
LLC    : Logical Link Control
CNLSNL : Connectionless Network Layer
LNCN   : Local Network COSMOS Network Layer
MAC    : Media Access Control
```

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ND-12.055.1 EN
Ethernet II Controller

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