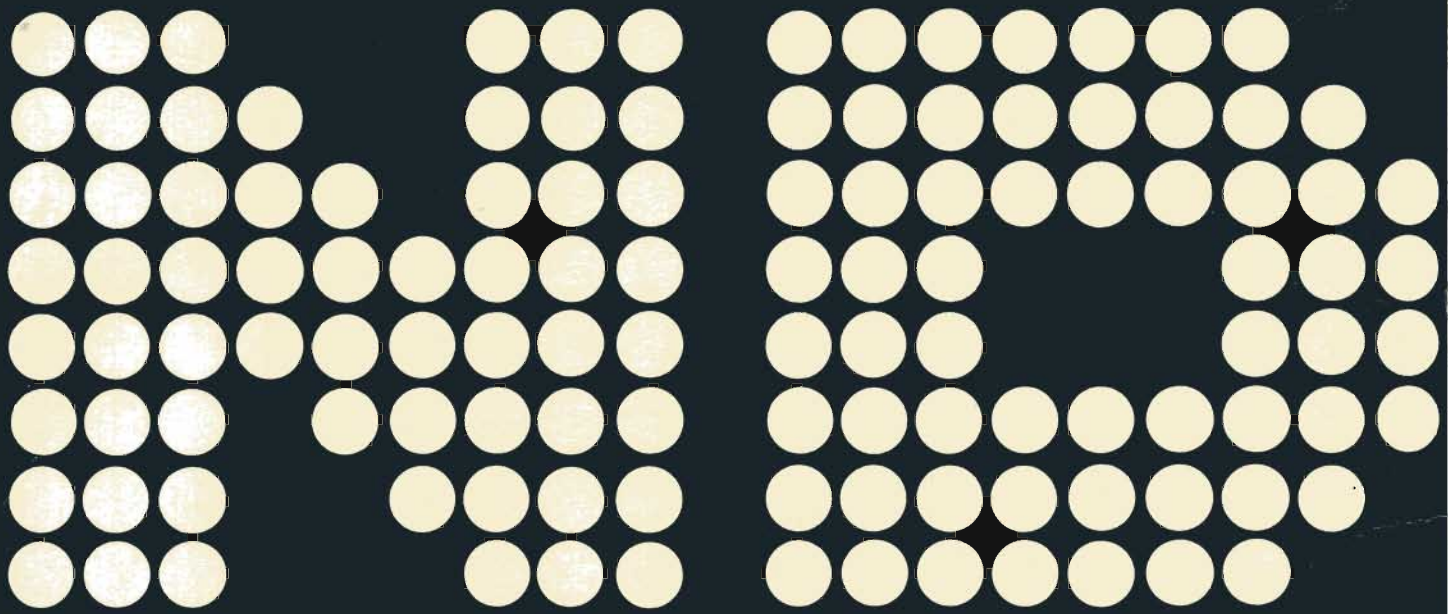
High Level Data Link Control (HDLC) Interface

NORSK DATA A.S



High Level Data Link Control (HDLC) Interface

REVISION RECORD

Revision	Notes
11/78	Original Printing

HDLC — High Level Data Link Control Interface
Publication No. ND-12.018.01

NORSK DATA A.S.
Lørenveien 57, Postboks 163 Økern, Oslo 5, Norway

MAIN CONTENTS
+ + +

Section:

HDLC INTERFACE
PART I

DETAILED CONTENTS
+ + +

I.1 INTRODUCTION

High Level Data Link Control (HDLC) INTERFACE is a synchronous modem interface, however, is also well suited as an intercomputer link interface (See Figure I.1.1).

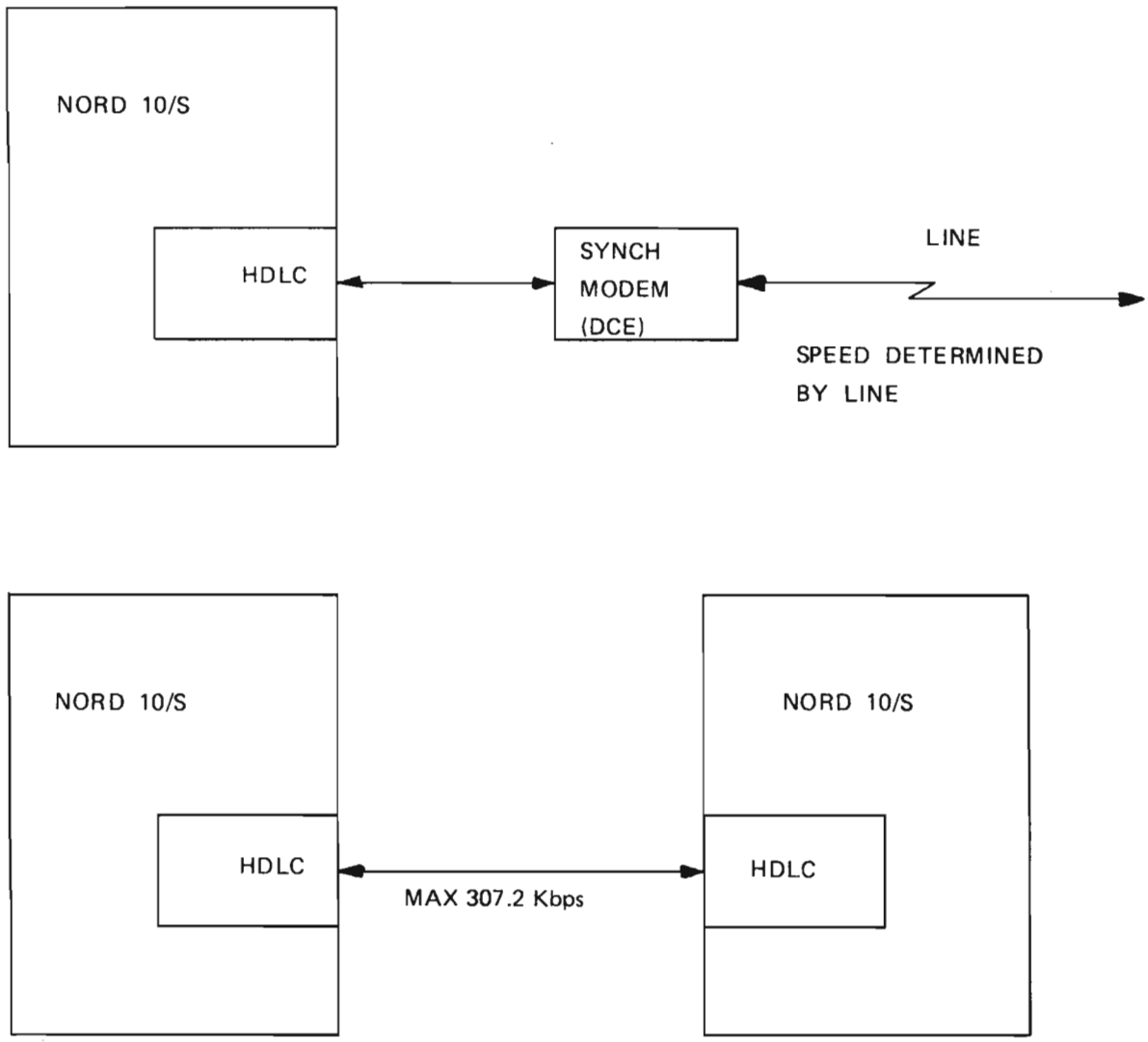


Figure I.1.1: APPLICATIONS OF HDLC INTERFACE

Used as a synchronous modem controller HDLC INTERFACE includes several features by means of communication standards implemented in hardware.

Used as an intercomputer link, HDLC INTERFACE contains internal timing. A strap switches from external timing (from modem) to internal timing which allows transfer rates from 2.4 kbps (kilo bits per second) up to 307.2 kbps.

Independent of the use, dependent of the maximum required speed, HDLC could be delivered as two different products serving the same functions as observed in the external device (modem line, connected computer).

–	ND No. 723:	CPU controlled input/output transfer (PIO) Maximum speed 19.2 kbps
–	ND No. 720:	Direct Memory Access (DMA) transfer including a DMA controller Maximum speed 307.2 kbps

I.2 HDLC CONFIGURATION, ND No.720 AND ND No.723

HDLC may consist of two modules both located in the I/O rack.

- 1181 HDLC DATA (ND No. 723)
- 1151 HDLC DMA CONTROL

} ND No. 720

Physical configuration in I/O-rack given in Appendix A1.

I.2.1 *HDLC I/O INTERFACE ND No. 723 MODULE 1181*

The DATA module may be used as an ordinary Programmed Input/Output (PIO) interface.

The data flow will be as indicated in Figure I.2.1.

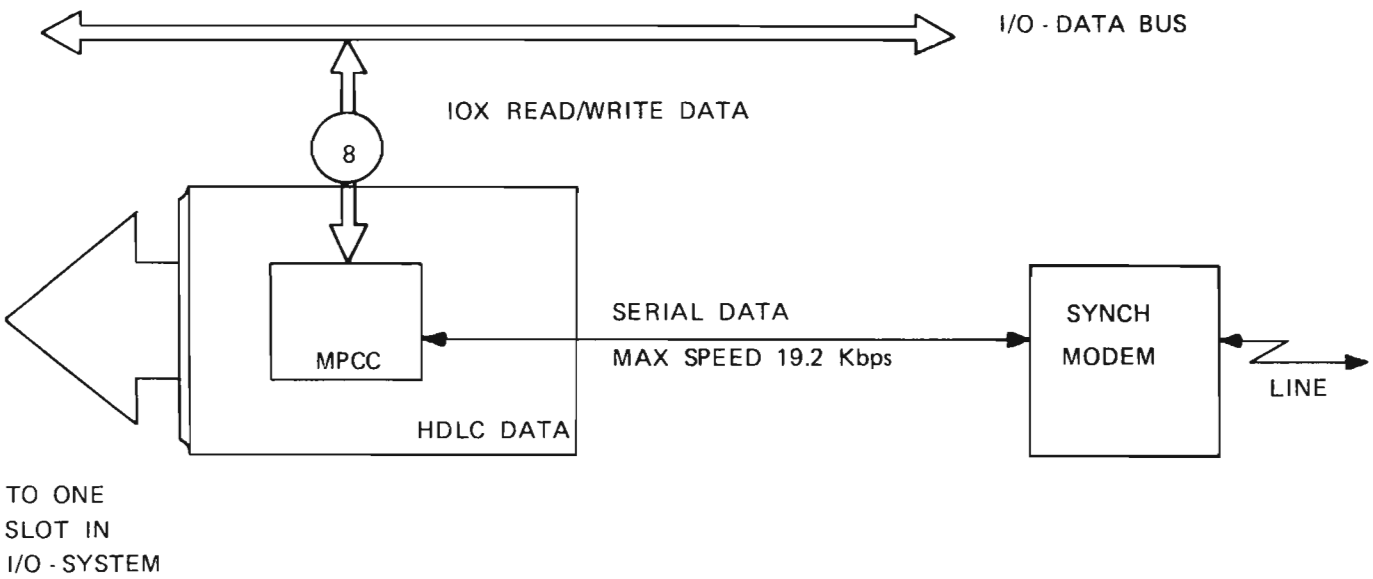


Figure I.2.1: ND No. 723 DATA FLOW

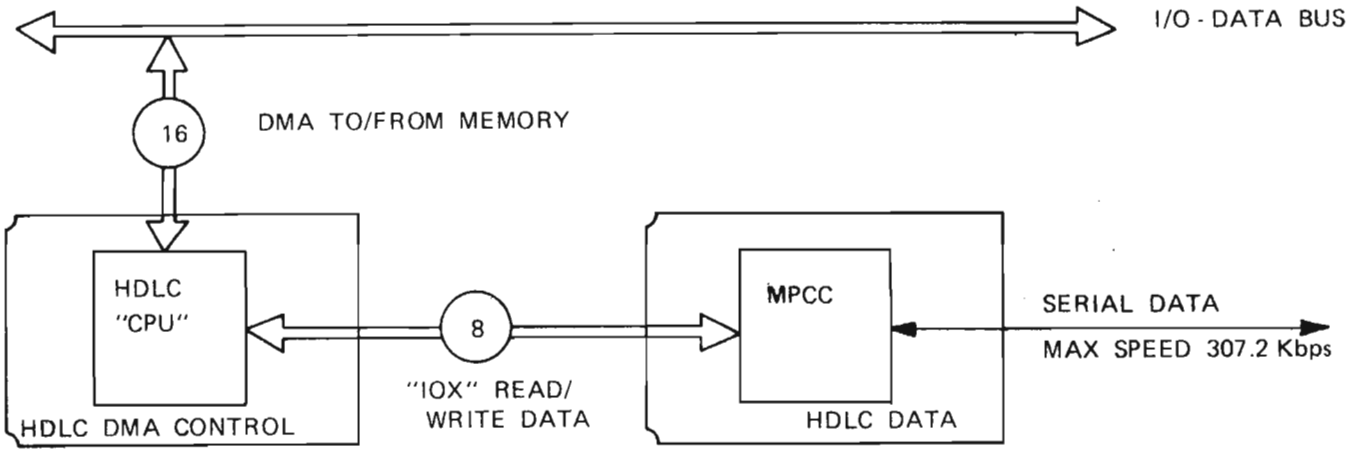
I.2.2 *HDLC INTERFACE (DMA) ND No. 720 MODULES 1181 AND 1151*

As indicated in Figure I.2.1, the maximum speed when using HDLC DATA alone is 19.2 kbps due to heavy CPU load on programmed input/output transfers. In order to increase speed and reduce CPU load to a minimum, the HDLC DMA CONTROL module (1151) could be used together with the DATA module.

The two modules are connected with special wiring in the plug field in the I/O-rack and occupy two slots in the I/O system.

HDLC DMA CONTROL and HDLC DATA working together allows DMA transfer of data from computer memory to the line and vice versa at a maximum speed of 307.2 kbps.

The data flow is shown in Figure I.2.2.



ND No. 720 occupies two slots in I/O - System

Figure I.2.2: ND No. 720 DATA FLOW

I.3 HDLC INTERFACE VERSUS COMMUNICATION STANDARDS

I.3.1 *INTRODUCTION*

As a communication adaptor HDLC contains more communication standards implemented in hardware than any other designed at NORSK DATA. This is a consequence of advances in integrated circuit technology and international standardization work.

All hardware related to communication standards is designed on HDLC DATA. That means that there is no difference between ND No. 720 (DMA version) and ND No. 723 (PIO version) observed from the network. The difference is seen on the CPU load. (See Functional Description Part II).

I.3.2 *STANDARDS*

The involvement of two or more users and equipment from more than one manufacturer in data communication systems gives an increased need of a compatible method for connecting all of it together, an interface protocol.

These protocols may be divided into levels (See Figure I.3.1.)

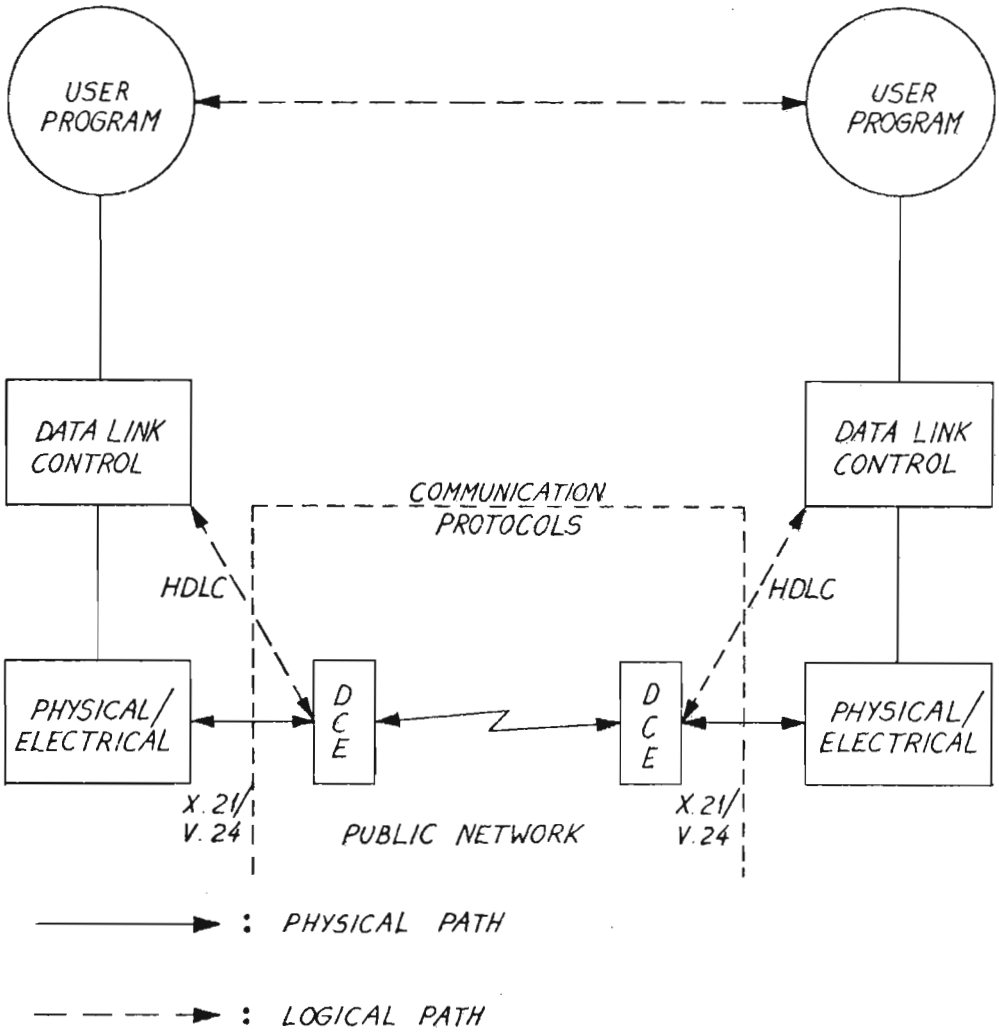


Figure I.3.1: INTERFACE STANDARDS

I.3.2.1 *Hardware Protocols (Electrical and Mechanical Standards)*

These interfaces apply to the physical connection between user equipment (DTE) and data communication equipment (DCE,modem).

Possible interface standards are as follows:

a) — CCITT V.24/V.28 and EIA RS-232c

— V.35 (wide band transmission)

For connection to the telephone network

b) — CCITT X.21 bis (V.28 signal levels)

— X.21 (X.27 signal levels)

For connection to the public data network

I.3.2.2 *Data Link Control Procedures (Link Access Procedures, LAP)*

These protocols which have the purpose of controlling the exchange of data are again divided up into the following levels:

— Frame format standards

— Communication procedures

I.3.2.2.1 Frame Format Standards

Most existing communication procedures transport data in blocks. However, each communication procedure (Byte Control Procedures - BCP) has its own block format, i.e., its own way of signaling "start of block", "end of block", checksum, etc.

One of the first steps in communication standardization is the definition of a uniform transmission format to be used for data and control information.

A transmission block is called a *frame* and a frame contains beginning and ending markers, control information, optional data and a checksum.

The internationally accepted HDLC frame format is fully defined in ISO IS3309.2 standard. This procedure allows full bit sequency transparent data transmission and is referred to as a Bit Oriented Procedure (BOP) (See Section 3.3).

At frame level HDLC (High Level Data Link Control) is fully compatible with SDLC (Synchronous Data Link Control) and with ADCCP (Advanced Data Communication Control Procedure).

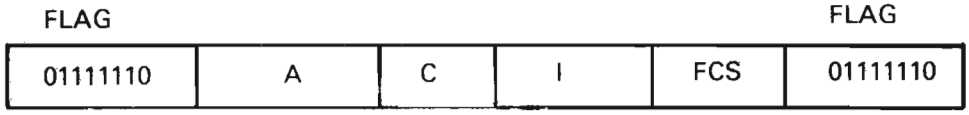
I.3.2.2.2 Communication Procedures

The standardization of communication procedures is not as easy as the standardization of a frame format. However, new standard procedures are emerging. SDLC procedures have existed for some time, HDLC procedures are being defined by CCITT and the X25 recommendation describes a procedure to be used in public packet switching networks.

All the new procedures will, however, use the HDLC frame format.

I.3.3 *HDLC FRAME FORMAT*

The HDLC frame format is depicted below.



The frame consists of:

1. A special bit sequence call, "flag", that marks the beginning of the frame. The end of the frame is also marked by such a flag.

   The flag sequence consists of one zero bit, six one-bits and a zero bit.

   The contents of the frame between the opening and the closing flag shall not contain a flag sequence. To guarantee this, the transmitter inserts an extra zero-bit following five consecutive one-bits. These inserted zero-bits are removed by the receiver. These extra bits are called "transparency bits".

2. An 8-bit byte called Address-Byte

   This field is meant as a station address, but the contents or use are not prescribed in the frame standard.

3. An 8-bit byte called Control-Byte

   This field is intended for link management information, but the frame standard does not describe its use or contents.

4. An Information field

   The information field may be any length, and may also be absent. The contents of the information field are not prescribed.

5. A 16-bit Frame Check Sequence (FCS)

   This field contains a 16-bit Cyclic Redundancy Check computed over the bits between the last bit of the opening flag and the first bit of FCS.

   Transparency bits are removed before the FCS is computed.

6. The closing flag that signals frame end

   The closing flag of one frame may be identical to the opening flag of the next frame.

Frame Size:

A valid frame shall contain at least 48 bits (Flag A, C, FCS).

There is no prescribed upper limit to the frame size. However, frame size is limited by the properties of transmission channels and the 16-bit FCS computation.

I.3.4 *STANDARDS IMPLEMENTED ON HDLC INTERFACE*

On HDLC DATA the following communication standards are hardware implemented.

I.3.4.1 *Electrical and Mechanical*

Strap selectable:

- V.24/V.28,RS-232C
- V.35

→ Telephone Network (V.series modem)

- X.21-bis (V.28-signal levels)

or

- X.21 (X.27 signal levels)

→ public data network

I.3.4.2 *Communication Protocols*

Selectable From Program:

- Byte Oriented Procedures

  Including automatic SYN character detection/generation

- Bit Oriented Procedures (BOP); HDLC (ISO-IS 3309), SDLC (IBM), ADCCP (ANSI) including:
  - automatic bit stuffing/stripping
  - automatic frame character detection/generation
  - valid frame protection
  - residue handling
  - selectable:
    - byte length 1-8 bits
    - error checking CRC (CRC-16, CCITT-0, CCITT-1)
      NONE
    - primary/secondary address mode
    - idle mode
    - point to point, multi-drop, loop configuration

I.3.4.3 *Transmitting and Receiving Frames in Accordance With HDLC Frame Format Using HDLC Interface*

The reason for calling the interface HDLC is related to the fact that frames in accordance with HDLC frame format are generated automatically in hardware when activated from driver software.

TRANSMISSION

When transmitting, software only has to know what should be in the address, control and information field. Observed from the frame format, these fields could contain any user defined information.

In order to pack the information into HDLC frame format before transmitting it on the line, HDLC DATA (which handles the procedure) must be activated by some control signals.

The control function is to first give the command Transmit Start Of Message (TSOM, i.e. send opening flag) and when all information in the frame is transmitted give the command Transmit End Of Message (TEOM, i.e. send closing flag).

The Cyclic Redundancy Checksum (CRC) is generated automatically and put into the frame when command TEOM is given.

RECEIVING

When receiving HDLC DATA will give status on Received Start Of Message (RSOM, i.e. opening flag received) and Received End Of Message (REOM, i.e. end marker of the frame is received).

Then software knows that all information received between RSOM and REOM has the sequence; address, control, information and CRC; that means, in accordance with HDLC frame format.

Therefore, successful communication against the line is related to successful control of HDLC DATA.

In the data phase, that is:

- Load X bits bytes ($1 \leqslant X \leqslant 8$) on output
- Read X bits bytes ($1 \leqslant X \leqslant 8$) on input
- Control of frame formatting functions (TSOM, TEOM and RSOM, REOM)

This could be done by NORD 10/S (HDLC in PIO version ND No. 723) introducing some overhead or by the DMA module (HDLC DMA, ND No. 720) reducing overhead to a minimum (See Part II).

PART II
FUNCTIONAL DESCRIPTION

DETAILED CONTENTS

+ + +

II.1 INTRODUCTION

As mentioned HDLC INTERFACE may consist of the following two modules:

- HDLC DATA (PIO Version)
- HDLC DMA CONTROL

} DMA Version

HDLC DATA may be used alone as a Programmed Input/Output interface.

HDLC DMA CONTROL can *only* operate together with HDLC DATA.

II.2 HDLC DATA

The HDLC DATA module is designed after the same basic principles as other parallel to serial (output to line), serial to parallel (input from line) interfaces designed at NORSK DATA (See Figure II.2.1).

The module contains the following:

- a device identification part including switches for setting of DEVICE NO. and IDENT CODE
- receivers for local I/O-address bus and receivers/transmitters for local I/O-data bus
- a 40 pins LSI chip, the MultiProtocol Communication Controller - MPCC, which performs:
  - parallel to serial convertion on output data
  - serial to parallel convertion on input data
  - selectable protocol
    - byte oriented (BCP) including automatic generation/detection of SYN character. (Block formatting must be done by driver software)

      or

    - bit protocols (BOP): HDLC,SDLC,ADCCP including automatic frame format generation
      - automatic bit stuffing/stripping
      - automatic frame character detection/generation
      - valid frame protection
      - residue handling
      - selectable:
        - byte length 1-8 bits
        - error checking CRC (CRC-16,CCITT-0,CCITT-1)
          NONE
        - primary/secondary address mode
        - idle mode
        - point to point,multi-drop,loop configuration

  For detailed description of the MPCC see Appendix A2.

- line adapter for connection to Data Communication Equipment (DCE, Modem) in accordance to standards

  - V.24/V.28, RS 232c
  - V.35

  } telephone network

  OR

  - X.21 bis (V.28 signal levels) public data
  - X.21 (X.27 signal levels) network

  For detailed description of line connection, pin configurations etc., see Appendix A3.

- special timing circuitry for inter-computer link connection, see also Appendix A3.

In addition HDLC DATA contains circuitry for connection to the DMA CONTROL module.

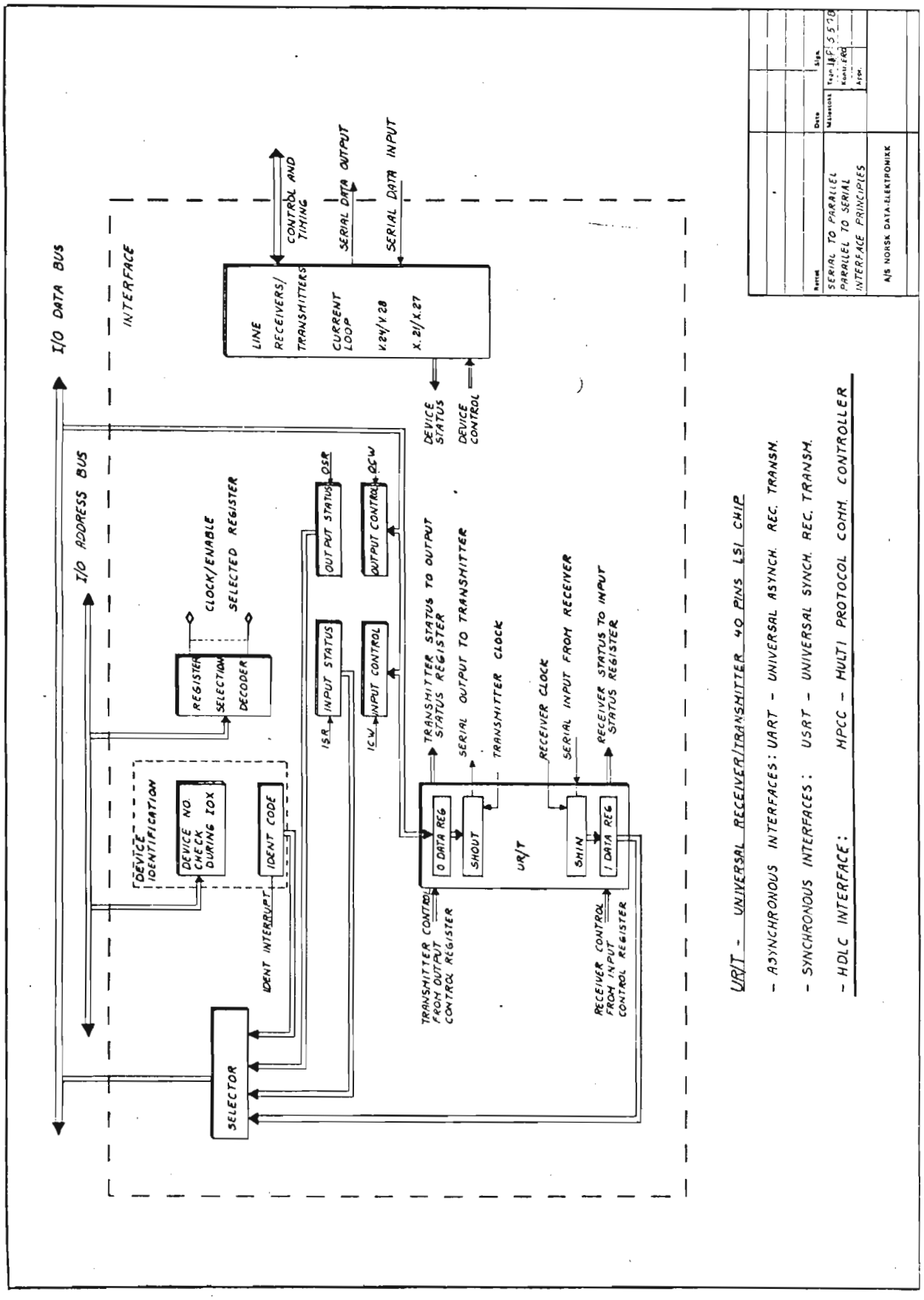


Figure II.2.1:SERIAL TO PARALLEL, PARALLEL TO SERIAL INTERFACE PRINCIPLES

The DMA module contains a microprocessor to control the data transfer to/from computer memory and HDLC DATA.

Therefore, HDLC DATA, in fact is designed to interface two processors:

— The NORD 10/S CPU (through standard I/O-system)

— The processor on the DMA module (through special inter-module connection; see Appendix A4)

Observed from the DATA module it makes no difference what processor is active.

That means that the control of HDLC DATA could be done either by NORD 10/S or the DMA processor.

The most effective solution of course is to leave the input/output handling to the DMA processor. Then NORD 10/S CPU will have more time for data processing which is the computers purpose.

II.2.1 *CONTROL OF HDLC DATA*

As mentioned in PART I, Section 3.4.3, successful communication between line and computer is related to successful control of HDLC DATA.

Including input and output data register there are 12 eight bits registers to control the DATA module. All registers could be accessed by IOX instructions (IOX<device no.> + $0\text{-}13_8$).

Instructions $0\text{-}7_8$ operate directly on 8 eight bits registers internally in the MPCC.

The instructions $10_8\text{-}13_8$ operate on single line indicators to/from the MPCC, interrupt enabling and modem status information. See Figure II.2.2 and the following description.

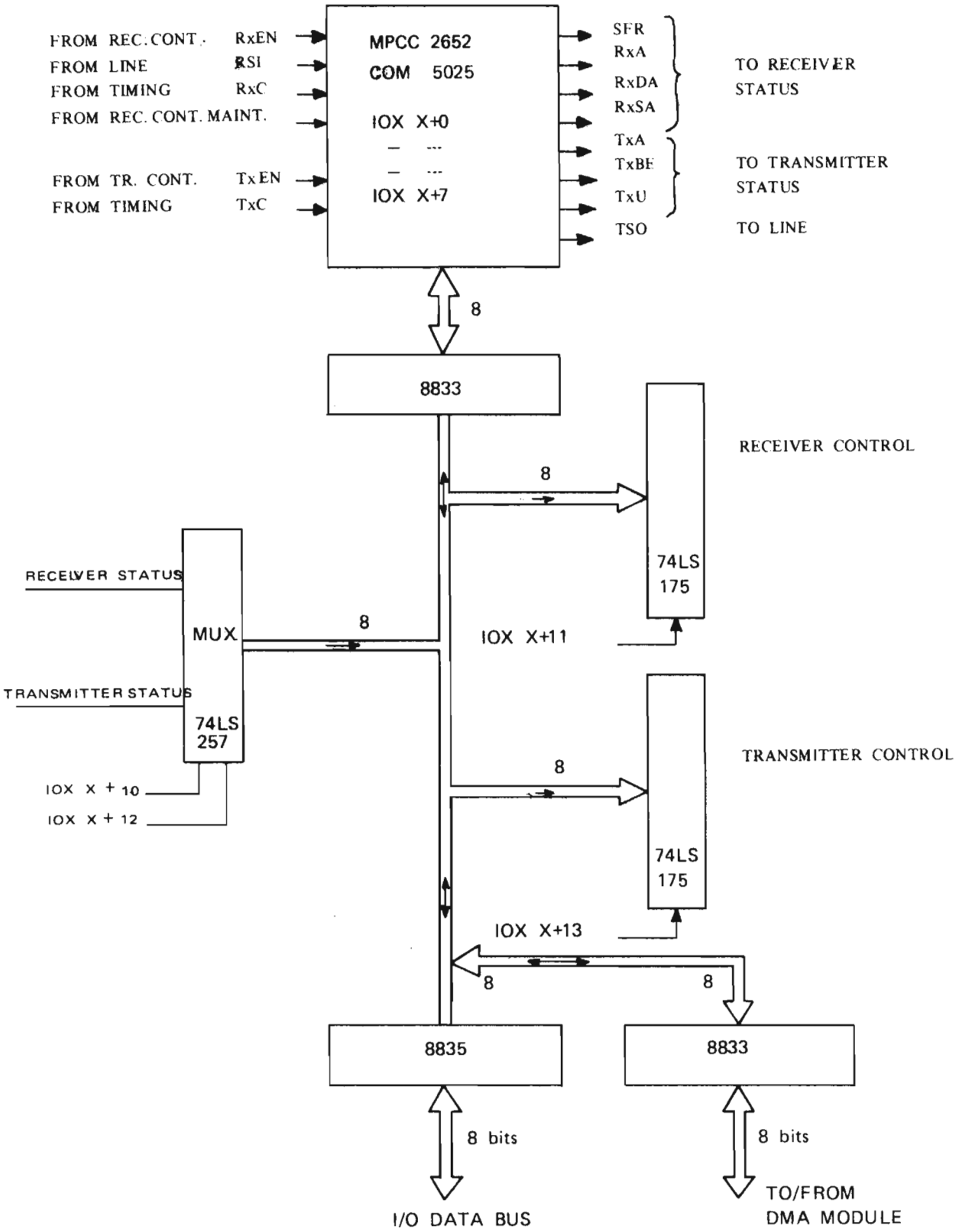


Figure II.2.2: HDLC DATA – BLOCK DIAGRAM

There are five registers related to the output channel, four registers related to the input channel and three registers common for operation mode control.

II.2.1.1 *Initialization of HDLC DATA, i.e. Loading of Mode Selection Registers*

Before enabling input/output transfers to HDLC DATA the module has to be initialized. That means after a MASTER CLEAR or DEVICE CLEAR, to load the mode selection registers.

The mode selection register is held internally in the MPCC to control the operation mode of the chip.

Remember that the MPCC performs the necessary frame formatting functions. Therefore, both a local and remote HDLC interface should be put in the same mode of operation given in the mode registers.

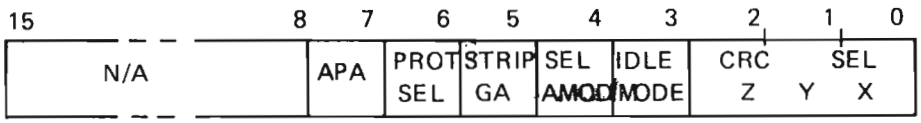
Loading of the mode registers is performed by IOX <device no.> + 1,3,4.

The format and function of the registers is given below:

IOX <DEVICE NO.> + 1

WRITE PARAMETER CONTROL REGISTER (PCR)

FORMAT:



BIT 0-2 ERROR CHECK SELECTION

0-2	*CRC SEL*	*BOP BCP*	*Error Control Mode*	*2*	*1*	*0*	*Mode*	*Char. Length*
			CRC-CCITT present to 1's	0	0	0	BOP	1-8
			CRC-CCITT present to 0's	0	0	1	BOP	1-8
			Not used	0	1	0	---	
			CRC-16 present to 0's	0	1	1	BCP	8
			VRC odd	1	0	0	BCP	5-7
			VRC even	1	0	1	BCP	5-7
			Not used	1	1	0	---	
			No error control	1	1	1	BCP	5-8

ECM should be loaded by the processor during initialization or when both data paths are idle.

BIT 3 IDLE MODE SELECTION

3	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE=0, transmit ABORT characters during underrun and when TABORT=1. IDLE=1, transmit FLAG characters during underrun and when TABORT=1.
		BCP	IDLE=0 transmit initial SYNC characters and underrun line fill characters from the S/AR. IDLE=1 transmit initial SYNC characters from TxDR (transmitter Data Register) and marks TxSO (transmitter serial output) during underrun.

BIT 4 SELECT SECONDARY ADDRESS MODE

Used in ring networks to select secondary station (remote site) dependent of received address compared with sync/address register (See IOX <device no.> 3).

4	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station. This facilitates automatic recognition of the received secondary station address. When transmitting, the processor must load the secondary address into TxDR (Output Data Register). SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received.

BIT 5 STRIP GO AHEAD/SYNC

Used in ring networks (BOP) to terminate message (frame).

5	SS/GA	BOP	Strip SYNC/Go Ahead. Operation depends on mode. For loop mode only. SS/GA=1 permits GA character to terminate a received message. When a GA is detected REOM and RAB/GA will be set and the processor should terminate the repeater function. SS/GA=0 permits only a FLAG or ABORT character to terminate a message.
		BCP	SS/GA=1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected. SYNC's in the middle of a message will not be stripped. SS/GA=0, presents any SYNC's after the initial two SYNC's to the processor.

BIT 6 PROTOCOL SELECTION

6	PROTO		Determines MPCC Protocol mode
		BOP	PROTO = 0 BOP
		BCP	PROTO = 1 BCP

BIT 7 ALL PARTIES ADDRESS

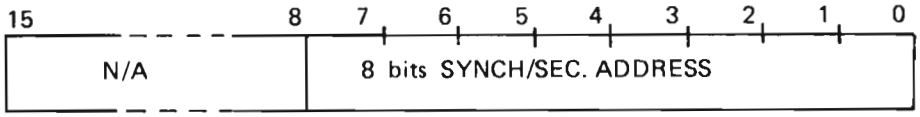
Used in ring networks to enable all connected computers as receivers, i.e. a broadcast function.

7	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address.

IOX <DEVICE NO.> + 3

WRITE SYNC/ADDRESS REGISTER (SAR)

FORMAT:

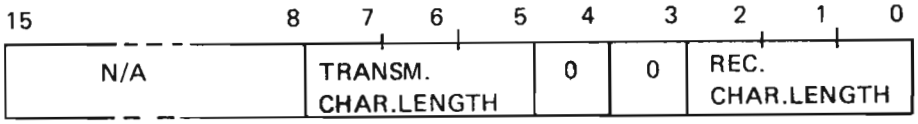


BIT	*NAME*	*MODE*	*FUNCTION*
00-07	S/AR	BOP	SYNC/ADDRESS Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register are compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor. It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL.

IOX <DEVICE NO.> + 4

WRITE CHARACTER LENGTH (CL)

FORMAT:



BIT	*NAME*	*MODE*	*FUNCTION*
08-10	RxCL	BOP/ BCP	
0-2			*2 1 0* — *Char.length (bits)* 0 0 0 — 8 0 0 1 — 1 0 1 0 — 2 0 1 1 — 3 1 0 0 — 4 1 0 1 — 5 1 1 0 — 6 1 1 1 — 7
5-7	TxCL	BOP/ BCP	Character bit length specification format is identical to RxCL.

II.2.1.2 *HDLC Data in the Data Phase*

After the initialization (See Section II.2.1.1), the DATA module is ready to be turned into the data phase.

As mentioned in Section II.2.1 there are five registers to control the transmitted (output) channel and four to control the receive (input) channel.

II.2.1.2.1 Receive (Input) Channel

The control of the input channel is used to:

- write receiver control word to enable the input transfer (interrupt enable, etc.)
- read receiver status register to check the transfer quality (valid data available, error, etc.)
- read x bit bytes ($1 \leqslant x \leqslant 8$) from input data register (see the following details)

The input channel on HDLC DATA is connected to interrupt level 13 (normally input is connected to level 12).

This is done in order to reduce possibility of receiver overrun at high transfer rates.

RECEIVER TRANSFER CONTROL REGISTER

Receiver control word is loaded by IOX <device no.> + 11.

Format and description of the bits are given in the programming specifications (See Appendix A5).

Special attention is drawn to control word bits 0, 1, 3, 4 and 7. Remember that HDLC DATA is designed to meet two processors.

The above mentioned bits decide what processor should be active controlling the input channel.

CASE 1 DMA Module Not Installed

Bit 3 and 4 in input control word should be "0" disabling the connection to the DMA module.

Bit 0, 1 and 7 should be "1" enabling changes on the input channel to be reported to NORD 10/S through interrupt on level 13.

The three following different "changes" can appear at the input channel:

- Receiver Data Available (RxDA)
  signifies that input data register contains a valid data byte to be read
- Receiver Status Available (RxSA)
  coming from MPCC indicating a change in status has occured. Further information is found by reading MPCC status register (See IOX <device no. > + 2)
- Modem Status Change (RMSC)
  signifies status change on the line

All "changes" mentioned will interrupt NORD 10/S to level 13. See Figure II.2.3 for illustration and Figure II.2.4 for details from HDLC DATA.

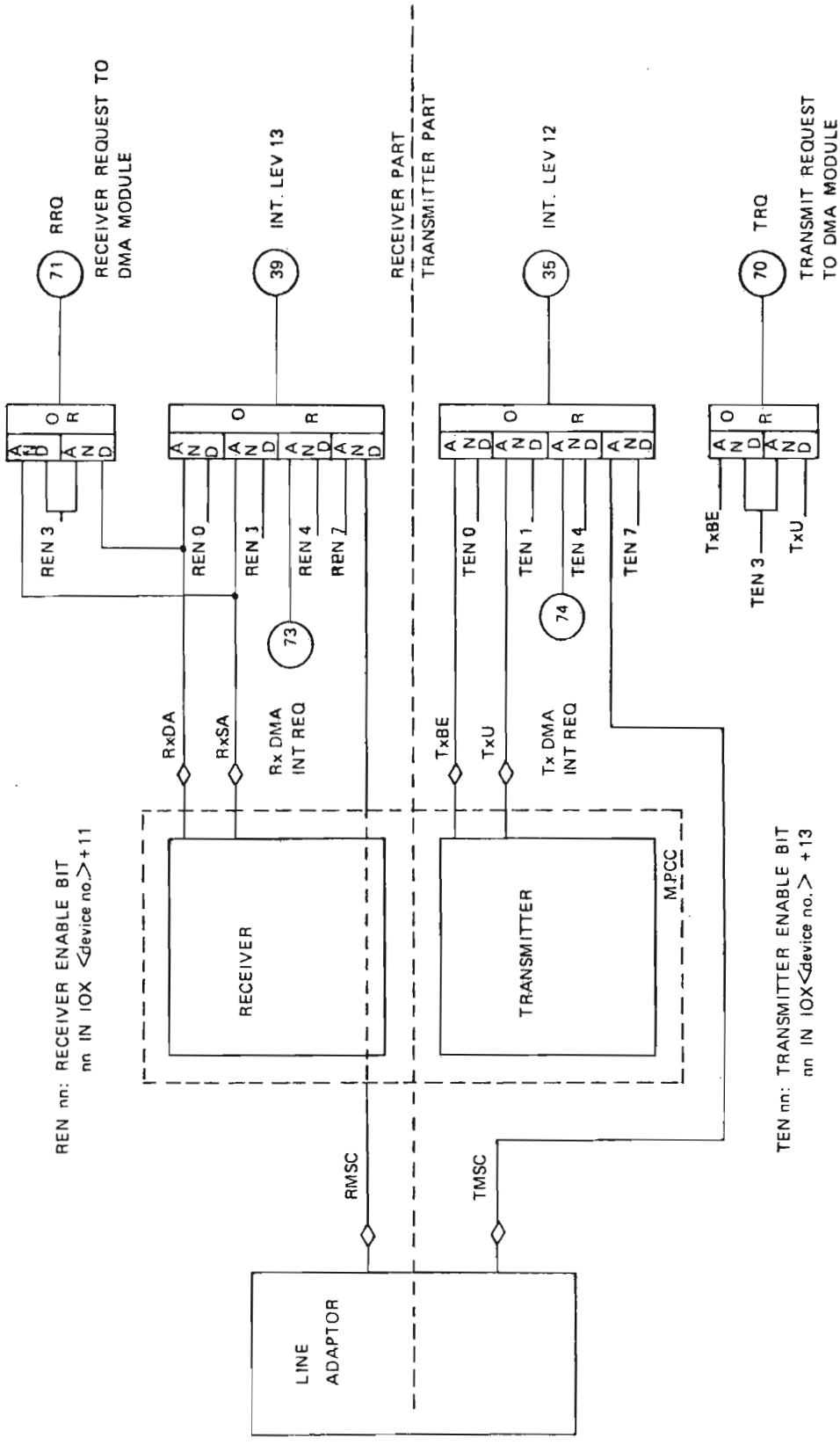


Figure II.2.3: HDLC DATA RECEIVER/TRANSMITTER CONTROL SIGNALS

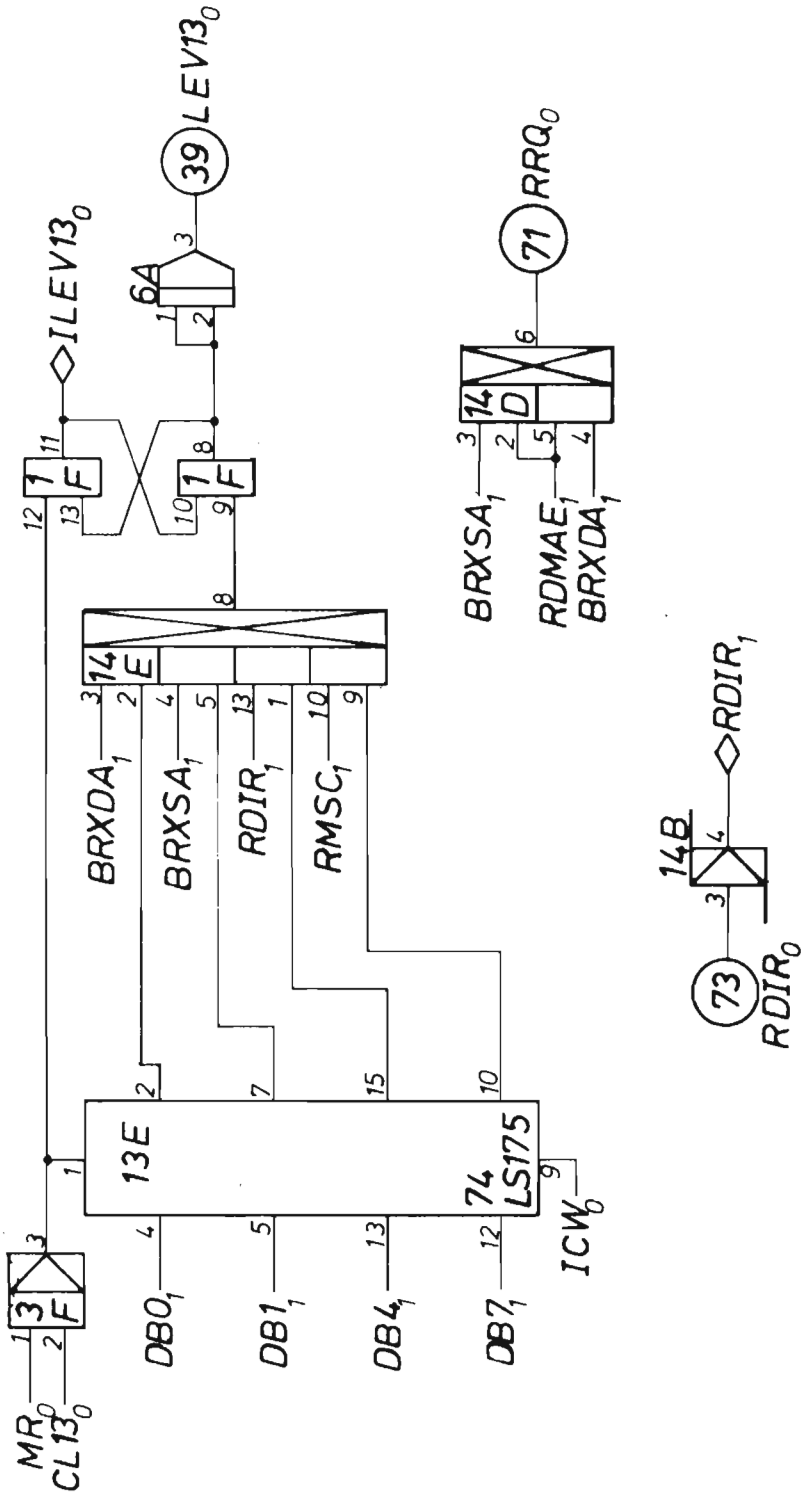


Figure II.2.4: HDLC DATA. DETAILS FROM MODULE

CASE 2 DMA Module Installed

Refer to Figure II.2.3. The idea is that NORD-10/S should not be disturbed by RxDA and RxSA, thus being interrupted for every received character/status. (This effect is illustrated in the following example).

This is done by disabling interrupt generation on RxDA and RxSA. That means, setting bit 0-1 in input control word to zero. Instead RxDA and RxSA is routed to the DMA processor as a Receiver Request (RRQ). That is accomplished by turning bit 3 on.

Then the DMA processor will read input status and data. The DMA module may have information to NORD 10/S (driver-software) related to the input transfer.

The DMA processor then generates a Receiver DMA Interrupt Request (RDIR) which gives interrupt on level 13 (enabled for in ICW bit 4).

Status change on the line (RMSC) is always reported directly to NORD 10/S.

EXAMPLE:

- Transfer RATE 19200 bits per second
- 8 bits per character
- Characters per second: 19200/8 = 2400 ^{ch}/s

That means 2400 interrupts to handle every second just to the input channel.

RECEIVE STATUS REGISTERS

It should be noted that HDLC contains two status registers for the input channel.

One of the registers is held internally in the MPCC. This register is accessed by IOX <device no.> + 2 and contains information about the frame formatting functions (See description below).

The other status register (Receiver Transfer Status) holds information about line status, feedback from the control register and single line status from the MPCC. This register is accessed by IOX <device no.> + 10 and is described in the programming specifications (See Appendix A5).

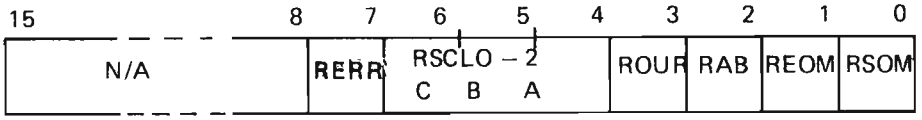
IOX <DEVICE NO.> + 2

READ RECEIVER STATUS – RxSR (FRAME INFORMATION)

This register is dynamically set and located internally in the MPCC. A change in the register will activate RxSA which is reset when the status is read.

The format of the register and description of the bits is given below.

FORMAT:

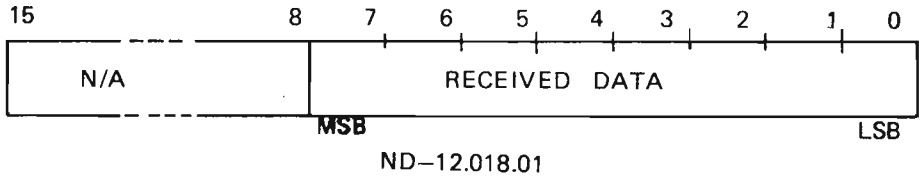


Bit	*Name*	*Mode*	*Function*
0	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
1	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading RSR (Receive Status Register) reset operation, or dropping of RxE.
2	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1. RAB/GA is cleared on reading RxSR operation or dropping of RxE. A received ABORT inhibits RxDA.
3	ROR	BOP/ BCP	Receiver Overrun = 1 indicates the processor has not read the last character in the RxDR (Receiver Data Register) within one character time. Subsequent characters will be lost. ROR is cleared on reading RSR, reset operation, or dropping or RxE (receiver enable).
4-6	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by WCLR (write character length register bit 0-2). Otherwise ABC = number of bits in the last data character. ABC is cleared when $RDSR_A$ is read, reset operation, or dropping RxE.
7	RERR		Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC.
		BOP	CRC-CCITT preset to 1's should be specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ FOB8) RERR = 0 indicates FCS received correctly (CRC = FOB8)
		BCP	CRC-16 preset 0's on 8-bit data characters specified by $PCSAR_{8-10}$: RERR = 1 indicates CRC-16 received correctly (CRC-0) RERR = 0 indicates CRC-16 error (CRC ≠ 0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct

IOX <DEVICE NO.> + 0

READ RECEIVER DATA REGISTER (RxDR)

FORMAT:



ND–12.018.01

II.2.1.2.2 Transmit (Output) Channel

The control of the output channel is to:

- write x bits bytes ($1 \leqslant X \leqslant 8$) to output data register
- load transmitter control registers to control the frame formatting functions (MPCC) and activate the output transfer
- read transmitter status registers to check end of transfer and error indicators (transmitter underrun)

Details follows.

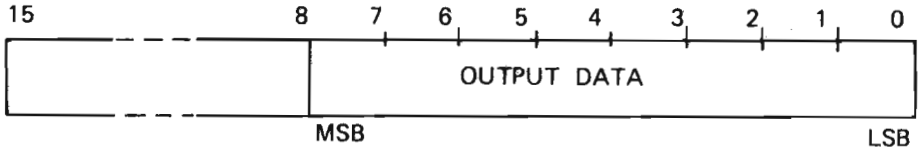
The output channel on HDLC DATA is connected to interrupt level 12 (normally output is connected to level 10). This is done to reduce the possibility of transmitter underrun at high tranfer rates.

TRANSMITTER DATA REGISTER (TxDR)

IOX <DEVICE NO.> + 5

This register is held internally in the transmitter part of the MPCC and loaded by IOX <device no.> + 5.

FORMAT:



TRANSMITTER CONTROL REGISTERS

There are two registers to control the transmit channel. One of the registers is loaded directly into the MPCC to control the frame formatting functions (See below).

The other control register (Transmitter Transfer Control Register – IOX <device no.> + 13) is used on the module and serves the same function for the output channel as the receiver control register for the input channel.

That is, to connect or disconnect NORD 10/S CPU or the DMA processor to the output channel of the DATA module.

The format and bit definitions are given in the programming specifications.

For a better understanding, refer to Figure II.2.3 and Figure II.2.5 for details from HDLC DATA.

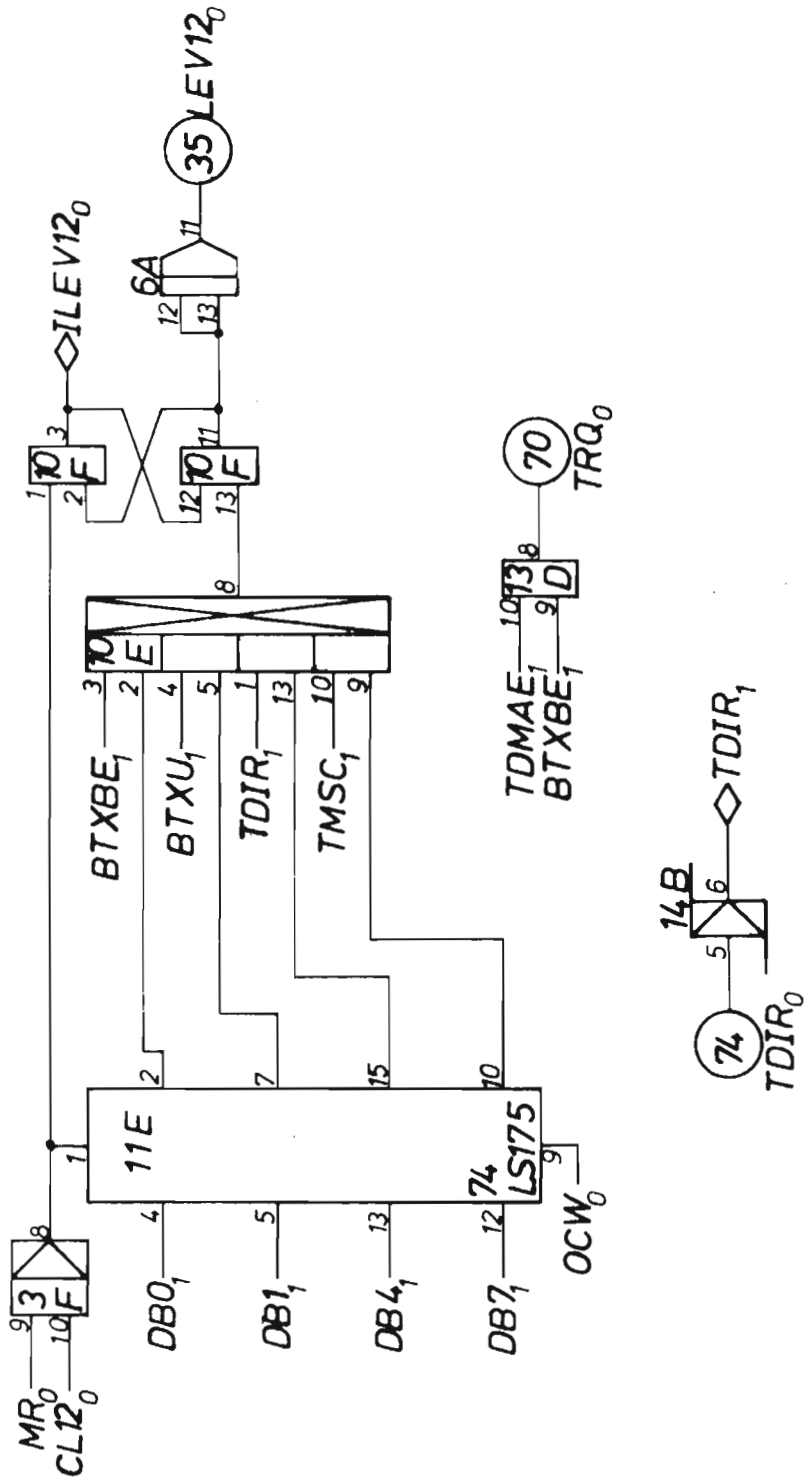


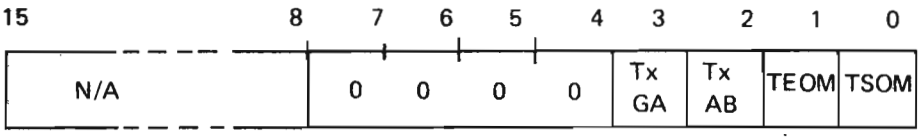
Figure II.2.5: HDLC Data, Details from Module

IOX<DEVICE NO.> + 7.

WRITE TRANSMITTER CONTROL REGISTER (TxCW)

In this register the frame formatting function on output data is controlled. By loading the MPCC with one of the four least significant bits set to one in this register, either an opening flag (TSOM), closing flag (TEOM), go-ahead, or abort character automatically will be transmitted on the line (See details below).

FORMAT:



Bit	*Name*	*Mode*	*Function*
0	TSOM		Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1.
		BOP	TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation begins. FCS, as specified by PCR_{0-2}, should be CRC-CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively. When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins.
1	TEOM	BOP	Transmit End of Message. Used to terminate a transmitted message when CRC error checking is used. TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from SAR_L or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
3	TABORT	BOP	Transmitter Abort = 1 will cause ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
4	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)

Bit 5-7: Not Used.

TRANSMITTER STATUS REGISTERS (TxSR)

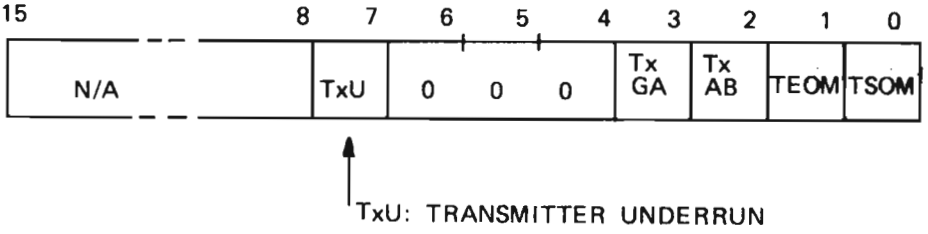
Feedback from the output channel is carried through two status-registers.

One of the registers is held internally in the MPCC and reached by:

IOX <device no.> + 6.

This register holds the copy of transmitter control register (IOX <device no.> + 7) except from bit 7 which signifies transmitter underrun. Transmitter underrun TxU will generate interrupt if enabled for.

FORMAT:



The other status register for the output channel contains information about line status and enabling done in output control register. The register (RECEIVER TRANSFER STATUS) is accessed by (IOX <device no.> + 12).

The format and bit definitions are given in the programming specifications.

II.3 HDLC DMA CONTROL

II.3.1 *INTRODUCTION*

In this chapter we will look at how the DMA module functions together with the DATA module and NORD 10/S.

We assume that the DATA module and DMA module are enabled to work together (See input/output transfer control words).

The DMA control is controlled by a microprocessor located on the module. The main functions of the processor are to:

ON INPUT

— read characters from HDLC DATA, group them into 16 bits words and place them in computer memory through Direct Memory Access (DMA)

— take care of status change in input channel

ON OUTPUT

— "DMA read" 16 bits words in computer memory, split them up into bytes transferred to output data register on the DATA module

— take care of status change in output channel

To do this the DMA processor has all IOX-instructions operating on the DATA module implemented in its microprogram.

NORD 10/S and the DMA processor communicates through a common memory area (the list structure).

NORD 10/S controls the DMA processor by means of commands given in IOX-instructions. The manner in which this is accomplished will be described in the following sections.

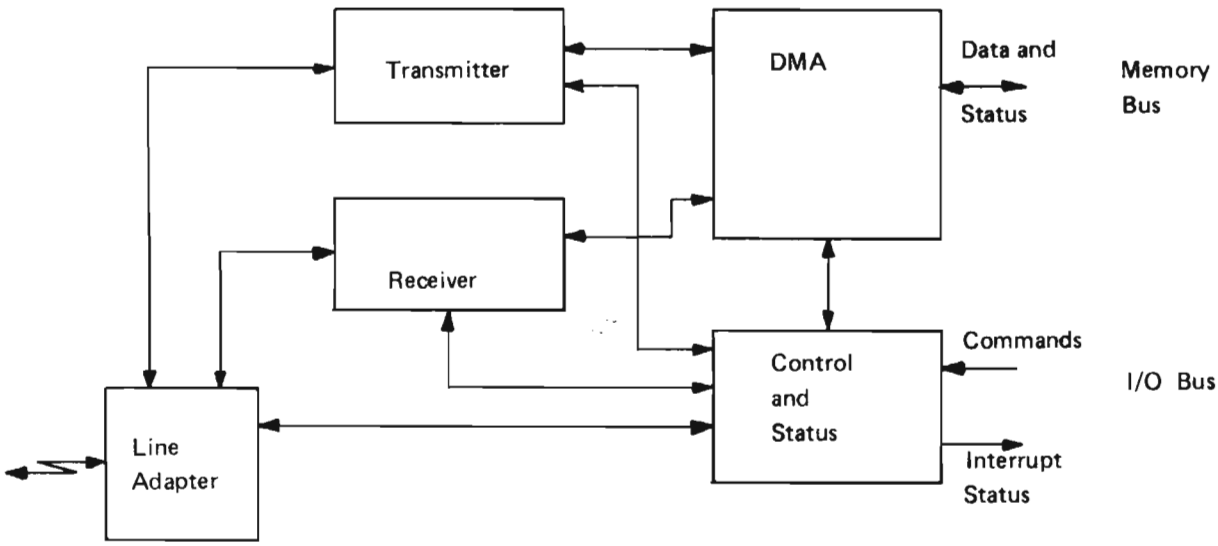


Figure II.3.1: BLOCK DIAGRAM OVER HDLC INTERFACE (DMA)

ND–12.018.01

II.3.2 *CONTROL OF THE DMA PROCESSOR (THE COMMANDS)*

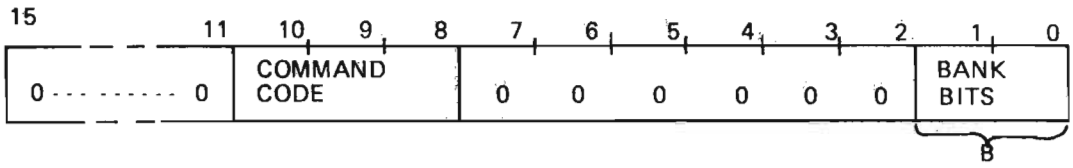
Driver software controls the HDLC INTERFACE by means of 8 different commands given in IOX-instructions. All commands (with the exception of DEVICE CLEAR) need an 18 bits physical memory address due to reasons explained in the following sections.

The 16 least significant bits of the address are transferred to the interface by IOX <device no.> + 15.

The most significant address bits (Bank bits) are given in IOX <device no.> + 17.

In the format of IOX <device no.> + 17, three bits are left to specify command no. (See format).

FORMAT:



IOX <DEVICE NO.> + 17

The commands may be divided up into the three following groups:

a)	INITIALIZATION		
	– DEVICE CLEAR	(0)	000040
	– INITIALIZE	(1)	00040B
b)	DATA TRANSFER		
	– RECEIVER START	(2)	00100B
	– RECEIVER CONTINUE	(3)	00140B
	– TRANSMITTER START	(4)	00200B
c)	MAINTENANCE		
	– DUMP DATA MODULE	(5)	00240B
	– DUMP REGISTERS	(6)	00300B
	– LOAD REGISTERS	(7)	00340B

II.3.2.1 *Initialization*

DEVICE CLEAR (Command 0)

Before operating HDLC INTERFACE (DMA), a DEVICE CLEAR should be performed to ensure safe operation.

Recommended program for Device Clear is:

```
SAA0                    % A reg. = 0
IOX GP + 11 (octal)     % Write Receiver Transfer Control
BSET ONE 50 DA          % A reg. = 40 (octal)
IOX GP + 11 (octal)     % Device Clear to Data Module
IOX GP + 17 (octal)     % Device Clear to DMA Module
```

The Device Clear sequence as described above will stop all data transfers to and from the interface, and it can be used anytime. Device Clear will clear all interrupts from the interface, and a dialed up modem connection will be broken.

INITIALIZE (Command 1)

The command INITIALIZE should be used after a Device Clear.

The command will initialize the DATA module (See Section II.2.1.1) and load the DMA module with necessary parameters related to the DMA structure (see Section II.3.3).

To obtain the necessary information to perform the initialization; the command requires 7 locations in memory (parameter buffer).

These locations should be set by driver software prior to execution of the command.

The contents of the parameter buffer are:

1	Parameter Control Register	(IOX <device no.> + 1)
2	Sync/Address Register	(IOX <device no.> + 3)
3	Character Length	(IOX <device no.> + 4)
4	Displacement 1	
5	Displacement 2	
6	Max.Receiver Block Length	
7	Checksum	

The contents of the three first locations are written into the DATA module. The bit mapping of locations is described in Section II.2.1.1.

Displacement 1 is the number of free bytes reserved at the beginning of each buffer containing the start of a message (Frame). *Displacement 2* is the number of free bytes reserved at the beginning of each buffer which do not contain the start of a message (Frame). *Max. Receiver Block Length* is the total number of bytes in a receiver buffer, including displacement. Long frames may be divided into blocks and stored in two or more buffers.

The use of these parameters will be illustrated in the next section, i.e. data transfer.

The checksum is set to 0 by driver software and set to 102164 by the DMA processor when INITIALIZE is finished. The interface should not be used in DMA mode if this checksum is wrong.

When started the DMA processor with Direct Memory Access will read the parameter buffer. To accomplish this an address pointer to the parameter buffer is needed. The address is given in the start INITIALIZE sequence which consists of the following:

— LDA <least address>
% write DMA address
IOX <device no.> + 15

Write least address to HDLC INTERFACE

— LDA 00040B
% write DMA command register
IOX <device no.> + 17

Write most address and start INITIALIZE

Refer to Figure II.3.2 for illustration.

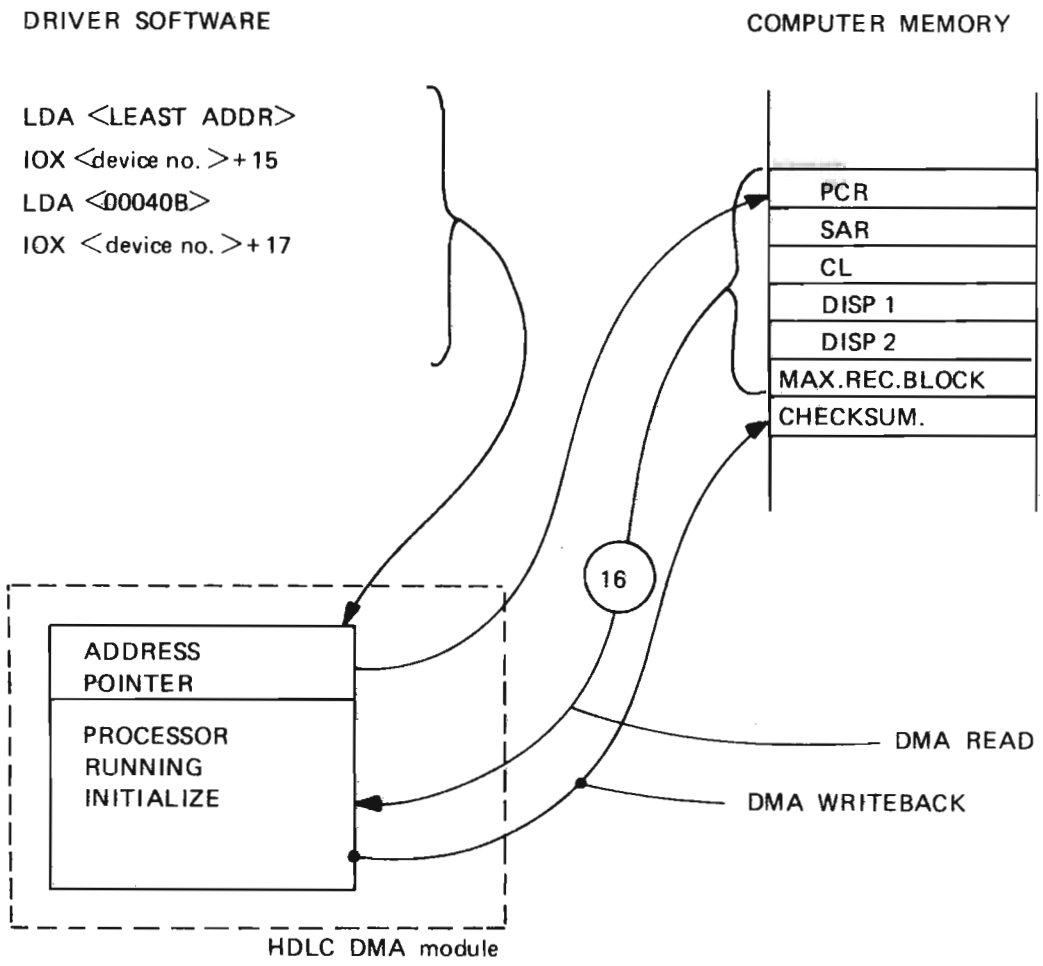


Figure II.3.2: COMMAND INITIALIZE ILLUSTRATION

II.3.2.2 *Data Transfer*

After initialization (See Section II.3.2.1) the commands:

RECEIVER START
RECEIVER CONTINUE
TRANSMITTER START

may be used.

Under this label only a description of how to use the command will be given. To understand how they operate, the reader is advised to study Section II.3.3 (HDLC DMA STRUCTURE).

RECEIVER START (Command 2)

The RECEIVER START command will as the name suggests, start the microprogrammed receiver on HDLC INTERFACE.

Three IOX-instructions are used to activate RECEIVER START.

LDA <least address>	Write 18 bits DMA
IOX <device no.> + 15	address to interface
LDA 00100B	and start Receiver
IOX <device no.> + 17	
LDA (3334	Enable receive channel
IOX <device no.> + 11	to DMA module. (See Appendix A5
	IOX <device no.> + 11)

The address written to the interface in a Receiver Start sequence is denoted a "List Pointer". This address is the first address of a list containing "Buffer Descriptors" (See HDLC DMA Structure). This command also selects Displacement 1 for the first buffer, and should therefore be used the first time the receiver is started after a power up or receiver disable.

The receiver should normally run. A Receiver Request from the DATA module will then automatically be handled.

RECEIVER CONTINUE (Command 3)

This command is used to write a new List Pointer to an enabled and working interface. It should only be used as a response to a "List Empty" interrupt.

TRANSMITTER START (Command 4)

This command is always used to start transmission of data. As for RECEIVER START, an address is written to the interface when the transmitter is started. To enable the transfer, the Transmitter Control register (IOX <device no.> + 13) has to be loaded.

II.3.2.3 *MAINTENANCE*

DUMP DATA MODULE (Command 5)

This command is mainly for maintenance purpose. It requires 5 locations in memory, where the contents of the following registers are stored:

1.	Parameter Control Register	(8 least sign. bits)
2.	Sync/Address Register	(8 least sign. bits)
3.	Character Length	(8 least sign. bits)
4.	Receiver Status Register	(8 least sign. bits, not accumulated)
5.	Transmitter Status Register	(8 least sign. bits, not accumulated)

The contents of the registers in the Multi Protocol Communication Controller (MPCC) are transferred to memory. The Receiver Status Register is also OR-ed into the Receiver Dataflow Status Register to prevent loss of information.

DUMP REGISTER (Command 6)

This command can be used to dump the contents of any number of the 256 random access memory registers in the DMA module. Required space in memory is 2 locations plus one location for each register to be dumped. The contents of the two locations are:

1. First Register Address
2. Number of Registers

If both values are zero, the contents of the 16 registers in the Bit Slice are written into memory.

The meaning of the different values is illustrated by the figure below.

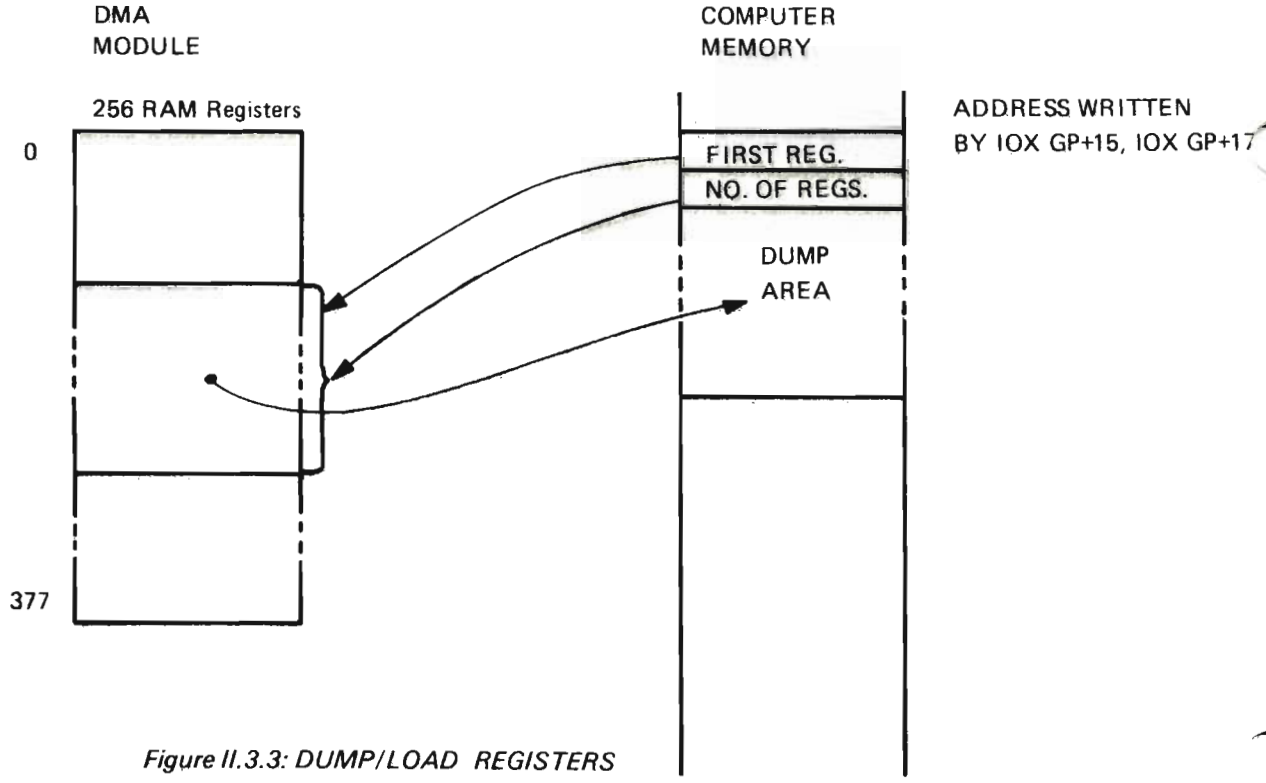


Figure II.3.3: DUMP/LOAD REGISTERS

LOAD REGISTER (Command 7)

This command can be used to load any number of the 256 random access memory registers in the DMA module. Required space in memory is 2 locations plus one location for each register to be loaded. The contents of the two locations are:

1. First register address
2. Number of Registers

The Load Register command is simular to Dump Register, except that data is moved in the opposite direction. It is not possible to load the registers in the Bit Slice by this command.

The commands, how to activate them and use them in some simple debugging programs are given in Appendix A5.

II.3.3 *HDLC DMA STRUCTURE*

The DMA structure is organized around lists which contain the necessary control and status information to connect "driver" software and DMA processor together.

The lists which reside in the computer memory could be accessed directly from driver software and through DMA requests to/from HDLC interface.

The receiver and the transmitter works from separate lists, with the same structure and format. The information exchange between driver software and DMA processor through the list structure provides dynamic allocation and linking of data buffers.

II.3.3.1 *The List Structure*

The list contains a number of entries of four words each. Each list entry describes a data block. In the receiver lists, each entry describes a receive data buffer where the received data is to be stored.

In the transmitter list, each entry describes a block of data that is to be transmitted.

The four words of each entry contain the following information:

WORD 1	Block status and key
WORD 2	Amount of information in the data block (Byte Count)
WORD 3–4	18 bits physical memory address of data block

More detailed description is given below.

II.3.3.1.1 Receiver List

In this section the operation of the receiver list is described.

After proper initialization (See Section II.3.2.1), the DMA processor is given a list pointer and the "RECEIVER START" command.

The liste pointer points to one of the entries in the receiver list (See Figure II.3.4).

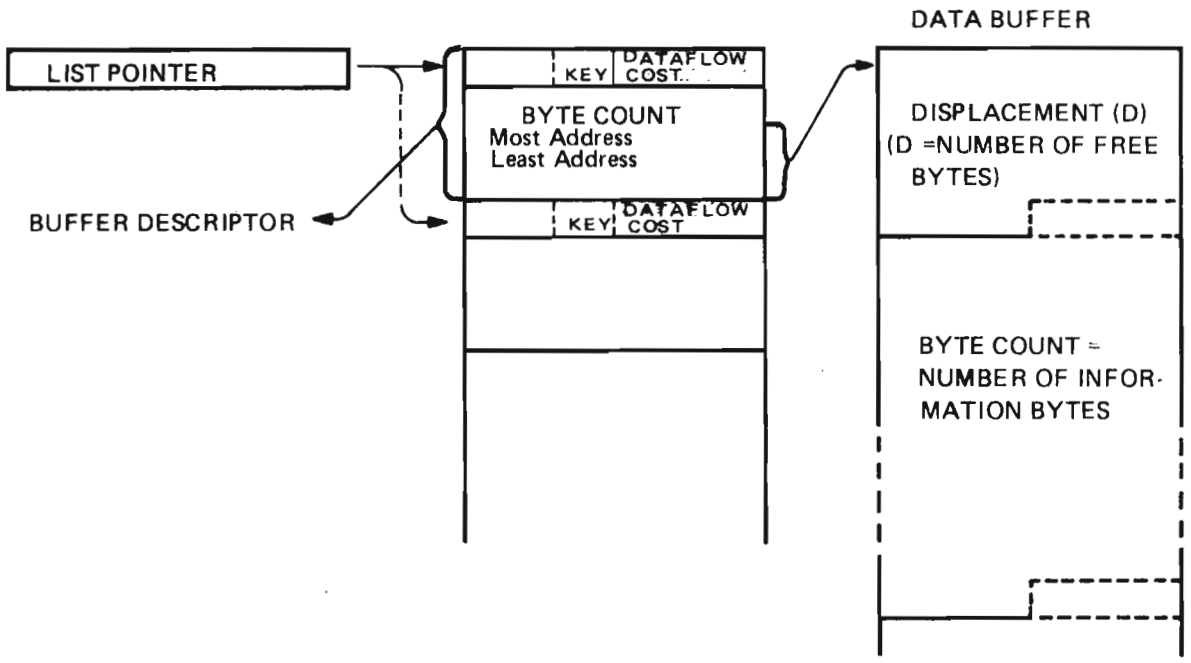
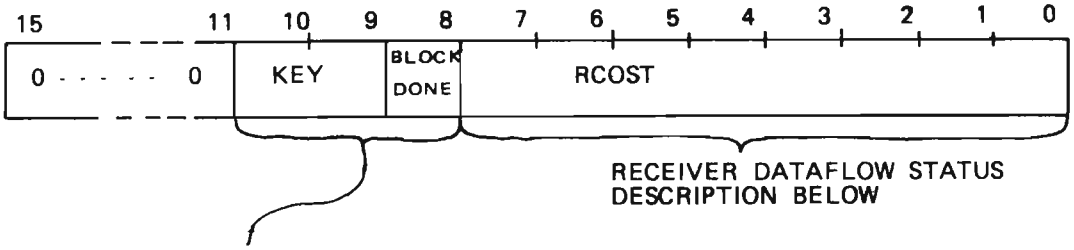


Figure II.3.4: LIST STRUCTURE

The DMA processor will now generate a DMA request using the list pointer as address and fetch the first entry from the list beginning with the status word.

FORMAT OF THE STATUS WORD



BITS	10	9	8	
	0	1	0	Empty Receiver Block
	0	1	1	Full Receiver Block
	1	0	0	Block to be Transmitted
	1	0	1	Already Transmitted Block
	1	1	0	New List Pointer

The status word should be all zero except for the key.

The BLOCK DONE bit signifies used block. That is, to prevent overwriting on input or duplicated transmission on output.

Legal keys for the receiver are 1000_8 (Bit 9 set) or 3000_8 (Bit 9 and 10 set).

CASE 1. Key is 1000_8

The key is legal saying empty receiver block. The DMA processor will now read the block address (word 3&4), add Displacement 1 and incoming data will be stored in the block.

When the block is filled (MAX.RECEIVER BLOCK) or the interface recognizes "frame end" (REOM), the DMA processor updates the list entry.

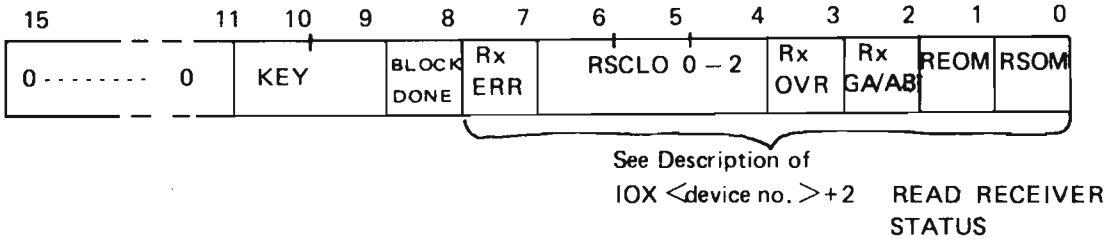
Updating the list entry includes updating the status word and writing the number of bytes received into the byte count.

Updating Status Word.

Updating the status word is to change the key and update RCOST.

The key is changed by setting the BLOCK DONE bit signifying Full Receiver Block.

Updating RCOST, let us first see what RCOST contains.



RCOST is identical to Receiver Status Register in the MPCC.

Suppose both bit 0 and 1 are set, that means the status word is updated to 1403_8. Then the list entry describes a Full Receiver Block which contains a whole frame because both RSOM and REOM are received within the block.

If only bit 0 is set (1401_8 in status word) the list entry describes a full receiver block which only contains the first part of a frame. That means that "MAX. RECEIVER BLOCK" was recognized before frame end (REOM). In other words, the frame contains more information than the receive block could store. In this case the DMA processor automatically will increment its list pointer by four and read next list entry describing next data buffer.

Suppose now that the new data block could store the last part of the frame. Than the status word of this list entry will be updated to 1402_8 signifiying full receive block and only closing flag received. This block change is accomplished fast enough to maintain continuous handling of incoming data. It is assumed possible to give BLOCK END interrupt (See Receive Transfer Control Register).

That means, when "driver" software should take care of the incoming information it looks at the status word of the list entries.

If status is 1403_8, it knows there are no errors and a whole frame of valid data is in the data block.

If status is 1401_8, it knows that the block contains the first part of a frame and the next list entry with status 1402_8 contains the last part.

This is illustrated in the receiver list illustrations (See Figures II.3.5, II.3.6, and II.3.7).

CASE 2. KEY is 3000_8

The key is legal, however it does not define a data block. Instead the list entry in word 3 and 4 contains the address to a new list.

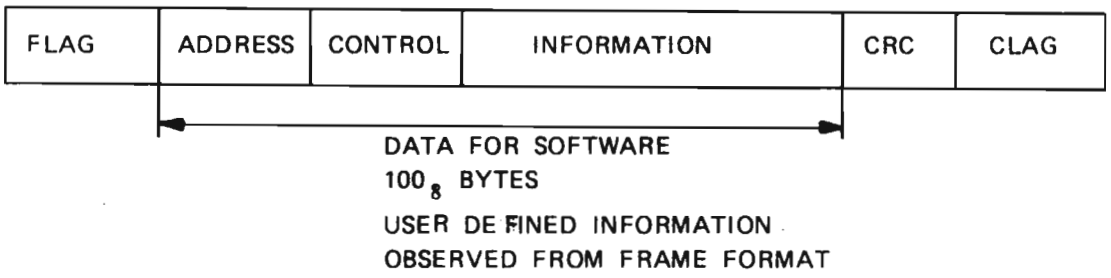
That means, word 3 and 4 are taken as a new list pointer and the receive procedure continues as in Case 1.

NOTE:

> If this list change occurs during input data, it takes too much time to maintain continuoùsly input handling. Therefore, this situation will give List End interrupt (See Receiver Transfer Control/Status registers).

RECEIVER LIST ILLUSTRATIONS.

Example: Frame Size.



Case 1. RECEIVER BLOCK SIZE: 1560 bytes

LIST STRUCTURE

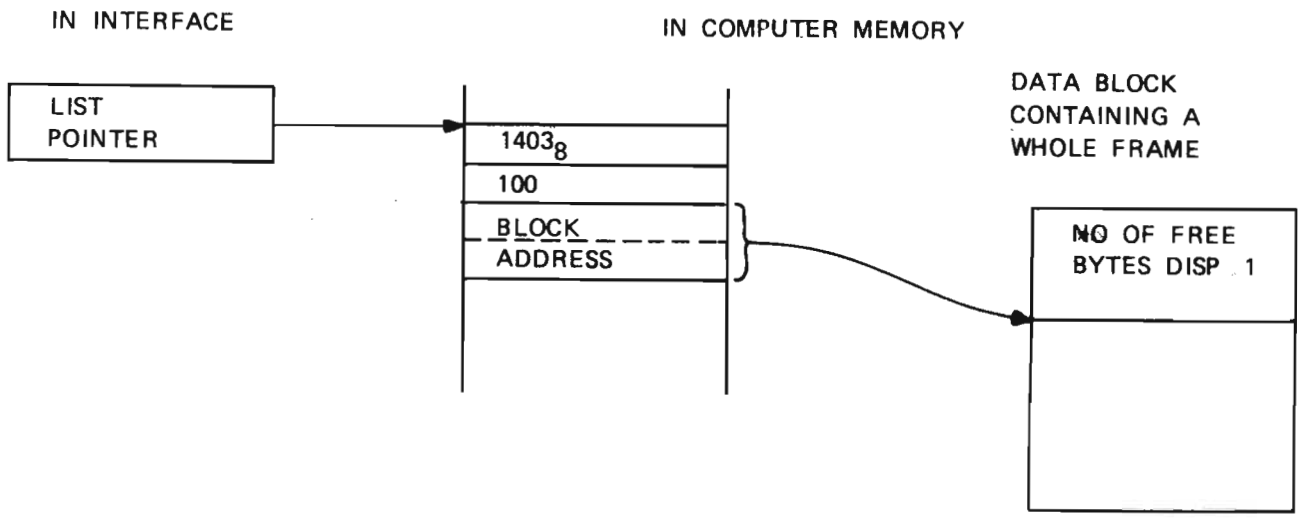


Figure 3.5: CASE 1 ILLUSTRATION

Case 1. RECEIVER BLOCK SIZE: 75 bytes

LIST STRUCTURE

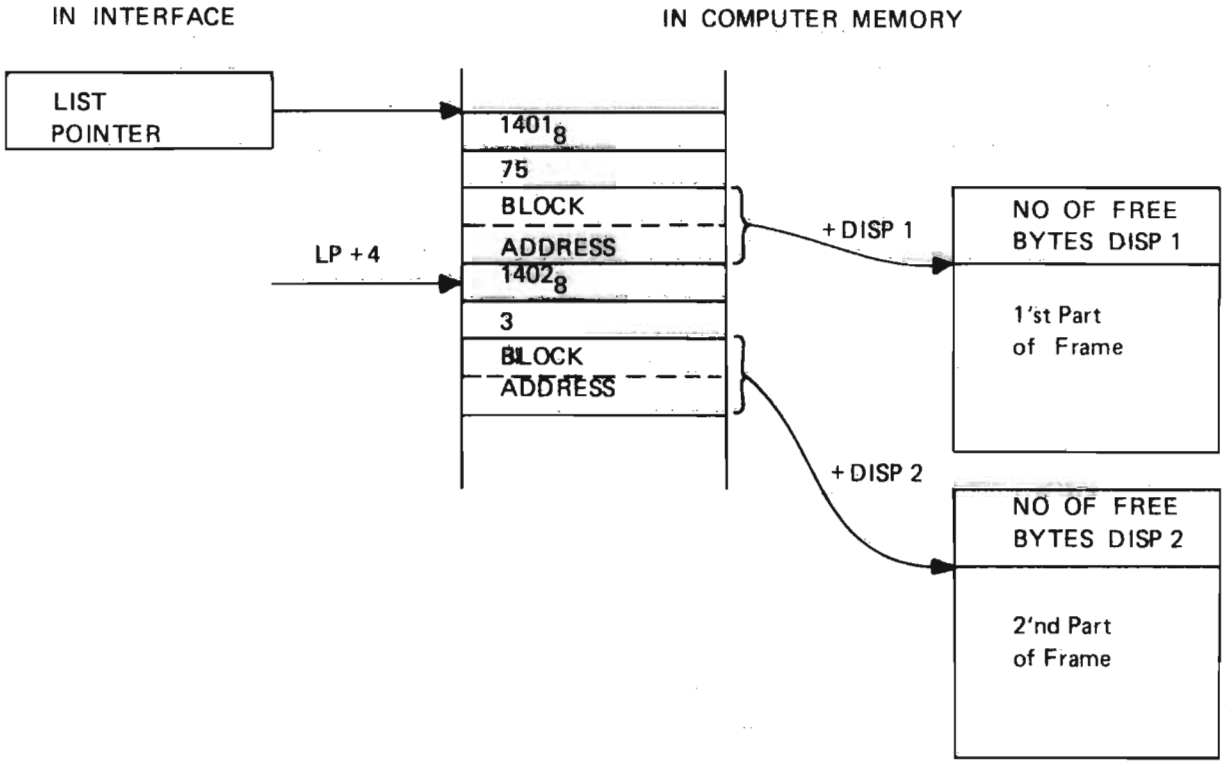


Figure 3.6: CASE 1 ILLUSTRATION

NOTE:

If a frame is stored in more than two data blocks "*middle*" blocks are marked by "not start of frame" and "not end of frame" (i.e. 1400_8).

The data stored in a receiver block is now "taken care of" by driver software which also resets the list entry of the block.

The resetting is to change the status word to "Empty Receiver Block", i.e. 1000_8 or 3000_8.

Typical use of data blocks and list entries is illustrated below.

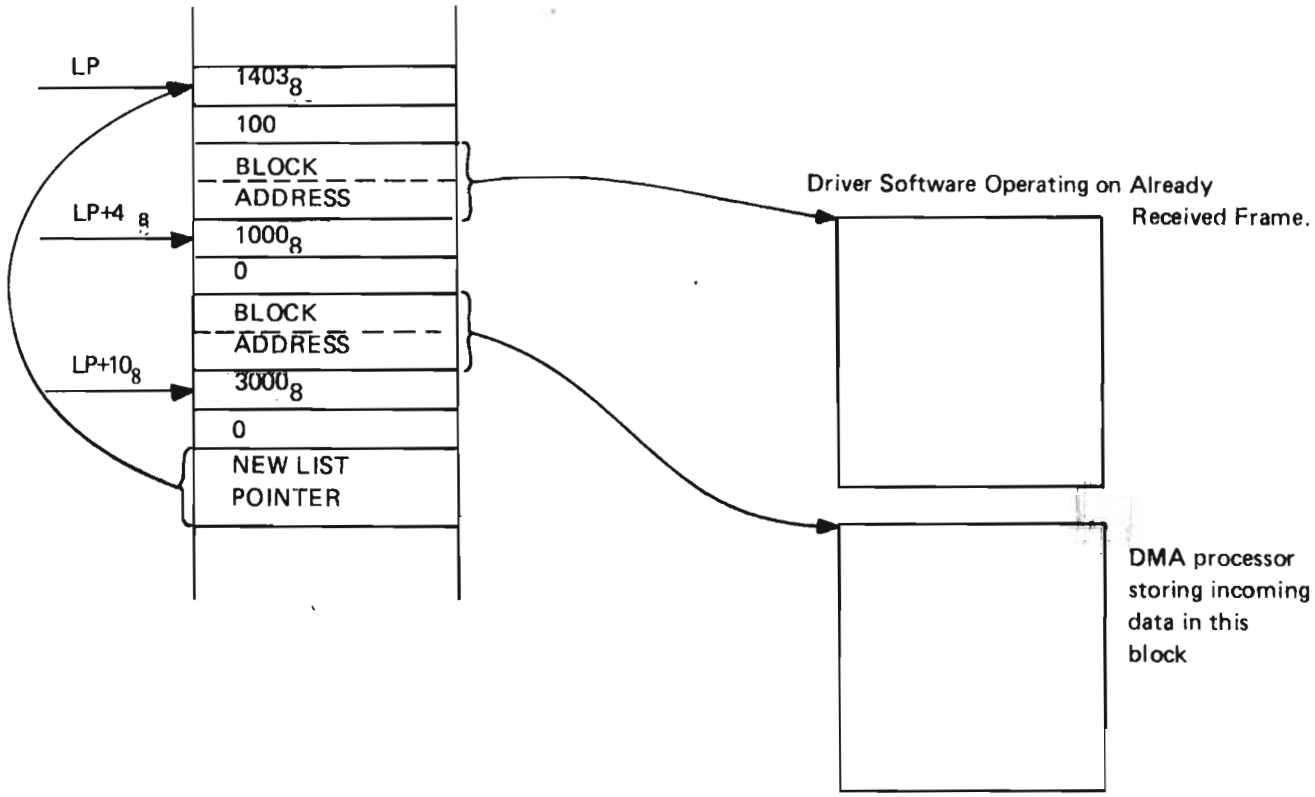


Figure II.3.7: TYPICAL LIST OPERATION

This looping in receiver list requires that driver software is fast enough to reset the list entries. If the DMA processor reaches the NEW LIST POINTER and than Full Receiver Block, a LIST EMPTY interrupt is generated. (See Receiver Transfer Status Register).

II.3.3.1.2 Transmitter List

The transmitter list is identical in structure to the receive list.

After initialization, the DMA processor is given a list pointer and the "TRANSMITTER START" command. The DMA processor will than process the transmitter list entries as described in Section II.3.3.1.1.

Note the following differences:

The transmitter list is updated by driver software and describes blocks of data to be transmitted.

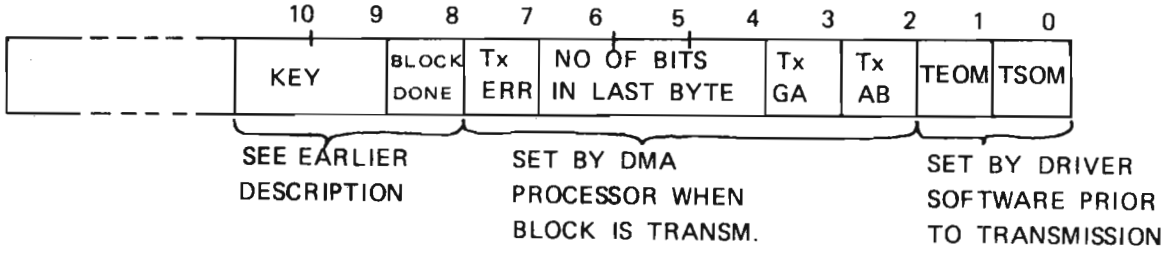
The DMA processor outputs data and sets the Block Done bit in the list entry signifying Already transmitted block.

As for the receiver list there are special cases also for the tramsmitter list.

The key could be either 2000_8 or 3000_8. This situation is treated identically as for the receiver list and will not be discussed again.

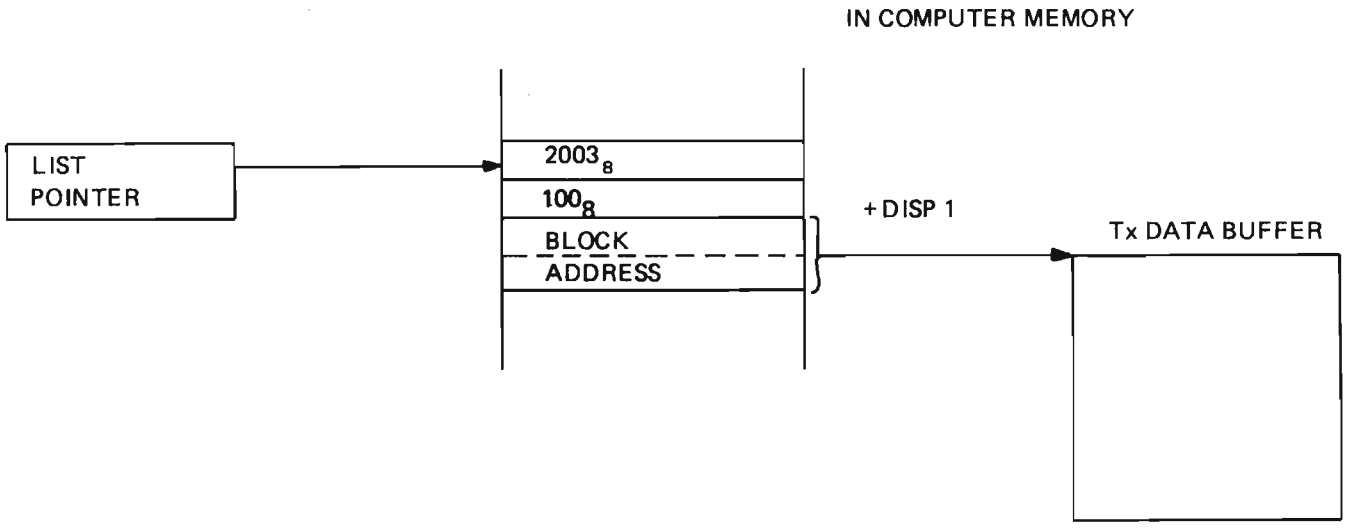
Data belonging to one frame could be placed in one, two or more data blocks. The case is set by driver software in the status word of the list entry.

FORMAT OF THE STATUS WORD



CASE 1. A Hole Frame In One Block

Suppose the frame contains 100 bytes. Then the list entry set by driver software will be as shown below.



The DMA processor will read the status word of the list entry. The status word contains legal key (Bit 10 set). Both TEOM and TSOM are set to 1.

That means for the DMA processor:

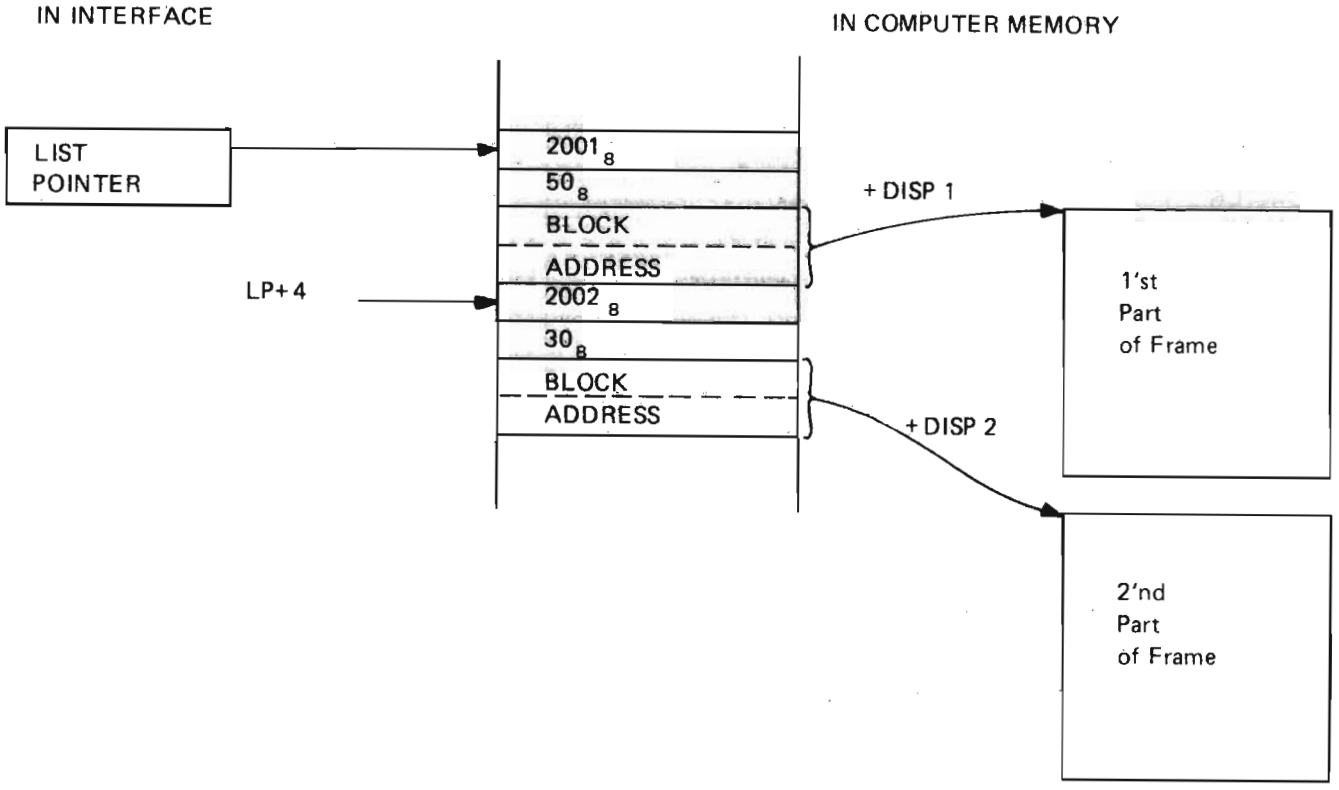
— first transmit TSOM (opening flag)

— when 100_8 bytes are transmitted, send TEOM (closing flag)

— update the list entry by setting the Block Done bit (in special cases also one of the bits 2-7)

CASE 2. A Hole Frame In Two Blocks

The list entries will now be as indicated below.



The first list entry, which contains the first part of the frame, contains legal key and *only* TSOM set.

The second list entry has also legal key and *only* TEOM set.

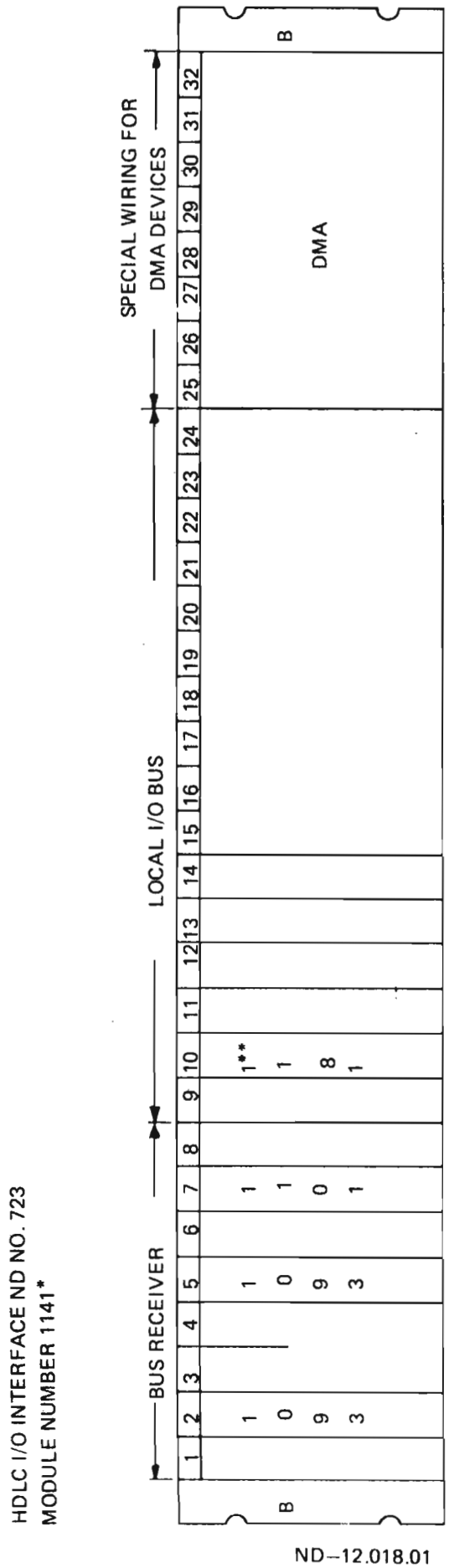
NOTE:

If a frame is held in more than two data blocks, the middle "blocks are marked by not start of frame" and "not end of frame" (i.e. 2000_8).

Use of data blocks and transmitter list is typically organized as for receiver list.

APPENDIX A

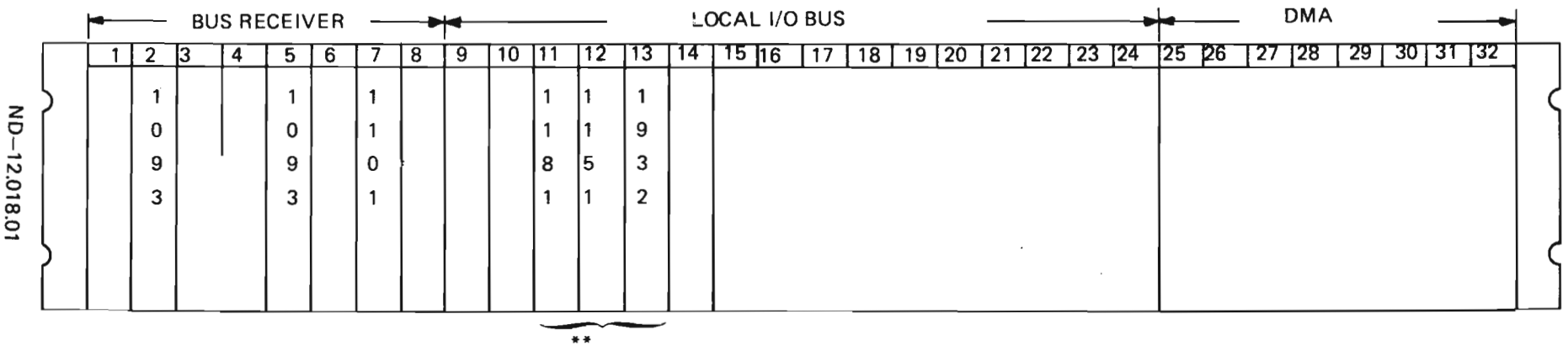
A.1 *HDLC I/O CONFIGURATION*



* Due to unreliable components many ECO's (Engineering Change Orders) on HDLC DATA (1141) the module is redesigned and the number is changed to 1181. 1181 contains all ECO's done on 1141. The module number change do not imply any change in functions of the module.

** Any position in Local I/O Bus. There should be modules in all positions from position 9 to HDLC DATA.

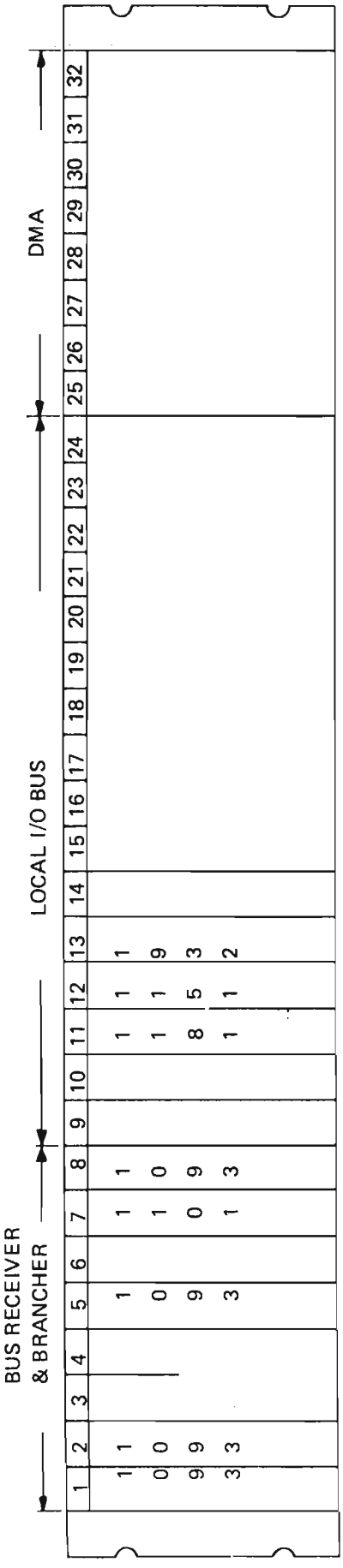
HDLC INTERFACE (DMA) ND NO. 720
DATA TO MEMORY VIA CPU MODULE NUMBERS 1141 (1181), 1151, 1932*



* Module number 1932 is called HDLC DMA SHADOW. HDLC DMA CONTROL is designed with 256 x 8 bits RAM locations. The memory chips used are not yet available from the semi-conductor manufacturer. HDLC DMA SHADOW is used to simulate the memory chips and will be removed when they are available.

** HDLC INTERFACE (DMA) should be placed behind unbuffered DMA devices and in front of bufferred DMA devices (Big Disk).

HDLC INTERFACE (DMA) ND NO. 720
DMA DIRECT TO MULTIPORT MEMORY



ND–12.018.01

* Same placement philosophy as under ** on the previous page.

A.2 *DETAILED DESCRIPTION OF THE MULTIPROTOCOL COMMUNICATION CONTROLLER*

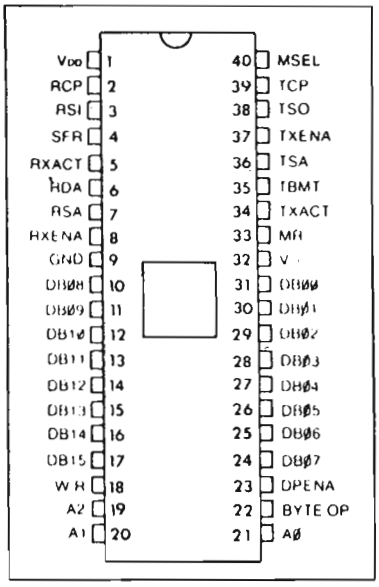
COM 5025
μPC FAMILY
Preliminary Specifications

Multi-Protocol Universal Synchronous Receiver/Transmitter
USYNR/T

FEATURES

- ☐ Selectable Protocol—Bit or Byte oriented
- ☐ Direct TTL Compatibility
- ☐ Tri-state Input/Output Bus
- ☐ Processor Compatible—8 or 16 bit
- ☐ High Speed Operation—2.0M Baud—typical
- ☐ Fully Double Buffered—Data, Status, and Control Registers
- ☐ Full or Half Duplex Operation—independent Transmitter and Receiver Clocks
  —individually selectable data length for Receiver and Transmitter
- ☐ Master Reset—resets all Data, Status, and Control Registers
- ☐ Maintenance Select—built-in self checking

PIN CONFIGURATION



BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP

- ☐ Automatic bit stuffing and stripping
- ☐ Automatic frame character detection and generation
- ☐ Valid message protection—a valid received message is protected from overrun
- ☐ Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available

SELECTABLE OPTIONS:

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —None
- ☐ Primary or Secondary Station Address Mode
- ☐ All Parties Address—APA
- ☐ Extendable Address Field—to any number of bytes
- ☐ Extendable Control Field—to 2 bytes
- ☐ Idle Mode—idle FLAG characters or MARK the line
- ☐ Point to Point, Multi-drop, or Loop Configuration

BYTE ORIENTED PROTOCOLS—BiSync, DDCMP

- ☐ Automatic detection and generation of SYNC characters

SELECTABLE OPTIONS:

- ☐ Variable Length Data—1 to 8 bit bytes
- ☐ Variable SYNC character—5, 6, 7, or 8 bits
- ☐ Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)
  —VRC (odd/even parity)
  —None
- ☐ Strip Sync—deletion of leading SYNC characters after synchronization
- ☐ Idle Mode—idle SYNC characters or MARK the line

APPLICATIONS

- ☐ Computer to Modem Interface
- ☐ Modem to Computer Interface
- ☐ Terminal to Modem Interface
- ☐ Modem to Terminal Interface
- ☐ Peripheral to Modem Interface
- ☐ Modem to Peripheral Interface
- ☐ Serial Data Bus

General Description

The COM 5025 is a COPLAMOS* n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modem interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

References:

1. ANSI—American National Standards Institute
   X353, XS34/589
   202-466-2299
2. CCITT—Consultative Committee for International
   Telephone and Telegraph
   X.25
   202-632-1007
3. EIA—Electronic Industries Association
   TR30, RS334
   202-659-2200
4. IBM
   General Information Brochure, GA27-3093
   Loop Interface—OEM Information, GA27-3098
   System Journal—Vol. 15, No. 1, 1976; G321-0044

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +18.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. Characteristics					
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC} − 1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level, V_{OL}			0.4	V	I_{OL} = 1.6ma
High Level, V_{OH}	2.4				I_{OH} = 40μa
INPUT LEAKAGE					
Data Bus		5.0	10.0	μa	0 ≤ V_{IN} ≤ 5v, DPENA = 0 or W/R = 1
All others				μa	V_{IN} = +5v
INPUT CAPACITANCE					
Data Bus, C_{IN}				pf	
Address Bus, C_{IN}				pf	
Clock, C_{IN}				pf	
All other, C_{IN}				pf	
POWER SUPPLY CURRENT					
I_{CC}				ma	
I_{DD}				ma	
A.C. Characteristics					T_A = 25°C
CLOCK-RCP, TCP					
frequency		2.0		MHz	
PW_H		250		ns	
PW_L		250		ns	
t_r, t_f		10		ns	
DPENA, T_{WDPENA}		350	50 μs	ns	
Set-up Time, T_{AS}		100		ns	
Byte Op. W/R A_2, A_1, A_0					
Hold Time, T_{AH}		60		ns	
Byte Op. WIR, A_2, A_1, A_0					
DATA BUS ACCESS, T_{DPA}		250		ns	
DATA BUS DISABLE DELAY, T_{DPD}		50		ns	
DATA BUS SET-UP TIME, T_{DBS}		100		ns	
DATA BUS HOLD TIME, T_{DBH}		60		ns	
MASTER RESET, MR		300		ns	

Description of Pin Functions

Pin No.	Symbol	Name	I/O	Function
1	V_{DD}	Power Supply	PS	+ 12 volt Power Supply.
2	RCP	Receiver Clock	I	The positive-going edge of this clock shifts data into the receiver shift register.
3	RSI	Receiver Serial Input	I	This input accepts the serial bit input stream.
4	SFR	Sync/Flag Received	O	This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received.
5	RXACT	Receiver Active	O	This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA.
6	RDA	Receiver Data Available	O	This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB.
7	RSA	Receiver Status Available	O	This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected). 2. BOP—in the event of ROR, CRC error (if selected). receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA.
8	RXENA	Receiver Enable	I	A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT.
9	GND	Ground	GND	Ground
10	DBØ8	Data Bus	I/O	Bidirectional Data Bus.
11	DBØ9	Data Bus	I/O	Bidirectional Data Bus.
12	DB1Ø	Data Bus	I/O	Bidirectional Data Bus
13	DB11	Data Bus	I/O	Bidirectional Data Bus.
14	DB12	Data Bus	I/O	Bidirectional Data Bus.
15	DB13	Data Bus	I/O	Bidirectional Data Bus.
16	DB14	Data Bus	I/O	Bidirectional Data Bus.
17	DB15	Data Bus	I/O	Bidirectional Data Bus. "OR" with DPØ7.
18	W/R	Write/Read	I	Controls direction of data port. W/R 1, Write. W/R 0, Read.
19	A2	Address 2	I	Address input—MSB.
20	A1	Address 1	I	Address input.
21	AØ	Address 0	I	Address input—LSB.
22	BYTE OP	Byte Operation	I	If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP 0, data port is 16 bits wide.
23	DPENA	Data Port Enable	I	Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT.
24	DBØ7	Data Bus	I/O	Bidirectional Data Bus—MSB.
25	DBØ6	Data Bus	I/O	Bidirectional Data Bus.
26	DBØ5	Data Bus	I/O	Bidirectional Data Bus.
27	DBØ4	Data Bus	I/O	Bidirectional Data Bus.
28	DBØ3	Data Bus	I/O	Bidirectional Data Bus.
29	DBØ2	Data Bus	I/O	Bidirectional Data Bus.
30	DBØ1	Data Bus	I/O	Bidirectional Data Bus.
31	DBØØ	Data Bus	I/O	Bidirectional Data Bus—LSB.
32	V_{CC}	Power Supply	PS	+ 5 volt Power Supply.
33	MR	Master Reset	I	This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT 1, TSO = 1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's.
34	TXACT	Transmitter Active	O	This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped.
35	TBMT	Transmitter Bulfer Empty	O	This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT 0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded.
36	TSA	Transmitter Status Available	O	TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM.
37	TXENA	Transmitter Enable	I	A high level input allows the processing of transmitter data.
38	TSO	Transmitter Serial Output	O	This output is the transmitted character.
39	TCP	Transmitter Clock	I	The positive going edge of this clock shifts data out of the transmitter shift register.
40	MSEL	Maintenance Select	I	Internally RSI becomes TSO and RCP becomes $\overline{TCP}$. Externally RSI is disabled and TSO = 1.

ND–12.018.01

Definition of Terms

Register Bit Assignment Chart 1 and 2

Term	Definition
RSOM	Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) character loaded into RDB. It is cleared when the second byte is loaded into the RDB.
REOM	Receiver End of Message—read only bit. In BOP mode only, set high when last byte of data loaded into RDB, or when an ABORT character is received. It is cleared on reading of Receiver Status Register or dropping of RXENA.
RAB/GA	Received ABORT or GO AHEAD character, read only bit. In BOP mode only, if LM = 0 this bit is set on receiving an ABORT character; if LM = 1 this bit is set on receiving a GO AHEAD character. This is cleared on reading of Receiver Status Register or dropping of RXENA.
ROR	Receiver Over Run—read only bit. Set high when received data transferred into RDB and previous data has not been read, indicating failure to service RDA within one character time. Cleared on reading of Receiver Status Register or dropping of RXENA.
ABC	Assembled Bit Count—read only bits. In BOP mode only, examine when REOM = 1. ABC = 0, message terminated on stated boundary. ABC = XXX, message terminated (by FLAG or GA) on unstated boundary, binary value of ABC = number of valid bits available in RDB (right hand justified).
ERR CHK	Error Check—read only bit. In BOP set high if CRC selected and received in error, examine when REOM = 1. In CCP mode: 1. set high if parity selected and received in error, 2. if CRC selected (tested at end of each byte) ERR CHK = 1 if CRC GOOD, ERR CHK = 0 if CRC NOT GOOD. Controller must determine the last byte of the message.
TSOM	Transmitter Start of Message—W/R bit. Provided TXENA = 1, TSOM initiates start of message. In BOP, TSOM = 1 generates FLAG and continues to send FLAG's until TSOM = 0, then begin data. In CCP: 1. IDLE = 0, transmit out of SYNC register, continue until TSOM = 0, then begin data. 2. IDLE = 1 transmit out of TDB. In BOP mode there is also a Special Space Sequence of 16-0's initiated by TSOM = 1 and TEOM = 1. SSS is followed by FLAG.
TEOM	Transmit End of Message—W/R bit. Used to terminate a message. In BOP mode, TEOM = 1 sends CRC, then FLAG; if TXENA = 1 and TEOM = 1 continue to send FLAG's, if TXENA = 0 and TEOM = 1 MARK line. In CCP: 1. IDLE = 0, TEOM = 1 send SYNC, if TXENA = 1 and TEOM = 1 continue to send SYNC's, if TXENA = 0 and TEOM = 1 MARK line. 2. IDLE = 1, TEOM = 1, MARK line.
TXAB	Transmitter Abort—W/R bit. In BOP mode only, TXAB = 1 finish present character then: 1. IDLE = 0, transmit ABORT 2. IDLE = 1, transmit FLAG.
TXGA	Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. Allows loop termination—GA character.
TERR	Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain continuous transmission. In BOP automatically transmit: 1. IDLE = 0, ABORT 2. IDLE = 1, FLAG. In CCP automatically transmit: 1. IDLE = 0, SYNC 2. IDLE = 1, MARK. Cleared by TSOM.
XYZ	Z Y X —W/R bits. These are the error control bits. 0 0 0 $X^{16} + X^{12} + X^5 + 1$ CCITT—Initialize to "1" 0 0 1 $X^{16} + X^{12} + X^5 + 1$ CCITT—Initialize to "0" 0 1 0 Not used 0 1 1 $X^{16} + X^{15} + X^2 + 1$—CRC16 1 0 0 Odd Parity—CCP Only 1 0 1 Even Parity—CCP Only 1 1 0 Not Used 1 1 1 Inhibit all error detection Note: Do not modify XYZ until both data paths are idle
IDLE	IDLE mode select—W/R bit. Effects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—controls the method of initial SNYC character transmission and underflow. "1" transmit SYNC from TDB, "0" transmit SYNC from SYNC/ADDRESS register.
SEC ADD	Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD = 1 or EXCON = 1.
STRIP SYNC/LOOP	Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT = 1, stop stripping.
PROTOCOL	PROTOCOL—W/R bit. BOP = 0, CCP = 1
*APA	All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP.
TXDL	Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode).
RXDL	Receiver Data Length—W/R bits. RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 0 1 Five bits per character 1 0 0 Four bits per character 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character
EXCON	Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1.
EXADD	Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD = 1.

*Note: This feature does not exist in the present version of the COM5025. It is in the Rev. A version due out in early 3Q77.

Register Bit Assignment Chart 1

REGISTER	DPØ7	DPØ6	DPØ5	DPØ4	DPØ3	DPØ2	DPØ1	DPØØ
Receiver Data Buffer (Read Only- Right Justified- Unused Bits = 0)	RD7 MSB	RD6	RD5	RD4	RD3	RD2	RD1	RDØ LSB
Transmitter Data Register (Read/Write- Unused Inputs = X)	TD7 MSB	TD6	TD5	TD4	TD3	TD2	TD1	TDØ LSB
Sync/Secondary Address (Read/Write- Right Justified- Unused Inputs = X)	SSA7 MSB	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSAØ LSB

Register Bit Assignment Chart 2

REGISTER	DP15	DP14	DP13	DP12	DP11	DP1Ø	DPØ9	DPØ8
Receiver Status (Read Only)	ERR CHK	C	B	A	ROR	RAB/GA	REOM	RSOM
TX Status and Control (Read/Write)	TERR (Read Only)	0	0	0	TXGA	TXAB	TEOM	TSOM
Mode Control (Read/Write)	*APA	PROTOCOL	STRIP SYNC/ LOOP	SEC ADD	IDLE	Z	Y	X
Data Length Select (Read/Write)	TXDL3	TXDL2	TXDL1	EXADD	EXCON	RXDL3	RXDL2	RXDL1

Register Address Selection

1) BYTE OP = 0, data port 16 bits wide

A2	A1	AØ	Register
0	0	X	Receiver Status Register and Receiver Data Buffer
0	1	X	Transmitter Status and Control Register and Transmitter Data Buffer
1	0	X	Mode Control Register and SYNC/Address Register
1	1	X	Data Length Select Register

X = don't care

2) BYTE OP = 1, data port 8 bits wide

A2	A1	AØ	Register
0	0	0	Receiver Data Buffer
0	0	1	Receiver Status Register
0	1	0	Transmitter Data Buffer
0	1	1	Transmitter Status and Control Register
1	0	0	SYNC/Address Register
1	0	1	Mode Control Register
1	1	0	———————
1	1	1	Data Length Select Register

TRANSMITTER OPERATION

Apply Power

Pulse MR: TSO = 1, TBMT = 1, TXACT = 0, TSA = 0, RXACT = 0, RDA = 0, RSA = 0

Protocol = BOP
APA = NO
Loop = NO
Sec Add = NO
IDLE = ABORT Character
ZYX = CCITT-1
TXDL3, TXDL2, TXDL1 = 8 bit
RXDL3, RXDL2, RXDL1 = 8 bit
EXADD = NO
EXCON = NO
All register bits set to zero

Set Byte Op = 1 (8 bits)

Apply TCP

Note: Example below based on initially Master Resetting. If other conditions are required (different Mode Control settings) load prior to TSOM = 1.

CONTROLLER	USYNRT	COMMENT
TXENA = 1 TXGA = TXAB = TEOM = 0, TSOM = 1	→	writing into TX Status & Control Register
	←TBMT = 0 ←TXACT = 1 TSO = FLAG ←TBMT = 1	
TXGA = TXAB = TEOM = TSOM = 0	→	take down TSOM
	←TBMT = 0	ignore
Load Address Byte	→	must be loaded prior to TBMT = 1
	←TBMT = 1 TSO = Address Character	
Load Control Byte	→	
	←TBMT = 0 ←TBMT = 1 TSO = Control Character	
Load Data Length	→	if other than 8 bits desired, must be finished prior to TBMT returning to a "1"
Load Data	→	
	←TBMT = 0 ←TBMT = 1 TSO = DATA	
Load Data	→	
	←TBMT = 0 ←TBMT = 1	
	⋮	repeat sequence until all DATA loaded
	←TBMT = 1 TSO = Last Data Byte	last data character being transmitted

Typical Ending Sequences

TXGA = TXAB = TSOM = 0, TEOM = 1	→	end of message
	←TBMT = 0 TSO = CRC ←TBMT = 1 TSO = FLAG	
TSGA = TXAB = TSOM = TEOM = 0	→	share flag, for next frame
	←TBMT = 0	ignore
Load Address Byte	→	must be loaded prior to TBMT = 1
	⋮	

OR

TXGA = TXAB = TSOM = 0, TEOM = 1	→	end of message
	←TBMT = 0 TSO = CRC ←TBMT = 1 TSO = FLAG	if desired, repeat FLAG sequence
TXGA = TXAB = TEOM = 0, TSOM = 1	→	
	←TBMT = 0 ←TBMT = 1 TSO = FLAG	of next frame
TXGA = TXAB = TEOM = TSOM = 0	→	take down TSOM
	←TBMT = 0	ignore
Load Address Byte	→	must be loaded prior to TBMT = 1
	⋮	

OR

TXGA = TXAB = TSOM = 0, TEOM = 1	→	end of message
	←TBMT = 0 TSO = CRC ←TBMT = 1 TSO = FLAG	flag will be sent
TXENA = 0	→	
	TSO = 1	after FLAG, shut down TX, mark line
	TXACT = 0	

RECEIVER OPERATION

Apply Power

Pulse MR: TSO = 1, TBMT = 1, TXACT = 0, TSA = 0, RXACT = 0, RDA = 0, RSA = 0

Protocol = BOP
APA = NO
Loop = NO
Sec Add = NO
IDLE = ABORT Character
ZYX = CCITT-1
TXDL3, TXDL2, TXDL1 = 8 bit
RXDL3, RXDL2, RXDL1 = 8 bit
EXADD = NO
EXCON = NO
All register bits set to zero

Set Byte Op = 1 (8 bits)

Apply RCP

Note: Example below based on initially Master Resetting. If other conditions are required (different Mode Control or Data Length settings) load prior to RXENA = 1.

CONTROLLER	USYNRT	COMMENT
W/R = 1, DPENA	→	if required, load Mode Control and Data Length Select Registers
RXENA = 1	→	enable reception begin FLAG search
	←SFR = 1	USYNRT synchronized begin filling pipeline
	←RDA = 1, RXACT = 1, RSOM = 1	address byte (8 bit) available RSA not raised
W/R = 0, DPENA	→	read address byte
	←RDA = 0	
	←RDA = 1, RSOM = 0	control byte (8 bit) available
W/R = 0, DPENA	→	read control byte
	←RDA = 0	
	←RDA = 1	first data byte (n bits) available
W/R = 0, DPENA	→	read data byte
	←RDA = 0	
	⋮	
	←RDA = 1, RSA = 1 REOM = 1, RXACT = 0	last data byte available
W/R = 0, DPENA	→	read data byte
	← RDA = 0	
W/R = 0, DPENA	→	read status
	←RSA = 0	
RXENA = 0	→	receiver inactive

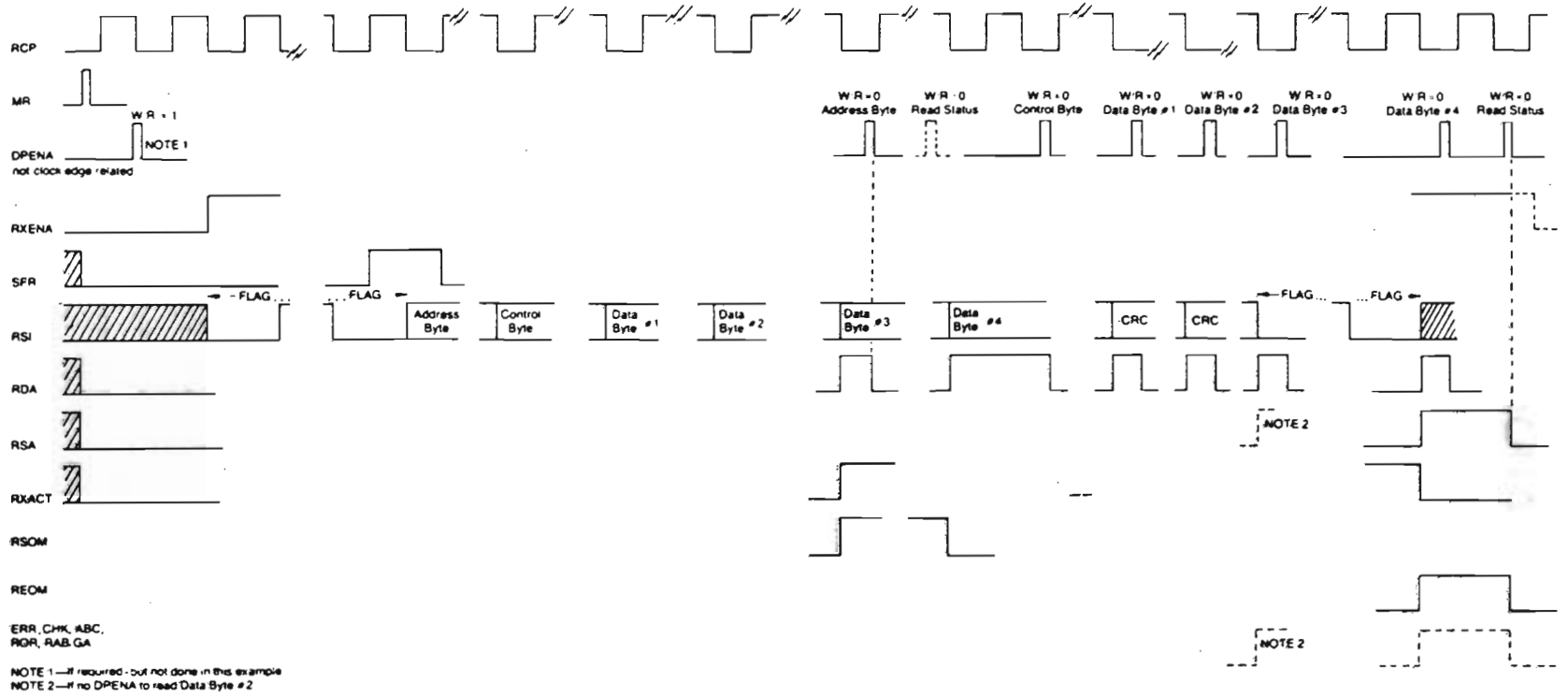
OR

	⋮	
	←RDA = 1	Nth byte available controller fails to read
	←RSA = 1, ROR = 1	RDB overwritten
W/R = 0, DPENA	→	read data byte
	←RDA = 0	
W/R = 0, DPENA	→	read status
	RSA = 0	
RXENA = 0	→	terminate reception
	RXACT = 0	

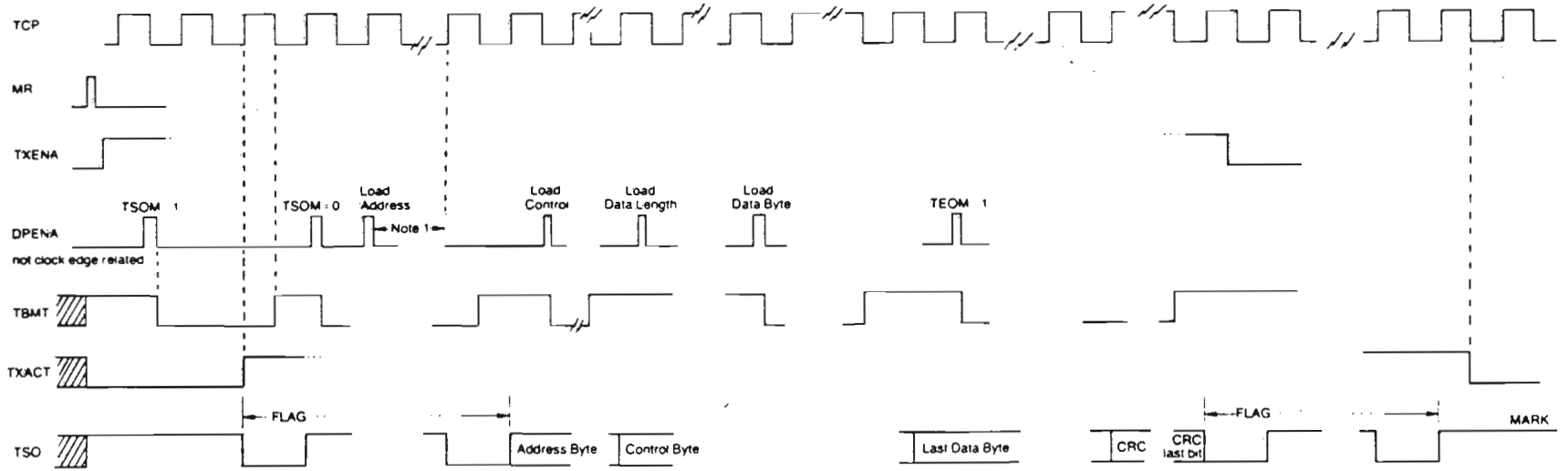
Terminology

Term	Definition	Term	Definition
BOP	Bit Oriented Protocols: SDLC, HDLC, ADCCP	GA	01111111 (0 (LSB) followed by 7-1's)
CCP	Control Character Protocols: BiSync, DDCMP	LSB	First transmitted bit, First received bit
TDB	Transmitter Data Buffer	MSB	Last transmitted bit, Last received bit
RDB	Receiver Data Buffer	RDP	Receiver Data Path
TDSR	Transmitter Data Shift Register	TDP	Transmitter Data Path
FLAG	01111110	LM	Loop Mode
ABORT	11111111 (7 or more contiguous 1's)		

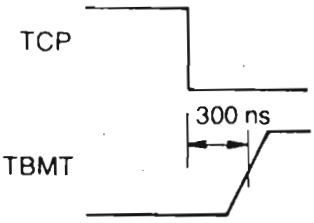
RECEIVER TIMING

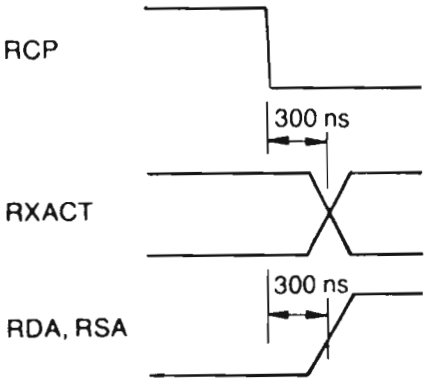


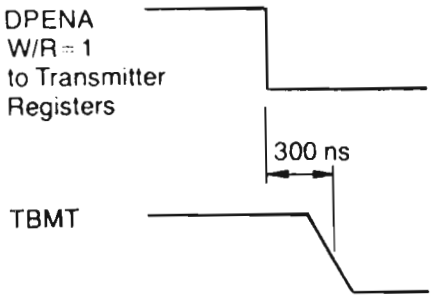
TRANSMITTER OPERATION

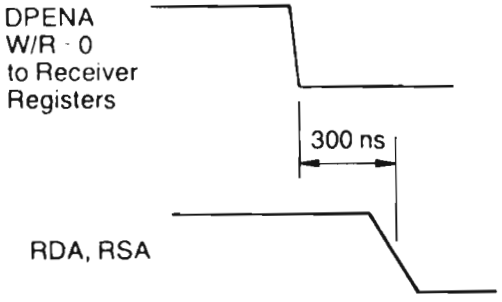


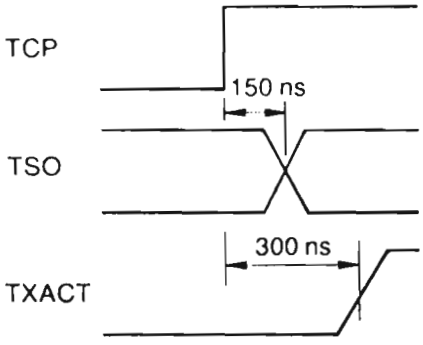
AC TIMING DIAGRAMS





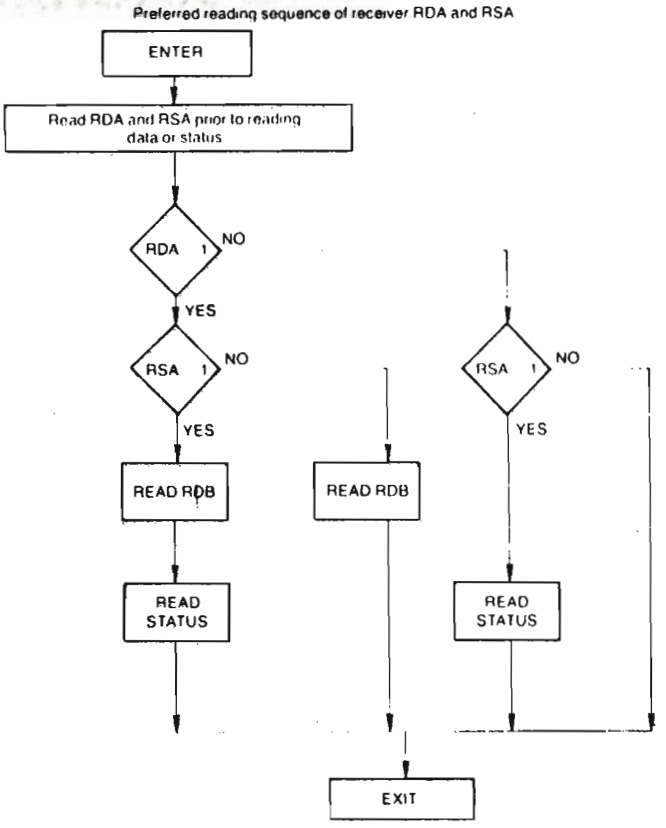




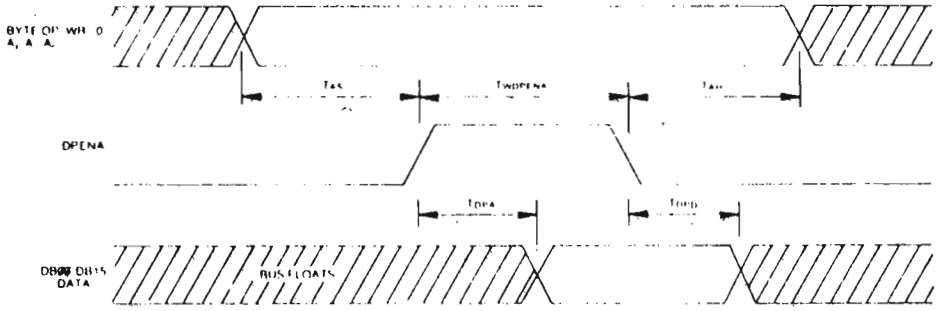


Resets: RDP-RDA, RSA, RXACT, receiver into search mode (for FLAG)

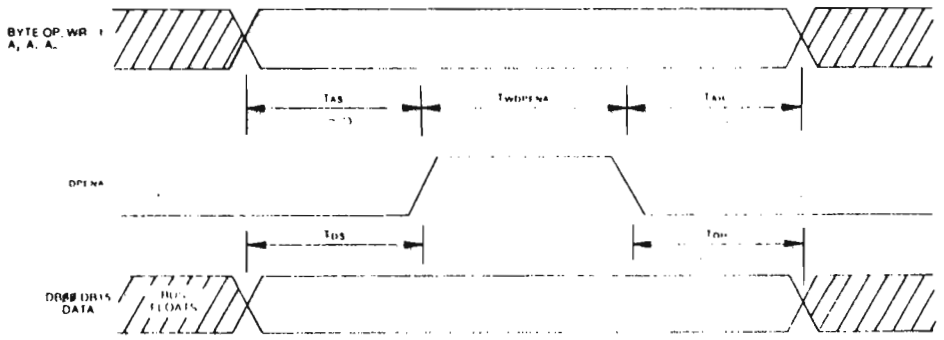
Receiver Data and Receiver Status Access Sequence



Data Port Timing



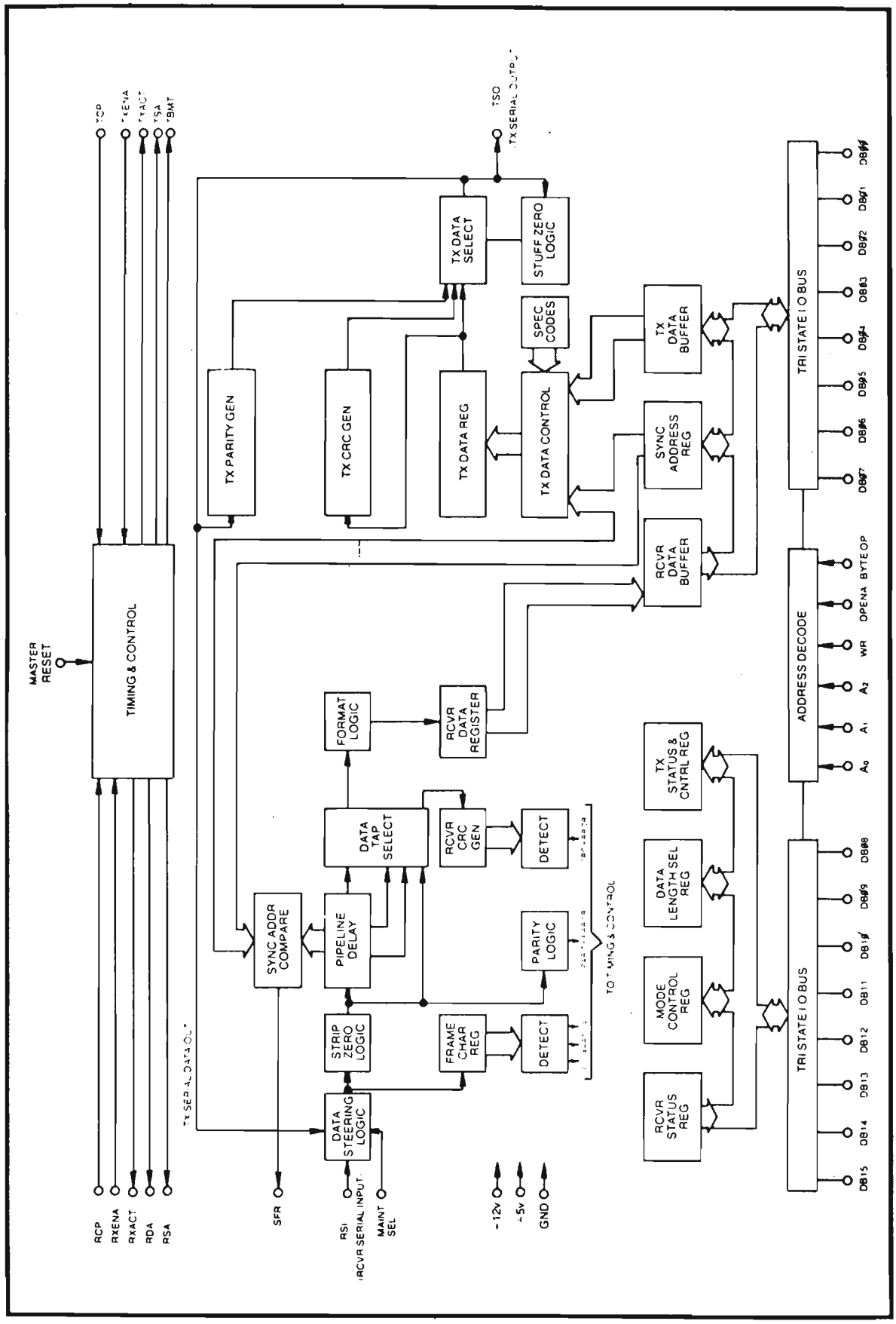
READ FROM USYNR/T



WRITE TO USYNR/T

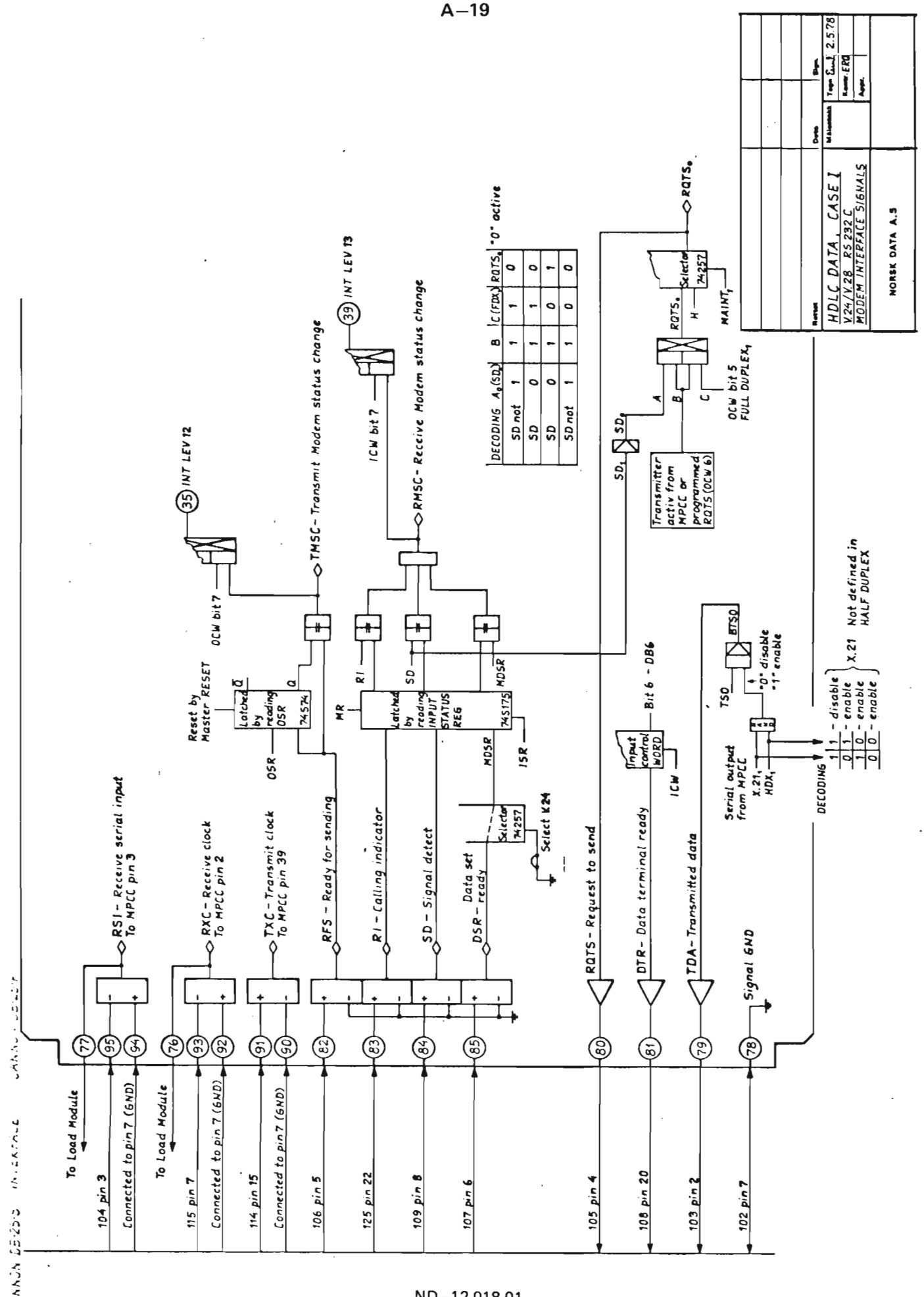
ND–12.018.01

BLOCK DIAGRAM



ND–12.018.01

A.3 *HDLC LINE CONNECTION AND DRIVER SPECIFICATIONS*

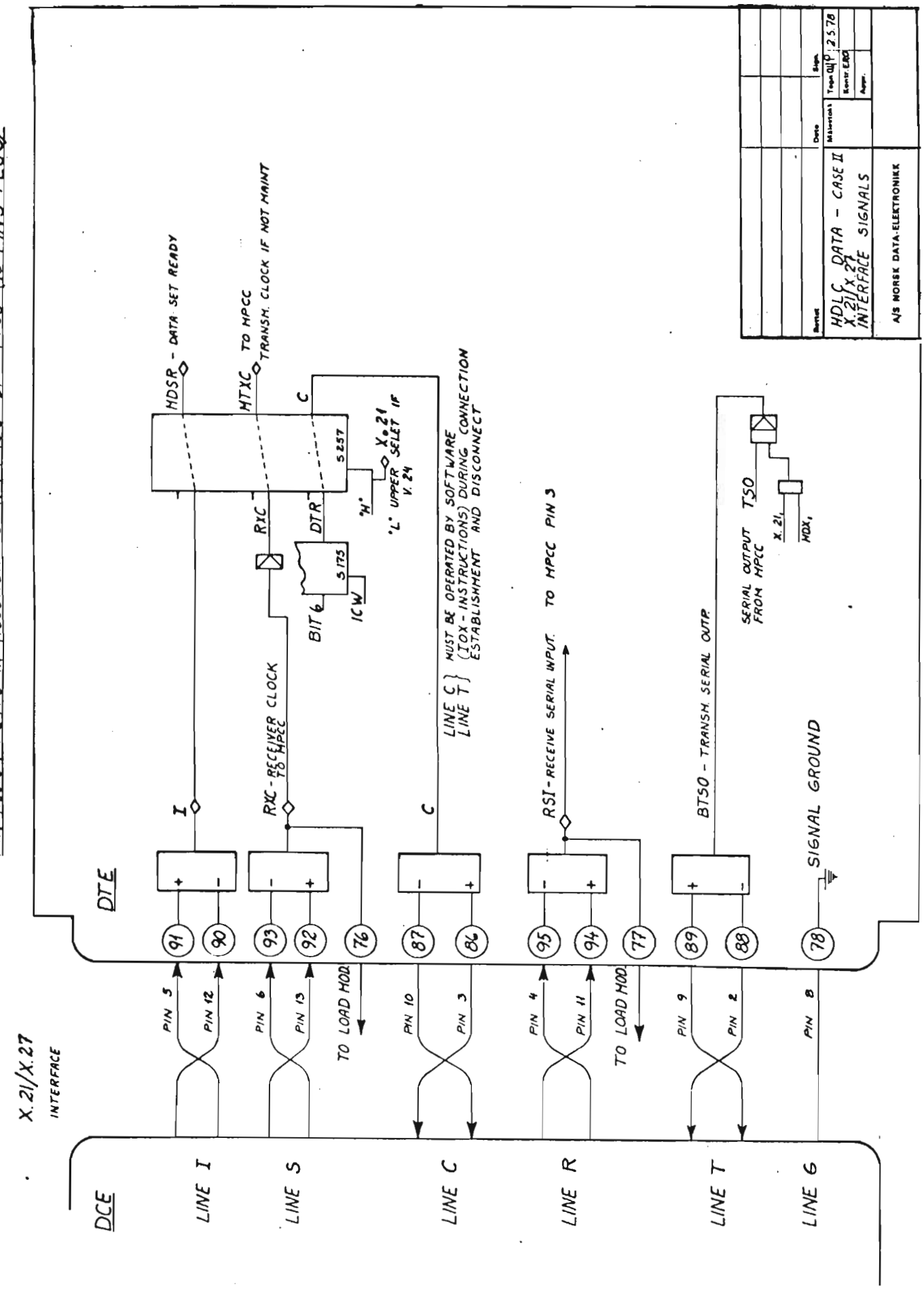


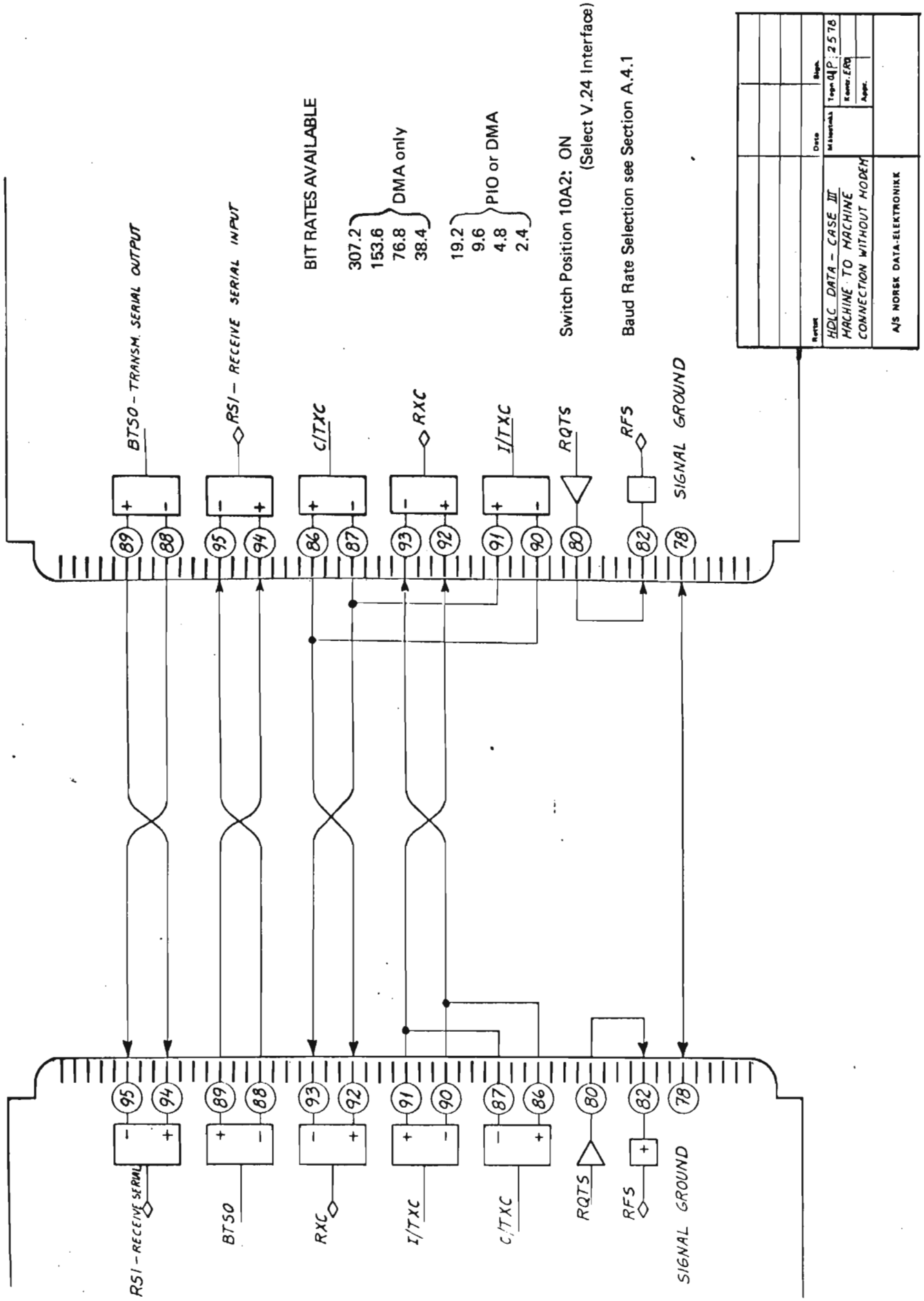
ND–12.018.01

A/S NORSK DATA-ELEKTRONIKK	Title: HDLC DATA 1141 V-24/X21BIS	Drawing no.

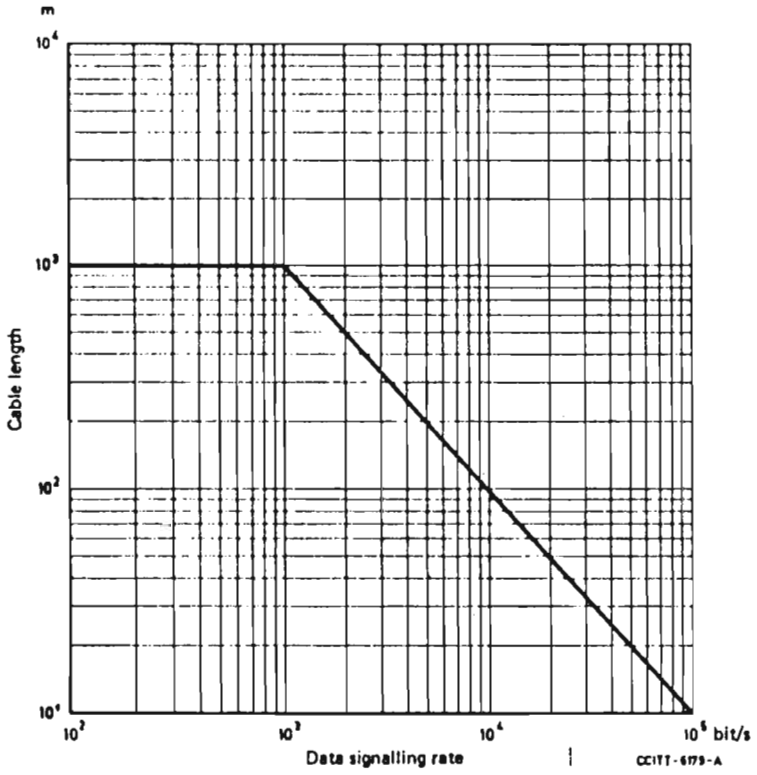
NO.	SIGNAL	PLUG BERG (CPU POS.)	PLUG BURNDY	CANNON DB-25P	
1	RECEIVE DATA A (D)	BERG 95	A	3	
	RECEIVE DATA B (D)	" 94	C	7	
2	RECEIVE CL.A (D)	" 93	B	17	
	RECEIVE CL.B (D)	" 92	D	7	
3	I/TRANSM.CL.A (D)	" 91	E	15	
	I/TRANSM.CL.B (D)	" 90	H	7	
4	TRANSM.DATA A (S)	" 89	F		
	TRANSM.DATA B (S)	" 88	J		
5	C/TRANSM.CLOCK (S)	" 87	K		
	C/TRANSM.CLOCK (S)	" 86	M		
6	DATA SET READY (D)	" 85	L	6	
	SIGNAL DETECT. (D)	" 84	N	8	
7	RING INDICATOR (D)	" 83	P	22	
	READY FOR SEND.(D)	" 82	S	5	
8	DATA TERM.READY(S)	" 81	R	20	
	REQUEST TO SEND(S)	" 80	T	4	
9	TRANSMIT DATA (S)	" 79	U	2	
	SIGNAL GND (S/D)	" 78	W	7	
10	RECEIVER DATA (S)	" 77	LOAD MOD.		
	RECEIVER CLOCK (S)	" 76	"		
11	CLOCK (S/D)	" 75	DMA MOD.		
	TRANSM.DMA INT.RQ (D)	" 74	"		
12	REC.DMA INT.RQ (D)	" 73	"		
	DMA MOD.REQ. (D)	" 72	"		
13	REC.DATA REQ. (S)	" 71	"		
	TRANSM.DATA REQ(S)	" 70	"		
14	MASTER RESET (S)	" 69	"		
	DMA MOD.WAIT (S)	" 68	"		
15	IDB7 DATA BUS(S/D)	" 67	"		
	IDB6 DATA BUS(S/D)	" 66	"		
16	IDB5 DATA BUS(S/D)	" 65	"		
	IDB4 DATA BUS(S/D)	" 64	"		
17	IDB3 DATA BUS(S/D)	" 63	"		
	IDB2 DATA BUS(S/D)	" 62	"		
18	IDB1 DATA BUS(S/D)	" 61	"		
	IDB0 DATA BUS(S/D)	" 60	"		
19	ICB3 CONTR.BUS (D)	" 59	"		
	ICB2 CONTR.BUS (D)	" 58	"		
20	ICB1 CONTR.BUS (D)	" 57	"		
	ICB0 CONTR.BUS (D)	" 56	"		

DRAWN BY HS/eml	Remarks	Replacement for Date
APPROVED BY		Replaced by Date
DATE 10/11/77		

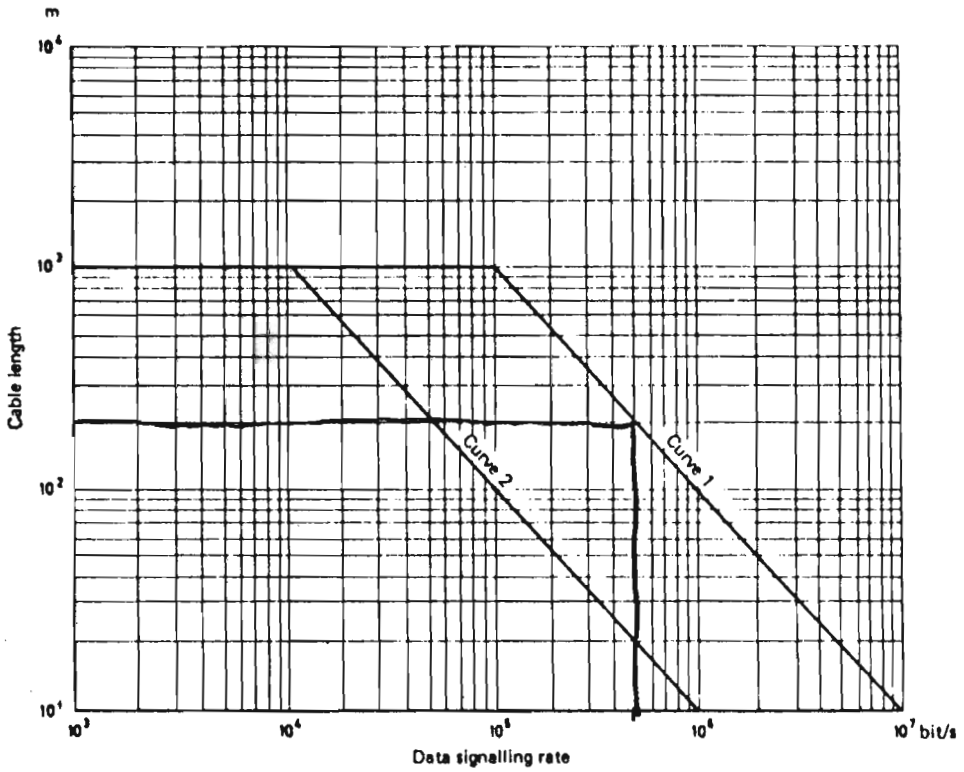




ND–12.018.01



Data signalling rate versus cable length for unbalanced interchange circuit related to V.10, X.26, RS 423.



Curve 1 : terminated interchange circuit
Curve 2 : unterminated interchange circuit

Data signalling rate versus cable length for balanced interchange circuit related to V.11, X.27, RS 422.

SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE

A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0V$
- Common Mode: $|V_{cmo}| \leq 3.0V$

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq \max(0.5V_{do}, 2.0V)$

Output Impedance
- Either logic state: $R_O \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| \quad |V_{dM}| \leq 0.4V$
- Common Mode: $|V_{cmS}| \quad |V_{cmM}| \leq 0.4V$

Output Short Circuit Current (to ground)
- Either Output: $|I_{SC}| \leq 150mA$

Output Leakage Current (power off)
- Voltage Range: $0.25V \leq V_x \leq +6.0V$
- Either Output at V_x: $|I_X| \leq 100\mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq \max(0.1T, 20ns)$

Ringing (across 100 ohm load)

Definitions

$V_{dSS} = V_d$ (steady state)

$V_{SS} = V_{dS} \quad V_{dM}$ (steady state)

Limits (either logic state)
- Percentage: $|V_d \quad V_{dSS}| \leq 0.1V_{SS}$
- Absolute: $2.0V \leq |V_d| \leq 6.0V$

B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0V$
- Common Mode: $|V_{CM}| \leq 7.0V$

Single-Ended Input Current (power ON or OFF)
- Either Input at V_x: $|V_x| \leq 10V$
- Other Input Grounded: $|I_V| \leq 3.25mA$

Single Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0V$

Single Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Either Logic State: $|V_T| \leq 200mV$

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12V$
- Single-Ended: $|V_x| \leq 10V$

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Differential Threshold (500 ohms in series with each input)
  - Either Logic State: $|V_t| \leq 400mV$

Termination (optional)
- Total Load Resistance (differential): $R_T \geq 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

C. Interconnecting Cable

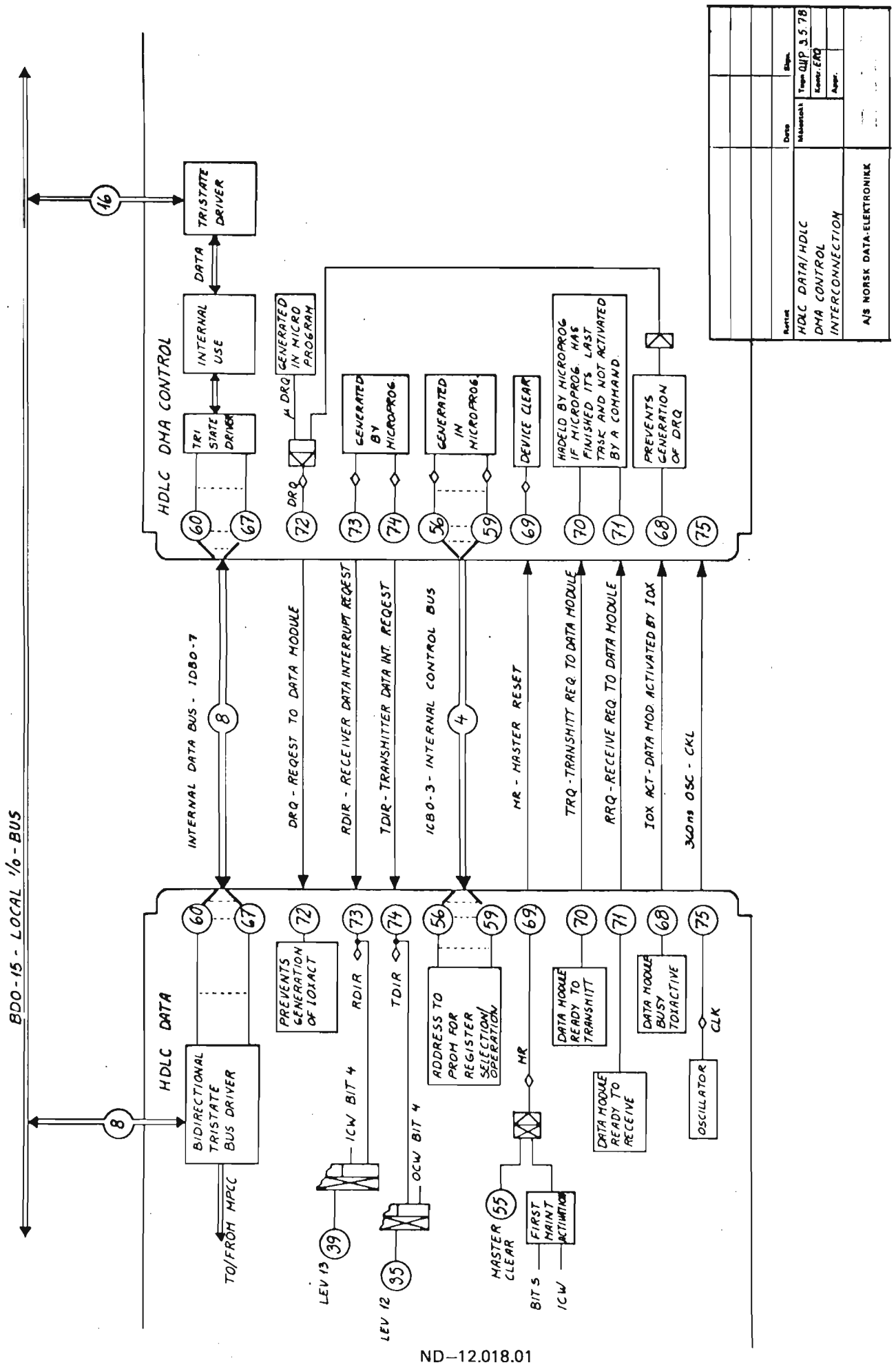
Type
- Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded): 24 AWG or larger
- Other (per conductor): R ≤ 30 ohms/1000 ft.

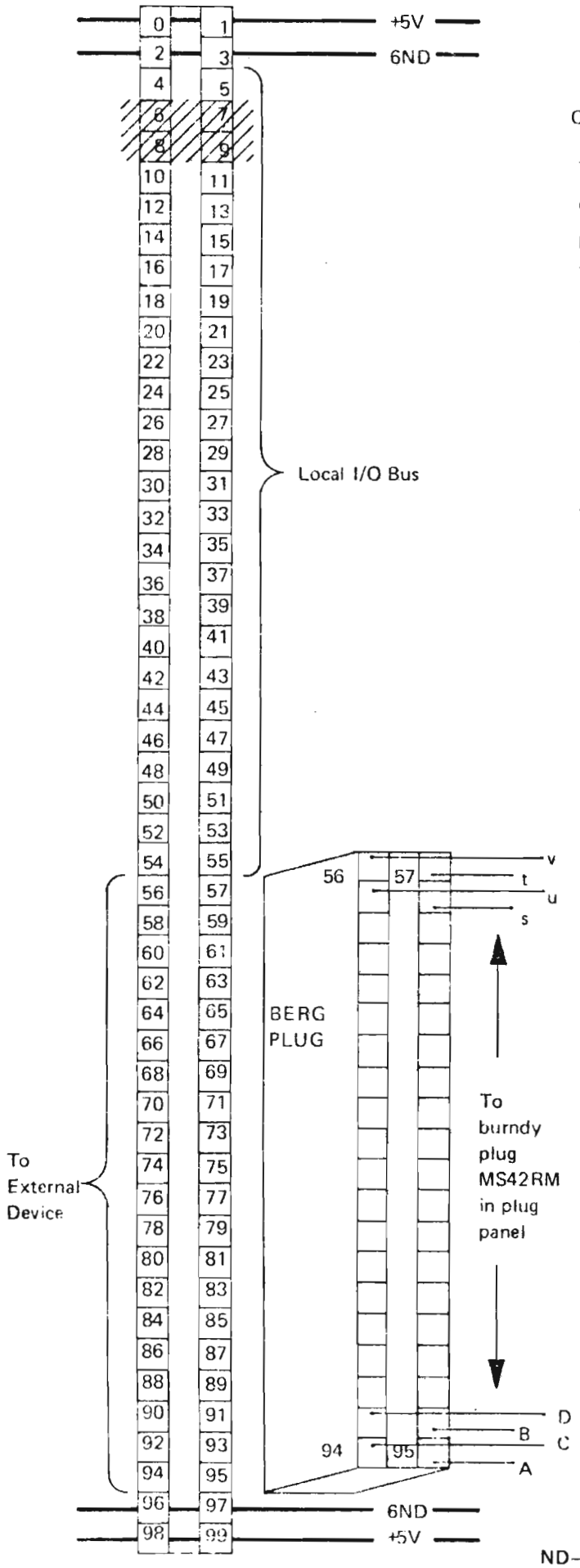
Capacitance
- Mutual Pair: C ≤ 20pF/ft.
- Stray: C ≤ 40pF/ft.

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150KHz: A ≥ 40dB

A.4 *HDLC DATA — HDLC DMA CONTROL INTERCONNECTION*



ND–12.018.01



Card Module:

The interface module is fit into a 100 terminal connector where 4 of the terminals are used for power (+5V) and 4 terminals for ground (GND). The terminals 4-55 are assigned for the local I/O BUS, while terminal 56-95 are used for connection to the external device via the plug-panel.

Local I/O Bus Signal Levels:

Local I/O Bus signals are TRI-STATE TTL for all signals except interrupt lines and DMA request line, which are open collector TTL.

Logical "1" signal $0 \leq S \leq 0{,}4V$

Logical "0" signal $2{,}4 \leq S \leq 5V$

These terminals do not have a 1-1 connection to the next I/O position (used for IDENT and GRANT)

ND–12.018.01

A.4.1 *Speed Selection (Switch Setting on 1181) Intercomputer Link*

	11F1	11F2	11F3	11F4	11F5	11F6
2,400 bps	OFF	OFF	OFF	ON	OFF	ON
4,8000 bps	OFF	OFF	ON	OFF	OFF	ON
9,600 bps	OFF	ON	OFF	OFF	OFF	ON
19,200 bps	ON	OFF	OFF	OFF	OFF	ON
38,400 bps	OFF	OFF	OFF	ON	ON	OFF
76,800 bps	OFF	OFF	ON	OFF	ON	OFF
153,600 bps	OFF	ON	OFF	OFF	ON	OFF
307,200 bps	ON	OFF	OFF	OFF	ON	OFF

A.5 *PROGRAMMING SPECIFICATIONS*

The HDLC interface for NORD-10 computers is designed around a Multi Protocol Communication Controller, MPCC, of the type X2652 from Signetics or the almost equivalent COM 5025 from SMC Micro systems.

Sixteen different I/O instructions are used to control the interface. Eight are used to read from or write into the MPCC, four are for status and control and four are for DMA Module Address and Command.

Possible interface standards are:

a) CCITT V-24, CCITT X-21 BIS, CCIT X-21 (X-27 signal levels), EIA RS-232-C and EIA RS-422.

b) CCITT V-35.

The interface is also equipped with an internal clock which makes it easy for two interfaces to communicate without external communication equipment (MODEMS).

The interface may be extended with a DMA module to reduce software load on interrupt and I/O handling. Four I/O instructions are used separate from the DMA module and four are used together with data module.

The 16 I/O instructions are:

Group No. + 0	Read Receiver Data Register	(RxDR)
Group No. + 1	Write Parameter Control Register	(PCR)
Group No. + 2	Read Receiver Status	(RxSR)
Group No. + 3	Write Synch/Address Register	(SAR)
Group No. + 4	Write Character Length	(CL)
Group No. + 5	Write Transmitter Data Register	(TxDR)
Group No. + 6	Read Transmitter Status Register	(TxSR)
Group No. + 7	Write Transmitter Control Register	(TxCW)
Group No. + 10	Read Receiver Transfer Status	
Group No. + 11	Write Receiver Transfer Control	
Group No. + 12	Read Transmitter Transfer Status	
Group No. + 13	Write Tranmitter Transfer Control	
Group No. + 14	Read DMA Address	
Group No. + 15	Write DMA Address	
Group No. + 16	Read DMA Command Register	
Group No. + 17	Write DMA Command	

Instructions 0-7 operate directly on the MPCC. For a detailed description of these registers (bit mapping, etc.) the reader is advised to study the data sheets from the manufacturers or the HDLC Interface Control Hardware Manual (ND-11.018).

Note that all I/O instructions operate only on bits 0-7 when the DMA module is not installed.

In this text registers 0-7 are named related to X2652 Signetics notations. For cross reference to COM 5025 and HDLC Hardware Manual equivalent register notations are given.

A.5.1 *IOX Instruction Overview Table*

IOX + GP 0, Read Receiver Data Register:

Receiver Data Register is the low byte of the Receiver Data/Status Register (RDSRL) as described in the data sheet. An assembled character (byte) is read from the interface into the A register in the CPU. (Character length is specified by IOX GP + 4 or indicated by RDSRH (IOX GP + 2.) The received character is right justified.

IOX GP + 1, Write Parameter Control Register (PCSARH):

This is the high byte (bits 8-15) of the Parameter Control Sync/Address Register (PCSARH) described in the data sheet. The register defines protocol, etc. Refer to the data sheet.

IOX GP + 2, Read Receiver Status Register:

This is the high byte of the Receive Data/Status Register (RDSRH) and contains receiver status information. Bit mapping is described in the data sheet.

IOX GP + 3, Write Sync/Address Register:

The Sync/Address Register holds the secondary station address in bit-oriented procedures or the SYNC character in byte-oriented procedures. It is the lower byte (Byte Control Procedure) of the Parameter Control Sync/Address Register (PCSARL). Refer to the data sheet.

IOX GP + 4, Write Character Length:

The high byte of the Parameter Control Register (PCRH) is used to specify character length for receiver (bits 0-2) and transmitter (bits 5-7). At this point there is a difference between X2652 and Signetics and COM 5025 from SMC Micro systems. See the data sheet. Equal operation when bits 3 and 4 are 0.

IOX GP + 5, Write Transmitter Data Register:

The low byte of the Transmit Data/Status Register (TDSRL) holds the character to be transmitted. The character length is specified by IOX GP + 4. Character must be right-justified.

IOX GP + 6, Read Transmitter Status Register:

The high byte of the Transmit Data/Status Register (TDSRH) contains transmitter command and status information. The functions of the different bits are described in the data sheets.

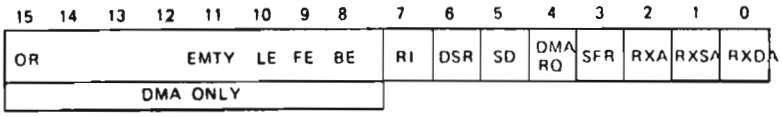
IOX GP + 7, Write Transmitter Control Register:

This is the same byte as may be read by IOX GP + 6.

IOX GP + 10, Read Receiver Transfer Status:

The low byte is the receiver transfer status from the data modules. The high byte is the transfer status from the DMA module, and is not used unless the DMA module is installed.

Bit mapping:



Bit 0: Data Available

Indicates that a character has been assembled and may be read from the Receiver Data Register (RDSRL). Interrupt on level 13 if enabled.

Bit 1: Status Available

Indicates that status information is available in the Receiver Status Register (RDSRH). Interrupt on level 13 if enabled.

Bit 2: Receiver Active

The receiver has seen the start of a frame, but not the end. This means that the receiver is active within a frame.

Bit 3: Sync/Flag Received

At least one SYNC character or FLAG has been receiver after the last reading of Receiver Transfer Status or Master Clear/ Device Clear.

Bit 4: 0 (DMA Module Request)

This bit is activated by the DMA module. If the DMA module is installed, this bit may be the reason for an interrupt on level 13 if enabled. It is, however, always read as 0 because it is cleared at the beginning of IOX GP + 10. If the DMA module caused an interrupt, the reason for this interrupt is given in the most significant byte of the Transfer Status.

Bit 5: Signal Detector (SD)

Status of the Signal Detector (CCITT circuit 109) from the Data Communication Equipment. A change in the status causes an interrupt on level 13 if enabled.

Bit 6: Data Set Ready/I (DSR)

Status of the Data Set Ready (CCITT circuit 107) signal (V-24, X-21 BIS) or the I signal (X-21) from the Data Communication Equipment. A change in the status causes an interrupt on level 13 if enabled.

Bit 7: Ring Indicator (RI)

Status of the Ring Indicator (CCITT circuit 125) from the Data Communication. A change in the status causes an interrupt on level 13 if enabled.

Bit 8: Block End Status bit from DMA module.

Bit 9: Frame End Status bit from DMA module.

Bit 10: List End Status bit from DMA module.

Bit 11: List Empty Status bit from DMA module.

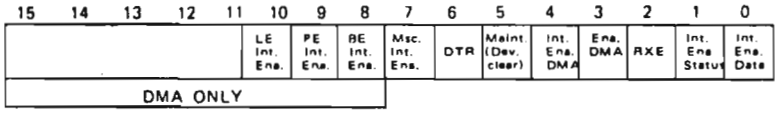
Bit 15: Receiver Overrun Status bit.

Note: Bits 8-15 are cleared by reading the Receiver Transfer Status.

IOX GP + 11, Write Receiver Transfer Control:

The low byte is for interrupt and data enabling on the data module and also some Data Communication Equipment control signals. The high byte is for DMA module control signal.

Bit mapping:



Bit 0: Data Available Interrupt Enable

A 1 in this bit together with Data Available (RXDA) will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 1: Status Available Interrupt Enable

A 1 in this bit together with Status Available (RXSA) will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 2: Enable Receiver (RXE)

Incoming serial data stream is enabled into the receiver. The bit is cleared by MASTER CLEAR.

Bit 3: Enable Receiver DMA

With a 1 in this bit, Data Available (RXDA) will cause a request to the DMA module. The bit is cleared by MASTER CLEAR and by a "List Empty" key during DMA operation.

Bit 4: DMA Module Interrupt Enable

A 1 in this bit together with a request from the DMA module will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 5: Device Clear/Select Maintenance

Writing a 1 into this bit first gives a DEVICE CLEAR, clearing interrupts and interrupt enabling flip-flops, control signals to the Data Communication Equipment, transmitter control signals, Data Communication Equipment status latches and the Multi Protocol Communication Controller. Then it turns the Multi Protocol Communication Controller into maintenance mode, looping transmitted data back to the received data. When the interface is in maintenance mode, the DEVICE CLEAR function is disabled. The bit is cleared by MASTER CLEAR.

Bit 6: Data Terminal Ready/C (DTR)

This bit controls a line to the Data Communication Equipment. It is the Data Terminal Ready (CCITT circuit 108) signal (V-24, X-21 BIS) or the C signal (X-21). The bit is cleared by MASTER CLEAR.

Bit 7: Modem Status Change Interrupt Enable

When set, this bit will cause an interrupt on level 13 when one or more of the Data Communication Equipment status signals connected to the receiver changed to a state different from the last reading (SD, DS/I, RI). The bit is cleared by servicing IDENT, by MASTER CLEAR and DEVICE CLEAR.

Bit 8: Block End Interrupt Enable

This bit will, together with Block End and DMA Module Interrupt Enable, cause an interrupt on level 13.

Bit 9: Frame End Interrupt Enable

This bit will, together with Frame End and DMA Module Interrupt Enable, cause an interrupt on level 13.

Bit 10: List End Interrupt Enable

This bit will, together with List End and DMA Module Interrupt Enable, cause an interrupt on level 13.

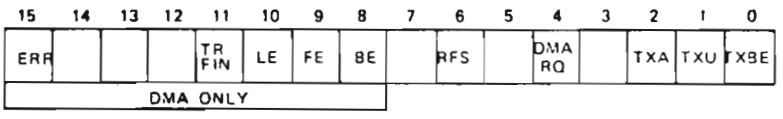
Bit 15: Always 1 after IOX + 11 if inspected after a DUMP command (M11).

Note that List Empty (Receiver Transfer Status, Bit 11) always gives a DMA Module Request (Bit 4).

IOX GP + 12, Read Transmitter Status:

The low byte is the transmitter transfer status from the data module. The high byte is the transfer status from the DMA module if installed.

Bit mapping:



Bit 0: Transmit Buffer Empty

Indicates that the Transmit Buffer (TDSRL) may be loaded with a new character. Interrupt on level 12 if enabled.

Bit 1: Transmitter Underrun

Indicates that the Transmit Buffer has not been loaded with a new character in time. The transmitter will act as defined by the IOX GP + 1 instruction (PCSARH). The underrun condition may cause an interrupt on level 12 if enabled. Transmitter Underrun may be cleared by Master Clear, Device Clear or Transmit Start of Message (TSOM) command.

Bit 2: Transmitter Active

This bit is turned on by sending Start of Message. It will go off when Transmitter Enable (TXE) is turned off and the characters or sequences already in the transmitter are shifted out on the Transmit Data Line (TSO).

Bit 3: Not used

Bit 4: 0 (DMA Module Request)

This bit is activated by the DMA module, and thus it has no meaning unless the DMA module is installed. It is, however, always read as 0 because it is cleared at the beginning of IOX GP + 12. If the DMA module is installed, additional information is given in the high byte. DMA Module Request causes an interrupt on level 12 if enabled.

Bit 5: Not used

Bit 6: Ready for Sending (RFS)

Status signal from the Data Communication Equipment (CCITT circuit 106). A change in the status causes an interrupt on level 12 if enabled.

Bit 7: Not used

Bit 8: Block End Status bit from DMA module.

Bit 9: Frame End Status bit from DMA module.

Bit 10: List End Status bit from DMA module.

Bit 11: Transmission Finished status bit from the DMA module.

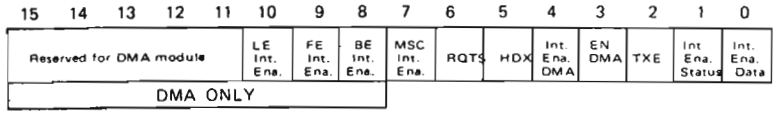
Bit 15: Illegal Key or Illegal Format in Transmitter Buffer Descriptor

This status bit indicates an error stop and the transmitter should be restarted.

IOX GP + 13, Write Transmitter Transfer Control:

The low byte is for interrupt and data enabling on the data module and also two signals concerning the connection to the Data Communication Equipment. The high byte if for the DMA module.

Bit mapping:



Bit 0: Transmit Buffer Empty Interrupt Enable

A 1 in this bit together with Transmit Buffer Empty (TXBE) will cause an interrupt on level 12. This bit is cleared by a servicing IDENT, by MASTER CLEAR or DEVICE CLEAR.

Bit 1: Transmitter Underrun Interrupt Enabled

A 1 in this bit together with a Transmitter Underrun condition will cause an interrupt on level 12. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 2: Transmitter Enabled (TXE)

A 1 in this bit together with Ready for Sending (RFS) (CCITT circuit 106) enables the transmitter part of the Multi Protocol Communication Control (MPCC) to be 1 (MARK) and the Transmitter (TXA) to go off when closing flag or last character has been transmitted. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 3: Enable Transmitter DMA

With a 1 in this bit, Transmitter Buffer Empty (TXBE) will cause a request to the DMA module. This bit is cleared by MASTER CLEAR by Transmission Finished or by Illegal Key/Format (DMA operation).

Bit 4: DMA Module Interrupt Enable

A 1 in this bit together with a request from the DMA module will cause an interrupt on level 12. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 5: Half Duplex

A 1 in this bit will cause the interface to operate in a half duplex mode. The request to send (RQTS) (CCITT circuit 105) signal is not turned ON unless the Signal Detector (SD) (CCITT circuit 109) is off. A 0 in this bit will cause the interface to operate in a full duplex mode. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 6: Request to Send (RQTS)

This is a control signal to the Data Communication Equipment (CCITT circuit 105). In full duplex, 1 means ON and 0 means OFF. In half duplex, Signal Detector (SD) (CCITT circuit 109) must be OFF before the Request to Send line goes ON. Normal response from the Data Communication Equipment is to turn Ready for Sending (CCITT circuit 106) ON when Request to Send is ON. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 7: Modem Status Change Interrupt Enable

When set, this bit will cause an interrupt on level 12 when Ready for Sending from the Data Communication Equipment changes to a state different from the last reading. The bit is cleared by servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 8: Block End Interrupt Enable

This bit will, together with Block End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 9: Frame End Interrupt Enable

This bit will, together with Frame End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 10: List End Interrupt Enable

This bit will, together with List End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 15: Always 1 after IOX GP + 13 if inspected after a DUMP command (M15)

Note that Transmission Finished (Transmitter Transfer Status, bit 11) always gives a DMA Module Request (bit 4).

Note that bit 15 is 1 if inspected after a DUMP command.

IOX GP + 14, Read DMA Address:

The last value written to this register by IOX GP + 15 is read back. May be used for debugging or control.

IOX GP + 15, Write DMA Address:

The 16 least significant bits for the first location in a load/dump area or the first location in a list of buffer descriptors are written into a register (M3) in the DMA module.

IOX GP + 16, Read DMA Command Register:

Before a new command is written to the DMA module, this register should be inspected. If it is zero, the new command sequence can be started. If not, wait until it becomes zero. A MASTER CLEAR command sequence can, however, be started even if the command register is not zero.

IOX GP + 17, Write DMA Command:

The two most significant bits of the address for the first location in a load/dump area or the first location in a list of buffer descriptors are written into a register (M2) in the DMA module together with a value giving one of 8 commands. The data format for this instruction is described in the next section.

The HDLC DMA module is partly controlled by I/O instructions, and partly by control information in buffers in main memory. I/O instructions are used to set buffer addresses, to start operations (give commands), to enable interrupts and to read status.

Control information in the memory is used as additional information for the interface when an operation has been started (by a command).

A.5.2 *The Commands*

The commands may be divided into 3 groups:

1. Device Clear (1)
2. Load/Dump and Initialize (4)
3. Data Transfer (3)

Device Clear

is started by placing octal 40 in the A register and executing IOX GP + 17 (octal).

Load/Dump and Initialize

is started by first writing the least significant 16 bits of a buffer address to the interface (IOX GP + 15 (octal)) and then writing the two most significant buffer address bits (bank bits) together with the command bits to the interface (IOX GP + 17 (octal)).

Data Transfer

is started by first writing the least significant 16 bits of a buffer address to the interface (IOX GP + 15 (octal)), then the two most significant bits (bank bits) together with the command bits (IOX GP + 17 (octal)) and at last enable interrupt and DMA module (IOX GP + 11(octal) for receiver and IOX GP + 13 (octal) for transmitter).

A command sequence should never be interrupted.

The Specific Commands

Eight different commands may be used. They are:
A register when IOX GP + 17 is executed. Y is bank address: B$\in$[0,3]

—	Device Clear	(0)	000040
—	Initialize	(1)	00040Y
—	Receiver Start	(2)	00100Y
—	Receiver Continue	(3)	00140Y
—	Transmitter Start	(4)	00200Y
—	Dump Data Module	(5)	00240Y
—	Dump Register	(6)	00300Y
—	Load Register	(7)	00340Y

Device Clear (Command 0)

Recommended program for Device Clear is:

```
SAA 0                   % A register = 0
IOX GP + 11 (octal)     % Write Receiver Transfer Control
BSET ONE 50 DA          % A register = 40 (octal)
IOX GP + 11 (octal)     % Device Clear to Data Module
IOX GP + 17 (octal)     % Device Clear to DMA Module
```

The Device Clear sequence as described above will stop all data transfers to and from the interface and it can be used at any time. Device Clear will clear all interrupts from the interface and a dialed up modem connection will be broken.

Initialize (Command 1)

The Initialize sequence uses 7 locations in memory. The contents of the locations are:

1. Parameter Control Reg. (8 least significant bits)
2. Sync/Address Register (8 least significant bits)
3. Character Length (8 least significant bits)
4. Displacement 1 (No. of bytes, first block in frame)
5. Displacement 2 (No. of bytes, other blocks in frame)
6. Max. Rec. Block Length (No. of bytes, including displacement)
7. Checksum (102164 is written back from interface

The content of the 3 first locations are written into the Data Module and the mapping of the control bits are described in data sheets for SMC COM 5025 and Signetics MPCC 2652. *Displacement 1* is the number of free bytes reserved at the beginnning of each buffer containing the start of a message (Frame). *Displacement 2* is the number of free bytes reserved at the beginning of each buffer which does not contain the start of a message (Frame). *Maximum Receiver Block Length* is the total number of bytes in a receiver buffer, including displacement. The *Checksum* written back from the interface may be used as a control. The interface should not be used in DMA mode if this checksum is wrong.

Receiver Start (Command 2)

The address written to the interface in a Receiver Start sequence is denoted a "List Pointer". The address is the first address of a list containing "Buffer Descriptors" (see the HDLC DMA List Structure). This command also selects Displacement 1 for the first buffer and should therefore be used the first time the receiver is started after a power up or receiver disable.

Receiver Continue (Command 3)

This command is used to write a new List Pointer to an enabled and working interface. It should only be used as a response to a "List Empty" interrupt.

Transmitter Start (Command 4)

This command is always used to start transmission of data. The address written to the interface is the "Transmitter List Pointer" or the start address for the list of "Buffer Descriptors".

Dump Data Module

This command is mainly for maintenance purposes. It requires 5 location in memory, where the contents of the following registers are stored:

1. Parameter Control Reg. (8 least significant bits)
2. Sync/Address Register (8 least significant bits)
3. Character Length (8 least significant bits)
4. Receiver Status Register (8 least significant bits, not accumulated)
5. Transmitter Status Reg. (8 least significant bits, not accumulated)

The contents of the registers in the Multi Protocol Communication Controller (MPCC) is transferred to memory. The Receiver Status Register is also ORed into the Receiver Dataflow Status Register to prevent loss of information.

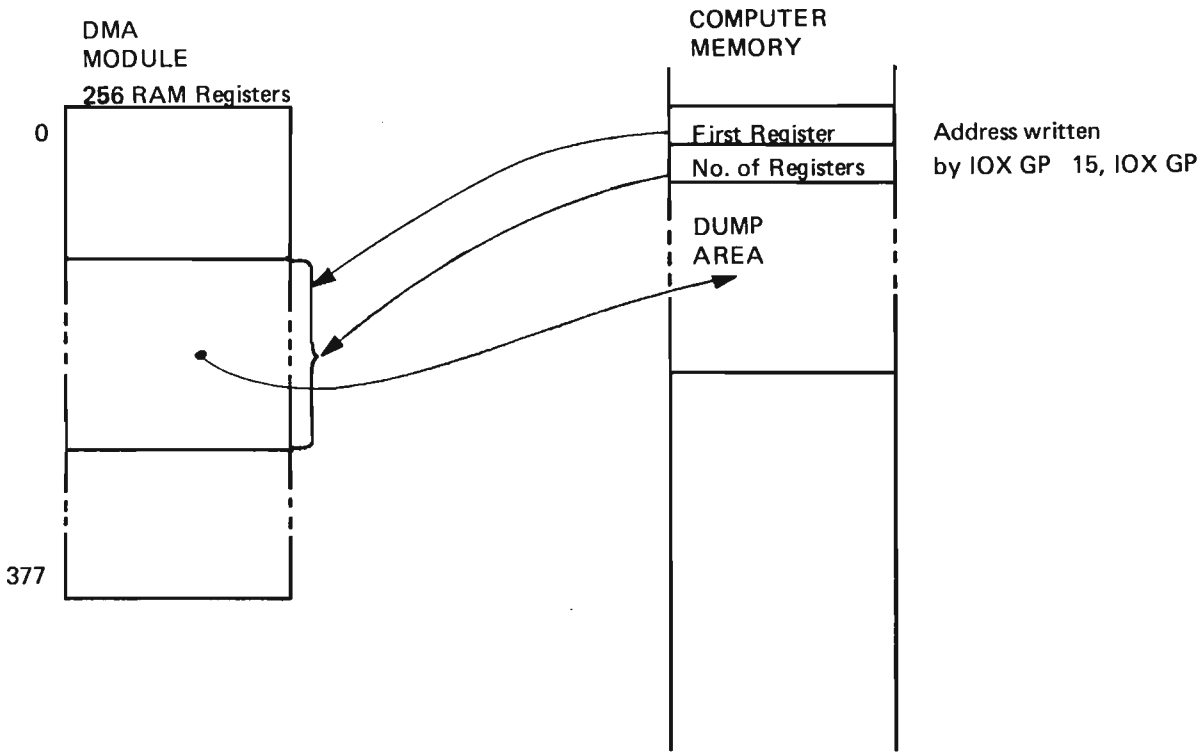
Dump Register

This command can be used to dump the contents of any number of the 256 random access memory registers in the DMA module. Required space in memory is 2 locations plus 1 location for each register to be dumped. The contents of the 2 locations are:

1. First Register Address
2. Number of Registers

If both values are zero, the contents of the 16 registers in the Bit Slice are written into memory.

The meaning of the different values are illustrated in the figure below.



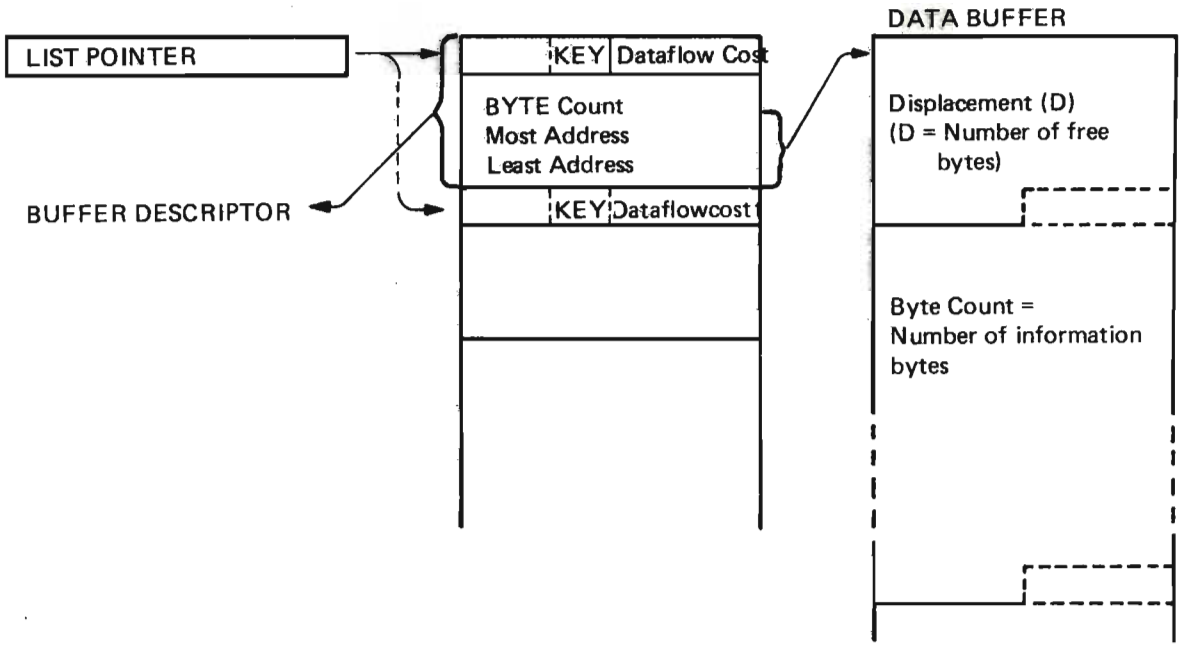
Load Register

This command can be used to load any number of the 256 random access memory register in the DMA module. Required space in memory is 2 locations plus 1 location for each register to be loaded. The contents of the 2 locations are:

1. First Register Address
2. Number of Registers

The Load Register command is simular to Dump Register except that data is moved in the opposite direction. It is not possible to load the register in the Bit Slice by this command.

HDLC DMA LIST STRUCTURE



New List Pointer is old List Pointer+4,
or loaded from memory (if New List Pointer)

	Bits 10	9	8	
Key for Empty Receiver Block is	0	1	0	$= 1000_8$
Full Receiver Block is	0	1	1	$= 1400_8$
Block to be Transmitted is	1	0	0	$= 2000_8$
Already Transmitted Block is	1	0	1	$= 2400_8$
New List Pointer is	1	1	0	$= 3000_8$

Legal Keys for the Receiver $= 1000_8$ and 3000_8
Legal Keys for the Transmitter $= 2000_8$ and 3000_8
All other key bit combintations mean list empty.

HDLC DATA 1181

Switch	*Position*	*Device No. (octal)*	*Ident Code (octal)*	*Comments*
3C1	OFF ON		0 1	
3C2	OFF ON		0 2	
3C3	OFF ON		0 4	
3C4	OFF ON		0 10	
3C5	OFF ON		0 20	
3C6	OFF ON		0 40	
3C7	OFF ON		0 100	
3C8	OFF ON		0 200	
10A1	OFF ON			Test, CLK Disconnected Normal, CLK Connected
10A2	OFF ON			X-21 Interface V-24 Interface
10A3	OFF ON	0 20		
10A4	OFF ON	0 40		
10A5	OFF ON	0 100		
10A6	OFF ON	0 200		
10A7	OFF ON	0 400		
10A8	OFF ON	0 1000		

Standard Device Numbers:

1640-1657
1660-1667
1700-1720
1740-1757
1760-1777

HDLC IOX INSTRUCTIONS

MPCC
1141
1141
1151

IOX GROUP NO. +	FUNCTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	READ RECEIVER DATA REGISTER									Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
1	WRITE PARAMETER CONTROL REG.									0	PROT SEL	STRIP SGA	SEC A MODE	IDLE MODE	CRC SEL2	CRC SEL1	CRC SEL0
2	READ RECEIVER STATUS									REBR	RSCL2	RSCL1	RSCL0	ROVR RUN	RABORT	REOM	RSOM
3	WRITE SYNC/ADDRESS REGISTER									SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
4	WRITE CHARACTER LENGTH									TxCL2	TxCL1	TxCL0	0	0	RxCL2	RxCL1	RxCL0
5	WRITE TRANSMITTER DATA REGISTER									TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
6	READ TRANSMITTER STATUS REG.									TUNDR	0	0	0	TGA	TABORT	TEOM	TSOM
7	WRITE TRANSMITTER CONTROL REG.									0	0	0	0	TGA	TABORT	TEOM	TSOM
10	READ RECEIVER TRANSFER STATUS	ROV RUN				LIST EMPTY	LE INT EN	FE INT EN	BE INT EN	RI	DSR	SD	DMA RQ	SFR	RXA	RXSA	RXDA
11	WRITE RECEIVER TRANSFER CONTROL	*								MSG INT E			DMA INT E	ENA DMA	RXE	INIT EN	INIT EN
12	READ TRANSMITTER TRANSFER STATUS	ERR				FIN	LE INT EN	FE INT EN	BE INT EN		RFS		DMA RQ		TXA	TXU	TXBE
13	WRITE TRANSMITTER TRANSF. CONTR	*								MSC INT E	RQTS	HDX	DMA INT E	ENA DMA	TXE	INT EN	INT EN
14	READ DMA ADDRESS	16 LEAST SIGNIFICANT BITS OF COMMAND ADDRESS															
15	WRITE DMA ADDRESS	16 LEAST SIGNIFICANT BITS OF COMMANDS ADDRESS															
16	READ DMA COMMAND REGISTER	0	0	0	0	0	Command Code			0	0	X	0	0	0	Bank Bits	
17	WRITE DMA COMMAND REG. + TRIGGER	0	0	0	0	0	Command Code			0	0	X	0	0	0	Bank Bits	

NOTES:

* THIS BIT IS 1 IF INSPECTED AFTER A DUMP COMMAND. DMA PQ IS ALWAYS READ AS 0 (CLEARED AT THE START OF THE IOX INSTRUCTION) IOX GP+10 or IOX GP+12.

X BIT 5 IN COMMAND SHOULD BE 0 EXCEPT FOR DEVICE CLEAR COMMAND

COMMANDS		1. IOX INSTRUCTION		2. IOX INSTRUCTION		3. IOX INSTRUCTION		MEMORY	NOTES
		A-REGISTER	IOX GP+	A-REGISTER	IOX GP+	A-REGISTER	IOX GP+	BUFFER	
DEVICE CLEAR	0	000040	17	–	–	–	–	–	
INITIALIZE	1	XXXXXX	15	00040Y	17	–	–	PCR SAR CL DISP 1 DISP 2 MAX BLOCK 1 0 2 1 6 4	PARAMETER CONTROL REGISTER SYNC ADDRESS REGISTER CHARACTER LENGTH DISPLACEMENT, FIRST BLOCK DISPLACEMENT, OTHER BLOCKS MAX. RECEIVER BLOCK LENGTH CHECKSUM FROM INTERFACE
RECEIVER START	2	XXXXXX	15	00100Y	17	(BIT 3 =1)	11	(BUFFER DESCRIPTOR)	SELECTS DISP 1
RECEIVER CONTINUE	3	XXXXXX	15	00140Y	17	(BIT 3=1)	11	(BUFFER DESCRIPTOR)	CONTINUES WITH SELECTED DISP
TRANSMITTER START	4	XXXXXX	15	00200Y	17	(BIT 3=1)	13	(BUFFER DESCRIPTOR)	SELECTS DISP 1, (TSOM)
DUMP DATA MODULE	5	XXXXXX	15	00240Y	17	–	–	PCR SAR CL RSR TSR	PARAMETER CONTROL REGISTER SYNC/ADDRESS REGISTER CHARACTER LENGTH RECEIVER STATUS REGISTER TRANSMITTER STATUS REGISTER
DUMP REGISTERS	6	XXXXXX	15	00300Y	17	–	–	1. REG NUMBER	0 ≤ 1 REG ≤ 377 NUMBER ≤400-1. REG OR 0 (NB)
LOAD REGISTERS	7	XXXXXX	15	00340Y	17	–	–	1. REG NUMBER	0 ≤ 1. REG ≤ 377 NUMBER ≤ 400 - 1. REG

XXXXXX 16 LEAST SIGN. BITS OF ADDRESS

.....Y 2 MOST SIGN. BITS OF ADDRESS (BANK BITS)

(NB) IF NUMBER =0 IN DUMP REGISTER, THE BIT SLICE REGISTER BLOCK IS COPIED INTO MEMORY.

	TRANSFER STATUS IOX GP + 10_8 (RTS) (M10)	TRANSFER CONTROL IOX GP + 11_8 (RTC) (M11)	DATAFLOW STATUS (RCOST) (M20, R10)	DATAFLOW CONTROL (RCOST) (M20, R10)
0	DATA AVAILABLE	ENABLE DATA INTERRUPT	RSOM	0
1	STATUS AVAILABLE	ENABLE STATUS INTERRUPT	REOM	0
2	RXA	RXEN	RABORT/GA	0
3	SFR	ENABLE RECEIVER DMA	ROVRUN	0
4	0 (DMA MODULE REQUEST)	ENABLE DMA MOD. INTERRUPT	RSCL 0	0
5	SD	MAINT	RSCL 1	0
6	DSR/1	DTR	RSCL 2	0
7	RI	ENABLE MODEM CHANGE INT.	ERR CHK	0
8	BLOCK END	ENABLE	BLOCK DONE	0
9	FRAME END	ENABLE	KEY (1)	KEY (1)
10	LIST END	ENABLE	KEY (0)	KEY (0)
11	LIST EMPTY	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	OVERRUN	0	0	0

	TRANSFER STATUS IOX GP + 12_8 (TTS) (M14)	TRANSFER CONTROL IOX GP + 13_8 (TTC) (M15)	DATAFLOW STATUS (TCOST) (M30)	DATAFLOW CONTROL (TCOST)(M20)
0	DATA REQUEST	ENABLE DATA INTERRUPT	TSOM	TSOM
1	TRANSMITTER UNDERRUN	ENABLE STATUS INTERRUPT	TEOM	TEOM
2	TXA	TXEN	TABORT	TABORT
3	0	ENABLE TRANSMITTER DMA	TGA	TGA
4	0 (DMA MODULE REQUEST)	ENABLE DMA MOD. INTERRUPT	TSCL0	TSCL0
5	0	HDX	TSCL1	TSCL1
6	RFS	RQTS	TSCL2	TSCL2
7	0	ENABLE MODEM CHANGE INT.	TERR	0
8	BLOCK END	ENABLE	BLOCK DONE	0
9	FRAME END	ENABLE	KEY (0)	KEY (0)
10	LIST END	ENABLE	KEY (1)	KEY (1)
11	TRANSMISSION FINISHED	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	ILLEGAL KEY/FORMAT	0	0	0

A.5.3 *Simple Debugging Programs with Memory Map*

HDLC DMA MODULE DEBUGGING PROGRAMS

USES DEVICE NUMBERS 1640 - 1657 ON INTERFACE

Device Clear	:	SAA 0	20/	170400
		IOX 1651		165651
		SAA 40		170440
		IOX 1651		165651
		IOX 1657		165657
		WAIT		15100
Init	:	LDA *5	30/	044005
		IOX 1655		165655
		LDA *4		044004
		IOX 1657		165657
		WAIT		151000
		(ADDRESS)		120
		(COMMAND)		400
	ADDRESS	/PC R	120	0
		SAR		0
		CL		0
		DISP 1		10
		DISP 2		7
		MAX BLOCK		100
		CHECKSUM		0→102164
Dump ALU	:	LDA *5	40/	044005
		IOX 1655	1	165655
		LDA *4	2	044004
		IOX 1657	3	165657
		WAIT	4	151000
		(ADDRESS)	5	136
		(COMMAND)	6	3000
	ADDRESS	/ 0	136/	0
		0	137	0
	ALU 0		140	—
			—	—
			—	—
				—
				—
				—
	ALU 17		157	—
DUMP MEMORY	:	LDA *5	50/	044005
		IOX 1655	1	165655
		LDA *4	2	044004
		IOX 1657	3	165757
		WAIT	4	151000
		(ADDRESS)	5	376
		(COMMAND)	6	3000
	ADDRESS	/ 0	376/	0
		40 (≤377)	377	40
	MO		400	—
	—		—	—
	—		—	—
	M37		437	—
	M40		440	—
	—		—	—
	11377		777	—

```
INIT RECEIVER    :          LDA *7                  60/     044007
                            IOX 1655                 1      165655
                            LDA *6                   2      044006
                            IOX 1657                 3      165657
                            LDA *5                   4      044005
                            IOX 1651                 5      165651
                            WAIT                     6      151000
                            (LIST ADDRESS)           7         200
                            (COMMAND)               10        1000
                            (CONTROL)               11         154
                                                               (maint.mode)
                       LIST
                       ADDRESS/ KEY                200/      1000
                            BYTE COUNT               1         0
                            DATA ADDRESS             2         0
                            DATA ADDRESS             3      1000
                            KEY                      4      1000
                            —
                            —

Init Transmitter    :       LDA * 7                 100/     044007
                            IOX 1655                         165655
                            LDA * 6                          044006
                            IOX 1657                         165657
                            LDA * 5                          044005
                            IOX 1653                         165653
                            WAIT                             151080
                            (LIST ADDRESS)                      240
                            (COMMAND)                          2000
                            (CONTROL)                           114
                       LIST
                       ADDRESS/ KEY                240/      2003
                            BYTE COUNT               1         40
                            DATA ADDRESS             2         0
                            DATA ADDRESS             3      2000
                            KEY                      4      0000
                            —
                            —
```

MEMORY MAPPING FOR HDLC DEBUGGING PROGRAMS

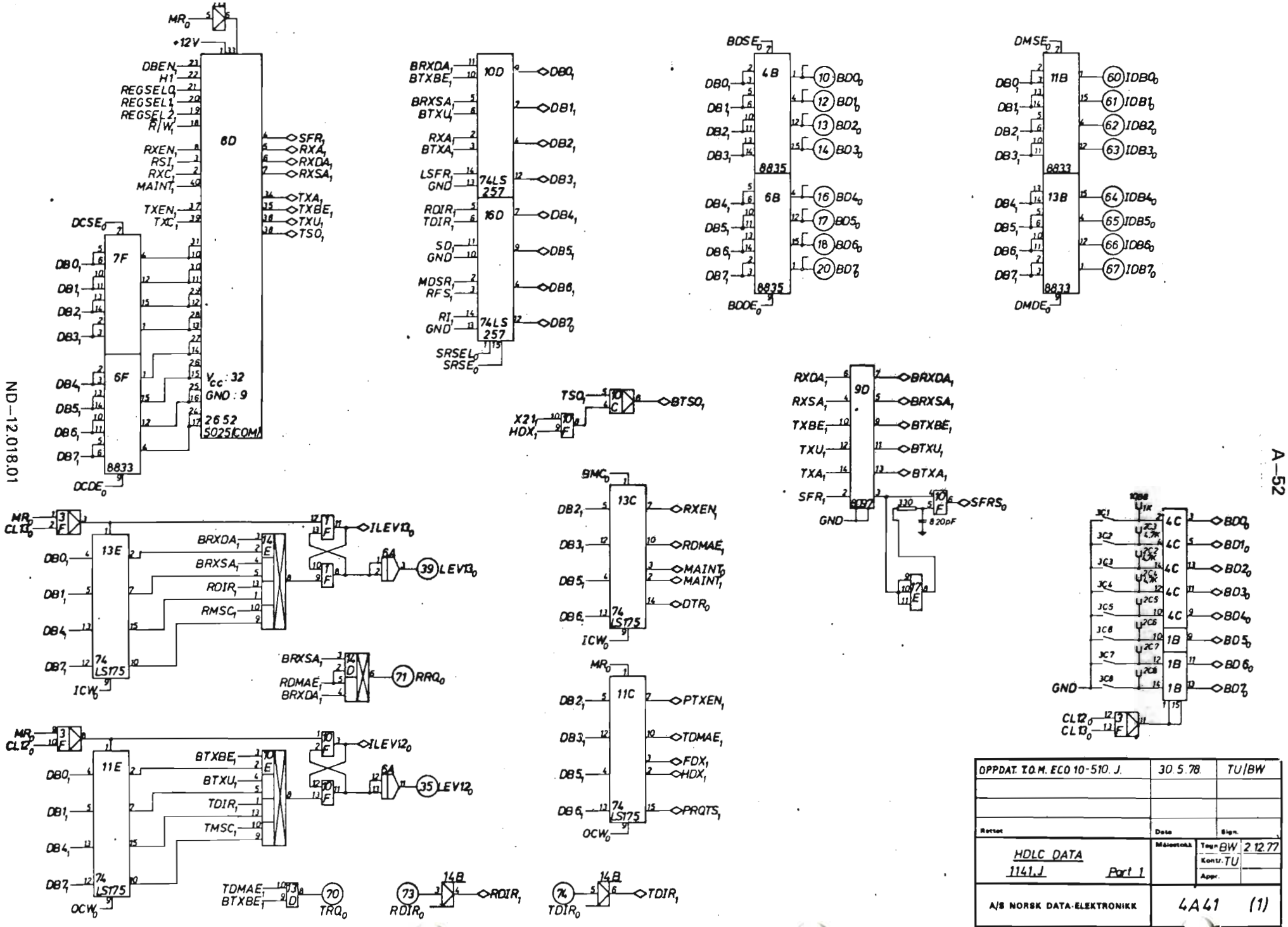
Address:	*Program:*	*Address:*	*Program:*
0		500	Memory Dump
10		.	"
20	Device Clear	.	"
30	Init	.	"
40	Dump ALU	.	"
50	Dump Memory	.	"
60	Init Receiver	.	"
70		.	"
100	Init Transceiver	600	Memory Dump
110		.	"
120	Init Parameters	.	"
130		.	"
140	ALU dump	.	"
150	ALU dump	.	"
160		.	"
170		.	"
200	Receiver List	1000	Receiver Buffers
210	Receiver List	.	"
220	Receiver List	.	"
230	Receiver List	.	"
240	Transmitter List	.	"
250	Transmitter List	.	"
260	Transmitter List	.	"
270	Transmitter List	.	"
300		2000	Transmitter Buffers
310		.	"
320		.	"
330		.	"
340		.	"
350		.	"
360		.	"
370		.	"
400	Memory Dump	3000	
.	"		
.	"		
.	"		
.	"		
.	"		
.	"		
.	"		

The following procedure should move the content of [2004, 2023] to [1004, 1023]:

```
20!
30!
60!
100!
```

Last DMA address (if displayed):	207
Content of 126 should be:	102164
Content of 200 should be:	1403
Content of 201 should be:	40
Content of 240 should be:	2403

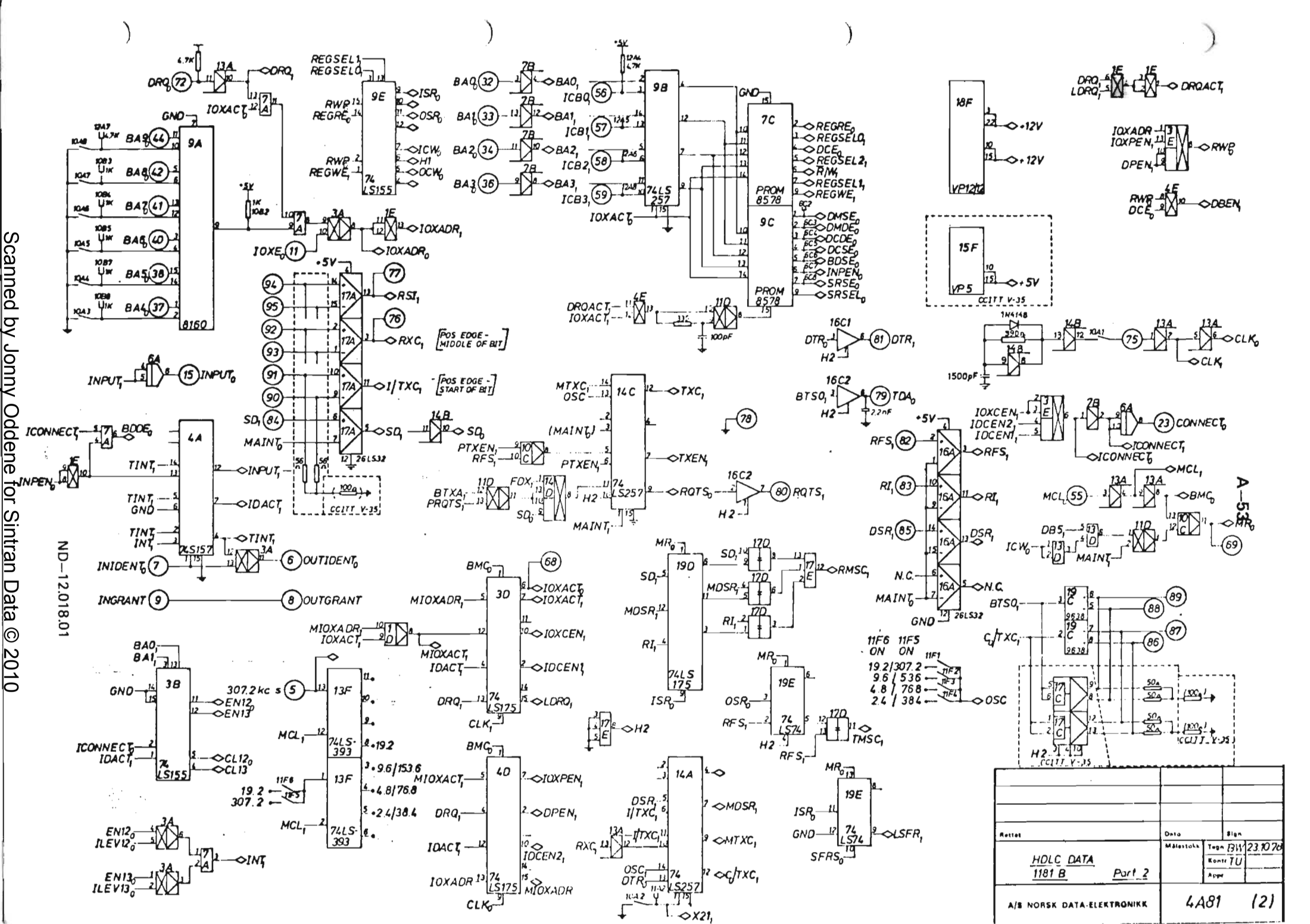
A.6 *HDLC LOGICAL DIAGRAMS*

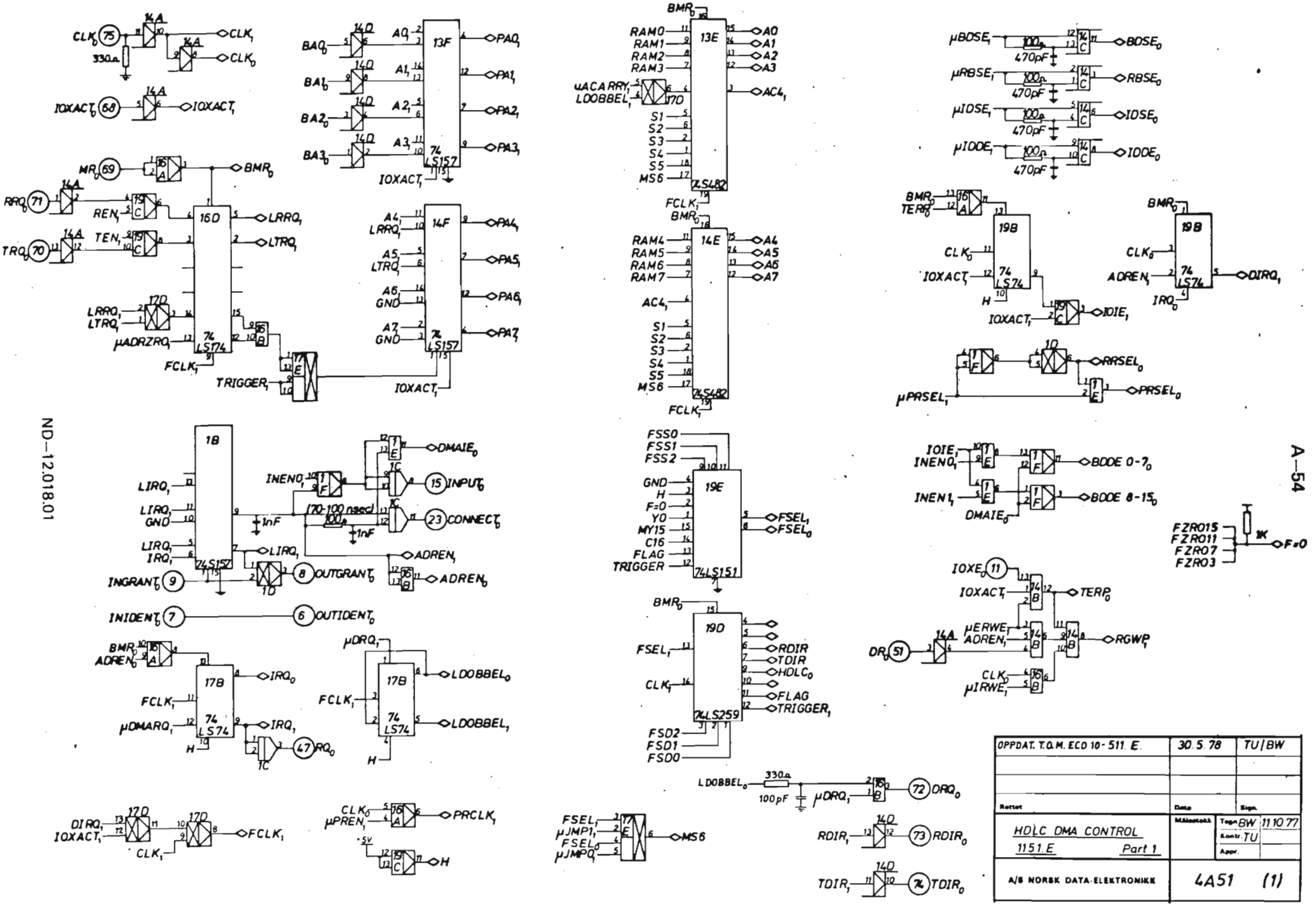


OPPDAT. I.O.M. ECO 10-510. J.	30.5.78	TU/BW
Rettet	Dato	Sign.
HDLC DATA 1141.1 Part 1	Målestokk	Tegn. BW 2.12.77 Kontr. TU Appr.
A/S NORSK DATA-ELEKTRONIKK	4A41 (1)	

ND-12.018.01

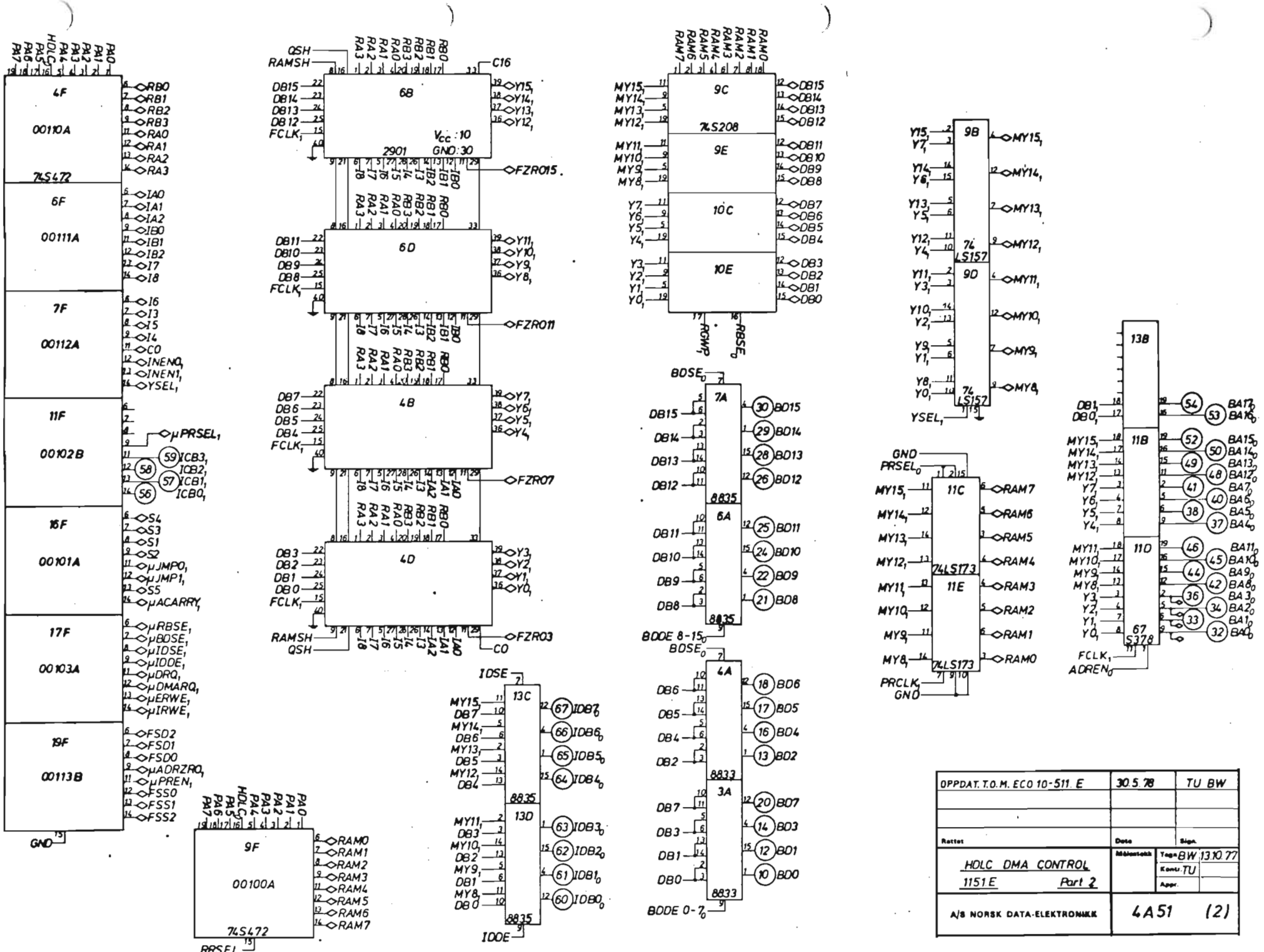
A-52





ND-12.018.01

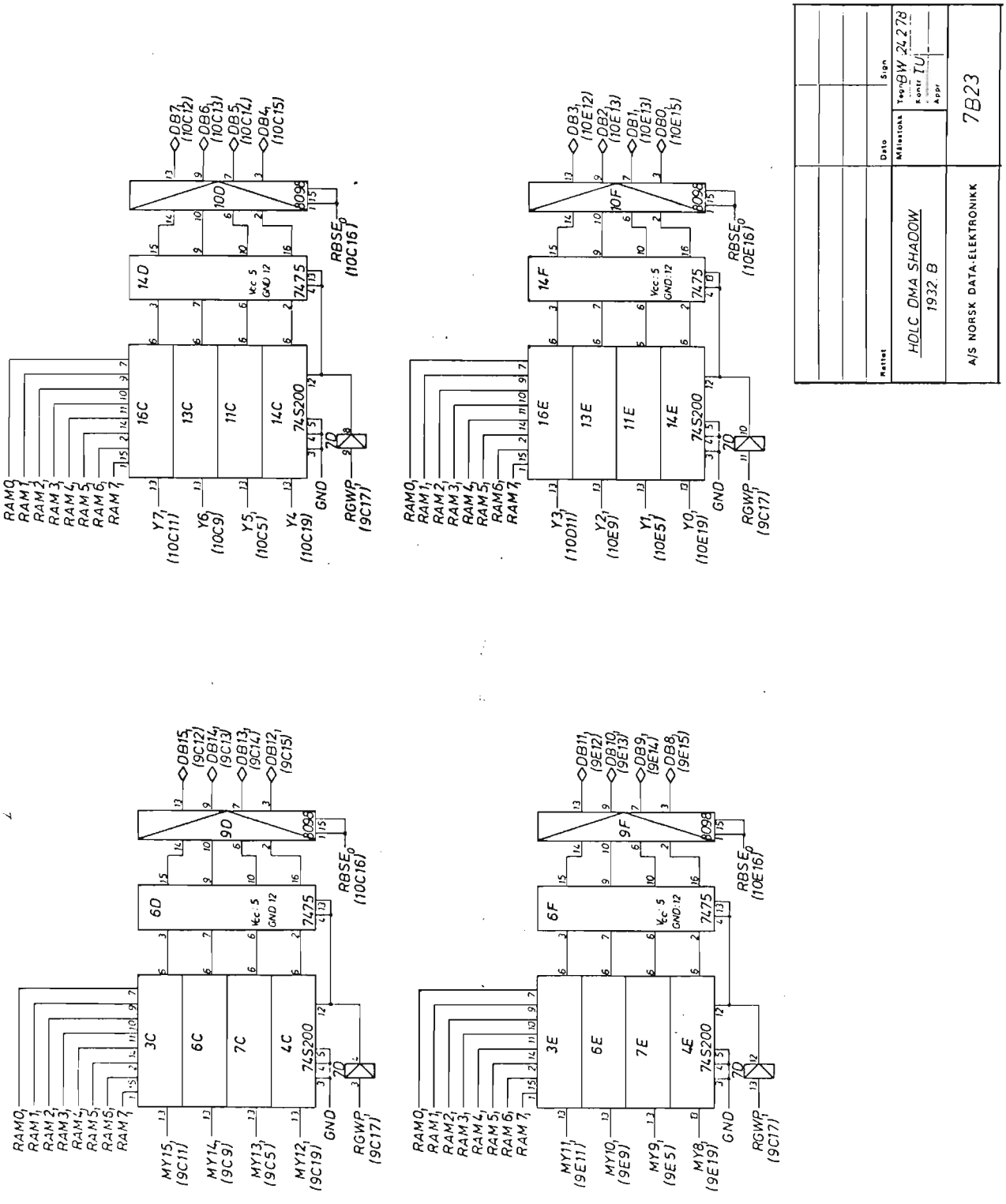
A-54



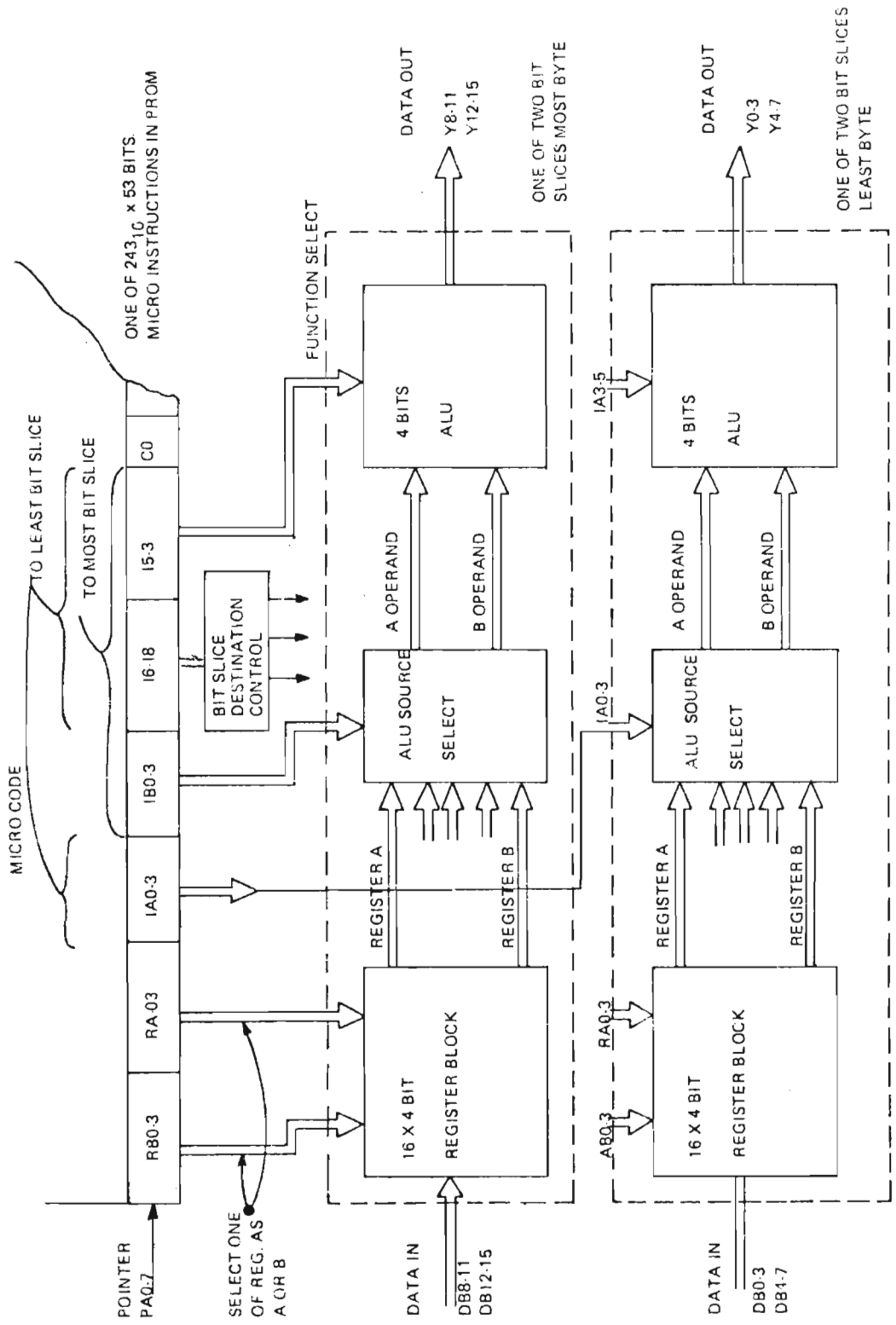
OPPDAT. T.O.M. ECO 10-511. E	30.5.78	TU BW
Rettet	Dato	Sign.
HOLC DMA CONTROL	Målestokk	Tegn. BW 13.10.77
1151 E Part 2		Kontr. TU
		Appr.
A/S NORSK DATA-ELEKTRONIKK	4A51 (2)	

ND-12.018.01

A-55



Retnet	Dato	Sign	
HOLC DMA SHADOW 1932 B	Milestolpe	Tegn BW 24 2 78 Kontr TU Appr	7823
A/S NORSK DATA-ELEKTRONIKK			



DMA PROCESSOR BLOCK DIAGRAM LOCATED ON HDLC DMA CONTROL IN POSITIONS 6B, 6D, 4B, 4D.

NORSK DATA A.S.
Lørenveien 57 - Postboks 163, Økern
OSLO 1

COMMENT AND EVALUATION SHEET

HIGH LEVEL DATA LINK CONTROL (HDLC) INTERFACE ND-12.018.01
NOVEMBER 1978

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM _____

_____

_____

– we make bits for the future

NORSK DATA A.S LØRENVEIEN 57 OSLO 5 NORWAY PHONE: 21 73 71 TELEX: 18284