CAMAC

CC-NORD-10 HARDWARE

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1 INTRODUCTION

CC-NORD-10 is a crate controller designed to interface CAMAC crates directly to the input/output bus of the NORD-10 computer. It is a two width module occupying the two rightmost positions of a standard CAMAC crate. (Positions 24 and 25.) For more general information, see CC-NORD-10 - General Information.

2 PROGRAMMING SPECIFICATION

2.1 CAMAC Addresses

The codes in Sections 2.2 to 2.8 are relevant for the crate with address 0. It is possible to have 16 crates on each NORD-10, with octal crate numbers from 0 to 17. The codes for any crate are found by adding $(C \cdot 100)_8$ to the codes given in Sections 2.2 to 2.8. The instruction format is:

IOX						Crate No.				Addr.			Function		
1	1	1	0	1	1	(4 bits)				(3 bits)			(3 bits)		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The address field is used to address 7 registers or commands. They are:

0	Dataway Z
1	Dataway C
2	Data Buffer
3	NAF Register
4	Graded LAM Pattern
5	Not used
6	Mask Register
7	Control and Status Register

The function bits are used to specify one of the following functions:

0	Read
1	Write
3	Clear all bits corresponding to 1 in the A register
5	Set all bits corresponding to 1 in the A register
7	Execute Dataway cycle

Not all functions are available on all addresses. The total address function table is:

		Function				
Address		Read	Write	Masked clear	Masked set	Execute DTW-cycle
Z	0					7
C	1					7
Data	2	0	1			7
NAF	3	0	1			7
LAM	4	0				
Mask	6	0	1	3	5	
Cost	7	0	1	3	5	

2.2 Dataway Z

IOX 2007

Generates a Dataway Z-cycle. Clears NAF register, Data buffer and COST register except bits 0, 12 and 13 (I, C and Z) in the crate controller and also clears the A register in the computer. All LAM sources are cleared due to the Z-cycle, so Graded LAM register is 0. The Mask register remains unchanged. Bits 0, 12 and 13 in COST register should be one after a Dataway Z-cycle.

2.3 Dataway C

IOX 2017

Generates a Dataway C-cycle. Clears NAF register and Data register in the controller, and also clears the A register in the computer. Bit 12 in COST register should be one after a Dataway C-cycle.

2.4 Data Buffer

The Data buffer is a 16 bits register.

2.4.1 Read Data Buffer

IOX 2020

Reads the content of the Data buffer into the A register in the computer.

2.4.2 Write Data Buffer

IOX 2021

Writes the content of the A register into the Data buffer.

2.4.3 Execute Data

IOX 2027

This instruction is split into three parts, dependent on the content of the NAF register at the moment the instruction is executed.

a) If the NAF code function bits indicate a read function, a dataway cycle is executed and the value of the dataway read lines (16 bits) are read into the Data buffer and also into the A register.

b) If the NAF code function bits indicate a write function, the content of the A register is written into the Data Buffer, and then enabled to the write lines during the dataway cycle.

c) If the NAF code function bits indicate a control function, the content of the A register is written into the Data Buffer, but the Data Buffer is not used or changed during the control function dataway cycle.

2.5 NAF Register

The NAF register is a 16 bits register, and the bits are:

Bit		
	0	F (1)
	1	F (2)
	2	F (4)
	3	F (8)
	4	F (16)
	5	A (1)
	6	A (2)
	7	A (4)
	8	A (8)
	9	N (1)
	10	N (2)
	11	N (4)
	12	N (8)
	13	N (16)
	14	X error enable
	15	Q error enable

2.5.1 Read NAF Register

IOX 2030

Reads the content of the NAF register into the A register.

2.5.2 Write NAF Register

IOX 2031

Writes the content of the A register into the NAF register.

2.5.3 Execute NAF

IOX 2037

Writes the content of the A register into the NAF register. Then a dataway cycle is executed, which may either be a Read, Write or Control cycle. If it is a Read cycle, the value of the Camac bus read lines are read into the Data register and the A register. If it is a Write cycle, the content of the Data register is enabled out on the Camac bus write lines.

2.6 Read Graded LAM Pattern

IOX 2040

Reads the value of the graded LAM into the A register (16 bits).

2.7 Mask Register

The Mask register is used, bit by bit, to enable the graded LAM to the interrupt handling logic. It is a 16 bits register.

2.7.1 Read Mask Register

IOX 2060

Reads the content of the Mask register into the A register.

2.7.2 Write Mask Register

IOX 2061

Writes the content of the A register into the Mask register.

2.7.3 Masked Clear Mask Register

IOX 2063

All bits in the A register which are one will clear the corresponding bits in the Mask register.

2.7.4 Masked Set Mask Register

IOX 2065

All bits in the A register which are one will set the corresponding bits in the Mask register.

2.8 Control and Status Register (COST Register)

The COST register is a 16 bits register. All bits are readable. All bits but bit 9 are writeable, and can also be separately cleared or set by Masked Clear and Masked Set instruction. Bits 12, 13, 14 and 15 are dataway status bits, and therefore clocked at S1 in a programmed dataway cycle. The control and status bits are:

Bit	0	I (Inhibit line)	C and S separate
	1	DMA enable	C and S same
	2	Continuous DMA enable	C and S same
	3	L demand enable	C and S same
	4	Error enable	C and S same
	5	RT enable	C and S same
	6	Interrupt level 10 select	C and S same
	7	Interrupt level 11 select	C and S same
	8	Interrupt level 12 select	C and S same
	9	LAM demand	Status
	10	Error demand	Status
	11	RT demand	Status
	12	C status	Status
	13	Z status	Status
	14	X response	Status
	15	Q response	Status

Comments:

Bit 0 is a control and status bit. The status bit is the OR function of the last written (set or cleared) value of the control bit and an external inhibit line. (Lemo socket on front.)

Bit 1 is used to enable (1) or block (0) DMA request to memory.

Bit 2 defines block mode (1) or interleaved mode (0) of DMA.

Bit 3 is the interrupt enable flip-flop for Look-at-me-interrupts. The Graded LAM lines are OR-ed together to a demand, and bit 3, if one, enables this demand to the level specified by bits 6, 7 and 8. (This bit is NOT cleared by IDENT. Instead the bit in the Mask register corresponding to the returned ident code is cleared.)

Bit 4 enables error interrupt to level 13. Error means expected Q and/or X response missing. This bit is cleared by IDENT when the interrupt is serviced.

Bit 5 enables external Real Time interrupt to level 13. (Lemo socket on front.) This bit is also cleared by IDENT when the interrupt is serviced.

Bit 6 selects interrupt level 10 for LAM demands.

Bit 7 selects interrupt level 11 for LAM demands.

Bit 8 selects interrupt level 12 for LAM demands.

Bit 9 is the OR function of masked Graded LAM.

Bit 10 is the OR function of expected and missing Q and X response.

Bit 11 is the latched external real time demand.

Bit 12 holds the status of the dataway C line during the last dataway cycle. (NB! also writeable.)

Bit 13 holds the status of the dataway Z line during the last dataway cycle. (NB! also writeable.)

Bit 14 holds the X-response of the last dataway cycle. (NB! also writeable.)

Bit 15 holds the Q-response of the last dataway cycle. (NB! also writeable.)

2.8.1 Read COST Register

IOX 2070

Reads the content of the COST register into the A register.

2.8.2 Write COST Register

IOX 2071

Writes the content of the A register, except bit 9, into the COST register.

2.8.3 Masked Clear COST Register

IOX 2073

All bits in the A register which are one, except eventually bit 9, will clear the corresponding bits in the COST register.

2.8.4 Masked Set COST Register

IOX 2075

All bits in the A register which are one, except eventually bit 9, will set the corresponding bits in the COST register.

2.9 IDENT

The serviced IDENT will clear the Mask register bit corresponding to the Graded LAM bit that generated the interrupt on level 10, 11 or 12. The format of the ident vector read into the A register is:

Bit	0	(1)	Coded Graded LAM level. (One of sixteen.)
	1	(2)	
	2	(4)	
	3	(8)	
	4		Crate number. (One of sixteen.)
	5		
	6		
	7		
	8		Always 1, indicating CAMAC

If more than one LAM source are requesting (on different levels) at the time, the IDENT instruction is executed, the one with the highest number is serviced.

Serviced IDENT on level 13 gives one in bit 8, indicating CAMAC. The Crate number field is the same as for LAM interrupts, and bits 0, 1, 2 and 3 are zero.

Serviced IDENT on level 13 clears the enable flip-flop (COST 4 or/and 5) for the interrupting source. (COST 10 or/and 11.)