CAMAC

CDMA NORD-10

CAMAC Direct Memory Access Controller

General Information

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1 INTRODUCTION

The Direct Memory Access Controller (CDMA) is a single width module with the necessary hardware to provide direct memory access to or from a CAMAC station.

Each CDMA can serve one CAMAC module in normal mode, or an array of modules in scan mode. Hence each module needing independent channel service it must have its private CDMA "daisy chained" to the LINK bus. The CDMA closest to the crate controller has highes priority and the furthest hase lowest priority.

The module contains:

- Memory Address register,
- Word Count register,
- NAF (CAMAC command) register,
- Control register, and
- Status register.

Furthermore it has the necessary control logic to communicate with the crate controller and other CDMA's along the LINK bus.

Channel access is requested at one of the two front panel trigger outputs. Triggers may be due to a LAM request or from a special sequence module managing complex data transfers.

2 PRINCIPLES OF OPERATION

A channel transfer may be performed in two modes of memory access and two modes of CAMAC module register access.

The Repeat Mode described in EUR 4100, Section 5.4.3.2, is not implemented. For Address Scan Mode (Section 5.4.3.1) and Stop Mode (Section 5.4.3.3), see Section 2.2.

2.1 Modes of Memory Access (CC control bit 2)

The channel may operate in Interleaved or Continous (Block) mode according to the CC - NORD-10 CAMAC crate controllers decision (control bit 2, set by program).

Interleaved mode is intended for single word and multiple asynchronous DMA transfer occuring at random times (Asynchronous communication between module and memory).

Continous (Block) mode is intended for fast block transfers with the Dataway cycle synchronized with the memory cycle of the CPU.

Blocks may also be transferred in Interleaved mode at an appreciable speed (about half the Continous (Block) speed).

As Interleaved transfer is asynchronous, idle Dataway and CPU time are avoided. This mode is therefore always recommended, unless very fast transfer is required.

Single word transfer in continous mode is also possible, but should be avoided as much CPU and Dataway time are vasted. This is due to the time required to prepare and terminate synchronization of the two cycles.

In Interleaved mode the CDMA loose control over the channel when one word is transferred, and must compete with higher priority controllers to retrieve it.

In Continous Block mode the same CDMA retains control of the channel untill end of block or removal of trigger (see Section 3.2) if no DMA in higher priority crates is requesting.

2.2 Modes of Register Access (CDMA control bit 2)

Single Register transfer is executed according to the content of the command (NAF) register within the CDMA. The transfer terminates when the specified word count is reached.

In Address Scan mode CAMAC registers at successive subaddresses in successive stations are accessed (see Section 2.3), according to the function F of the CDMA command register which start the scan at address NA. The scan terminates at an unoccupied station or at a specified word count, whichever occurs first.

Termination at an empty station is a safety measure, yet it may be avoided as explained in Section 2.6.

Stop mode may be considered as a premature termination of the Single Register mode (see Section 2.6).

Repeat mode is not implemented due to lack of security against system lockup, and the general uselessness of this mode except in special cases where the whole computer can be dedicated to completion of a single data transfer. Single Register transfer in Interleaved mode is a better choice in a practical real time system.

2.3 Interpretation of Q- and X-response

Error conditions may arise, depending on the expected Q- and X-response. Errors are enabled by bit 14 and 15 of command register, identical to the convention for PIO (see Section 4.3).

In the following Q* means ($Q+\overline{NAF15}$) and X* means ($X+\overline{NAF14}$). Hence if both X and Q errors are disabled (NA14 = NAF15 = 0), Q* and X* will always be true.

At S1 time of a channel transfer CDMA examine Q* and X*, and for each word transferred, the following actions take place:

Q* = X* = 1	Data valid. Increment Memory Address register. Decrement Word Count register. In Scan mode only: If A = 15; increment A. If A = 15; clear A, increment N.
Q* = 0, X* = 1 Q* = 1, X* = 0	Command accepted; Data invalid or Module invalid. (Not practical.) Except for Status, all registers are uneffected. Premature termination.
Q* = X* = 0	Data invalid; Command not accepted. Memory Address and Word Count unaffected. In Single Register mode: Premature termination. In Scan mode: If A = 0; clear A, increment N. If A = 0; normal termination.

2.4 Normal Termination

At normal termination the following status bits are affected:

COST 15 (X-FER OK) = 1
COST 14 (ERROR) = 0
COST 11 (LAM STATUS) = 1
COST 9 (BUSY) = 0

Since COST 10 (LAM Request enable) of necessity must be 1 (see Section 4.4) a LAM Request is also issued.

2.5 Premature Termination

In this case the status is:

COST 15 (X-FER OK) = 0
COST 14 (ERROR) = 1
COST 11 (LAM STATUS) = 1
COST 9 (BUSY) = 0
COST 10 · COST 11 (LAM REQUEST) = 1

2.6 Special Features

Whether the termination is normal or not, Memory Address register points to the next "unused" location, and Word Count register contains the number of words left in the block. Hence no "error holes" arise in the data buffer due to premature termination. It is thus possible to continue the transfer without modification of Word Count or Memory Address.

In order to continue, LAM must be cleared and reenabled, which sets BUSY (see Section 4.4).

Observe the possibility to implement Stop mode (EUR 4100, 5.4.3.3). Even though the Status register indicates error termination caused by Q 0, it it easy to identify the valid data buffer by means of Memory Address register.

In Scan mode empty stations will be ignored if NAF14 = NAF15 = 0, and hence the scan will continue untill Word Count reaches zero or the N register overflows. When N overflows, missing X error is automatically enabled and will cause termination owing to missing X response from station number 0 (!). (Commands with station numbers 0 and 24-31 are dummy.)

If scanning accidently runs riot, there is no risk that the content of the CDMA will be overwritten, as writing is inhibited during DMA - Dataway cycles.

However, one CDMA may be written into when the Dataway is under the command of another CDMA. E.g. one CDMA loads NAF commands from a core table into another CDMA, which thereupon executes them.

3 FRONT PANEL CONNECTORS

To obtain communication outside the Dataway, a number of connectors are mounted on the front panel.

3.1 LINK Bus in/out

Two CANNON 52 pins connectors are provided for entry and exit of the LINK bus. The IN connector is linked to the Crate controller or the OUT connector of the previous DMA or AFC controller.

In addition to several control signals the LINK bus furnishes the station address N to the control station (25) and the memory address to the NORD-10 I/O bus. The pin allocation is summarized in table 1.

3.2 Trigger Inputs

The four (active and low) 1K pullup trigger inputs are functionally equivalent. The two least significant bits of COST register enables one of the trigger inputs when the DMA module is BUSY (B). (Binary coded).

The significance of BUSY is stated in Section 4.4 and in the following.

Triggers may be levels or pulses of minimum width 50 ns. The resulting request is stored in a flip-flop untill the trailing edge of S1 (see Logic Diagram). If the trigger is removed before this time, the flip-flop is cleared. If still present, the request is maintained, asking the computer for another cycle. Hence the decision whether it should be removed or not, should be made at latest as a response to the leading edge of S1.

When BUSY → 0 any existing request is cleared, and all triggers appearing whilst BUSY 0 are ignored. Consequently an unprocessed trigger pulse will not be remembered for subsequent handling when BUSY 1 reappears.

In continous (Block) mode the trigger should be present until termination of block for economy of CPU and Dataway time (see Section 2.1).

3.3 BUSY Output

The BUSY active low-TTL output may be utilized by trigger logic to detect termination. (READY FOR TRIGGER) (Lemo socket at front)

Pin	Signal	Signal Standard
1	N1	OC-TTL
2	N2	- " -
3	N4	- " -
4	N8	- " -
5	N16	- " -
6	GND	
7	RQAFC 1	Not used by CDMA
8	GR AFC 1	- " -
9	GND	
10	GND	
11	RQAFC 2	Not used by CDMA
12	GRAFC 2	- " -
13	RQ DMA	TTL
14	GR DMA (DATAWAY)	"
15	GR CPU	"
16	CHAN READY	"
17	GND	
18	INPUT	"
19	BA 0 (S)	TSL
20	BA 0 (R)	"
21	BA 1 (S)	"
22	BA 1 (R)	"
23	BA 2 (S)	"
24	BA 2 (R)	"
25	BA 3 (S)	"
26	BA 3 (R)	"
27	BA 4 (S)	"
28	BA 4 (R)	"
29	BA 5 (S)	"
30	BA 5 (R)	"
31	BA 6 (S)	"
32	BA 6 (R)	"

CONT.

Pin	Signal	Signal Standard
33	BA 7 (S)	TSL
34	BA 7 (R)	"
35	GND	"
36	Not used	"
37	BA 8 (S)	"
38	BA 8 (R)	"
39	BA 9 (S)	"
40	BA 9 (R)	"
41	BA 10 (S)	"
42	BA 10 (R)	"
43	BA 11 (S)	"
44	BA 11 (R)	"
45	BA 12 (S)	"
46	BA 12 (R)	"
47	BA 13 (S)	"
48	BA 13 (R)	"
49	BA 14 (S)	"
50	BA 14 (R)	"
51	BA 15 (S)	"
52	BA 15 (R)	"

Table 1: Pin Allocation for LINK Bus Connectors

4 REGISTERS

The least significant bit of the registers is designated 0 to conform with the NORD-10 notation. Hence Dataway lines R1 and W1 relate to bit 0 etc.

X* and Q* are used in the sense stated in Sections 2.3 and 4.3.

4.1 Word Count (WCR) Register

This 12 bits register is initially loaded with the desired block length. It is decremented after each valid word transferred (see Section 2.3). Accordingly it contains the number of words left in the block at all times. Word Count 0 will cause termination of transfer.

Observe that the block length will be equal to the content of the Word Count register, and not Word Count + 1. E.g. Word Count = 377_8 will cause 255_{10} words to be transferred.

Note that only Word Count - 0 is detected as termination. Hence a transfer starting with Word Count = 0 will be interpreted to signify a block length of 10000_8.

For maintenance purposes a jumper may be inserted on the printed circuit board to prevent Word Count decrement and Memory Address increment.

Read	:	F(0) A(0)
Write	:	F(16) A(0)
Decrement	:	$Q^* \cdot X^* = 1$, F(25) A(0) $\cdot \overline{\text{COST10}}$
Clear	:	Z

If BUSY 1, F(25) A(0) requests a cycle, and Word Count is decremented (and Memory Address incremented) only if the resulting Q and X response indicate "data valid".

4.2 Memory Address (MAR) Register

This 16 bit register holds the memory address of the next word to be transferred to/from memory. It is incremented after each valid word of data transferred (see Section 2.3).

When preparing a transfer, the register is loaded with the start address of memory data buffer.

Read	:	F(0) A(1)
Write	:	F(16) A(1)
Increment	:	$Q^* \cdot X^* = 1$
Clear	:	Z

4.3 CAMAC Command (NAF) Register

The CAMAC command to be executed during a channel transfer is contained in this 16 bits register. The format is:

Bit 0:	F1
" 1:	F2
" 2:	F4
" 3:	F8
" 4:	F16
" 5:	A1
" 6:	A2
" 7:	A4
" 8:	A8
" 9:	N1
" 10:	N2
" 11:	N4
" 12:	N8
" 13:	N16
" 14:	X error enable
" 15:	Q error enable

The sense of bits is identical to that defined for Crate Controller NAF register. (CC - NORD-10.)

In Scan mode A and N are modified after each Dataway cycle according to the expected Q and X response (see Section 2.3).

Bits 14 and 15 enable error termination to occur if X or Q response is missing. I.e. error = $\overline{Q} \cdot NAF15 + \overline{X} \cdot NAF14 = \overline{Q^*} + \overline{X^*}$. Error = 0 means "data valid". In Scan mode however, $Q^* = X^* = 0$ has a special meaning as stated in Section 2.3.

Read	:	F(0) A(3)
Write	:	F(16) A(3)
Clear	:	Z

In Scan mode:

Clear A	:	$Q^* \cdot X^* \cdot A(15) = 1$, $\overline{Q}^* \cdot \overline{X}^* \cdot \overline{A(0)} = 1$
Increment A:		$Q^* \cdot X^* \cdot \overline{A(15)} = 1$
Increment N:		$Q^* \cdot X^* \cdot A(15) = 1$, $\overline{Q}^* \cdot \overline{X}^* \cdot \overline{A(0)} = 1$

4.4 Control and Status (COST) Register

This is a 10 bits register which governs the autonomous action of the module.

Read	:	(All bits) :	F(0) A(2)
Write	:	(Bits 0-2):	F(16) A(2)

Set and Clear are to a certain extent controlled by program as stated in the following.

	Set	Clear	Test
Bit 0: Trig 1 enable		Z	
Bit 1: Trig 2 enable		Z	
Bit 2: Scan enable		Z	
Bit 3-8: Not used			
Bit 9: Transfer BUSY	F(26) A(0) if LAM status cleared	F(10) A(0), F(24) A(0), Z	
Bit 10: LAM Request enable	F(26) A(0)	F(10) A(0), F(24) A(0), Z	
Bit 11: LAM Status		F(10) A(0), Z	
Bit 12: Dataway X-response	F(10) A(0), Z		
Bit 13: Dataway Q-response	F(10) A(0), Z		
Bit 14: Q+X response ERROR		F(10) A(0), Z	F(27) A(1)
Bit 15: Transfer OK (complete)		F(10) A(0), Z	

Description of the individual bits:

Bit 0: Enables Trigger input 1 to set Request flip-flop

Read : F(0) A(2)

Write : F(16) A(2)

Clear : Z

Bit 1: Enables Trigger input 2 to set Request flip-flop

Read : F(0) A(2)

Write : F(16) A(2)

Clear : Z

Bit 2: Enables CDMA to operate in Scan mode

Read : F(0) A(2)

Write : F(16) A(2)

Clear : Z

Bit 9: Indicates that CDMA is ready for channel transfer and that triggers are accepted.

COST9 = COST10 · $\overline{\text{COST11}}$

Read : F(0) A(2)

Set : F(26) A(0) if COST11 = 0

Clear : F(10) A(0), F(24) A(0), Z, COST14 = 1, COST15 = 1

Test : F(27) A(0); generates Q = 1 if COST9 = 1

Bit 10: Enables LAM status to become a LAM request. Setting of this bit is necessary to execute a channel transfer.

Read : F(0) A(2)

Set : F(26) A(0)

Clear : F(10) A(0), F(24) A(0), Z

Bit 11: Is the LAM status indicating that termination has occurred?

COST11 = COST14 + COST15

Read : F(0) A(2)

Set : COST14 = 1, COST15 = 1

Clear : F(10) A(0), Z

Bit 12: Is the X-response of the last DMA-Dataway cycle under command of this CDMA?

Read : F(0) A(2)

Write : Status of X-line at S1

Set : F(10) A(0), Z

Bit 13: Is the Q-response of the last DMA-Dataway cycle under command of this CDMA?

Read : F(0) A(2)

Write : Status of Q-line at S1

Set : F(10) A(0), Z

Bit 14: Is set if the expected Q or X response of the DMA-Dataway cycle is missing, LAM source.

Read : F(0) A(2)

Set : $\overline{\text{COST13}}$ · NAF15 1, $\overline{\text{COST12}}$ · NAF14 = 1

Clear : F(10) A(0), Z

Test : F(27) A(1); generates Q 1 if COST14 = 1

Bit 15: Is set on normal termination of a transfer, LAM source.

Read : F(0) A(2)

Set : Word Count → 0, $\underline{COST2} \cdot \overline{COST12} \cdot \overline{COST13} \cdot A(0) = 1$
$(A(0) = \overline{NAF5} \cdot \overline{NAF6} \cdot \overline{NA\ F7} \cdot \overline{NAF8})$

Clear : F(10) A(0), Z

5 OTHER SIGNALS PARTLY CONTROLLED BY PROGRAM

5.1 LAM Request

Informs the computer that termination has occurred, whether normal or premature.

LAM request = LAM status · LAM request enable.

Note: As LAM request must be enabled to allow channel transfer, a LAM request is always issued at termination.

Read : As part of Graded LAM status in Crate Controller

Set : COST10 ·COST11 = 1

Clear : F(10) A(0), F(24) A(0), Z

Test : F(8) A(0), generates Q = 1 if LAM request = 1

5.2 DMA Request Flip-Flop

It holds the request for the channel. It is primarily set by external triggers (see Section 3.2), but may be set by program for test purposes.

Set : Selected TRIGGER ·COST9, F(25) A(0) ·COST9

Clear : COST9 = 0, End of S1 if trigger is absent.

If COST10 = 0, F(25) A(0) decrements Word Count only.

6 PROGRAMMING SPECIFICATIONS (SUMMARY)

6.1 Commands decoded

F(0) A(0) :	READ WCR
F(0) A(1) :	READ MAR
F(0) A(2) :	READ COST
F(0) A(3) :	READ NAF
F(8) A(0) :	TEST LAM REQUEST, Q = 1 IF SET
F(10) A(0) :	CLEAR LAM STATUS, ERROR STATUS, TRANSFER OK STATUS DISABLE LAM REQUEST SET Q STATUS, X STATUS
F(16) A(0) :	WRITE WCR
F(16) A(1) :	WRITE MAR
F(16) A(2) :	WRITE COST
F(16) A(3) :	WRITE NAF

NOTE! WRITING IS NOT EXECUTED IF COMMAND IS DUR TO INTERNAL NAF REGISTER

F(24) A(0) :	DISABLE LAM REQUEST
F(25) A(0) :	REQUEST DMA CYCLE IF DMA BUSY. DECREMENT WORD COUNT IF LAM DISABLED
F(26) A(0) :	ENABLE LAM REQUEST
F(27) A(0) :	TEST BUSY STATUS, Q = 1 IF SET
F(27) A(1) :	TEST ERROR STATUS, Q = 1 IF SET

6.2 Other Command

Z :	CLEAR WCR, MAR, NAF, COST EXCEPT BITS 12-13 SET COST BITS 12-13

6.3 Response

X :	TO ALL DECODED FUNCTIONS
Q :	TO ALL READ FUNCTIONS TO ALL WRITE FUNCTIONS PROVIDED THE COMMAND IS NOT DUE TO INTERNAL NAF REGISTER TO TEST FUNCTIONS F(8) A(0), F(27) A(0) AND F(27) A(1)

6.4 Control Signal

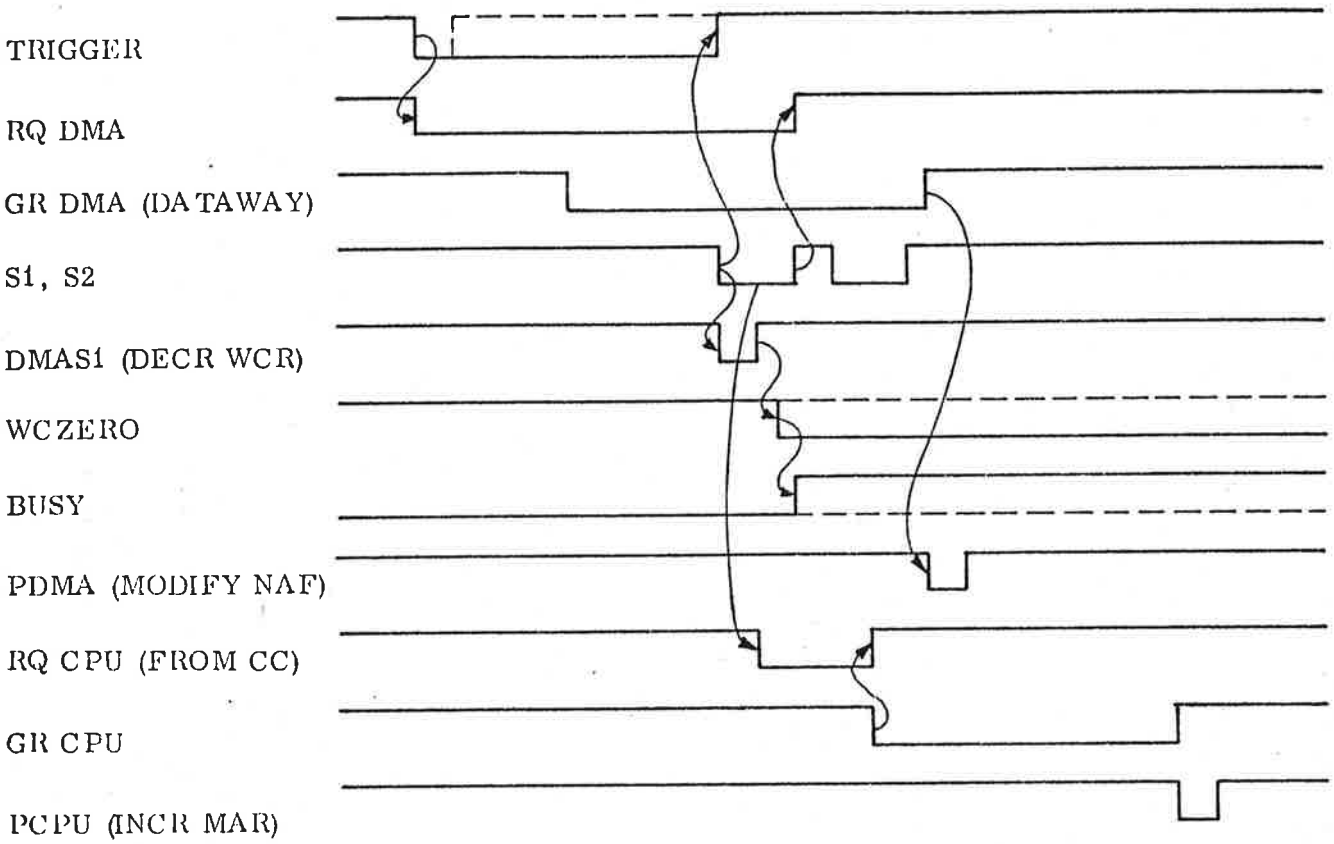
L : RAISED ON NORMAL OR PREMATURE TERMINATION

Warning

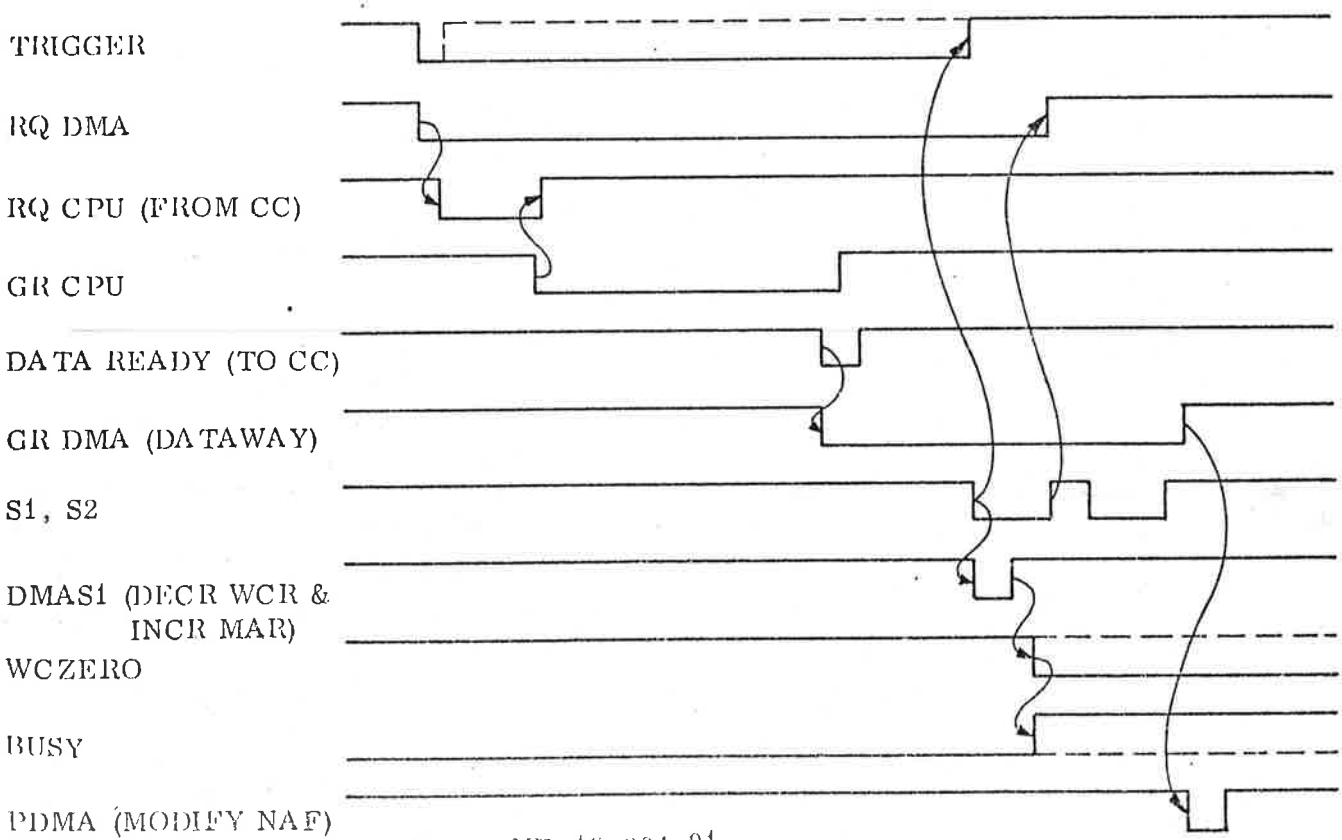
IF TRANSFER IS STARTED WITH WORD COUNT = 0, THE BLOCK LENGTH IS TAKEN TO BE 4096_{10}.

7 TIMING DIAGRAM (INTERLEAVED MODE)

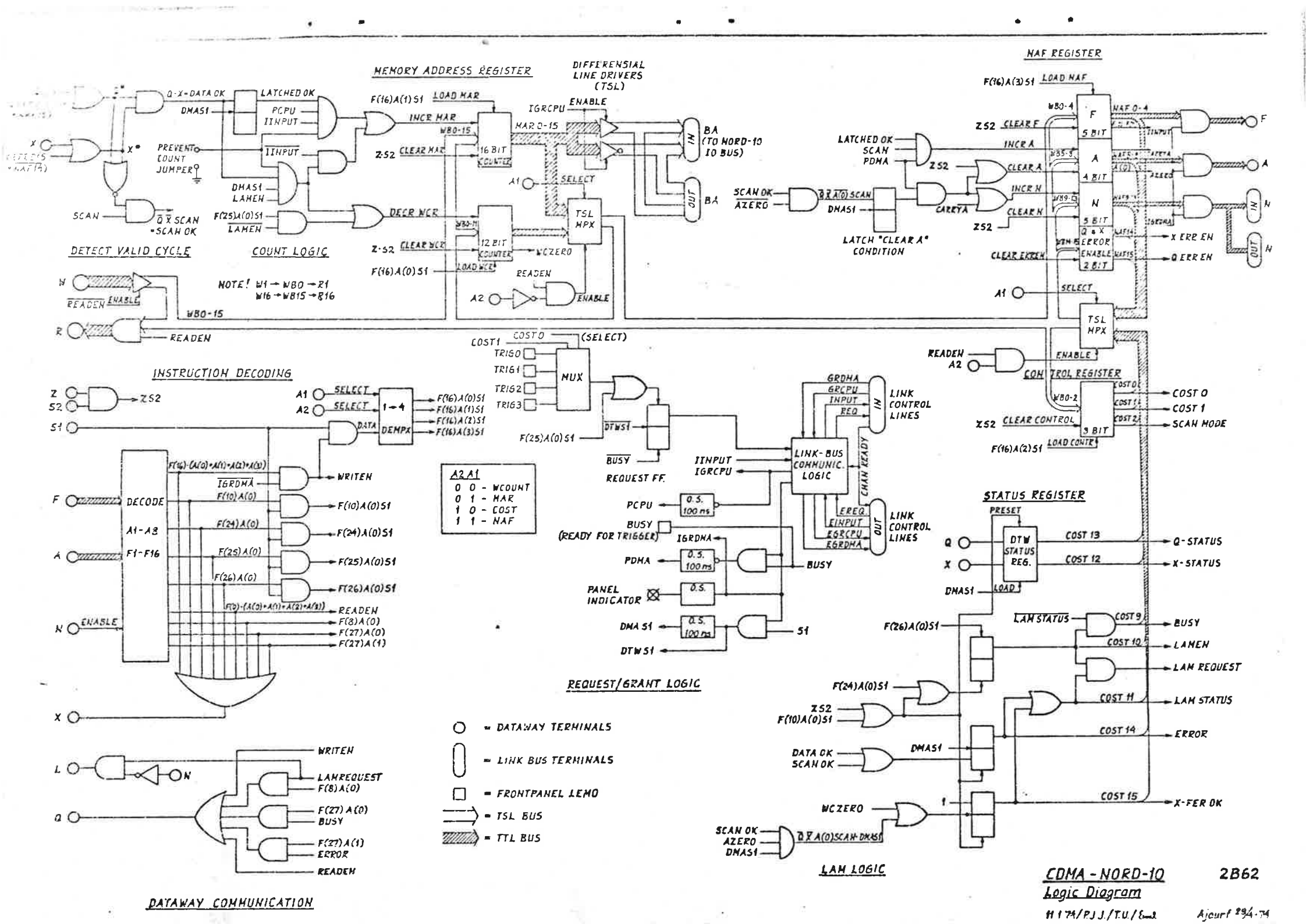
7.1 Input to CPU

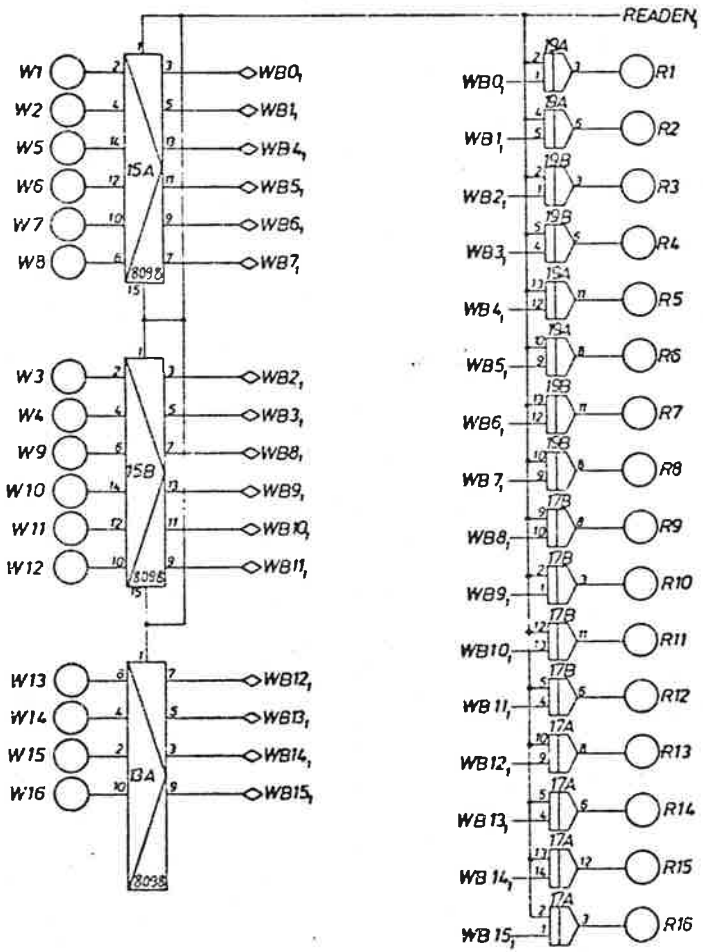


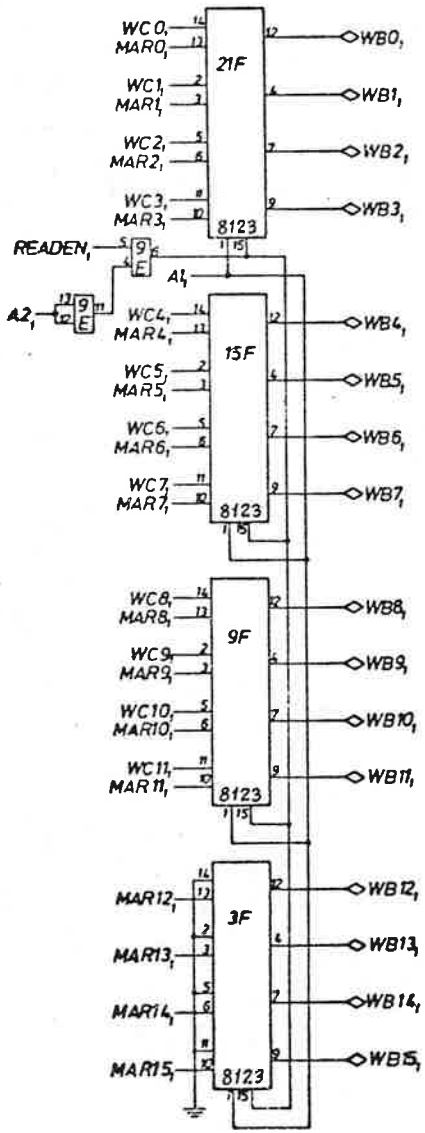
7.2 Output to CAMAC

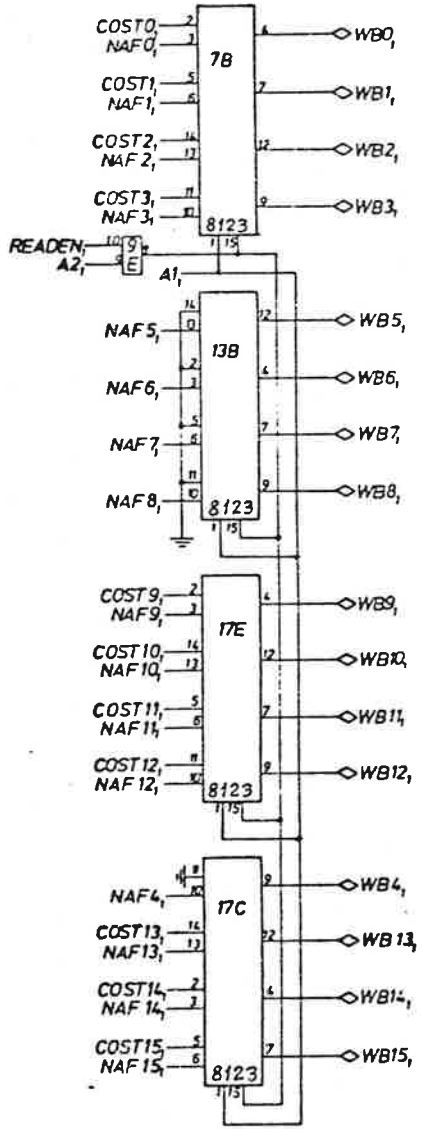


8 LOGIC DRAWINGS


MEMORY ADDRESS REGISTER
DIFFERENSIAL LINE DRIVERS (TSL)
NAF REGISTER
DETECT VALID CYCLE
COUNT LOGIC
NOTE! W1 → WB0 → R1
W16 → WB15 → R16
INSTRUCTION DECODING
DECODE
MUX
CONTROL REGISTER
STATUS REGISTER
LINK-BUS COMMUNIC. LOGIC
REQUEST/GRANT LOGIC
DATAWAY COMMUNICATION
LAM LOGIC
A2 A1
0 0 - WCOUNT
0 1 - MAR
1 0 - COST
1 1 - NAF
= DATAWAY TERMINALS
= LINK BUS TERMINALS
= FRONTPANEL LEMO
= TSL BUS
= TTL BUS
CDMA - NORD-10
Logic Diagram
2B62
H174/PJJ/TU/Emd
Ajourf 23/4-74







Rettet	Dato	Sign.
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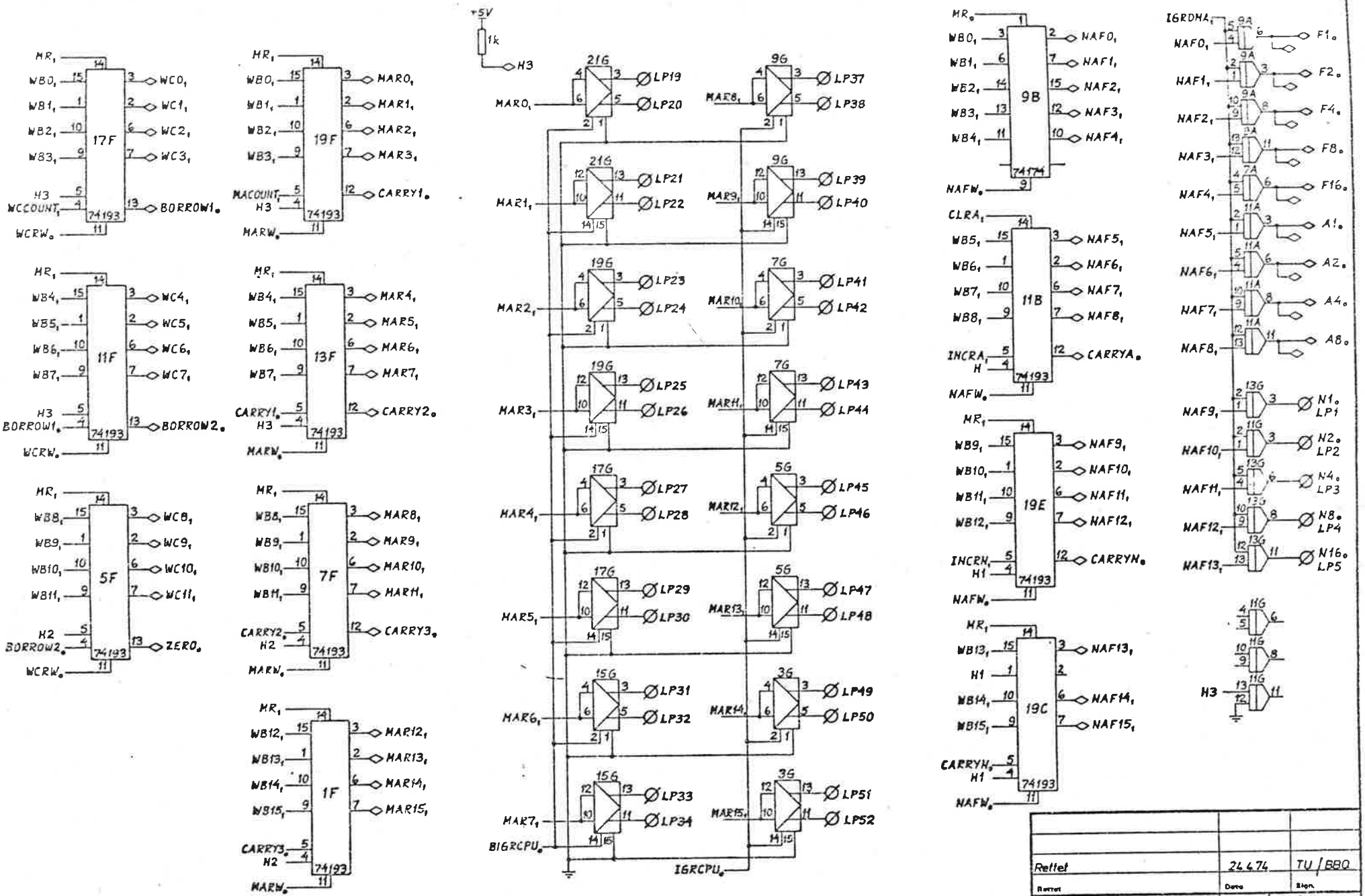
A/S NORSK DATA-ELEKTRONIKK	5B24	



Rettet	24.4.74	TU / BBO
Retter	Dato	Sign.
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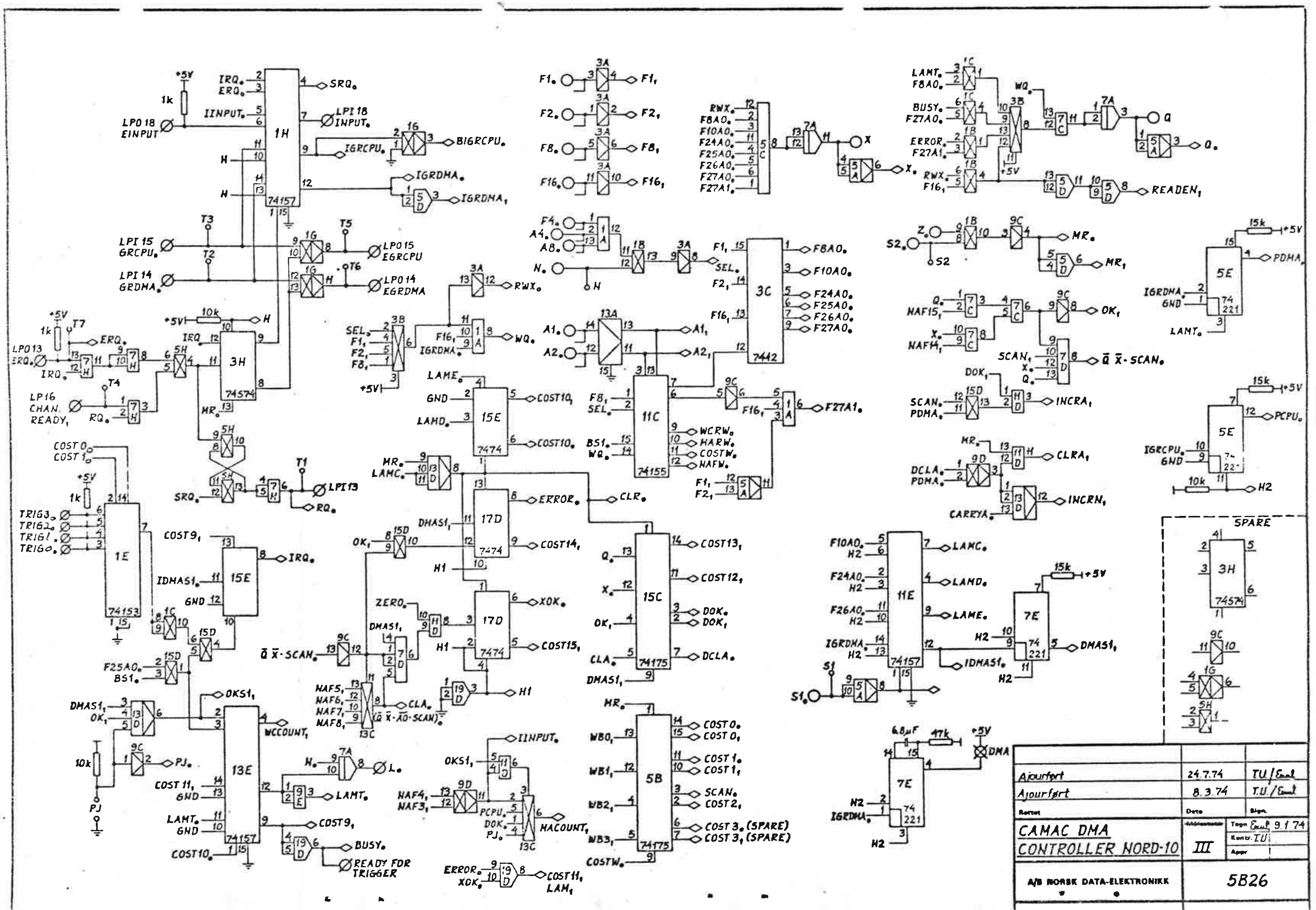
A/S NORSK DATA-ELEKTRONIKK	5B25	


Ajourført 24.7.74 TU/Emil
Ajourført 8.3.74 T.U./Emil
Rettet
Dato
Sign.
Tegn Emil 9.1.74
Kontr. TU
Appr
CAMAC DMA
CONTROLLER NORD-10
III
A/S NORSK DATA-ELEKTRONIKK
5B26