Floppy and Streamer Controller 3106/3112

ND-11.021.1 EN

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Preface:

THE PRODUCT

This is a microprocessor-based controller/formatter which performs control functions and data transfer between the CPU and a floppy disk drive or a streaming tape drive. The controller/formatter consists of an interface towards a ND-100 bus, a complete floppy disk controller, and a QIC-02 streaming tape cartridge, all based on an 8 bit microprocessor.

A maximum of four Streaming Tape Drives and four Floppy Disk drives may be connected to the controller.

Floppy and Streamer Controller 8" - Card no. 3106 : ND-630
Floppy and Streamer Controller 8" and 5 1/4" - Card no. 3112 : ND-317

THE READER

This manual is intended for maintenance-, workshop- and other personnel needing a description of the Floppy and Streamer Controller.

PREREQUISITE KNOWLEDGE

Basic knowledge of the old 3027 controller is recommended. This knowledge can be obtained by studying Norsk Data manuals.

THE MANUAL

The manual is a detailed describtion of the Floppy- and Streamer Controller, provided into 11 chapters. It also contains descriptive block diagrams and logic block interconnections in the appendixes. It describes both the 8" floppy and streamer controller - card no. 3106, and the 8" and 5 1/4" floppy and streamer controller - card no. 3112. Where no card number is specified in the text, the same applies to both cards.

RELATED MANUALS

Floppy Disk Controller ND-11.015

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CHAPTER 1

INTRODUCTION TO THE FLOPPY AND STREAMER CONTROLLER

1 INTRODUCTION TO THE FLOPPY AND STREAMER CONTROLLER

The FLOPPY DISK CONTROLLER can read/write on single/double density and single/double sided diskettes. Data transfer and exchange of commands/status are performed with DMA (Direct Memory Access).

The controller is designed and built around the

- Z80A microprocessor
- AM9517 DMA controller
- FD1797 floppy disk controller

The controller is compatible with previous single sided controllers. For "stand-alone" use, a new version of FLO-MON (FLOppy-MONitor-2010F or newer) must be dumped on the diskette.

Possibilities of simulating DMA-loads are implemented. However, due to the microprogram in the ND-100, this can only be performed from terminal (21560$) (DMA-load), and not by setting the ALD (Automatic Load Descriptor) selector on the CPU (Central Processor Unit) module.

When DMA-load is performed, "the first page" on floppy is dumped to "first page" on the ND-100. It is also possible to "load" BPUN-files (Binary PUNch) of maximum 64 Kwords directly from the floppy by pressing LOAD.

There is a new driver program in the ND-100 SINTRAN, which is smaller than those used in previous floppy controllers.

The main functions of the floppy and streamer controller are shown in the high level block diagram on page 4 - for a physical description of the controller, see appendix C for the 8" (card no. 3106), and appendix E for the 8" and 5 1/4" (card no. 3112).

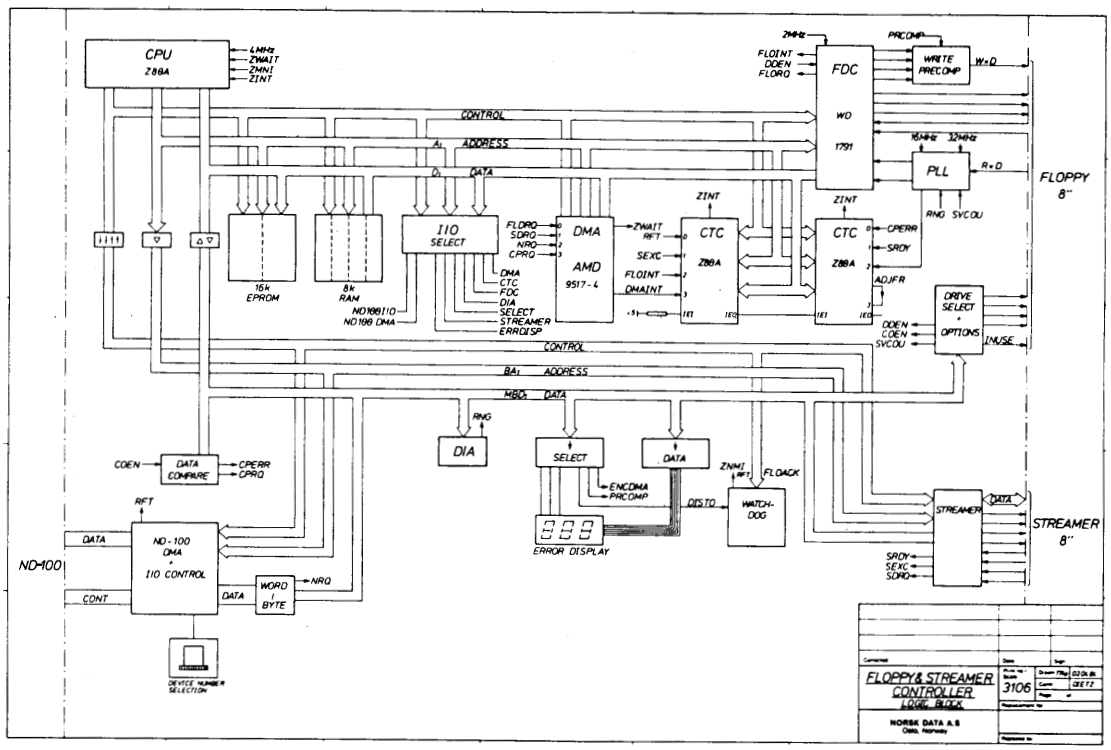


Fig. 1. High Level Block Diagram of the Floppy and Streamer Controller

The controller works in a 'mail box' scheme. This is to say, that very little of the information (command) is given to the controller by means of IOXs. Instead an area in the ND-100 memory is used to pass the details concerning the commands. See figure 2.

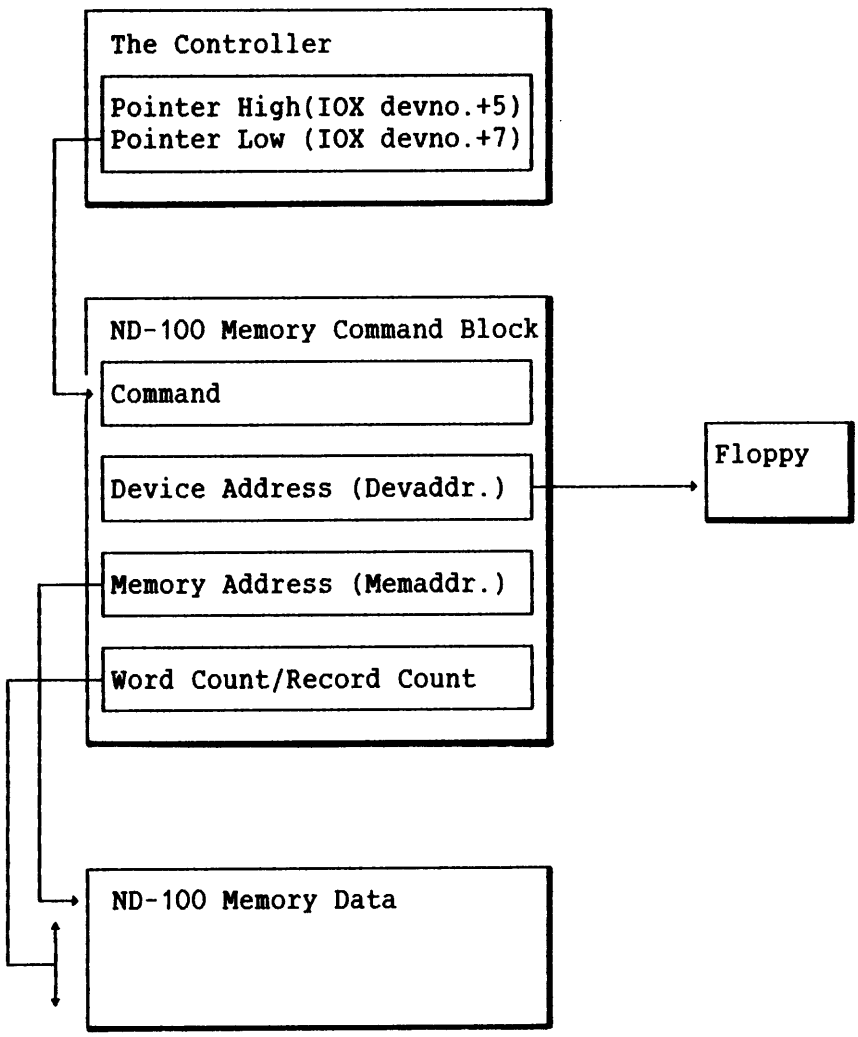


Fig. 2. Programmer's Model of the Controller

When activating for read/write operations follow these steps:

1) Enter command block to the ND-100 memory. (Consisting of 6 words - command - floppy disk address - DMA address - Word count/number of sectors.)

2) Load command block pointers to the controller by means of IOX. (IOX DEVNO+5 , IOX DEVNO+7 .)

3) Activate controller by loading the control word.

When the control word is loaded, an interrupt is given to the Z80 processor. A DMA transfer of the command block from the ND-100 to the floppy controller's local memory is initiated. The command is analyzed and executed.

When data transfer has terminated, the status block of 6 words (1 word = 16 bits) is transferred to the ND-100 and placed in memory after the command block.

Finally the "READY-FOR-TRANSFER" signal is set, which also gives an interrupt to the ND-100 (if interrupt is enabled).

The controller is designed to handle both floppy and streamer. Used as floppy controller it fully replaces the older 3027 controller. Up to 4 floppy drives and 4 streamer drives may be connected at the same time. The selection between floppy and streamer is made by a bit in the hardware control word.

The 3112 controller is also capable of handling 5 1/4" floppies. Apart from this it is equal to the 3106 controller (it replaces the 3106 controller).

CHAPTER 2

HARDWARE

2 HARDWARE

2.1 Standard Hardware

The controller is equipped with standard IOX and DMA logic.

It is possible to choose between the device numbers 1560 and 1570. They are represented by 0 and 1, respectively, on the thumb wheel.

Conversion of 16-bit words to bytes is done during the DMA transfer of a sequence made up of a PAL10L8 (Programmable Area Logic which is of the PROM-type) and two flip-flops. Internally, this module has an eight- bit bus. Normally, there will be 8 Kbyte PROMs and 4 Kbyte RAMs, both of which can be easily extended to 8 Kbytes by adding more circuits.

A CMOS counter controls the timeout function (watchdog). It is set when loading the control word, and reset each time data is transmitted between the floppy drive and the controller. Timeout occurs after approximately 10 seconds.

As the old 3027 controller, this controller has a hardware compare circuit which verifies data read from or written to the diskette.

The control part of the floppy is taken care of mainly by FD1797 (floppy controller) circuits delivered by Western Digital. These circuits carry out most of the control functions. However, the synchronizing and separating of data and clock must be done outside this circuitry, in a data separator.

The data separator consists of an analog-phase locked loop, and some circuitry to compensate for the loss of time margin in the floppy control circuit.

Precompensation is done outside FD1797 and may be turned ON/OFF from the processor.

CHAPTER 3

PROGRAMMING SPECIFICATIONS

3 PROGRAMMING SPECIFICATIONS

3.1 IOX Numbers

Devno + 0	- Read Data
Devno + 1	- Not Used
Devno + 2	- Read Status (see note below)
Devno + 3	- Load Control Word
Devno + 4	- Read Status (see note below)
Devno + 5	- Load Pointer High (Bit 16-23)
Devno + 6	- Not Used
Devno + 7	- Load Pointer Low/Load Data

Unused IOXs do not give an IOX error.

The IOXs devno + 5 and devno + 7 are used to form the pointer to the location in the ND-100 memory where the controller finds the Command block. In tests, these IOXs are given direct meaning in different tests.

NOTE !

Reading either status gives the same result. They are duplicated to make it possible for microprograms in the ND-100 CPU to perform both Binary Format Load and Mass Storage Load (1560& and 21560)

3.2 Thumb Wheel Settings

0	-	Devno 1560
1	-	Devno 1570
2-15	-	Not used

3.3 Command Block (CB) with Status Part

In the ND-100 Memory:

		15 8	7 0
CB	+ 0	Command word	
	+ 1	Device address 15-0	
	+ 2	Devaddr 23-16	Memaddr 23-16
	+ 3	Memaddr 15-0	
	+ 4	Options	Word Count 23-16
	+ 5	Word Count/Record Count	
	+ 6	Status 1	
	+ 7	Status 2	
	+10		Last addr 23-16
	+11	Last Memory address 15-0	
	+12	Not used	Rem. Words 23-16
	+13	Remaining Words 15-0	

In Z80 Memory.

7 4	3 0
0	1
2	3
4	5
6	7
8	9
A	B
C	D
E	F
10	11
12	13
14	15
16	17

POINTS TO NOTE : Bytes not used should be zero!

CB + 6 to CB + 13 Is the Status-part of the Command Block and is written by means of DMA from the Controller at the end of a Command execution.

DEVICE ADDRESS : This is the logical address on the floppy where the operation will start. Logical address is sector count from the beginning of the floppy.

This parameter is not used when streamer is used.

MEMORY ADDRESS : This is the location in the ND-100 where data will be read/written.

OPTIONS :

Bit	Meaning
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Word/record count.

BIT 15: Word/Record Count = 1 indicating Word Count
Word/Record Count = 0 indicating Record Count

Reserved and unused bits should be set to ZERO.

WORD/RECORD COUNT: This is the amount that the operation should be performed upon. The amount is interpreted either as word count or record count by the contoller. The controller looks at the options field to determine how to interpret.

3.4 Status Word 1

BIT	Meaning
0	Not used
1	RFT (Ready For Transfer) - Interrupt enabled
2	Device active (same as hardware status word)
3	Device ready for transfer
4	Or of errors
5	Deleted record
6	Retry on controller
7	Hard-error
8	Not used
9	→ Error code from controller (see page 22)
10	
11	
12	
13	
14	
15	Not used

3.5 Status Word 2

3.5.1 Status word 2 - Streamer

BIT	Meaning
0	A copy of the SS register (Streamer Status).
1	
2	
3	
4	
5	
6	
7	
8	If error in PREVIOUS TRANSFER after giving interrupt, this byte holds the ERROR-CODE. Zero means no error.
9	
10	
11	
12	
13	
14	
15	

3.5.2 Status word 2 - Floppy

3.5.2.1 Card no. 3106

BIT	Meaning
0	Bytes/Sector Double sided Double density → Format read from diskette valid for read format command or when error 12 (format mismatch).
1	
2	
3	
4	Not used
5	
6	
7	
8	Selected unit
9	
10	Not used
11	
12	
13	
14	
15	

3.5.2.2 Card no. 3112

BIT	Meaning
0	
1	→ Bytes/Sector
2	Double sided
3	Double density → Format read from diskette valid for read format command or when error 12 (format mismatch).
4	5 1/4" Drive
5	Non standard
6	96 tpi
7	Not used
8	
9	→ Selected unit
10	
11	
12	→ Sector/track
13	
14	
15	Not used

3.6 Hardware Control Word

IOX (Devno + 3)

BIT	Meaning
0	Not used
1	Enable interrupt on RFT
2	Activate Autoload
3	Test Mode
4	Device Clear
5	Enable Streamer
6	Not used
7	Not used
8	Fetch Command & Execute
9	
10	
11	
12	→ See table on the
13	following page
14	
15	

Table 1. Relation between the Bit 2, 3, 5 and 8 in the Control Word

BIT / STATE	2	3	5	8	Controller action	Meaning of BITS 9 -15
I	1	X	X	X	Load floppy monitor	Not used - should be zero
II	0	1	X	X	Run controller in test mode	Specifies test - see 30
III	0	0	0	1	Command is fetched from the ND-100 and executed on the specified floppy drive.	bit 9: Step rate " 10: In use " 11: Disable preomp " 12: 96 TPI " 13: Compare " 14: Reserved " 15: Reserved
IV	0	0	1	1	Command from mem. is executed on streamer	Not used - should be zero.

3.7 Hardware Status Word

IOX (Devno + 2 or 4)

BIT	Meaning
0	Not Used
1	RFT Interrupt Enabled
2	Device Active
3	Device Ready for Transfer
4	OR of Errors
5	Not Used
6	Streamer Active
7	Hard Error - DMA Transfer
8	Reserved
9	
10	
11	
12	
13	
14	Streamer interface
15	Dual density controller

3.8 Command Word

3.8.1 Command word streaming tape

15	14 13 12	11 10 9 8	7 6	5 4 3	2 1 0
Not used		Record length	Unit	Function	

BITS 0-5:	OCTAL	HEXA	FUNCTION
	0	0	Read data
	1	1	Write data
	7	7	Erase tape
	10	8	Advance to EOT (End Of Tape)
	12	A	Write EOT
	13	B	Rewind to BOT (Beginning Of Tape)
	20	10	Read status
	36	1E	Read extended status
	56	2E	Check cartridge (read and test CRC - Cyclic Redundancy Code)
	57	2F	Test cartridge capacity (write)
	70	38	Retention cartridge
	74	3C	Read data continues
	75	3D	Write data continues
BITS 6-7:	0	0	Select unit 0
	1	1	Select unit 1
	2	2	Select unit 2
	3	3	Select unit 3
BITS 8-11:			Record length
	0	0	512 Bytes/record.
	1-17	1-F	Reserved
BITS12-15:	0-17	0-F	Not used (should be zero)

The various functions are described in chapter 4.

3.8.2 Command word floppy

3.8.2.1 Card no. 3106

15 14	13 12	11 10 9 8	7 6	5 4 3	2 1 0
Copy dest	Not used	Format	Unit	Function	

BITS 0-5:	Octal	Hex.	Function
	0	0	Read data
	1	1	Write data
	2	2	Find EOT (read without data transfer)
	5	5	Write EOT
	20	1E	Read Status
	41	21	Format floppy
	42	22	Read format
	43	23	Read deleted record
	44	24	Write deleted record
	54	2C	Copy floppy
	55	2D	Format track
	56	2E	Check floppy
BITS 6-7:	0	0	Select unit 0
	1	1	Select unit 1
	2	2	Select unit 2
	3	3	Select unit 3
BITS 8-11:	0-17	0-F	Format
BITS12-13:	0-3	0-3	Not used
BITS12-13:	0-3	0-3	Destination floppy if Copy floppy

The various functions are described in chapter 4.

BIT:	9	8	Meaning
	0	0	512 Bytes/sector
	0	1	256 Bytes/sector
	1	0	128 Bytes/sector
	1	1	1024 Bytes/sector

BIT:	10	Meaning
	0	Single sided
	1	Double sided

BIT:	11	Meaning
	0	Single density
	1	Double density

3.8.2.2 Card no. 3112

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Copy dest		Format						Unit		Function					

BITS 0-5:	Octal	Hex.	Function
	0	0	Read data
	1	1	Write data
	2	2	Find EOT (read without data transfer)
	5	5	Write EOT
	41	21	Format floppy
	42	22	Read format
	43	23	Read deleted record
	44	24	Write deleted record
	54	2C	Copy floppy
	55	2D	Format track
	56	2E	Check floppy
	70	38	Identify floppy
BITS 6-7:	0	0	Select unit 0
	1	1	Select unit 1
	2	2	Select unit 2
	3	3	Select unit 3
BITS 8-13:			Format
BITS14-15:	0-17	0-17	Not used

BIT:	9	8	Meaning
	0	0	512 Bytes/sector
	0	1	256 Bytes/sector
	1	0	128 Bytes/sector
	1	1	1024 Bytes/sector

BIT:	10	Meaning
	0	Single sided
	1	Double sided

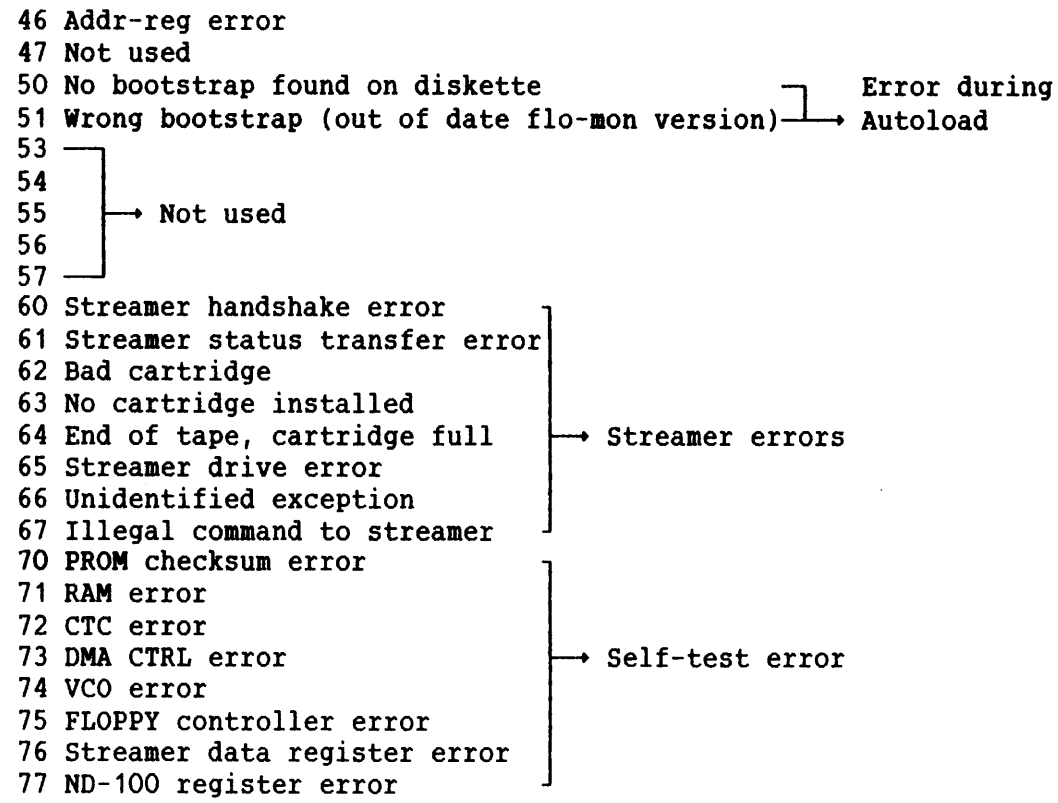
BIT:	11	Meaning
	0	Single density
	1	Double density

3.9 Error Codes

These error codes are given in bits 9-15 of status word 1. The codes are also shown in the digit display on the rear edge of the controller.

OCTAL

00 OK
01 ┐
02 │
03 ├→ Not used
04 ┘
05 CRC error
06 Sector not found
07 Track not found
10 Format not found
11 Diskette defect (impossible to format)
12 Format mismatch
13 Illegal format specified
14 Single sided diskette inserted
15 Double sided diskette inserted
16 Write protected diskette/cartridge
17 Deleted record
20 Drive not ready
21 Controller busy on start
22 Lost data (over or underrun)
23 Track zero not detected
24 VCO (Voltage Controlled Oscillator) frequency out of range
25 Microprogram out of range
26 Timeout
27 Undefined error
30 Track out of range
31 Not used
32 Compare error (during compare of data)
33 Internal DMA errors
34 ┐
35 │
36 ├→ Not used
37 ┘
40 ND-100 Bus error command fetch
41 ND-100 Bus error status transfer
42 ND-100 Bus error data transfer
43 Illegal command
44 Word count not zero
45 Illegal completion (cont. transf.)



3.10 Explanation of the Error Codes

00 OK

If no error is detected, the output will display 00.

05 CRC Error

Whenever a sector is written onto the floppy diskette, the floppy controller will always calculate a CRC from the data written. This CRC is then written after the data part of each sector.

Whenever a sector is read back, the CRC is again calculated from the data read. When the CRC written onto the floppy diskette is retrieved, it is compared to the one calculated at read time. If the two are different, the CRC Error code is given.

The CRC error is an indication of bad media, dirty read/write heads or interference on the cable lines (termination problems).

06 Sector Not Found

Whenever a read/write operation takes place, the address part of the sectors passing under the read/write heads is compared to the address of the desired sector. If the right sector is not found in the course of 5 revolutions, the Missing Sector error is given.

The Sector Not Found error indicates a destroyed format, bad media or dirty read/write heads.

07 Track Not Found

There is no track with this number. No ID field with this track number is found.

The Track Not Found error indicates a destroyed format, bad media or dirty read/write heads.

10 Format Not Found

This error is an indication that the floppy diskette has not been formatted.

11 Diskette Defect (Impossible to Format)

When a format is written, the formatted track (or diskette if Format Diskette command) is tested. If an error occurs, the track is re-formatted. If it still gives an error, the error code Diskette Defect (Impossible to Format) is given.

12 Format Mismatch

The specified format is not the same as the one found on the diskette. Status 2 gives the current format of the diskette.

13 Illegal Format Specified

Whenever a read/write operation takes place, the format specified is tested. If it is 3 or 8, the error code Illegal Format Specified is given.

14 Single Sided Diskette Inserted

Whenever a read/write operation takes place, the format specified is tested. If the format is double sided and the floppy inserted is single sided, the error code Single Sided Diskette Inserted is given.

15 Double Sided Diskette Inserted

Whenever a read/write operation takes place, the format specified is tested. If the specified format is single sided and the floppy inserted is double sided, the error code Double Sided Diskette Inserted is given.

16 Write Protected Diskette/Cartridge

When an attempt to write on a write protected diskette/cartridge is made, the error Protected Diskette/Cartridge is given.

17 Deleted Record

Whenever an unspecified deleted record is read, the error code Deleted Record is given.

20 Drive Not Ready

If an operation is attempted on a drive which is not available (inexsistent), the error code Drive Not Ready is given.

This error may also indicate that no diskette has been entered, that a diskette has been inserted in the wrong direction, a power failure or no drive with this number.

21 Controller Bust on Start

If the floppy controller (Western Digital 1797-02) is busy at the same time as the program attempts to activate it, the error code Controller Busy on Start is given.

This should never occur, and indicates an error in the microprogram or the floppy controller.

22 Lost Data (Over- or Underrun)

If the DMA controller is not capable of feeding the floppy controller fast enough, the error code Lost Data (Over- or Underrun) is given.

This should never occur, and indicates an error in the microprogram or the DMA/floppy controller.

23 Track Zero Not Detected

If the track zero signal is not read from the floppy controller after a return to zero seek, the error code Track Zero Not Detected is given.

This should never occur, and indicates an error in the floppy controller or in the floppy drive. Too fast step-rate may also give this error (NB! Patch in SINTRAN data filled).

24 VCO Frequency Out of Range

As a part of the self test, the idle frequency of the VCO is adjusted to 4 MHz. If this is impossible, the error code VCO Frequency Out of Range is given.

The error should be found in the VCO and its D/A (Digital/Analog) converter.

25 Microprogram Out of Range

If the Z80 tries to execute a program from an inexistent memory, it will fetch FFhex (the bus is terminated high). This instruction is RST 038H, which gives the error code Microprogram Out of Range.

This should never occur, and indicates an error in the microprogram or in the Z80.

26 Timeout

The given command has not been executed within the expected time, and has been aborted by the watchdog timer.

This can be caused by an error in the DMA controller.

27 Undefined Error

If the floppy controller gives an interrupt which the microprogram does not expect because of data transport, and if no error bits are set in the floppy controller status, the error code Undefined Error is given.

This should never occur, but might be caused by an error either in the floppy controller, or in the electronic associated with it.

30 Track Out of Range

If an attempt is made to read/write on a track number higher than the largest possible track on the floppy, the error code Track Out of Range is given.

32 Compare Error (during compare of data)

If the error bit during a read/write operation and the data read the second time are not equal to the data read/written, the error code Compare Error (during compare of data) is given.

33 Internal DMA Errors

After each DMA transfer between the interface and the ND-100, the contents of the Memory Address Register are read and checked. If it is not corrected, the error code Internal DMA Errors is given.

40 ND-100 Bus Error Command Fetch

During DMA transfers between the controller and the ND-100 memory, the ND-100 bus signal BERROR is watched. If the BERROR signal is true during a fetch of the command block from the ND-100, the error code ND-100 Bus Error Command Fetch is given.

It can be caused by specifying a pointer to an inexistent memory when the pointer to the CCB is given (IOX DEVNO+5 and IOX DEVNO+7). It can also be caused by a memory parity error in the area where the CCB is situated.

41 ND-100 Bus Error Status Transfer

During DMA transfers between the controller and the ND-100 memory, the ND-100 bus signal BERROR is watched. If the BERROR signal is true during a transfer of the status to the ND-100, the error code Bus Error Status Transfer is given.

It can be caused by specifying a pointer to an inexistent memory when the pointer to the CCB is given (IOX DEVNO+5 and IOX DEVNO+7). It can also be caused by a memory parity error in the area where the CCB is situated.

CHAPTER 4

COMMANDS

4 COMMANDS

4.1 Streamer Command Descriptions

4.1.1 Read data - (00 Oct.)

Data is read from the tape to the ND-100 memory. The parameters for the transfer are given in the command field of the ND-100 memory. The reading must start either at the beginning of the media or following a file mark. The number of records specifies the amount of data to be read.

4.1.2 Write data - (01 Oct.)

Data is read from the ND-100 memory and written on the tape. Parameters are supplied as for Read Data. The writing will always start at the beginning of the tape - at BOT, and the data transfer should be fast enough to keep the tape streaming - that is, at least 90 Kbytes/sec. If the transfer rate is too slow, the tape will stop, it will be rewound and then it will go on writing - this is called underrun and is a result of to little data on the cartridge. Usage of the continuous transfer (see page 35 and 36) mode should avoid this problem.

4.1.3 Erase tape - (07 Oct.)

The whole tape is erased from BOT to EOT on the first pass. (One pass is one run one way.) The whole tape can be erased on one pass, because of the erase heads' size in proportion to the read and write heads, see figure 3.

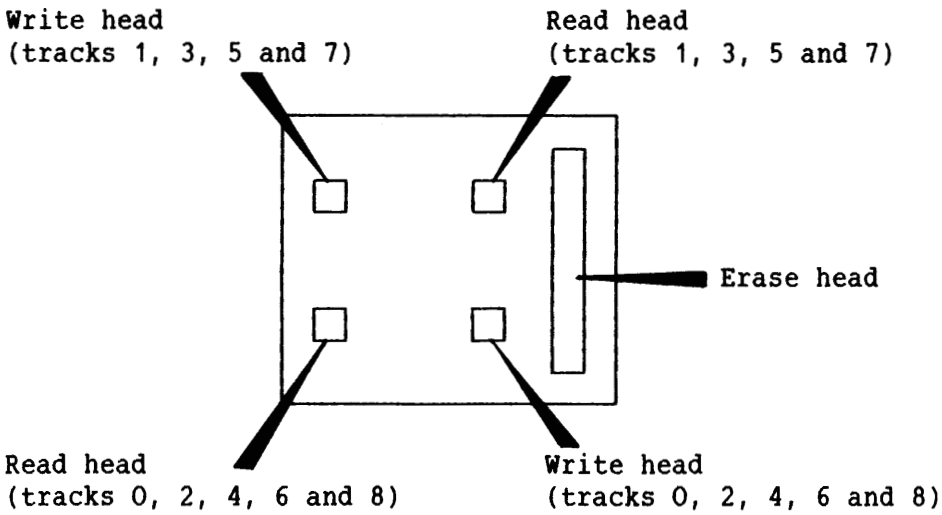


Fig. 3. Read, Write and Erase Heads

4.1.4 Advance to EOT - (10 Oct.)

The drive starts reading the tape, looking for a file mark. When a file mark is encountered, the tape motion is stopped. A repeat of the command might be given to position the tape to the next file mark. It is also possible to start reading data from the file mark onward.

4.1.5 Write EOT - (12 Oct.)

The drive will write a file mark on the tape at the current position. File marks may be used by the host to distinguish between different groups of data or between different records on the tape. File marks contain no valuable data information.

4.1.6 Rewind - (13 Oct.)

The tape is moved back to the physical beginning of the tape - BOT.

4.1.7 Read extended status - (36 Oct.)

Read status from the drive, and transfer it to the ND-100 memory.

The status is written into the ND-100 as if a Read Data were performed.

The amount of status transferred is specified by the word count. If the word count >32 oct. or =0 it will be set to 32. (This is true if record count specified.)

Spare locations are not defined, and may contain any data.

Memaddr:			
	Board no.		→ Board Status
+ 1	15-8 Sub ver.no	7-0 µ prog ver.no	→ PROM Status
+ 2	Buffer Start address		→ RAM Status
+ 3	Buffer size		
+ 4	Z80 IX-Reg.		→ Z80 Status
+ 5	Z80 AF-Reg.		
+ 6	Z80 BC-Reg.		
+ 7	Z80 DE-Reg.		
+ 10	Z80 HL-Reg.		
+ 11	Z80 SP-Reg.		
+ 12	Z80 PC-Reg.		
+ 13	Z80 IY-Reg.		
+ 14	Status 1		→ Controller Status
+ 15	Status 2		
+ 16	Not used	Last addr. 23-16	
+ 17	Last Memory address 15-0		
+ 20	Not used	Rem. Words 23-16	
+ 21	Remaining Words 15-0		
+ 22	Status byte 0	Status byte 1	→ Streamer Drive Status
+ 23	Status byte 2	Status byte 3	
+ 24	Status byte 4	Status byte 5	

Status byte 0

Bit no.	Meaning
0	File mark detected
1	Bad block not located
2	Unrecoverable data error
3	End of Media
4	Write protected cartridge
5	Unselected drive
6	Cartridge not in place
7	Status byte 0 bits active

Status byte 1

Bit no.	Meaning
0	Power-on/reset occurred
1	End of recorded data
2	Reserved for bus parity error
3	Beginning of Media
4	Eight or more read retries for one block
5	No data detected
6	Illegal Command
7	Status byte 1 bits active

Spare locations are not defined and may contain any data.

Status byte 0

Bit no.	Meaning
0	File mark detected
1	Bad block not located
2	Unrecoverable data error
3	EOT
4	Write protected cartridge
5	Unselected drive
6	Cartridge not in place
7	Status byte 0 bits active

Status byte 1

Bit no.	Meaning
0	Power-on/reset occurred
1	End of recorded data
2	Reserved for bus parity error
3	BOT
4	Eight or more read retries for one block
5	No data detected
6	Illegal Command
7	Status byte 1 bits active

4.1.8 Check cartridge - (56 Oct.)

Starts reading the cartridge at BOT and checks for valid CRC. The tape motion is stopped, and the test is finished with the first error discovered. The address (number of blocks from BOT) of the erroneous block is reported in LAST MEMADDR in the status part of the command block (24-bit).

4.1.9 Test cartridge capacity - (57 Oct.)

All tracks are written with data supplied by the controller micro-processor in order to measure the capacity of that specific tape. Capacity is reported in the status part of the command block. REMAINING WORDS (CB+12 & CB+13 - see Command Block (CB) page 14), holds the number of blocks successfully written on the tape.

To obtain the number of Mb, divide by 2048 (2^{11}). One block is 512 bytes.

4.1.10 Retention cartridge - (70 Oct.)

The tape is run to BOT, then to EOT, and then back to BOT again. This will ensure correct tape tension, and should always be done before reading/writing on a tape that has not been used for some time.

4.1.11 What is continuous transfer

The streaming-tape is primary a backup device, and it is not meant to be a start/stop tape drive. However, if the host is unable to supply data at the rate required to keep the tape streaming, the drive will go into an underrun condition, where a termination block is written and the tape is stopped until the drive buffers are refilled. Several underruns will result in a waste of time and capacity. It should therefore be avoided. The continuous transfer mode is our solution to keep the streaming-tape streaming.

4.1.12 How does continuous transfer work

The standard way to do a transfer to/from a peripheral device, is to set up a command, activate the controller and then wait for the transfer to be completed either by looping on read-status, or by means of interrupts. If it is a write-peripheral transfer, the controller will not be ready until all the data is transferred to the peripheral device. During a read-peripheral transfer, the reading will stop when the appropriate bytes are transferred. Using this scheme in accessing the streaming-tape will lead to under/overrun.

4.1.13 Continuous read-transfer - (74 Oct.)

On a read-peripheral transfer with the controller in the continuous transfer mode, the interrupt will be given at the time all of the data is correctly transferred to the ND-100. It thus performs a usual transfer. However, the controller will continue to read from the drive and fill the buffer. When the ND-100 gives a new read command, the data is fed from the controller buffer to the memory of the ND-100. It takes approximately 30 milliseconds to fill the buffer, and thus the ND-100 should start a new transfer in less than this time. The continuous-read transfer has to be terminated by a Read Data in order to get a correct status.

4.1.14 Continuous write-transfer - (75 Oct.)

The continuous-transfer mode works in such a way, that when the transfer of data between the ND-100 and the controller buffer is finished during a write-peripheral transfer, the controller will give a interrupt to the ND-100 without waiting for the data to be written on the tape. Thus the controller buffer will ensure continuous writing on the tape while the ND-100 is preparing the next transfer. The time required to empty the buffer is approximately 30 milliseconds. If an error occurs in the time between two transfers, this error will be reported together with the interrupt on the following transfer. The continuous-write transfer has to be terminated by a Write Data in order to get a correct status.

4.1.15 Points to note when using continuous-transfer

A interrupt will be given on every transfer. If it is a read-transfer, the status is completely correct. However, if it is a write-transfer, the status is not final when the continuous transfer bit is set. This is due to the fact that the data is not written onto the tape at the time the status is given. Should an error occur after an interrupt is given to the ND-100, this error will be reported in the status of the next transfer. This means that during continuous-write the error bit (bit 4) in the HARDWARE-STATUS WORD is an OR of errors in the current and the preceding transfer. The STATUS WORD 2 in memory tells which transfer that failed.

It is also important to note that the last transfer in a series must be given as a NON-continuous transfer, in order to get a true status.

Not following these rules will lead to errors.

4.2 Floppy Command Descriptions

4.2.1 Read data

Data is read from the floppy disk to the ND-100 memory. The start address is given as the logical sector address, and a choice can be made between the word count and the number of sectors to indicate the length of the transfer.

The parameters for the transfer are given in the command field in the ND-100 memory.

> NOTE !
>
> The transfer will always start at the beginning of a sector, but the number of words to be read may be preset to any number of words.

4.2.2 Write data

Same procedure as READ DATA, except that transfer is now from the ND-100 to the diskette.

4.2.3 Find EOT

Same procedure as READ DATA, except that data is only read to the local buffer. There is no transfer to the ND-100, except for the status. Bit 5 in status word 1 indicates if it is an EOT (deleted record).

4.2.4 Write EOT

The sector given in the command block is read to the local memory and written back as a deleted record.

4.2.5 Format floppy

The floppy diskette placed in the specified drive is formatted to the format given in the command word.

4.2.6 Read format

The format is read from the floppy disk and returned to status word 2. The disk address and the format of the command block indicate where the format should be read.

4.2.7 Read deleted record

Reads data from a record marked as a deleted record, and transfers the data to the ND-100.

4.2.8 Write deleted record

Writes a record from the ND-100 and marks it as a deleted record.

4.2.9 Copy floppy

Copies from one drive to another. The entire floppy is copied.

4.2.10 Format track

One track on one side is formatted. This command can be used to make IBM compatible diskettes.

4.2.11 Check floppy

Data is read to the controller's local memory to test for CRC-errors. The test halts with the first error discovered. The address of the erroneous sector is held in LAST MEMADDR in the status field. The failing sector is in the least significant part of LAST MEMADDR.

> NOTE !
>
> The address given is to the sector after the one that failed.

The layout of the bits is like this:

Bit no :	15	14 13 12 11	11 10 9	8 7 6	5 4 3	2 1 0
Meaning:	Side	Track number		Sector number		

CHAPTER 5

SUMMARY OF FLOPPY FORMATS

5 SUMMARY OF FLOPPY FORMATS

5.1 Card no. 3106

0	IBM SYS-32-II	512 Bytes/sector	single side, single density
1	IBM 3600	256 Bytes/sector	single side, single density
2	IBM 3740	128 Bytes/sector	single side, single density
3	Illegal		
4	Non IBM	512 Bytes/sector	double side, single density
5	Non IBM	256 Bytes/sector	double side, single density
6	Non IBM	128 Bytes/sector	double side, single density
7	Illegal		
10	Non IBM	512 Bytes/sector	single side, double density
11	IBM SYS-34	256 Bytes/sector	single side, double density
12	Illegal		
13	Non IBM	1024 Bytes/sector	single side, double density
14	Non IBM	512 Bytes/sector	double side, double density
15	IBM SYS-34	256 Bytes/sector	double side, double density
16	Illegal		
17	Non IBM	1024 Bytes/sector	double side, double density

5.2 Card no. 3112

0	IBM SYS-32-II	512 Bytes/sector	single side, single density
1	IBM 3600	256 Bytes/sector	single side, single density
2	IBM 3740	128 Bytes/sector	single side, single density
3	Illegal		
4	Non IBM	512 Bytes/sector	double side, single density
5	Non IBM	256 Bytes/sector	double side, single density
6	Non IBM	128 Bytes/sector	double side, single density
7	Illegal		
10	Non IBM	512 Bytes/sector	single side, double density
11	IBM SYS-34	256 Bytes/sector	single side, double density
12	Illegal		
13	Non IBM	1024 Bytes/sector	single side, double density
14	Non IBM	512 Bytes/sector	double side, double density
15	IBM SYS-34	256 Bytes/sector	double side, double density
16	Illegal		
17	Non IBM	1024 Bytes/sector	double side, double density
20	Illegal		
21	Illegal		
22	Basic 5 1/4"	128 Bytes/sector	single sided, single density
23	- 33 Illegal		
34	IBM PC		
35	- 57 Illegal		
60	- 77 User specified		

CHAPTER 6

TESTING

6 TESTING

6.1 Self-Testing

When an MC (Master Clear) pulse is given to the floppy and streamer controller, the processor will perform a self-test. This can be observed on the error display which is first "turned OFF", then set to 000 upon successful completion of the test. During self-test, drive 0 is selected and restored.

Upon detection of errors, the codes E70-E75 are displayed.

If the display is not lit or shows codes other than the ones specified, the processor will not be able to perform a self-test.

The phases of the self-test are as follows:

1) The PROMs are read and a checksum is calculated and checked. (If not OK error 70.)

2) A RAM test is performed. (If not OK error 71.)

3) The Z80A-CTC (timer/interrupt controller) is tested. (If not OK error 72.)

4) The DMA-controller AM9517-4 is run in test mode. (If not OK error 73.)

5) The VCO SN74LS629 is measured and adjusted to be within the limits of the phase locked loop. (If not OK error 74.)

6) A test of the floppy controller chip FD1797. (If not OK error 75.)

7) Test of the MARs (Memory Address Registers). (If not OK error 77.)

8) Test of registers which communicate with the QIC-02 bus. (If not OK error 76.)

6.2 RAM-Test

The part of the RAM being used for buffering of data from/to the floppy disk will be tested continuously. The test starts when the controller has been idle for approximately 3 minutes.

This is a comprehensive test that uses approximately 30 minutes to test 1Kbyte.

A new access from the ND-100 will stop the test.

NOTE !

If errors are discovered during a self-test or a RAM test, it will not carry out commands. This is to prevent destruction of data on the diskettes.

Bit 4 (OR of errors) and bit 7 (hard error - DMA transfer) in the status word (hardware) will be set. The status field will not be written to the ND-100 memory. However, the status word 1 will be written to the controller data register and may be read from this (IOX DEVNO.+0).

CHAPTER 7

TEST MACROS

7 TEST MACROS

7.1 Test Options

A total of 24 different tests are supported by the microprocessor program.

This should make it easy to write test and maintenance programs.

As an example, the T13 makes it possible to write a Z80 program, load it from the ND-100 to the local RAM and start program execution by T15.

T7 -T8-T24 make it possible to read and write to all registers in the controller.

7.2 Hardware Control Word in Test Mode

The floppy controller has a program containing various test routines. These routines are activated from the ND-100. It is done by setting bit 3 in the control word. This indicates that bits 9-15 have a special meaning. They will contain the number of the test to be activated.

The significance of the contents of registers POH (POinter High 16-23), POM (POinter Medium 8-15) and POL (POinter Low 0-7) will vary with the different tests. However, it will normally be these registers that are used to transfer parameters used in the testing. This avoids using the COMMAND BLOCK in memory.

The tests T13 and T14 are exceptions. They use a field in the ND-100 memory to specify addresses and byte count when loading program/data to/from the ND-100.

The tests T13, T14, T16, T17 and T18 will write the status word 1 to the data out register. All tests will write status to the data-out register if an error occurs. This register can be read with the IOX READ-DATA (IOX (Devno + 0)).

7.3 Test Routines in the Floppy and Streamer Controller

```
Bits 0 - 8 Standard (when test bit 3 is set)
Bits 9 - 15 Specify test
```

The tests and the control words are given on the following page.

Table 2. The Tests and the Control Word in the Floppy and Streamer Controller

TEST	CONTROL WORD	ACTION
0	00041X	Do nothing (set RFT)
1	00141X	Stop controller (test timeout)
2	00241X	Data input regs. (POL & POM) are copied to data output registers (DLO - Data LOw & DHI - Data HIgh).
3	00341X	POH is copied to DLO (BITS 0-7)
4	00441X	POH is copied to address given by POL & POM
5	00541X	DLO-reg. is loaded with byte addressed by POL & POM
6	00641X	Mem. size (upper address in RAM) loaded to POL & POM
7	00741X	POM is written to register addressed by POL
8	01041X	DLO loaded with contents of reg. addressed by POL
9	01141X	DMA input test (Z80 → ND-100) POH = block number in Z80 memory block 1 starts at 2000H in controller POL & POM = ND-100 address (only first 64 Kwords are used) Z80 ADDR.= 2000H+[80H (POHI-1)]
10	01241X	DMA output test (ND-100 → Z80) Parameter same as T9
11	01341X	Compare test POL & POM = start address Compare the two following blocks of 128 bytes in the Z80 memory. DLO & DHI = remaining bytes after compare error If DLO & DHI = 0 then OK
12	01441X	Display test. display count from 0 to 9
13	01541X	Load ND-100 → Z80 Address in ND-100 and Z80, word count is fetched from ND-100 memory POH, POM & POL are pointers to parameter field

NOTE: If X = 0, no interrupt - if X = 2 interrupt when finished

Table 2. The Tests and the Control Word in the Floppy and Streamer Controller - Continued.

TEST	CONTROL WORD	ACTION
14	01641X	Load Z80 → ND-100 (parameter same as T13)
15	01741X	Start program in address given by POL & POM
16	02041X	Generate CRC error on; POL = sector number, POM = Track, POH = DEVICE-SEL-REG. (FDVSEL)
17	02141X	Destroy track; POM = Track, POH = DEV-SEL-REG.
18	02241X	Destroy 1 sector POM = TRACK, POH = DEV-SEL-REG.
19	02341X	TAP-TAP TEST. POH = Number of taps.
20	02441X	Stop display
21	02541X	Change to interrupt address in PROM (for RAM test)
22	02641X	Load stack pointer (POL & POM = value)
23	02741X	Read stack pointer
24	03041X	Execute FD1797 command POH = FD1797 track register POL = FD1797 command register When finished: POM = FD1797 track-reg POL = FD1797- status
25	03141X	Disable RAM self-test. The RAM self-test is not started after 3 min. idle as usual. After a clear the test is enabled again.

NOTE: If X = 0, no interrupt - if X = 2 interrupt when finished

7.4 Address Field for Up/Down Load

(Used for T13 and T14)

IN Z80 RAM:

20F2H 20F1H	ND-100 Load addr. ND-100 Load addr.
20F2H 20F3H	Z80 Addr. Z80 Addr.
20F4H 20F5H	Byte count Byte count

8 Bits

IN ND-100:

Address field	ND-100 Load address
+ 1	Z80 Address
+ 2	Byte count

16 Bits

POL, POM and POH point to address field

CHAPTER 8

REGISTERS IN THE FLOPPY AND STREAMER CONTROLLER

8 REGISTERS IN THE FLOPPY AND STREAMER CONTROLLER

Description of the registers in the DMA controller AM9517, the floppy controller FD1797, the counter-timer Z80-CTC and the digital/analog converter AD558 can be found in the respective data books.

Name :	Register function	: Value (hex)	: Value (oct)
INTERRUPT/TIMER/COUNTER - Z80-CTC			
CNB	CTC-CHNL 0: Int From ND-100	10	20
CC-S	CTC-CHNL 1: Int From streamer exception	11	21
CFC	CTC-CHNL 2: Int From floppy contr	12	22
CDMA	CTC-CHNL 3: Int From DMA-contr	13	23
	CTC-CHNL 4: Int From compare error	14	24
	CTC-CHNL 5: Int From streamer ready	15	25
	CTC-CHNL 6: Int From timer	16	26
	CTC-CHNL 7: Int From timer	17	27
DMA CONTROLLER AM9517			
DCOM	Command register	28	50
DMOD	Mode register	2B	53
DRQ	Request register	29	51
DMSK	Mask register (write bit)	2A	52
DMSKW	Mask register (write all bits)	2F	57
DTEMP	Temporary register	2D	55
DSTAT	Status register	28	50
DMC	Master clear (programmed)	2D	55
DCFF	Clear internal flip-flop	2C	54
DADR	Address register channel 0	20	40
DBC	Byte count channel 0	21	41
ND-100 BUS CONTROL			
	Z80 Write-only registers.		
ADL	DMA Address bit 0-7	50	120
ADM	DMA Address bit 8-15	51	121
ADH	DMA Address bit 16-23	52	122
DD-T	DMA Direction and test	53	123
DLO	Data out bit 0-7	54	124
DHI	Data out bit 8-15	55	125
NSTAT	Status register read by the ND-100	56	126
NFINI	Set RFT and status (finish)	57	127

Name :	Register function	: Value (hex)	: Value (oct)
	Z80 Read-only registers.		
CW1	Control word low-part	50	120
POL	Pointer or data in bit 0-7	51	121
POM	Pointer or data in bit 8-15	52	122
POH	Pointer address bit 16-23	53	123
CW2	Control word bit 16-23	54	124
	ND-100 MAR Bits 0-7	55	125
	ND-100 MAR Bits 8-15	56	126
	ND-100 MAR Bits 16-23	57	127
FLOPPY CONTROLLER FD1797			
FCCOM	Command register	70	160
FCST	Status	70	160
FCTRK	Track	71	161
FCSEC	Sector	72	162
FCDAT	Data	73	163
FDVSEL	Device select and mode	74	164
FCCLR	Floppy controller clear	75	165
FADC	Digital/analog converter	76	166
FLSTAT	Floppy drive status	77	167
FMOD2	Floppy modus register 2	70	160
STREAMER CONTROLLER			
SRD	Streamer read-data	60	140
SWR	Streamer write-data	60	140
SS	Streamer status-register	61	141
SMR	Streamer mode-register	61	141
DISPLAY			
SDISP	Set data to the display	40	100
ENDISP	Enable display - set modes	41	101

C H A P T E R 9

RAM - PROM AND PALS USED ON THE F&S CONTROLLER

9 RAM - PROM AND PALS USED ON THE F&S CONTROLLER

Several kinds of memory and PALS are used on the F&S controller

PROM - used as device number decoder.
EPROM - used for storage of the microprogram.
PAL - used as logical circuits and decoders.
RAM - used as the memory for the microprogram and as a data buffer.

9.1 PROMs

Two PROMs are used, holding the device number and the identification code (ident code).

PROM NO	ND-ID NO.	LOCATION	TYPE
1	00900	8C	TBP 18S030
2	05800	3C	TBP 18S030

9.2 EPROMs

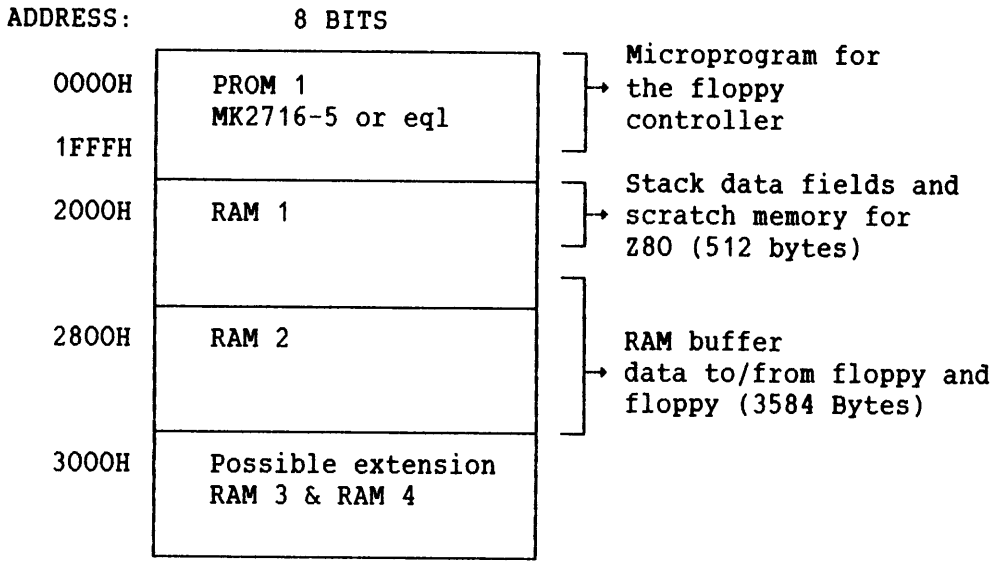
The EPROMs are used to hold the microprocessor program. These devices might be of the types 2716, 2732 or 2764.

A PAL16L8 is used for decoding the memory-chip-select and thus the PAL must be programmed according to the PROM-type used.

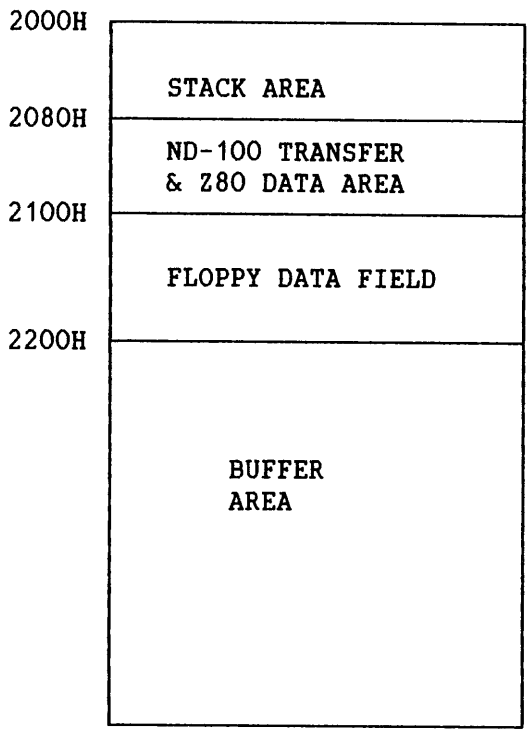
The standard floppy and streamer controller will use one EPROM of the 2764-type, located in position 12G.

9.3 Memory Organization

(H = Hexadecimal)



RAM 1 LAYOUT (2000H TO 27FFH)



9.4 RAM

RAM is used by the microprossessor to store variable data. It is also used to buffer data to/from the peripheral device.

As for the EPROMs, the decoding of chip-select is performed by means of a PAL16L8, and thus the RAM might be a 8 x 2K or a 8 x 8K device.

The controller will usually hold two 8 x 2K RAMs, 4802, HM 6116 or the equivalent.

Because the controller itself tests how much RAM there is on the board, the data buffer is easily expanded by inserting new RAMs on the board.

9.5 PALs

PALs are used in the ND-100 DMA controller, in the STREAMER interface and for decoding memory-chip-select. The table below gives a summary of the PALs used.

PAL	ND-ID-NO	POS.	TYPE	FUNCTION
1	34400	12F	16L8	Memory decoding for Z80
2	34500	11E	16L8	ND-100-DMA control
3	34600	14B	16L8	Streamer control

9.5.1 Possible memory configurations

PAL 1 decodes the chip enable to the memory positions: 12G, 10G, 8G, 7G, 5G and 3G. The following configurations are possible :

The configuration given by 34400A is:

Position	Size (K byte)
12G	8
10G	8
8G	2
7G	2
5G	2
3G	2

9.5.2 Program for PAL - PAL-344-00

```
PAL16L8
STREAMER 8-24-82

MEMORY DECODING FOR 2*8K PROMS IN POS 12G &10G, AND 4*2K RAMS

Input  :  BA11 BA12 BA13 BA14 BA15 /ZM1 /ZMREQ AEN MDIS /WE GND VCC
Output :  /CS1 /A11WE /WRCPR /CS5 /CS4 /CS3 /CS2 /CS0

 /CS0= /BA13*/BA14*/BA15*ZM1*/MDIS
      +/BA13*/BA14*/BA15*ZMREQ*/MDIS
      +/BA13*/BA14*/BA15*AEN*/MDIS

 /CS1= BA13*BA14*BA15*ZM1*/MDIS
      +BA13*BA14*BA15*ZMREQ*/MDIS
      +BA13*BA14*BA15*AEN*/MDIS
 /CS2= /BA11*/BA12*BA13*/BA14*/BA15*ZM1*/MDIS
      +/BA11*/BA12*BA13*/BA14*/BA15*ZMREQ*/MDIS
      +/BA11*/BA12*BA13*/BA14*/BA15*AEN*/MDIS

 /CS3=  BA11*/BA12*BA13*/BA14*/BA15*ZM1*/MDIS
       +BA11*/BA12*BA13*/BA14*/BA15*ZMREQ*/MDIS
       +BA11*/BA12*BA13*/BA14*/BA15*AEN*/MDIS

 /CS4= /BA11*BA12*BA13*/BA14*/BA15*ZM1*/MDIS
      +/BA11*BA12*BA13*/BA14*/BA15*ZMREQ*/MDIS
      +/BA11*BA12*BA13*/BA14*/BA15*AEN*/MDIS

 /CS5=  BA11*BA12*BA13*/BA14*/BA15*ZM1*/MDIS
       +BA11*BA12*BA13*/BA14*/BA15*ZMREQ*/MDIS
       +BA11*BA12*BA13*/BA14*/BA15*AEN*/MDIS

 /WRCPR= MDIS*WE

 /A11WE=  WE*ZMREQ*BA13*/BA14*/BA15
        + WE*AEN*BA13*/BA14*/BA15
        +/BA11*/BA13*/BA14*/BA15
        +/BA11*BA13*BA14*BA15

 STOP!
```

9.5.3 Program for PAL - PAL-345-00

```
 PAL16L8
 STREAMER 7-4-82

 CONVERSION BYTE <===> WORD  & DMA CONTROL

Input  :  /DMAEN /NACK /IOWR /IORD READFL /SETLO /SETHI /RPOL /RPOM
          /NREQ VCC GND
Output :  /ENDLO /ENDHI /LATCH /LAST /DMAST /NRQ /LODHI /LODLO

 /LODLO= SETLO
       + LAST*IOWR*READFL*NACK

 /LODHI= SETHI
       + DMAEN*/LAST*IOWR*READFL*NACK

 /DMAST= DMAEN*LAST*IOWR*READFL*NACK
       + DMAEN*LAST*IORD*/READFL*NACK
       + DMAEN*/READFL*/NACK*/NRQ*LATCH

 /NRQ= DMAEN*/NACK*/NREQ*/LATCH*/LAST*/DMAST
     + NRQ*/DMAST*DMAEN

 /LAST= LATCH*/IOWR*NACK*READFL*DMAEN
      + LATCH*/IORD*NACK*/READFL*DMAEN
      + LATCH*DMAST*/READFL
      + LAST*/NREQ*DMAEN

 /LATCH= /READFL*/DMAEN
       + LATCH*/LAST*/READFL
       + LODHI*NACK*DMAEN*READFL
       + ENDHI*NACK*DMAEN*/READFL

 /ENDHI= RPOM
       + DMAEN*/LAST*IORD*/READFL*NACK

 /ENDLO= RPOL
       + LAST*IORD*/READFL*NACK

 STOP!
```

9.5.4 Program for PAL - PAL-346-00

```
PAL16L8
GB 20-08-82

STREAMING-TAPE CONTROL.

Input  :  /IOWR /IORD /SEN BAO /SDACK SWR /SGDRQ /SDMAINT SONL SACK
          GND VCC
Output :  /SLWD /SXFER /SDISD /SRDRQ /SSCG /SLMR /SRS /SERD

 /SERD  = SEN*/BAO*IORD
        + SDACK*IORD

 /SLWD  = SEN*/BAO*IOWR
        + SDACK*IOWR

 /SRS   = SEN*BAO*IORD

 /SLMR  = SEN*BAO*IOWR

 /SSCG  = SEN*/BAO

 /SRDRQ = SDACK*SGDRQ
        + /SWR*/SONL
        + SEN*SRDRQ*/SDACK

 /SDISD = SDMAINT*SDACK
        + /SONL

 /SXFER = /SGDRQ*/SDACK*/SACK*SWR*SONL
        + SDACK*/SWR*SONL
        + SXFER*SACK*/SWR*SONL

 STOP!
```

9.5.5 Card no. 3112 - Programmable write precompensation

The amount of precompensation is programmable. There are four possible values selected by two bits in the Floppy Mode 2 Register (FMOD2). The values are :

125 nanosec.

187.5 nanosec.

250 nanosec.

312.5 nanosec.

Three signals are used to switch the precompensation on and off. Two of this signals are bits in the FMOD2 register :

- Enable Precompensation (ENPRE)
- Track Gate X (TGX)

The third signal comes from the Floppy Disk Controller :

- TG43

Selection of the right time and duration of the write pulse is done by means of a PROM called WP-PROM (1K x 4 bits). The signals used to select the Write Data Pulse (WDAT), are attached to the address input pins of the WP-PROM in the following order :

Table 3. Card no 3112 - The Signals Used to Select the Write Data Pulse (WDAT)

Address	Signal	Meaning of the signal
A0	PA0	Address counter bit 0
A1	PA1	Address counter bit 1
A2	PA2	Address counter bit 2
A3	PA3	Address counter bit 3
A4	LEARLY	Latched EARLY signal from FD1797
A5	LLATE	Latched LATA signal from FD1797
A6	PAM0	Precomp amount select bit 1
A7	PAM1	Precomp amount select bit 0
A8	PRENOW	Precompensation is desired (Track > X)
A9	ENPRE	Enable precompensation

The rules for precompensation are given by the following table :

Table 4. Card no 3112 - The Rules for Precompensation

ENPRE	PRENOW	PAM1	PAMO	LATE	EARLY	Precompensation
0	X	X	X	X	X	0 - Nominal
1	0	X	X	X	X	0 - Nominal
1	1	X	X	0	0	0 - Nominal
1	1	0	0	0	1	- 125 ns (before Nominal)
1	1	0	0	0	1	- 187.5 ns
1	1	1	0	0	1	- 250 ns
1	1	1	0	0	1	- 312.5 ns
1	1	0	1	1	0	+ 125 ns (after Nominal)
1	1	0	1	1	0	+ 187.5 ns
1	1	1	1	1	0	+ 250 ns
1	1	1	1	1	0	+ 312.5 ns

Table 5 lists the contents of the WP-PROM as a function of input addresses.

Table 5. Card no 3112 - The WP-PROM as a Function of the Input Addresses

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Description
000	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Nominal - no precomp.
2F0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Addr 000-2F0 are equal
300	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Nominal - no precomp.
310	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	EARLY 125 ns
320	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	LATE 125 ns
330	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Illegal
340	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Nominal - no precomp.
350	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	EARLY 187.5 ns
360	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	LATE 187.5 ns
370	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Illegal
380	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Nominal - no precomp.
390	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	EARLY 250 ns
3A0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	LATE 250 ns
3B0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Illegal
3C0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	Nominal - no precomp.
3D0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	EARLY 312.5 ns
3E0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	LATE 312.5 ns
3F0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Illegal

9.5.5.1 Source list of the WP-PROM

```
A10Q4
GB 13-01-84

WP-PROM - WRITE PRECOMPENSATION

Input  : PA0 PA1 PA2 PA3 LEARLY LLATE PAM0 PAM1 PRENOW ENPRE NU1 NU2
         NU3
Output : Q0

 Q0 = /PA3* PA2* PA1*/PA0*/ENPRE
    + /PA3* PA2* PA1* PA0*/ENPRE
    +  PA3*/PA2*/PA1*/PA0*/ENPRE
    +  PA3*/PA2*/PA1* PA0*/ENPRE
    +  PA3*/PA2* PA1*/PA0*/ENPRE
    + /PA3* PA2* PA1*/PA0*/PRENOW
    + /PA3* PA2* PA1* PA0*/PRENOW
    +  PA3*/PA2*/PA1*/PA0*/PRENOW
    +  PA3*/PA2*/PA1* PA0*/PRENOW
    +  PA3*/PA2* PA1*/PA0*/PRENOW
    + /PA3* PA2* PA1*/PA0* PRENOW*ENPRE*/LEARLY*/LLATE
    + /PA3* PA2* PA1* PA0* PRENOW*ENPRE*/LEARLY*/LLATE
    +  PA3*/PA2*/PA1*/PA0* PRENOW*ENPRE*/LEARLY*/LLATE
    +  PA3*/PA2*/PA1* PA0* PRENOW*ENPRE*/LEARLY*/LLATE
    +  PA3*/PA2* PA1*/PA0* PRENOW*ENPRE*/LEARLY*/LLATE
    + /PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1*/PAM0
    + /PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1*/PAM0
    + /PA3* PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1*/PAM0
    + /PA3* PA2* PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1*/PAM0
    +  PA3*/PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1*/PAM0
    + /PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1* PAM0
    + /PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1* PAM0
    + /PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1* PAM0
    + /PA3* PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1* PAM0
    + /PA3* PA2* PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE*/PAM1* PAM0
    + /PA3*/PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1*/PAM0
    + /PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1*/PAM0
    + /PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1*/PAM0
    + /PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1*/PAM0
    + /PA3* PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1*/PAM0
    + /PA3*/PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1* PAM0
    + /PA3*/PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1* PAM0
    + /PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1* PAM0
    + /PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1* PAM0
    + /PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY*/LLATE* PAM1* PAM0
    +  PA3*/PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1*/PAM0
    +  PA3*/PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1*/PAM0
    +  PA3*/PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1*/PAM0
    +  PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1*/PAM0
    +  PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1*/PAM0
    +  PA3*/PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1* PAM0
    +  PA3*/PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1* PAM0
    +  PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1* PAM0
    +  PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1* PAM0
```

```
    +  PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE*/PAM1* PAM0
    +  PA3*/PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1*/PAM0
    +  PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1*/PAM0
    +  PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1*/PAM0
    +  PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1*/PAM0
    +  PA3* PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1*/PAM0
    +  PA3*/PA2* PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1* PAM0
    +  PA3* PA2*/PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1* PAM0
    +  PA3* PA2*/PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1* PAM0
    +  PA3* PA2* PA1*/PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1* PAM0
    +  PA3* PA2* PA1* PA0*PRENOW*ENPRE*LEARLY* LLATE* PAM1* PAM0

END$SPEC
```

C H A P T E R 10

CABLE WIRING

10 CABLE WIRING

The controller may be connected to up to 4 floppy drives and 4 streamer drives. The floppies are connected via a daisy chain from the A plug on the controller. The streamers are connected via a daisy chain from the B plug on the controller. See figure 4 below.

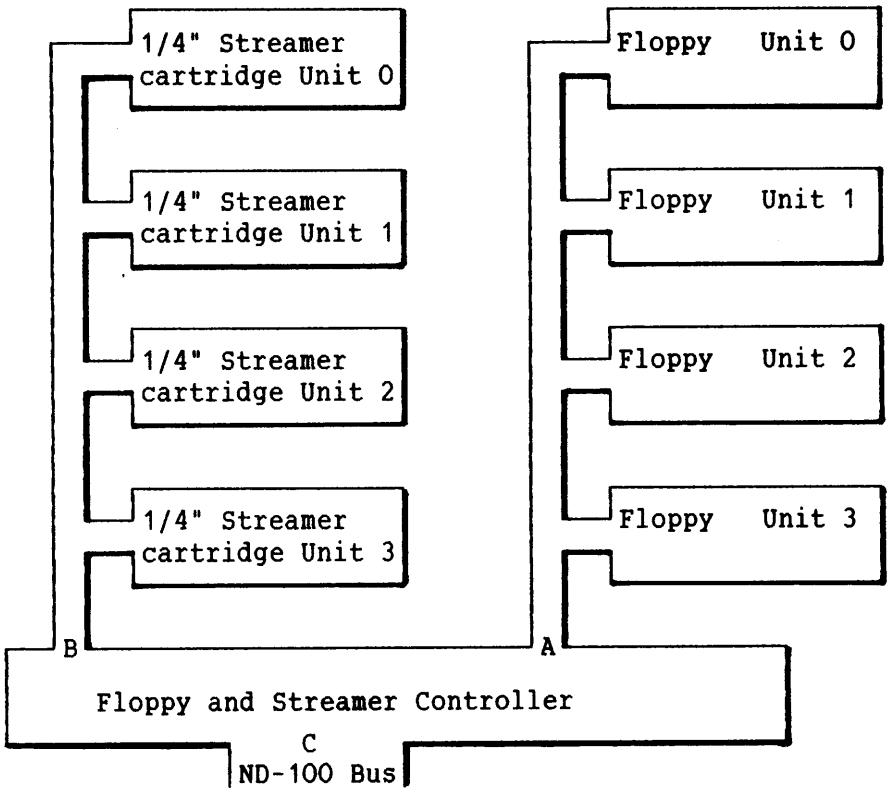


Fig. 4. Cable Wiring

The following pages contain the wiring lists for the cables going from the controller to the floppies and the streamers.

10.1 Wiring List for Floppy A Connector

Table 6. Wiring List for Floppy A Connector

Wire no.	Signal	Polarity	ND-100 plug Pin no.	Plug Panel 2*25 pins connector	Plug on Floppy Box 2*25 pin no.	50 Pin Card Edge Floppy Drive
1	GND		c 1	1	1	1
2	CURRSW	0	a 1	14	14	2
3	GND		c 2	2	2	3
4			a 2	15	15	4
5	GND		c 3	3	3	5
6			a 3	16	16	6
7	GND		c 4	4	4	7
8			a 4	17	17	8
9	GND		c 5	5	5	9
10	TWOS	0	a 5	18	18	10
11	GND		c 6	6	6	11
12	DISKCH	0	a 6	19	19	12
13	GND		c 7	7	7	13
14	SSEL	0	a 7	20	20	14
15	GND		c 8	8	8	15
16	INUSE	0	a 8	21	21	16
17	GND		c 9	9	9	17
18	HLP	0	a 9	22	22	18
19	GND		c 10	10	10	19
20	FINDEX	0	a 10	23	23	20
21	GND		c 11	11	11	21
22	FREADY	0	a 11	24	24	22
23	GND		c 12	12	12	23
24			a 12	25	25	24
25	GND		c 13	13	13	25
26	DS 0	0	a 13	1	1	26
27	GND		c 14	14	14	27
28	DS 1	0	a 14	2	2	28
29	GND		c 15	15	15	29
30	DS 2	0	a 15	3	3	30
				Ext.cable ←	Int.cable in box →	

Table 6. Wiring List for Floppy A Connector - Continued.

Wire no.	Signal	Polar-ity	ND-100 Plug Pin no.	Plug Panel 2*25 pin connector	Plug on Floppy Box 2*25 pin no.	50 Pin Card Edge Floppy Drive
31	GND		c 16	16	16	31
32	DS 3	0	a 16	4	4	32
33	GND		c 17	17	17	33
34	DIR	0	a 17	5	5	34
35	GND		c 18	18	18	35
36	STEP	0	a 18	6	6	36
37	GND		c 19	19	19	37
38	WOAT	0	a 19	7	7	38
39	GND		c 20	20	20	39
40	WG	0	a 20	8	8	40
41	GND		c 21	21	21	41
42	FTROO	0	a 21	9	9	42
43	GND		c 22	22	22	43
44	FWPRT	0	a 22	10	10	44
45	GND		c 23	23	23	45
46	RD	0	a 23	11	11	46
47	GND		c 24	24	24	47
48			a 24	12	12	48
49	GND		c 25	25	25	49
50			a 25	13	13	50
				Ext.cable ←→	Int.cable in box ←→	

Internal Cable : 50 wire flatcable
External Cable : 50 wire flatcable

If a twisted pair of flatcables is used, then 20 ft. (6 meters).

10.1.1 Terminating the floppy

150 ohm. to +5v, on the last drive in the chain. NB!! Only on the last one. Cable length max. 10 ft. (3 meters).

10.2 Wiring List for Streamer B Connector

Table 7. Wiring List for Streamer B Connector

Wire no.	Signal	Polarity	ND-100 Plug Pin no.	50 Pin Card Edge Streamer
1	GND		c 1	1
2	SPARE		a 1	2
3	GND		c 2	3
4	SPARE		a 2	4
5	GND		c 3	5
6	SPARE		a 3	6
7	GND		c 4	7
8	SPARE		a 4	8
9	GND		c 5	9
10	SPARE		a 5	10
11	GND		c 6	11
12	DB7	0	a 6	12
13	GND		c 7	13
14	DB6	0	a 7	14
15	GND		c 8	15
16	DB5	0	a 8	16
17	GND		c 9	17
18	DB4	0	a 9	18
19	GND		c 10	19
20	DB3	0	a 10	20
21	GND		c 11	21
22	DB2	0	a 11	22
23	GND		c 12	23
24	DB1		a 12	24
25	GND		c 13	25
26	DB0	0	a 13	26
27	GND		c 14	27
28	ONL	0	a 14	28
29	GND		c 15	29
30	REQ	0	a 15	30
31	GND		c 16	31
32	RESET	0	a 16	32
33	GND		c 17	33
34	XFER	0	a 17	34
35	GND		c 18	35

Table 7. Wiring List for Streamer B Connector - Continued.

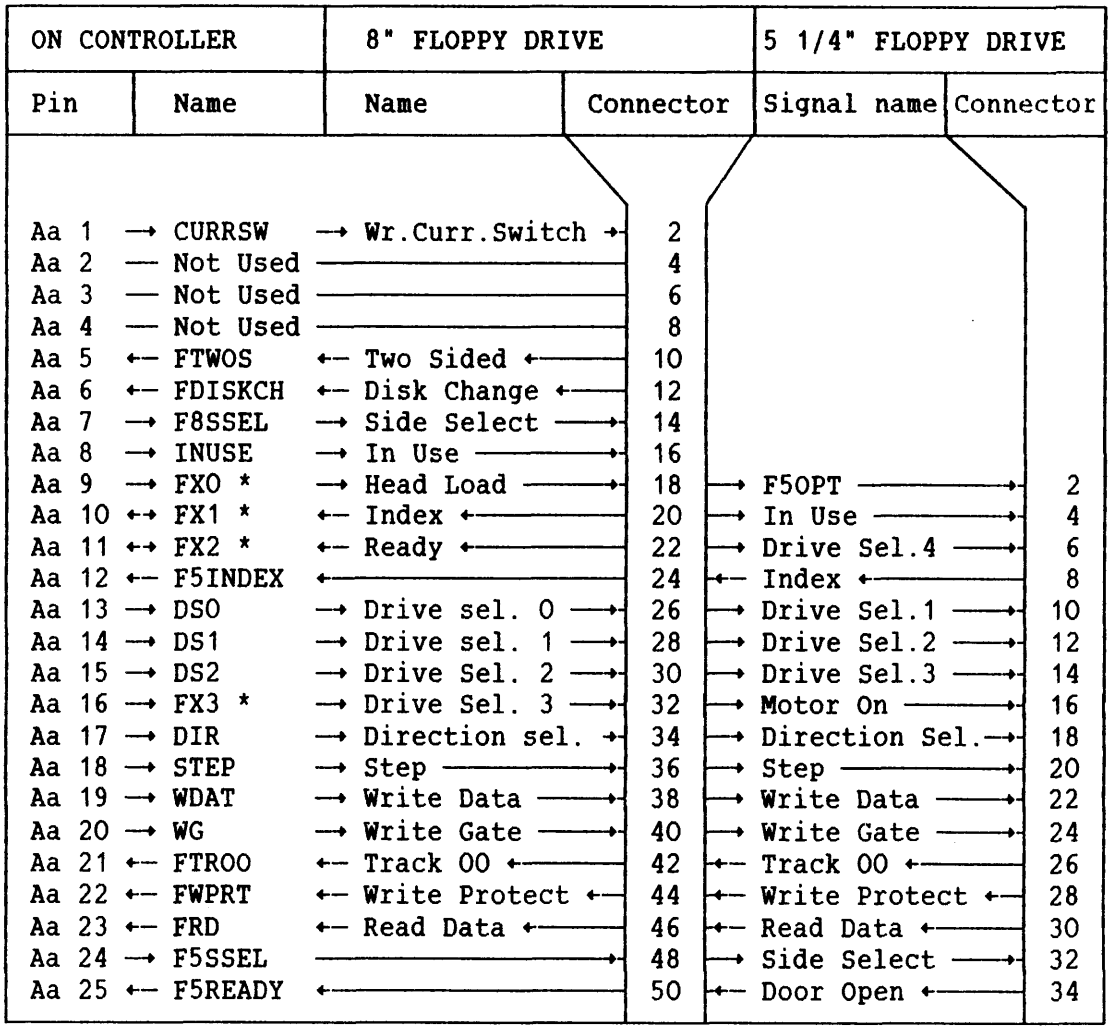
Wire no.	Signal	Polar-ity	ND-100 Plug Pin no.	50 Pin Card Edge Streamer
36	ACK	0	a 18	36
37	GND		c 19	37
38	RDY	0	a 19	38
39	GND		c 20	39
40	EXC	0	a 20	40
41	GND		c 21	41
42	DIR	0	a 21	42
43	GND		c 22	43
44	SPARE	0	a 22	44
45	GND		c 23	45
46	SPARE	0	a 23	46
47	GND		c 24	47
48	SPARE		a 24	48
49	GND		c 25	49
50	SPARE		a 25	50

50 wire flatcables. Cable length max. 10 ft. (3 meters). If a twisted pair of flatcables is used, then 20 ft. (6 meters).

10.2.1 Terminating the streamer

220 ohm. to +5v, and 330 ohms to ground. On the last drive in the chain. NB!! Only on the last one.

10.2.2 Cable for 8" and 5 1/4" floppy - Card no 3112



* - Signals marked with a * , are dependent upon the type of drive selected (82 or 5 1/4").

On Controller	8" Floppy	5 1/4" Floppy
FX0 - F8HLD/F5OPT	Head Load - output	Option - output
FX1 - F8INDEX/F5INUSE	Index - input	In Use - output
FX2 - F8READY/F5DS3	Ready - input	Drive Sel.3 - output
FX3 - F8DS3/F5MOTOR	Drive Sel.3 - output	Motor On - output

CHAPTER 11

ONE-SHOTS AND RC-DELAYS ON THE FLOPPY DISK CONTROLLER

11 ONE-SHOTS AND RC-DELAYS ON THE FLOPPY DISK CONTROLLER

Table 8. One-Shots and RC-Delays on the Floppy Disk Controller

Page	Position	Time	Component & Value	Comments
1	2C	1us	R27=10K, C16=220pF	Master clear pulse to controller
5	25D	35-50ms	R41=27K, C19=2,2uF	Head load delay (settle time on drive)
5	25D	50-80us	R42=82K, C20=10nF	Reset pulse to floppy chip (fd 1797)
5	15D	150-200ns	R45=220, C25=470pF	Read data to floppy chip
5		40ns	C26 AND C27	Delay to compensate for lost margin in fd1797
5	26E	200-300ns	R44=680, C24=680pF	Write data pulse (only 3106)
5	27F	120-180ns	R43=390, C21=330pF	Precomp. time (only 3106)

A P P E N D I X A

REGISTER SPECIFICATIONS

DD-T Register - (53 Hex.)

BIT 0 : 0 DMA to the ND-100 - 1 DMA from the ND-100
" 1 : Enable DMA-TRANS ND-100 <=> Z80
" 2 : Not used
" 3 : Not used
" 4 : TEST-BIT 0 - Select registers to be tested.
" 5 : TEST-BIT 1 - See note below.
" 6 : Not used
" 7 : NTEST - Enable testing of registers in bus-ctrl.

NOTE !

Bits 4 and 5 :

Test-bit	0	1	Select registers:
Value	0	0	Not used
	0	1	Address registers
	1	0	Data registers
	1	1	Status register

NSTAT ND-100 Status-Register - (56 Hex.)

BIT 0 : ND-100-Status bit 08
" 1 : ND-100-Status bit 09
" 2 : ND-100-Status bit 10
" 3 : ND-100-Status bit 11
" 4 : ND-100-Status bit 12
" 5 : ND-100-Status bit 13
" 6 : ND-100-Status bit 05
" 7 : ND-100-Status bit 06

NOTE !

For the meaning of these bits see page 14.

NFINI Set RFT and Status - (57 Hex.)

BIT 0 : OR of errors (bit 4 in hardware status word)
" 1 : Hard error (bit 7 in hardware status word)
BIT 2-7 : Not used

NOTE !

RFT is always set when writing to this register.

CW1 Control Word-Low and DMA-Status - (50 Hex.)

BIT 0 : Autoload
" 1 : Test mode (sets controller in test mode)
" 2 : This command is for the streamer
" 3 : Continue current transfer (used to enable for into)
" 4 : Activate - fetch command from the ND-100
" 5 : ENI - Interface is enabled for int.
" 6 : DMA Is enabled (DMA ND-100 <=> Z80)
" 7 : Transfer error DURING DMA - BERROR.

CW2 Control Word High-Part - (54 Hex.)

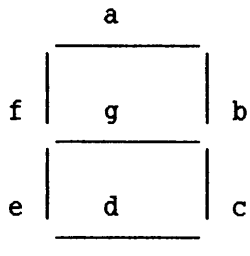
BIT 0 : Not used (GND)
" 1 : Hardware Control word Bit 9
" 2 : Hardware Control word Bit 10
" 3 : Hardware Control word Bit 11
" 4 : Hardware Control word Bit 12
" 5 : Hardware Control word Bit 13
" 6 : Hardware Control word Bit 14
" 7 : Hardware Control word Bit 15

NOTE !

See Hardware Control word on page 17 for the meaning of these bits.

SDISP Set Data to Display - (40 Hex.)

BIT	0	-	SEGMENT	a
"	1	-	"	b
"	2	-	"	c
"	3	-	"	d
"	4	-	"	e
"	5	-	"	f
"	6	-	"	g



The display contains 3 numbers. The number to be lit is selected by loading ENDISP.

ENDISP Display and Mode Register - (41 Hex.)

BIT	0	Disable timeout
"	1	Enable continues DMA
"	2	Not used
"	3	Precompensation (0=off, 1=on)
"	4	Not used
"	5	Select first digit in display
"	6	" second digit in display
"	7	" third digit in display

SS Streamer Status Register - (61 Hex.)

BIT	0	: SEXC - Exception
"	1	: SRDY - Drive/formatter ready
"	2	: SACK - Acknowledge on data transfer
"	3	: SXFER- Transfer from drive
"	4	: SPAER- QIC-02 Bus parity error
"	5	: Not used
"	6	: Not used
"	7	: Not used

SMR Streamer Modus Register - (61 Hex.)

BIT 0 : SWR - Write transfer
" 1 : SONL - Online to drive
" 2 : STEST - Test mode
" 3 : SEIRDY- Enable interrupt on ready
" 4 : DTR - Data transfer
" 5 : SPAPO - Set parity polarity

FDVSEL Device Select and Mode Register - (74 Hex.)

BIT 0 - Select drive 0
" 1 - Select drive 1
" 2 - Select drive 2
" 3 - Select drive 3
" 4 - Select density (Dual=0, Single=1)
" 5 - Enable compare circuit
" 6 - Enable VCO adjustment
" 7 - Set in-use-line

FCCLR Register - (75 Hex.)

Used to produce a clear pulse for the FD1797, no data required.

FDST Floppy Drive Status - (77 Hex.) Card no. 3106

Read the status lines from the selected drive.

BIT 0 - Ready
" 1 - Double sided diskette
" 2 - Disk changed while selected
" 3 - On track 00
" 4-6 - Not used
" 7 - High to distinguish between 3106 and 3112

All bits are true when zero.

CARD NO. 3112 :

FLSTS Floppy Drive Status - (77 Hex.)

Bit 0 - 8" ready
" 1 - Double sided diskette
" 2 - Disk changed
" 3 - On track 00
" 4 - 5 1/2" ready
" 5-6 - Not used
" 7 - Low to distinguish between 3106 and 3112

FMOD2 Floppy Modus 2 Register - (77 Hex.)

The FMOD2 register is used to hold parameters that selects the 5 1/4" or the 82 floppy interface. In addition, it is used to program the write precompensation circuit.

Bit	Name	Polarity	Function
0	EN5CLK	1	Selects the 5 1/4" clock rate (250 kbit)
1	EN5IF	1	Selects the 5 1/4" interface/connector
2	MOTORON	1	Turns the floppy drive motor ON
3	F5OPT	1	Connected to 5 1/4" cable - line 2
4	PAM0	1	Bit 4-5 specifies the amount of write
5	PAM1	1	precomp. (125, 187.5, 250, 312.5 ns)
6	ENPRE	1	Enables precompensation
7	TGX	1	Turn precompensation on if ENPRE is true

FLSTS FLoppy Drive Status - (77 Hex.)

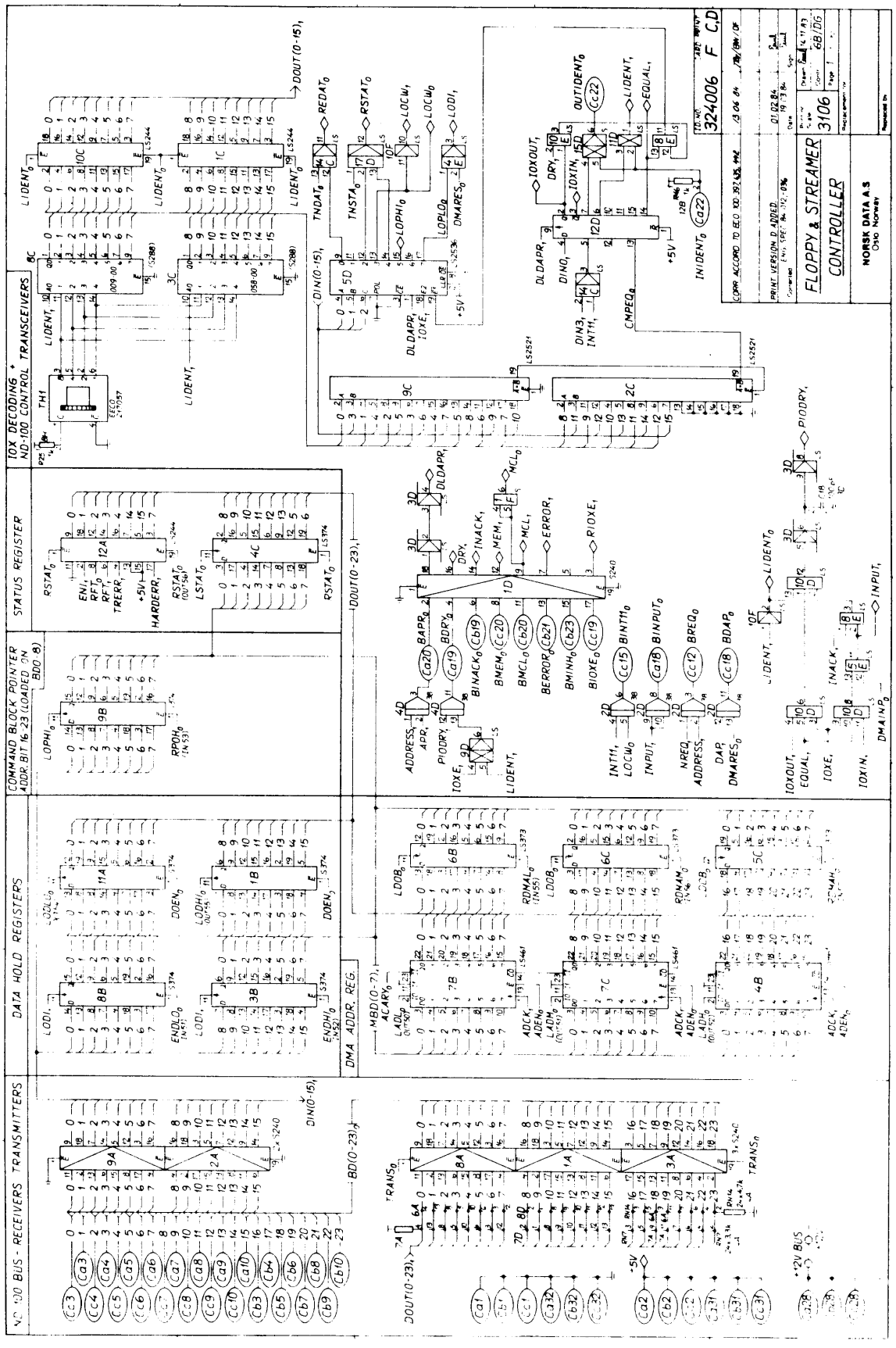
The FLSTS is expanded with two bits, one used to differ between the 3106 and the 3112 board, the other being the Ready signal from the 5 1/4" drives.

Bit	Name	Polarity	Function
0	F8READY	0	Ready signal from the 8" drives
1	FTWOS	0	Two-sided signal from the 8" drives
2	FDISKCH	0	Disk-change signal the 8" drives
3	TR00	0	On Track Zero signal from all the drives
4	F5READY	0	Ready signal from the 5 1/4" drives
5	SPARE	0	Reserved
6	SPARE	0	Reserved
7	GND	0	0 = 3112 Board, 1 = 3106 Board

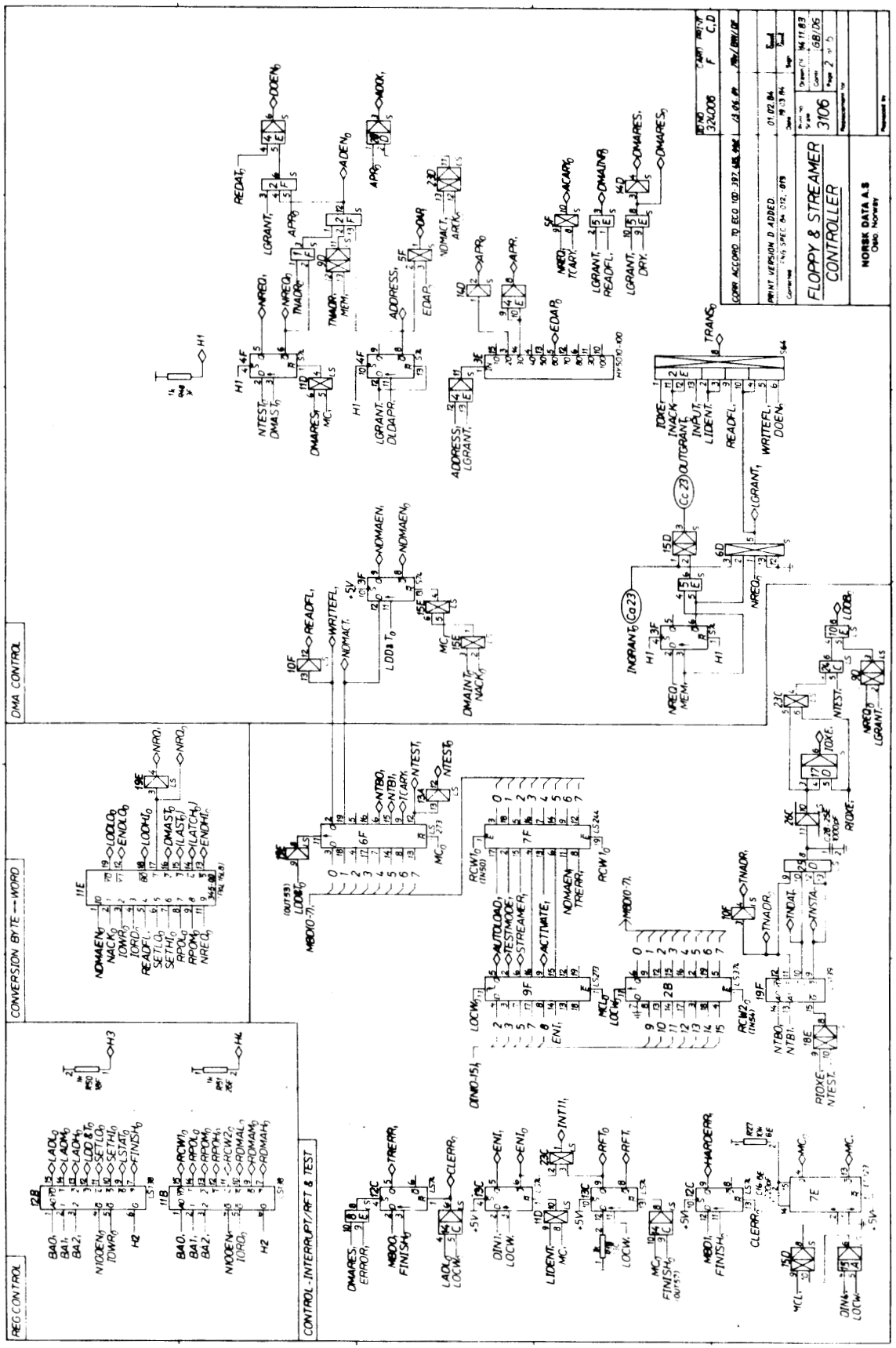
A P P E N D I X B

LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

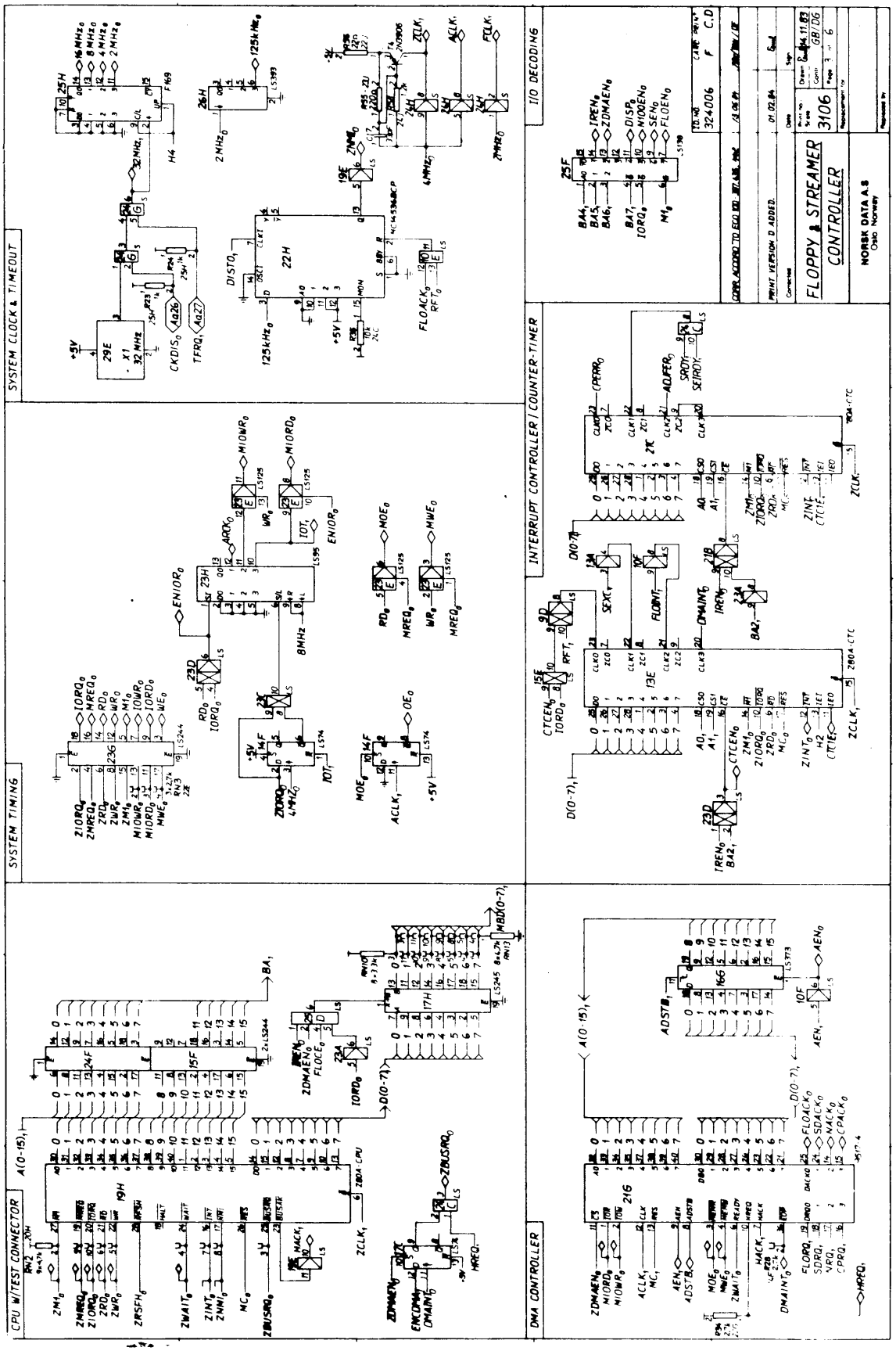


LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

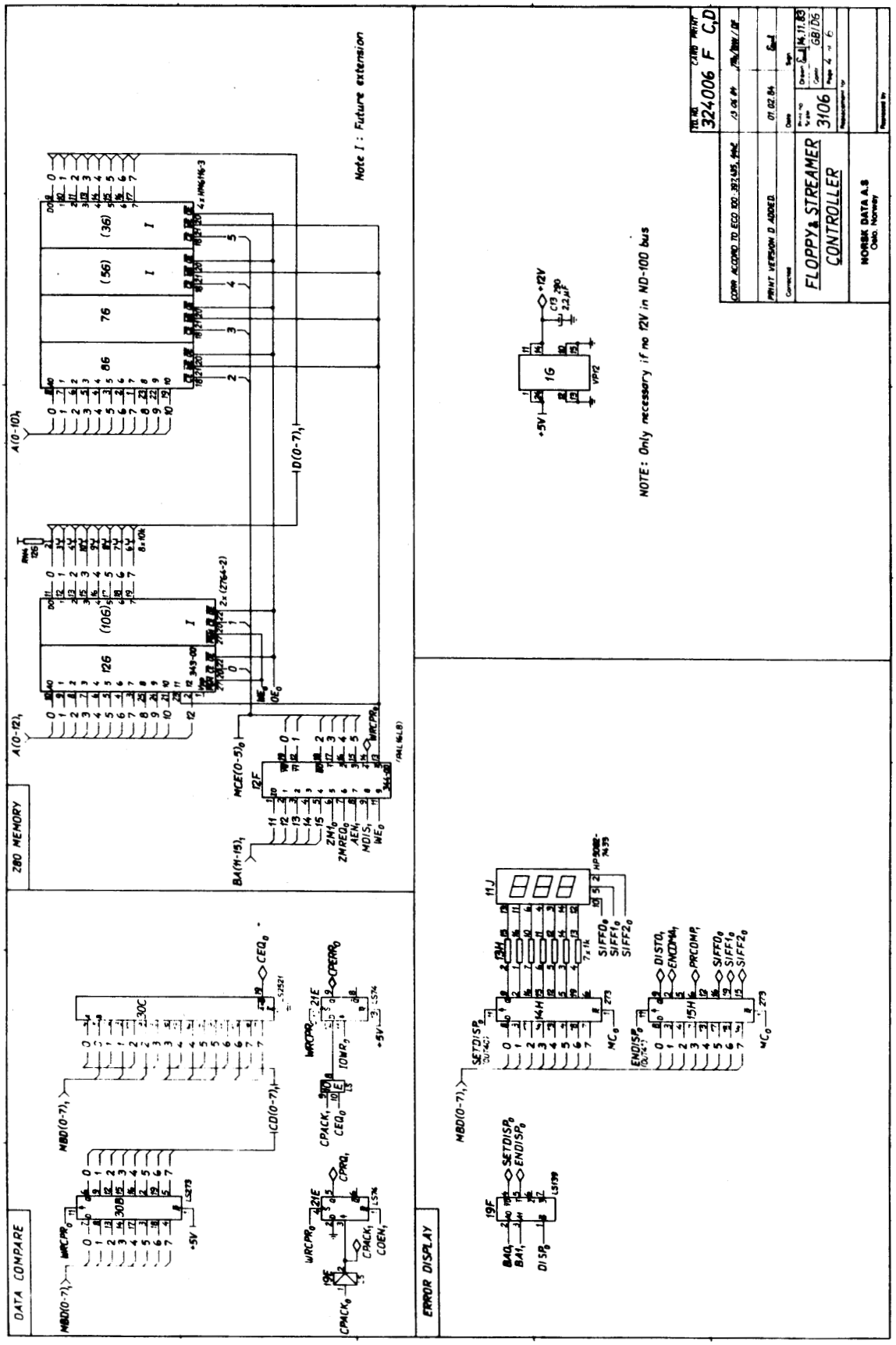


ND-11.021.01

LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)



LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)



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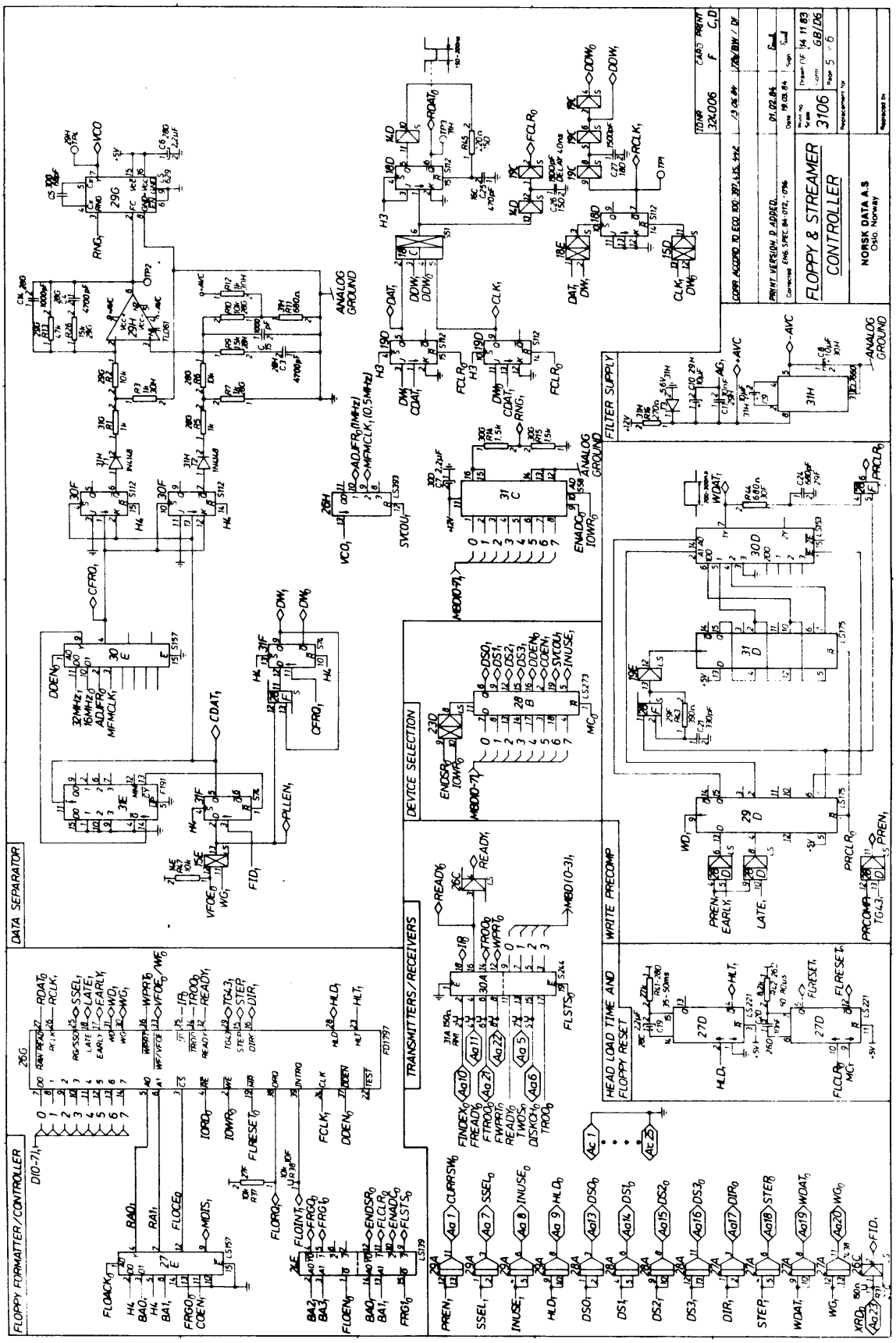
LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)



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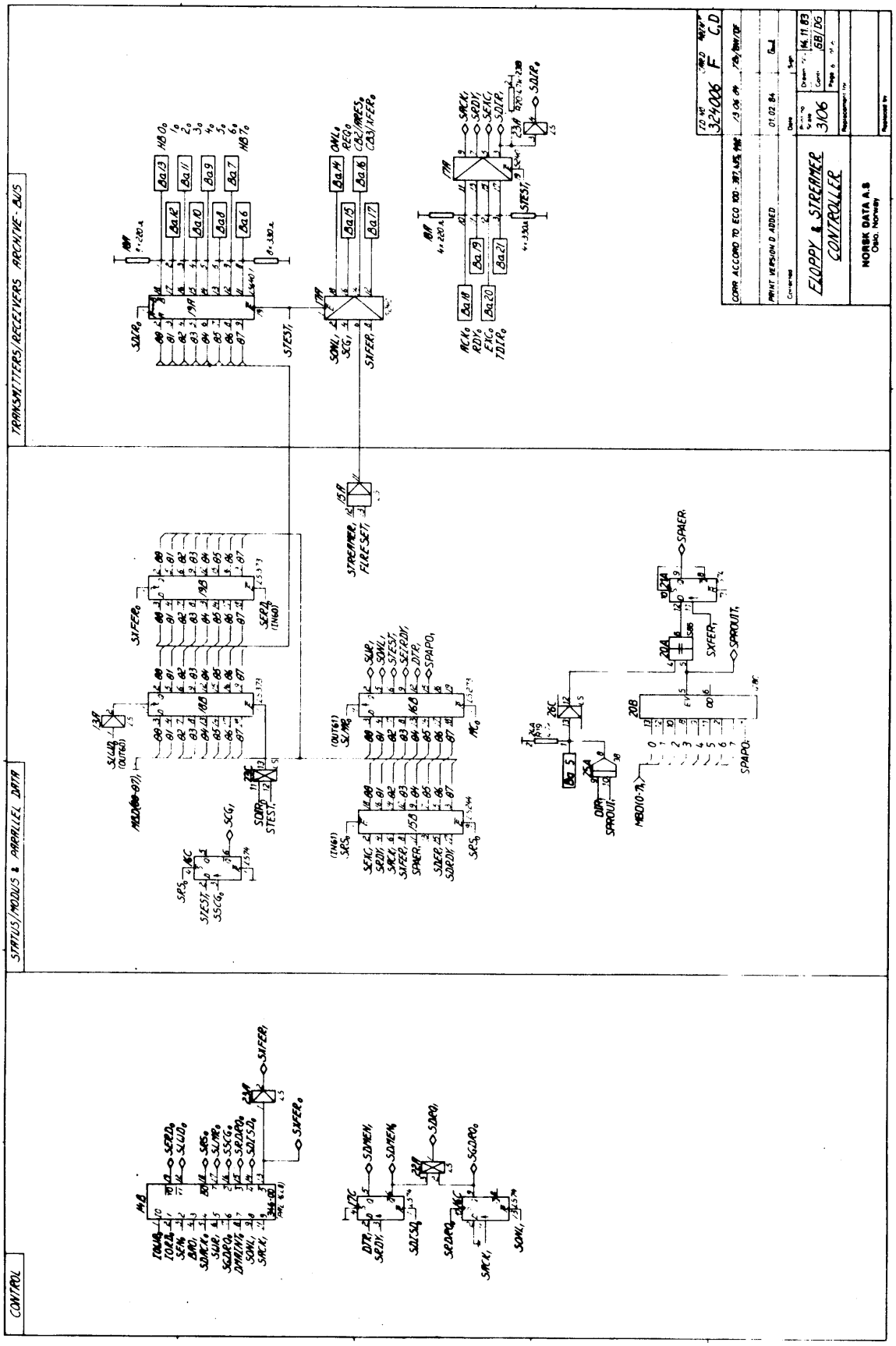
LOGIC DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

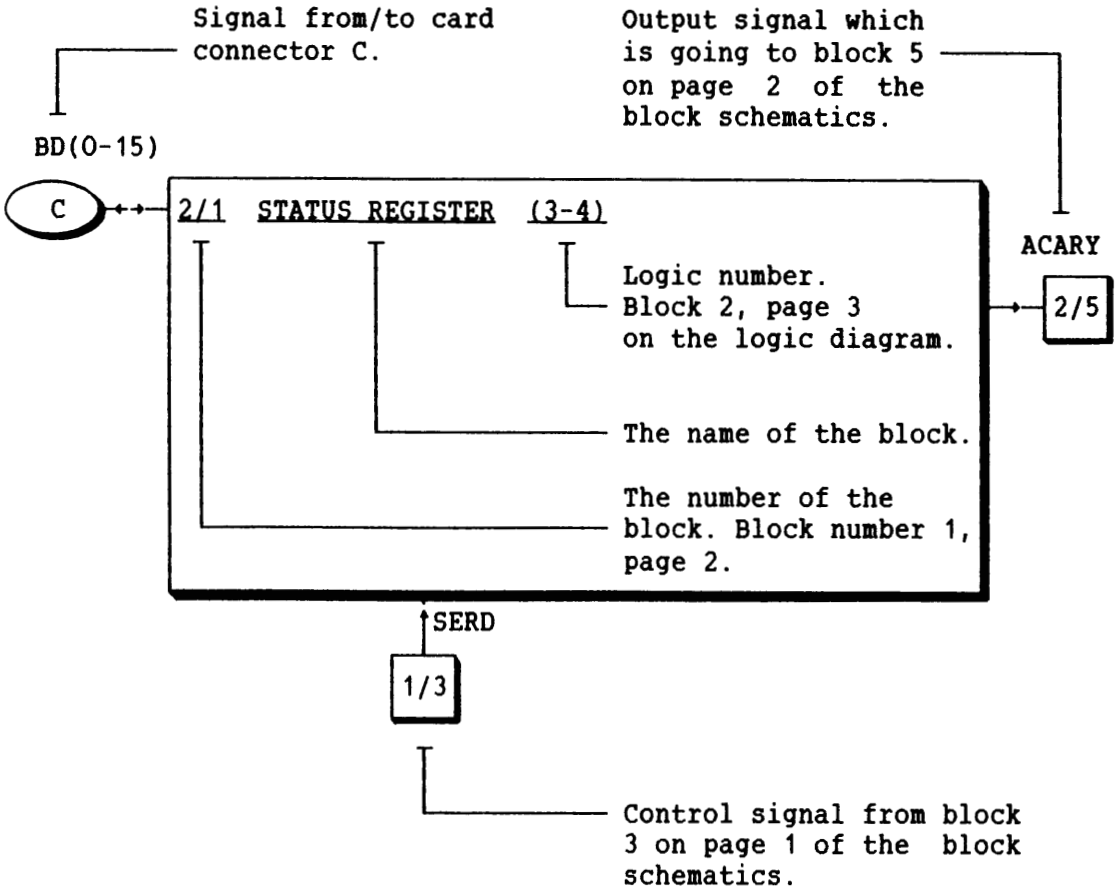


A P P E N D I X C

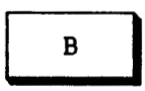
DESCRIPTIVE BLOCK DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

DESCRIPTIVE BLOCK DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

HOW TO READ THE BLOCK SCHEMATICS :



Connector A

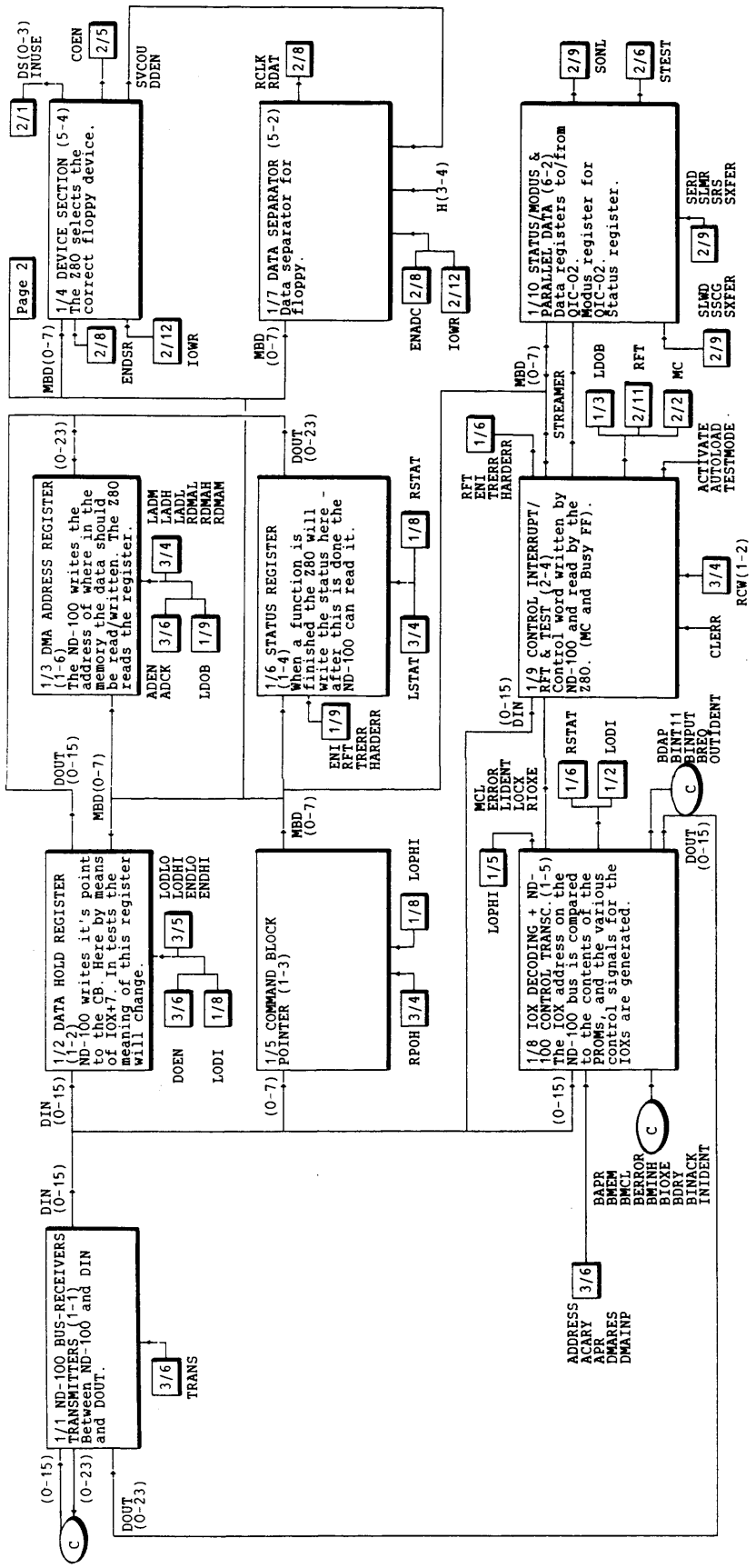


Connector B

Connector C

DESCRIPTIVE BLOCK DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

DESCRIPTIVE BLOCK DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)



ND-11.021.01

DESCRIPTIVE BLOCK DIAGRAM - 8" FLOPPY AND STREAMER CONTROLLER (Card no. 3106)

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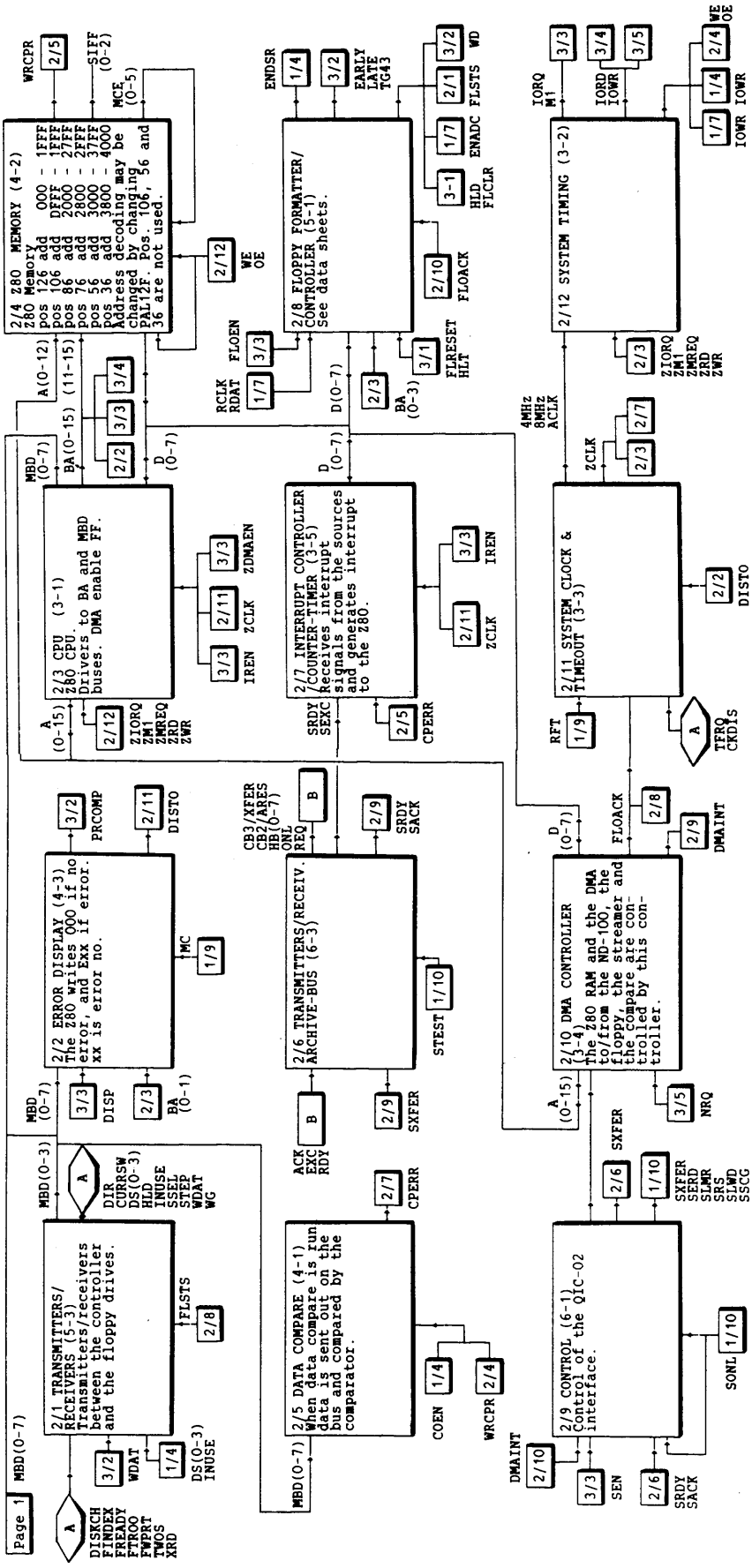

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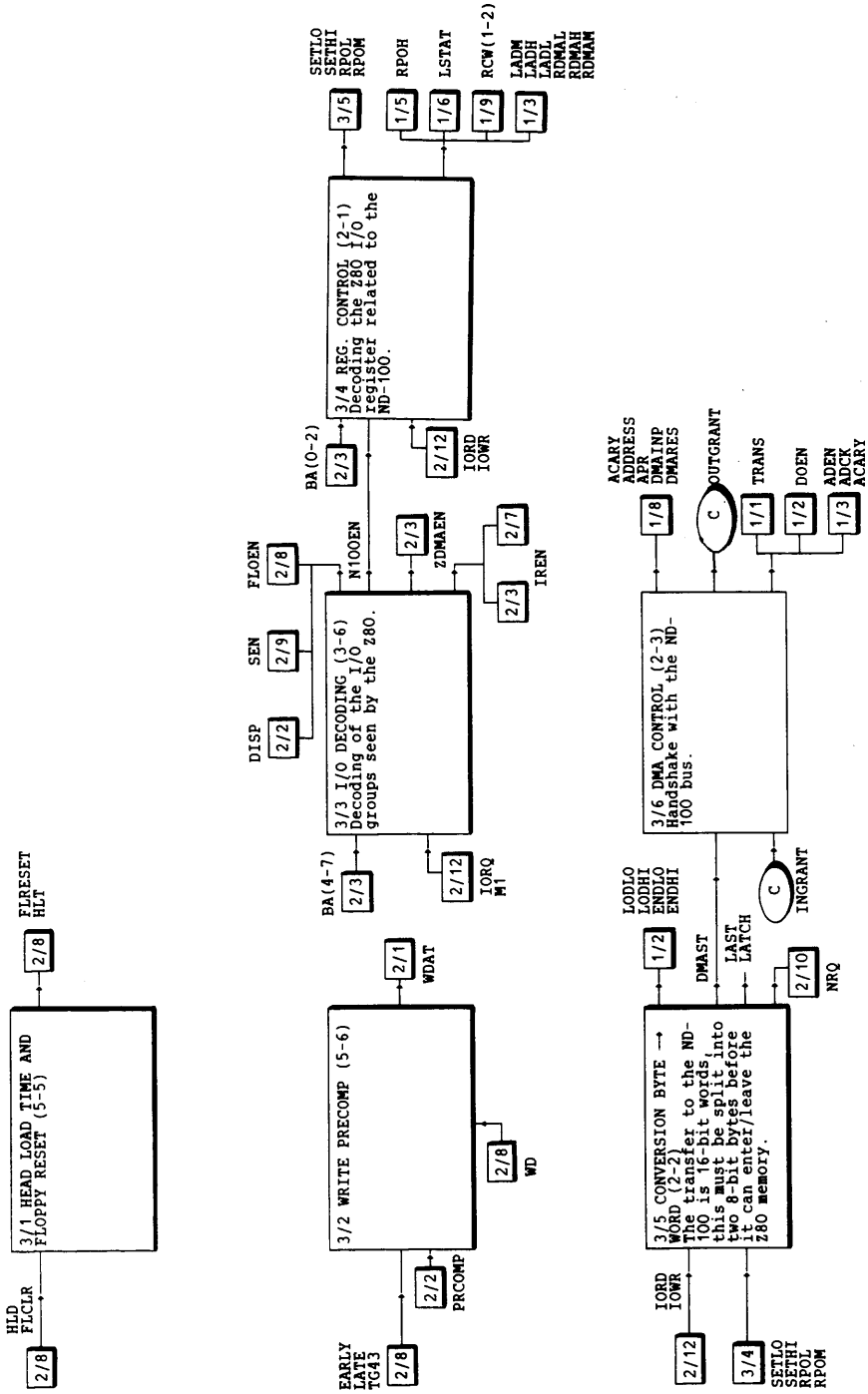
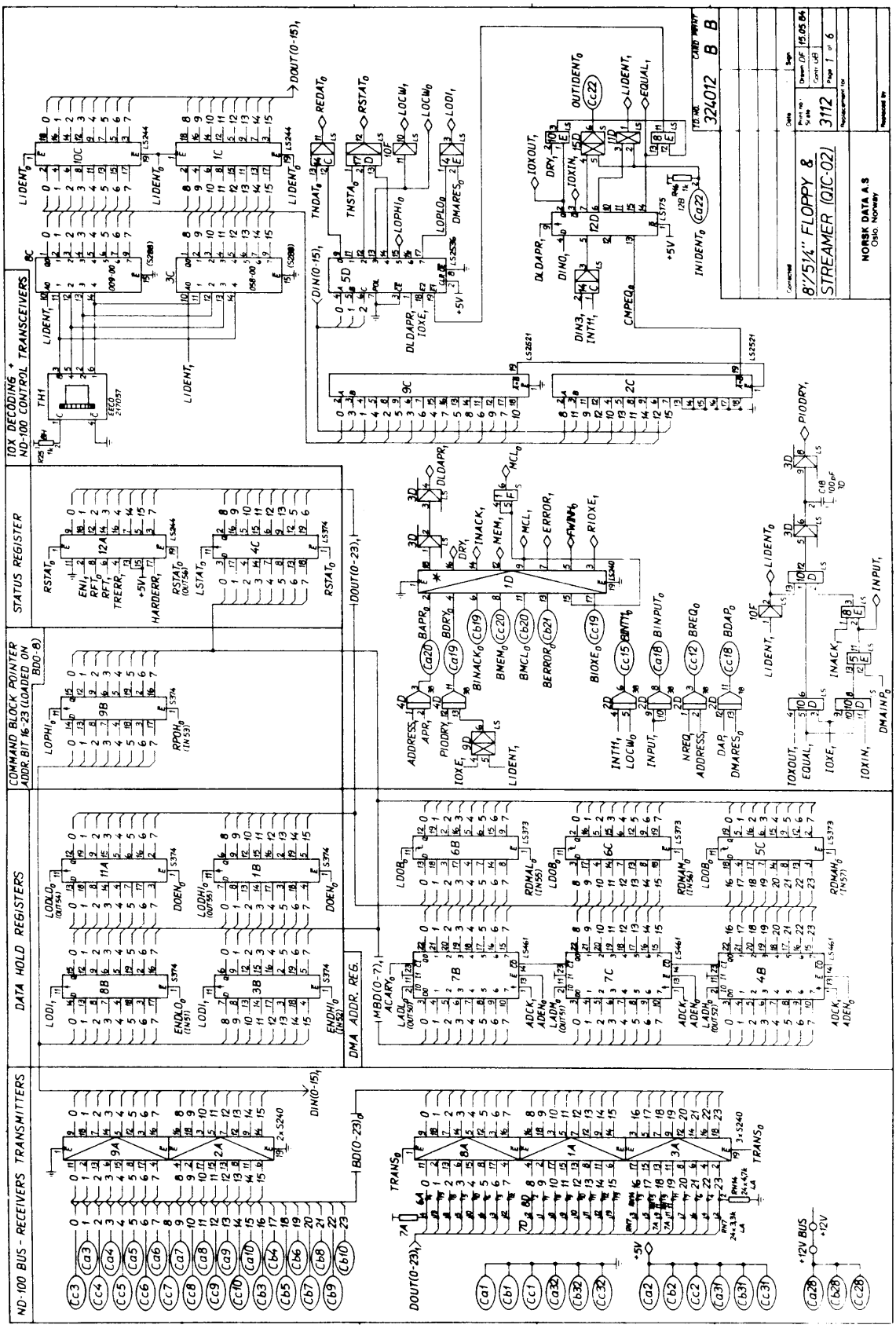


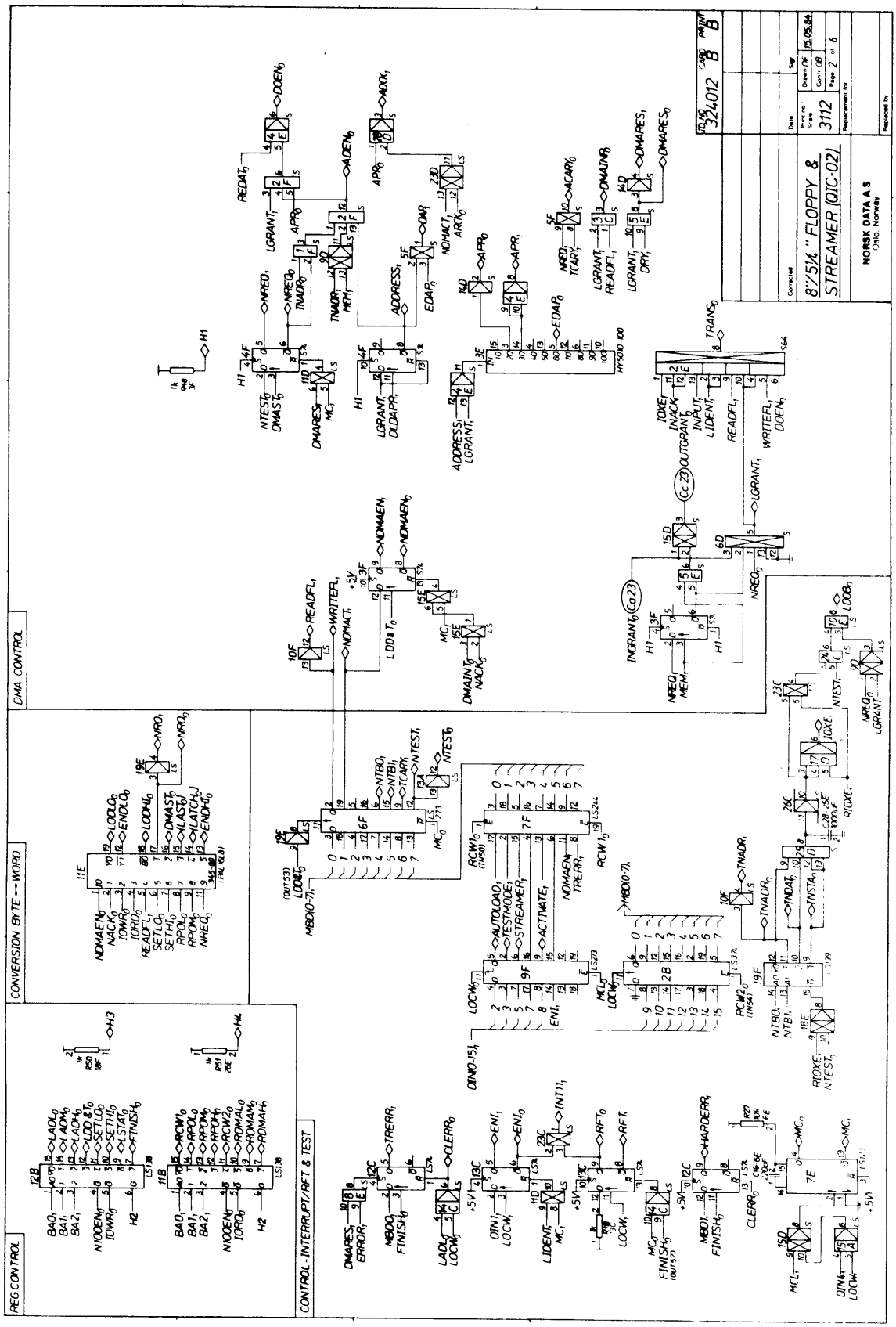
A P P E N D I X D

LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

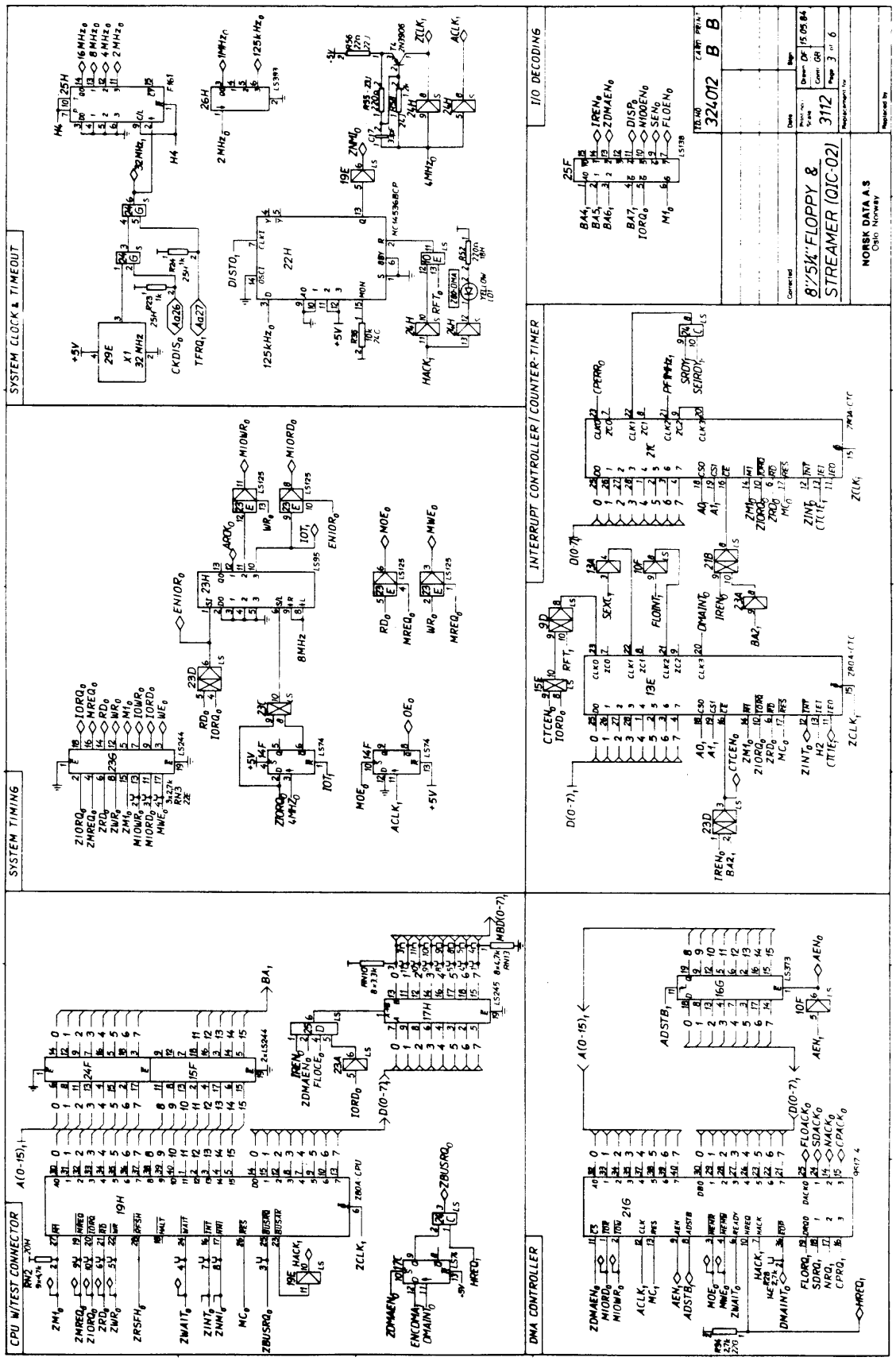
LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

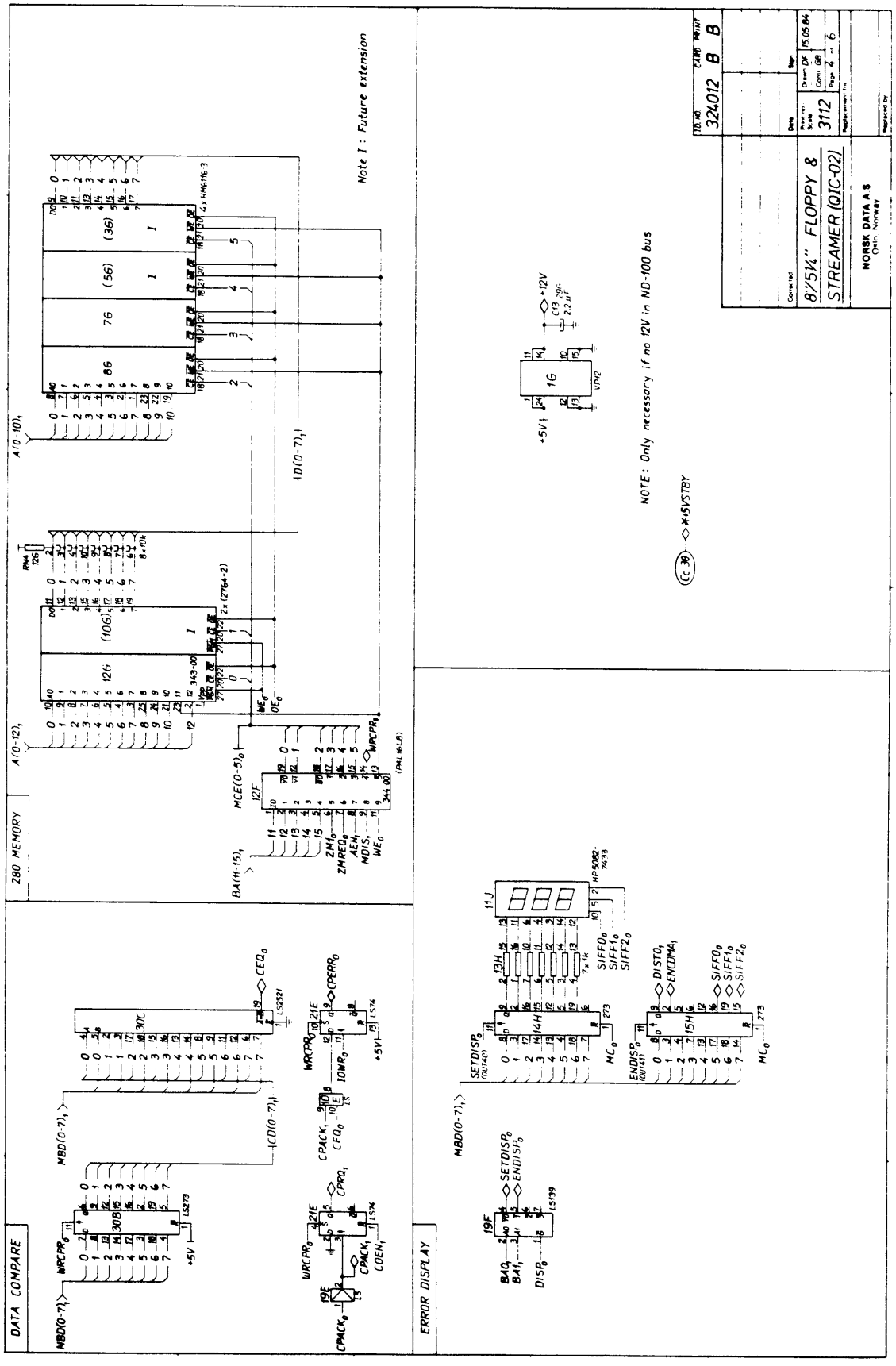


LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

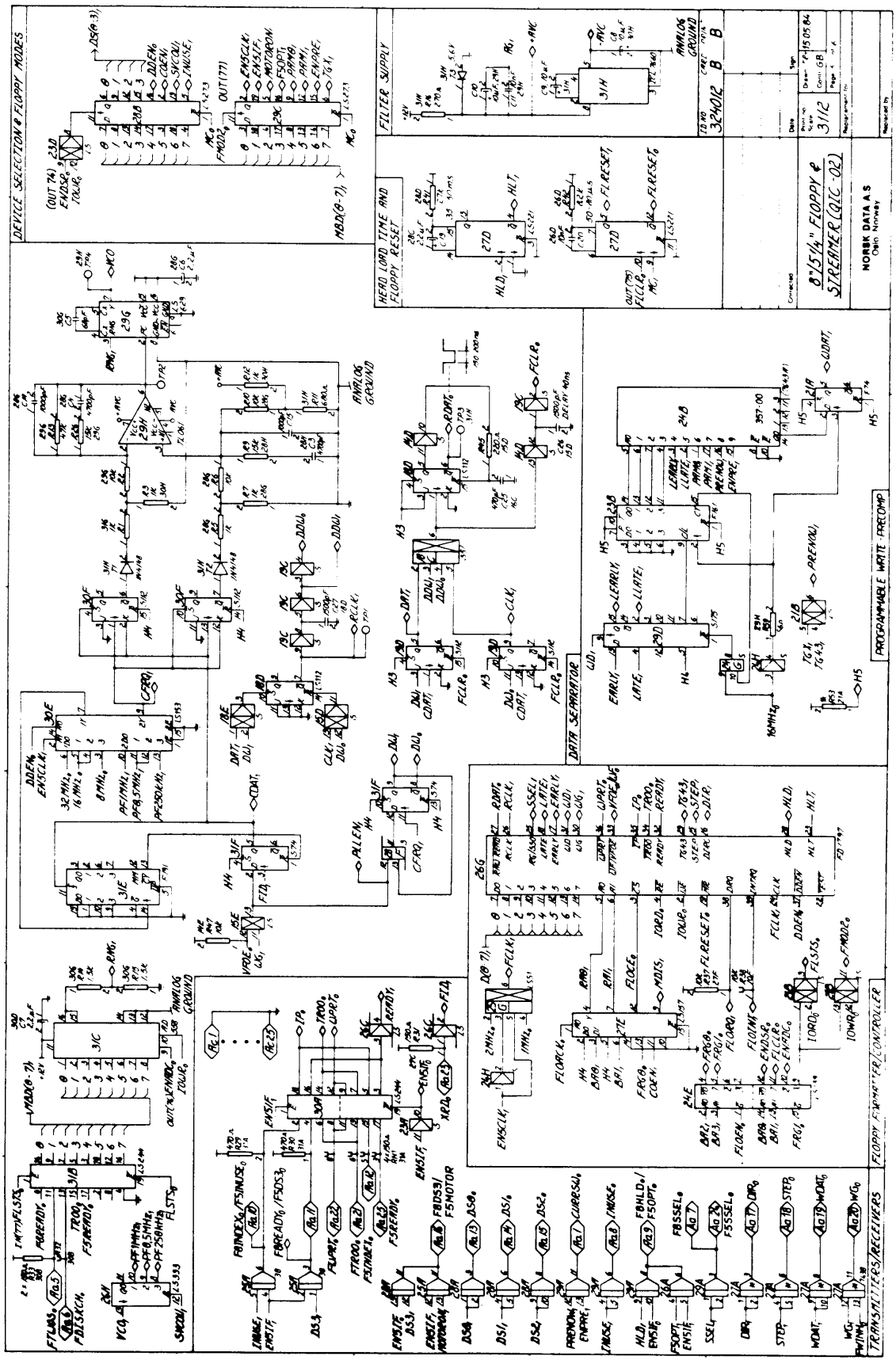


LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)



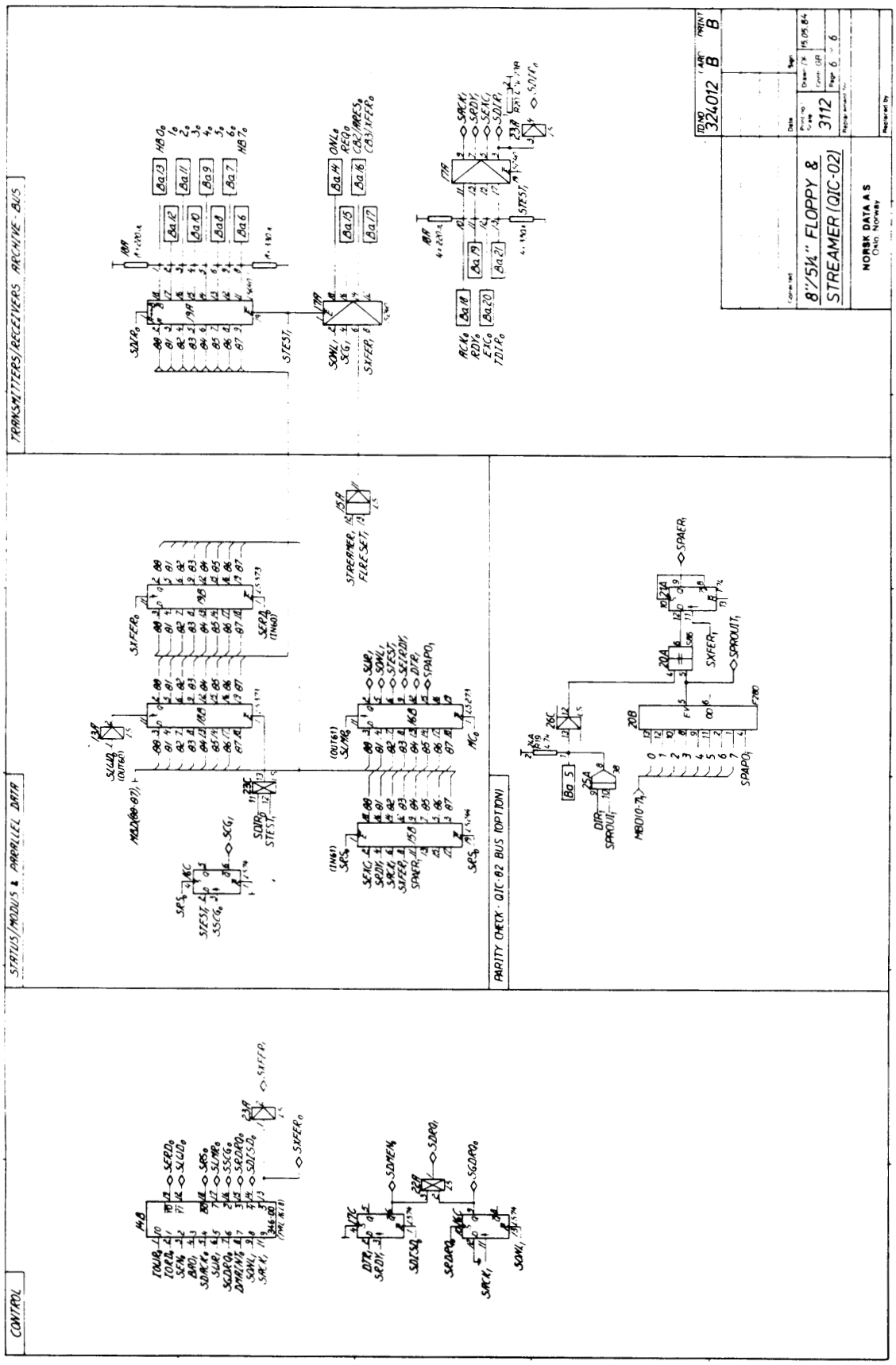

Note 1 : Future extension
NOTE: Only necessary if no 12V in ND-100 bus
8"/5¼" FLOPPY & STREAMER (QIC-02)
NORSK DATA A.S
Oslo, Norway
324012 B 8
3112
Z80 MEMORY
DATA COMPARE
ERROR DISPLAY

LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)



ND-11.021.01

LOGIC DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)



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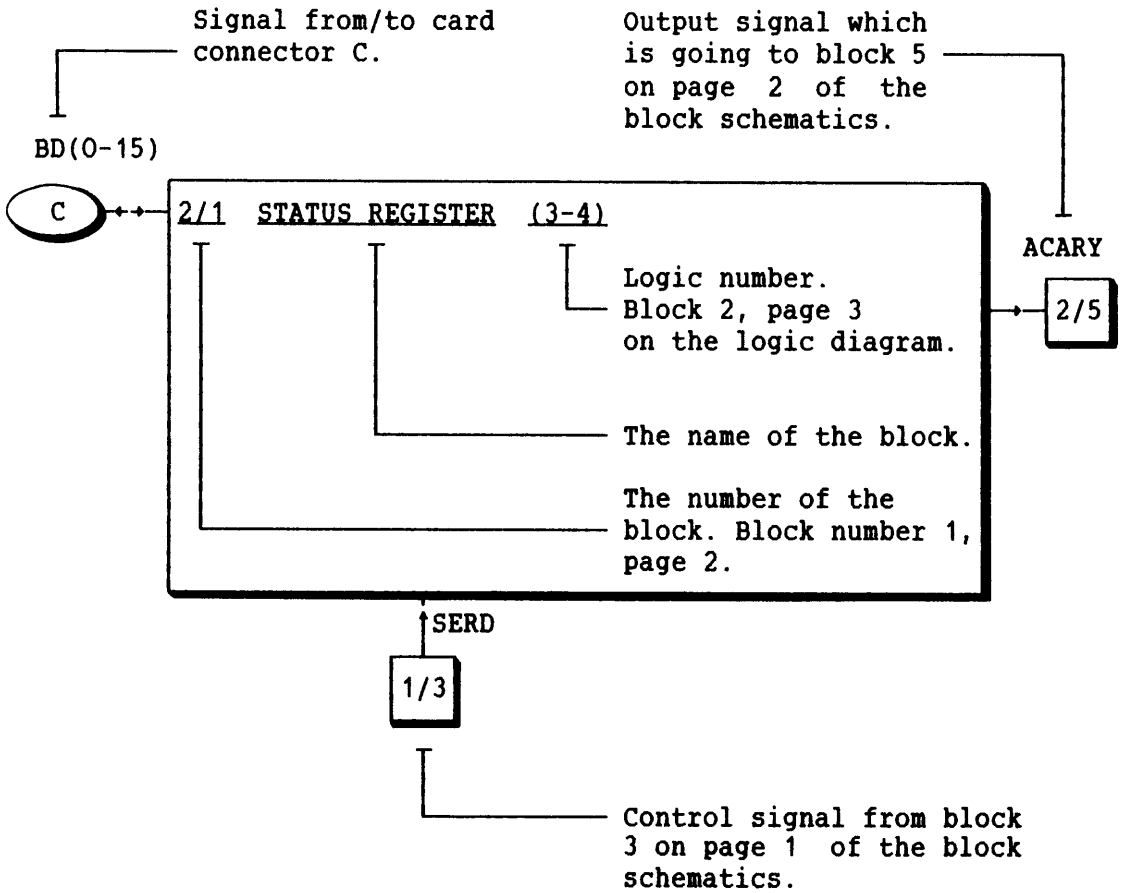
A P P E N D I X E

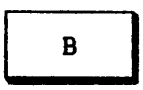
DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

HOW TO READ THE BLOCK SCHEMATICS :



Connector A



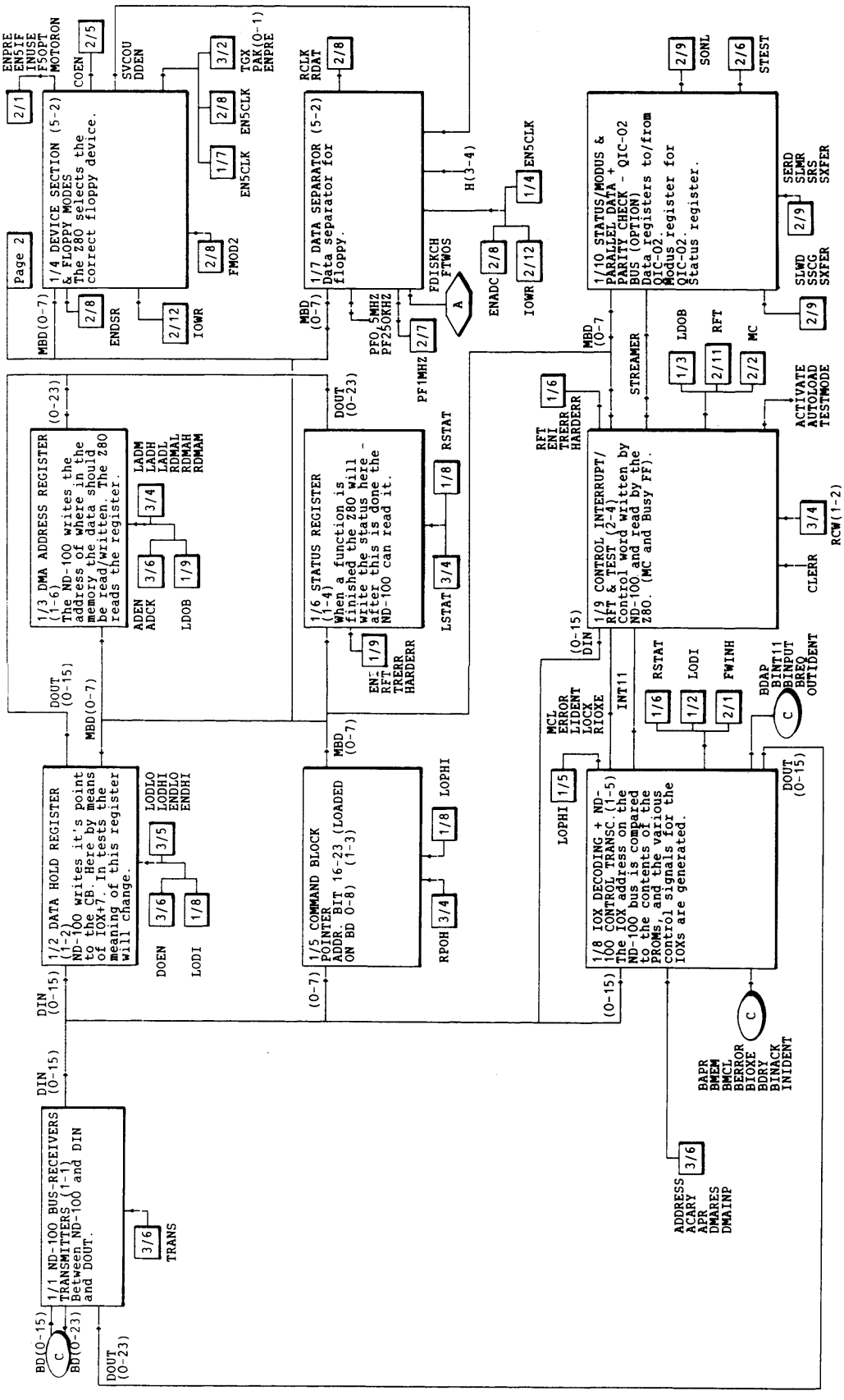
Connector B

Connector C

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

FLOPPY AND STREAMER CONTROLLER - 3106/3112

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

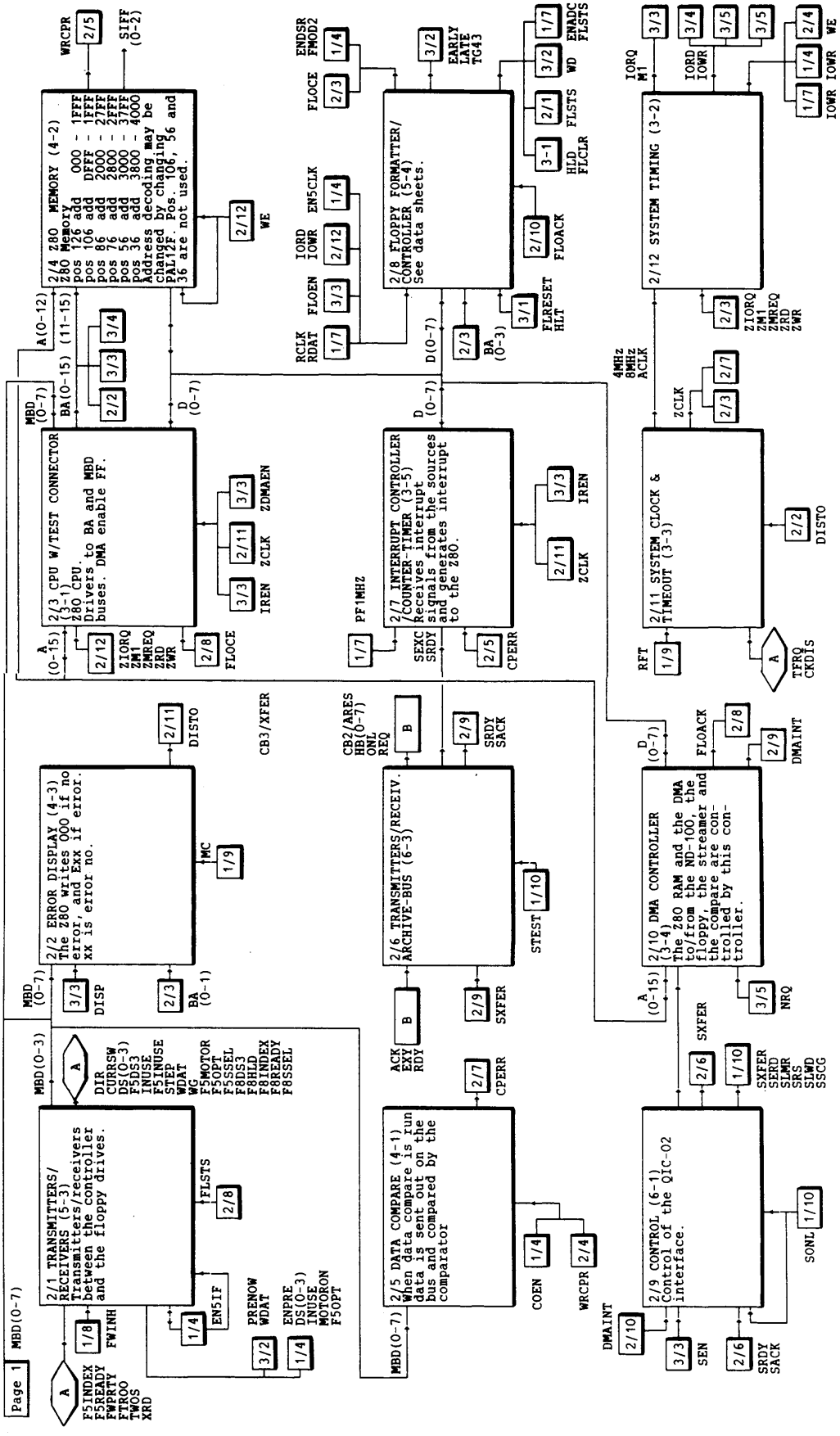


ND-11.021.01

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

FLOPPY AND STREAMER CONTROLLER - 3106/3112

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)



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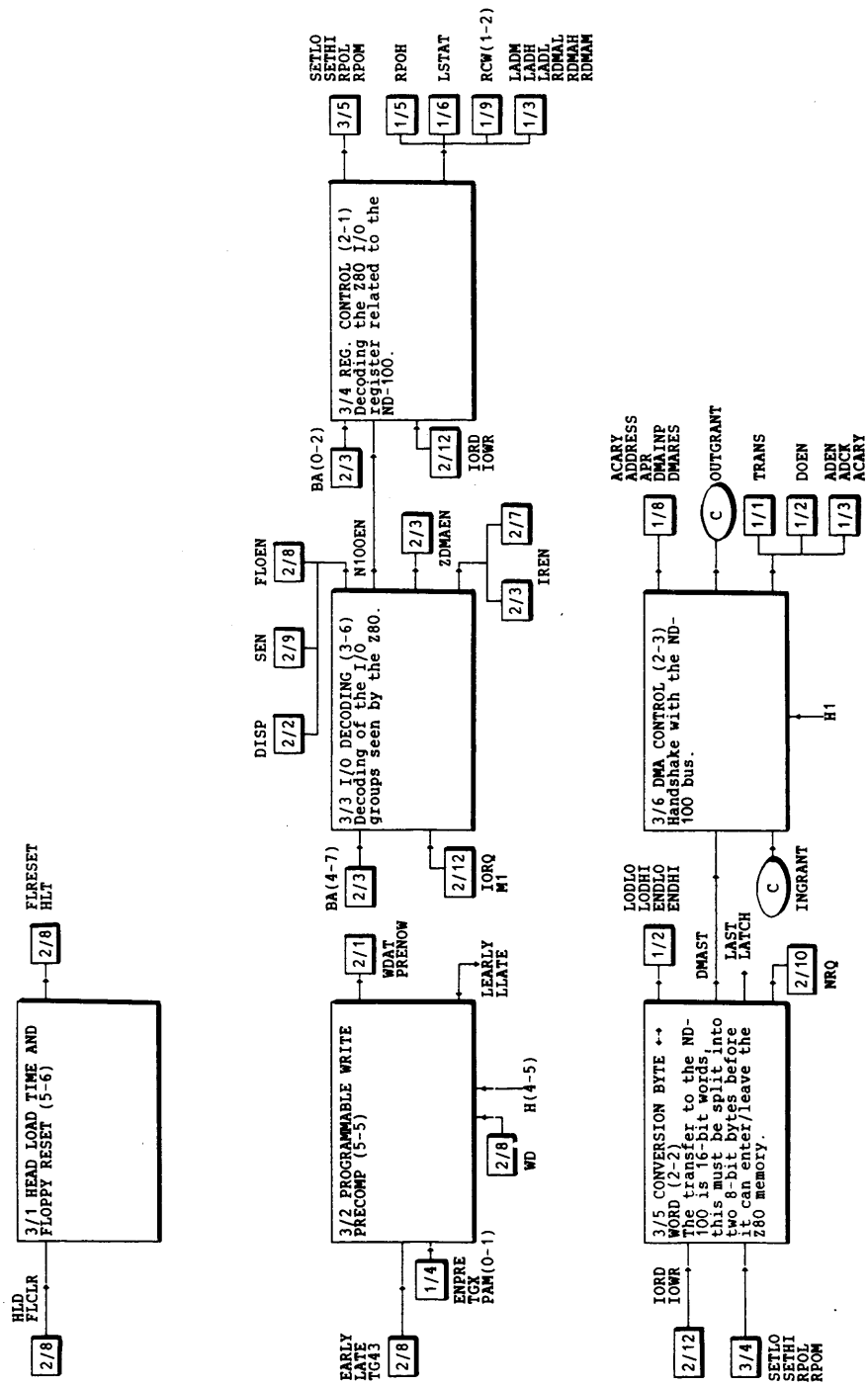

DESCRIPTIVE BLOCK DIAGRAM - 8" AND 5 1/4" FLOPPY AND STREAMER CONTROLLER (Card no. 3112)

Index

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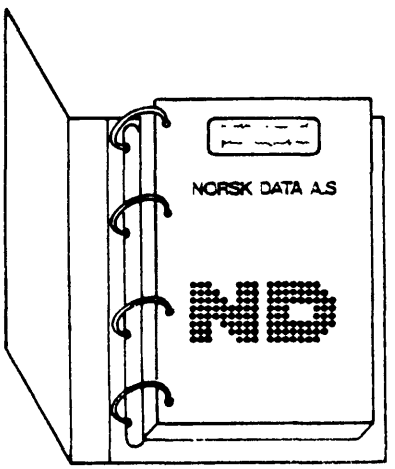

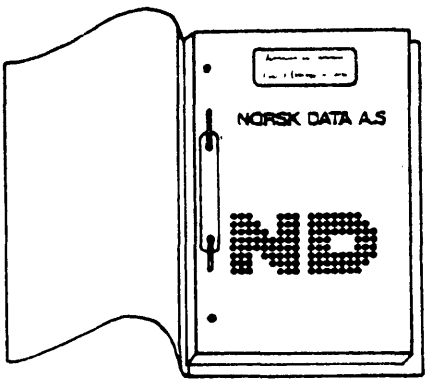

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Manual name: Floppy and Streamer Controller – 3106/3112 Manual number: ND-11.021.01

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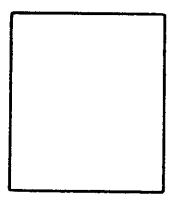

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