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SMD Disk Controller

ND-11.020.01

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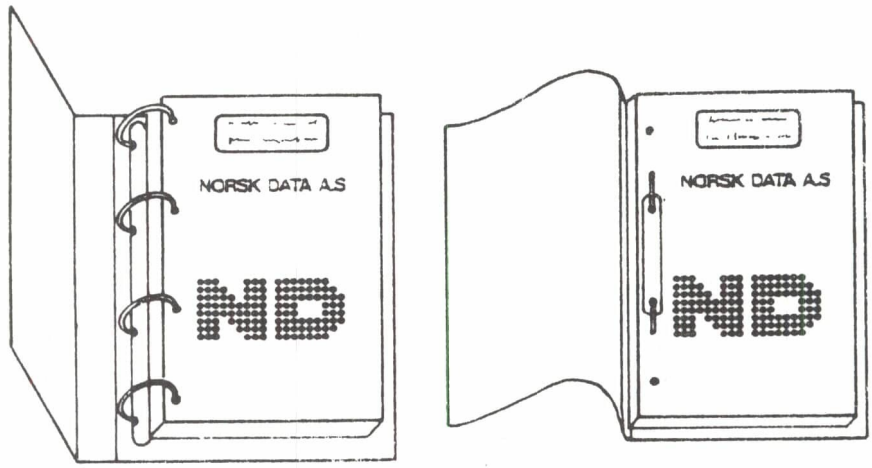

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Preface:

THE PRODUCT

The 15MHz SMD Disk Controller, ND-632, consists of two cards - 3043 and 3044. This new and faster Disk Controller takes care of the dialog between the controller and the disk drives connected to it.

THE READER

This manual is written for maintenance, workshop and other personnel who need a description of the SMD (Storage Module Drive) Controller.

PREREQUISITE KNOWLEDGE

Basic knowledge of the ND-100 computer and the ECC (Error Correction Control) Disk Controller is recommended.

THE MANUAL

The manual describes the SMD controller, provided in 8 chapters:

- 15MHZ SMD Disk Controller
- Programming Specifications
- Functional Description
- Troubleshooting
- Installation
- Connector List

It also contains logic diagrams and descriptive block diagrams, in the appendixes.

RELATED MANUALS

Test Program Description for ND-100, NORD-10/S, NORD-10 and NORD-12	ND-30.005

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15MHZ SMD DISK CONTROLLER

C H A P T E R 1

INTRODUCTION TO THE 15MHZ SMD DISK CONTROLLER

1 INTRODUCTION TO THE 15MHZ SMD DISK CONTROLLER

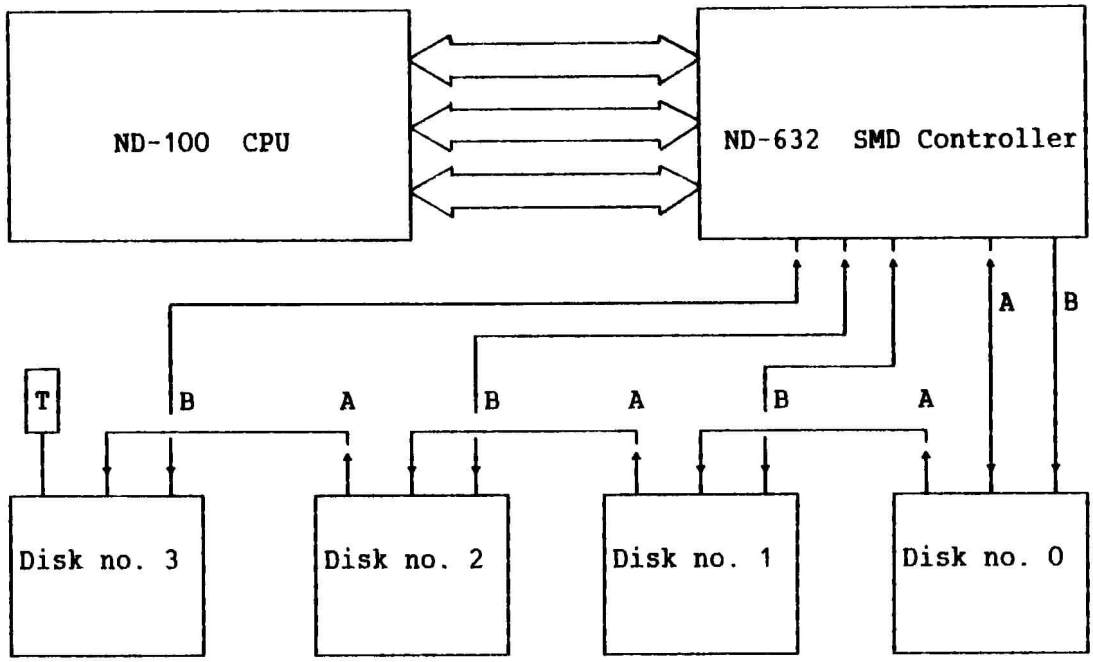
The 15MHz SMD Disk Controller (ND632) is designed to handle from one to four disks.

The controller can transfer data between any ND-100 memory address and any disk address. The maximum transfer rate between the disk drive and the controller is raised from 10 to 15 MHz, to handle new high capacity disk drives. Both 10 and 15 MHz disk drives may be daisy chained on the same controller (See figure 1). Because of this, the new controller should replace the old one in all future installations.

Any combination of the four units may be connected to the same controller. ECC (Error Correction Control) is standard. ECC implies, for this controller, that all error bursts of up to 11 bits are detected and corrected.

All error bursts of up to 34 bits are detected, but not corrected.

The controller converts the DMA data flow (data to/from memory) to a serial bit stream (to/from the selected unit). Read more about the DMA transfer in chapter 3.



A = A-cable
B = B-cable

Fig. 1. The Disk Drives are Daisy Chained on the Same Controller

CHAPTER 2

PROGRAMMING SPECIFICATIONS

2 PROGRAMMING SPECIFICATIONS

Card no. : 3043,3044
Standard device no. : 1540,1550
Standard ident. code : 17,20
Standard interrupt level: 11

The IOX address and IDENT code are 16 bits wide, and more controllers using IOXT may be added.

Both 10MHz and 15MHz drives may be daisy chained on this controller.

Switch setting on 3043 :

DIP switch (in position 7E) contains one switch for each of the four units. This switch must be in the OFF (open) position to be compatible with the old controller.

If the B-cables are flat cables all the way from the controller to the drives, the switches for those units must be in the ON position :

Unit 0 - Switch 1 (pin 1-8)
Unit 1 - Switch 2 (pin 2-7)
Unit 2 - Switch 3 (pin 3-6)
Unit 3 - Switch 4 (pin 4-5)

Switch setting on 3044 :

Thumbwheel switch 8 - Controller 1 (IOX 1540)
Thumbwheel switch 9 - Controller 2 (IOX 1550)

Which register the instructions shall activate is controlled by bit 15 in the Control Word Register (CWR) (Dev.No. + 5).

	CWR bit 15 = 0	/	CWR bit 15 = 1
DEV.NO. + 0 :	Read Memory Address	/	Read Word Count
DEV.NO. + 1 :	Load Memory Address	/	Count Memory Address & Word Count
DEV.NO. + 2 :	Read Seek Condition	/	Read ECC Count
DEV.NO. + 3 :	Load Block Address I	/	Load Block Address II
DEV.NO. + 4 :	Read Status Register	/	Read ECC Pattern
DEV.NO. + 5 :	Load Control Word	/	Load Control Word
DEV.NO. + 6 :	Read Block Address I	/	Read Block Address II
DEV.NO. + 7 :	Load Word Count	/	Load ECC Control

2.1 DEV.NO. + 0 : Read Memory Address (24 bits) / Read Word Count (24 bits)

The Memory Address Register is read by two successive IOX instructions. The first one gets the lower 16 bits (Address bits 0-15 into the A-reg. 0-15), and the second one gets the upper bits (Address bits 16-23 into A-reg. 0-7). When reading the most significant bits, the upper byte of the A-reg. is undefined and has to be masked.

The Word Count Register is read the same way as the memory address register.

After a transfer, the upper/lower memory address (or word count) control bit (flip-flop) is reset. A Read Status instruction (DEV.NO. + 4) or a Device Clear will also reset this bit.

2.2 DEV.NO. + 1 : Load Memory Address / Count Memory Address & Word Count

The Memory Address Register is loaded by two successive instructions. The first loads the 8 upper bits (A-reg. 0-7 into Address bits 16-23), and the second one loads the lower 16 bits (A-reg. 0-15 into Address bits 0-15).

After a transfer, the upper/lower memory address control bit (flip-flop) is reset. A Read Status instruction (DEV.NO. + 4) or a Device Clear will also reset this bit.

Count Memory Address & Word Count: This instruction is implemented for maintenance purposes only. By first loading the control word with 102010, a special test mode, each of these instructions will increment the memory address and decrement the word count by one. (Refer to section 3.1, the DMA transfer.)

2.3 DEV.NO. + 2: Read Seek Condition / Read ECC Count

Read Seek Condition:

BIT	MEANING
0	→ Seek Complete
1	
2	
3	
4	→ Not used
5	
6	
7	
8	Unit Select
9	Unit Select
10	Not used
11	Seek error
12	Always 1
13	ECC Correctable
14	ECC Parity Error
15	Address Field

Bits 0-3: Seek complete status for units 0-3. True if :

- the unit has moved the heads to the correct cylinder, and the heads are under the sector number specified by the block address loaded prior to the initiate seek command.

- a seek error has occurred.

The seek complete status will only be set if an initiate seek command for that unit has first been issued. Note that the sector address loaded before the initiate seek command should be at least two sectors prior to the sector to be read or written.

Thus, after an initiate seek command is given, the Seek Complete bit for that unit will appear once per revolution after the unit is positioned on the correct cylinder, or a seek error has occurred. The condition will last until a transfer command is given.

Bits 8-9: The unit number as loaded by the last control word.

Bit 11 : Seek error for the selected unit. This signal indicates that :

- The unit was unable to complete a move within 500 ms.
- The heads have moved to a position outside the recording field.
- An address greater than the maximum number of tracks has been issued.

The signal will only be cleared by performing a Return to Zero command on the unit. Pushing the Master Clear button on the operators panel will also perform a Return to Zero command.

Bit 12 : This bit was always 0 on the NORD-10 controller.

Bit 13 : After the hardware ECC operation has been performed (M8) (after a data error), this bit signals that the error is correctable; and that the ECC Count and ECC Patterns Registers contain valid information for correction of the data. The bit is reset by Device Clear.

Bit 14 : This bit signals that a hardware fault condition exists in the ECC polynomials. This condition will also set bit 7 of the Status Word register (Hardware Error), and hence trigger an error interrupt if this is enabled. The error is reset by the Reset ECC signal (ECC Control register bit 0) or by Device Clear (CWR bit 4). The error is forced set when ECC Control register bit 1 is active. (Force Parity Error).

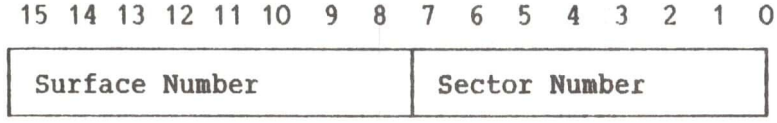
Bit 15 : This bit indicates that the error (status bit 9) was in the address field of a sector. This bit is only cleared by Reset ECC (ECC control register bit 0).

Read ECC Count: When a correctable data error has been detected, this register will contain the bit displacement + 2 from the beginning of the data field to the last bit of the error burst. It means that if the last error bit is bit no. n (starting at 0), the ECC count will be n+2.

2.4 DEV.NO. + 3: Load Block Address I/II

Both block address registers have to be loaded to completely specify a disk address.

Block Address Register I:

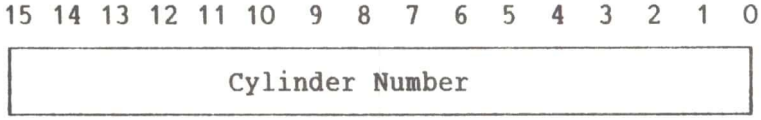


Bits 0-7: Sector number
10 MHz drives have 18 sectors (0-21 oct.).
15 MHz drives, examples:
CDC 515 Mb FSD -- 26 sectors (0-31 oct.) + 1 spare
CDC 825 Mb XMD -- 44 sectors (0-53 oct.) + 1 spare
FUJITSU 474 Mb M2351A (EAGLE)
-- 24 sectors (0-27 oct.) + 1 spare

Bits 8-15: Surface number
10 MHz drives, examples:
for 38/75 Mb disk -- 5 (0-4)
for 150 Mb disk -- 10 (0-11 oct.)
for 288 Mb disk -- 19 (0-22 oct.)
for Phoenix disk -- 1-5 (20-24 oct.) fixed
-- 1 (0) removable

15 MHz drives,examples:
CDC 515 Mb FSD -- 24 (0-27 oct.)
CDC 825 Mb XMD -- 16 (0-17 oct.)
FUJITSU 474 Mb M2351A (EAGLE) -- 20 (0-23 oct.)

Block Address Register II:



Bits 0-15: Cylinder number
- for 38 Mbytes disk: 411 max.(0- 632 oct.)
- for 75/150/288 Mbytes/Phoenix disk: 823 max.(0-1466 oct.)
- for CDC 515 Mb FSD : 711 max.(0-1306 oct.)
- for CDC 825 Mb XMD :1024 max.(0-1777 oct.)
- for FUJITSU 474 Mb M2351A (EAGLE) : 842 max.(0-1511 oct.)

2.5 DEV.NO. + 4: Read Status Register/Read ECC Pattern

Read Status Register:

BIT	MEANING
0	Controller not active, interrupt enabled
1	Error interrupt enabled
2	Controller active
3	Controller finished with a device operation
4	Inclusive OR of errors (bits 5-13)
5	Illegal load
6	Timeout
7	Hardware error
8	Address mismatch
9	Data error
10	Compare error
11	DMA channel error
12	Abnormal completion
13	Disk unit not ready
14	On cylinder
15	Always 0. Read back of Control Word bit 15

Bit 5: Load of any register while status bit 2 is true.

Bit 7: Disk fault, missing read clocks, missing servoclocks, ECC parity error.

Bit 11: FIFO over/underrun or ND-100 Bus error.

Bit 13: Inclusive OR of bits 5, 6, 7, 8 and 13.

Bit 15: Used to distinguish the two IOX banks.

Read ECC Pattern Register:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	Error pattern										

Bits 0-10 Error pattern.
11-13 Always 1.
14 Always 0. To distinguish from the old ND-100 SMD controller.

15 Always 1. Read-back of Control Word bit 15.

Bits 0-10: These bits contain the right-justified error pattern, such that the last bit in error always occupies bit position 0 of this register. This pattern (the contents of this register bits 0-10) should be exclusively ORed with the data in the CPU memory at the proper location.

2.6 DEV.NO. + 5: Load Control Word

BIT	MEANING
0	Enable interrupt on device not active
1	Enable interrupt of errors
2	Activate device operation
3	Test mode
4	Device clear
5	Not used
6	Not used
7	Unit select
8	Unit select
9	Not used
10	Marginal recovery cycle
11	┐
12	│
13	├→ Device operation code
14	│
15	┘ Register multiplex bit

Bits 7-8: When a Control Word is loaded, the disk unit number (0-3) has to be set up in bits 7-8.

Bit 10: The marginal recovery cycle may be used in connection with read operation codes M0, M2 and M3, as defined under bits 11-14. This control bit is included as an aid in recovering marginal data.

If a marginal recovery cycle is started, this bit has to be set every time this instruction (Load Control Word) is given. Otherwise the marginal recovery cycle will be interrupted, and it will start in position 1 again the next time this bit is set in the Control Word.

For consecutive read transfers with this bit set, the controller will cycle through the following conditions :

1) Servo-offset positive, data strobe early.

2) No servo-offset, data strobe early.

3) Servo-offset negative, data strobe early.

4) Servo-offset positive, nominal data strobe.

5) Servo-offset negative, nominal data strobe.

6) Servo-offset positive, data strobe late.

7) No servo-offset, data strobe late.

8) Servo-offset negative, data strobe late.

9) Servo-offset positive, data strobe early.

Bits11-14: Device operation code: All device operation codes will be activated when the code is given together with bit 2 (activate device). For all codes except M6, the correct unit number must also be selected.

Bit 14	13	12	11		
0	0	0	0	M0	Read transfer
0	0	0	1	M1	Write transfer
0	0	1	0	M2	Read parity
0	0	1	1	M3	Compare
0	1	0	0	M4	Initiate seek
0	1	0	1	M5	Write format
0	1	1	0	M6	Seek complete search
0	1	1	1	M7	Return to zero seek
1	0	0	0	M8	Run ECC operation
1	0	0	1	M9	Select/Release

M0: Read transfer
This operation causes the controller to transfer data from the disk to the computer memory. The number of blocks transferred depends upon the word count, as defined by the Word Count Register.

M1: Write transfer
Data is transferred from the computer memory to the disk.

M2: Read parity transfer
The controller will check the parity on the address and data of the sector specified. Data is transferred to the controller and the cyclic check word, for both the address field and the data field of a sector, is compared with the correct check word as generated by the controller. No data transfer to the computer memory is performed.

M3: Compare transfer
This function is included to positively check the data written on the disk. During compare transfer, the controller compares the data read from the disk and the data from the computer memory bit by bit. A mismatch causes compare error to be set.

M4: Initiate seek
This function is included to enable a unit to position the heads prior to a data transfer. The heads will be positioned according to the content of the Block Address Register. The sector address must be at least two sectors prior to the one to be read or written. As soon as this function is accepted by the disk, the operation will be completed.

M5: Write format
This function will cause the controller to write the address field within each sector. (See section 2.8)

M6: Seek complete search
This function will enable the controller to go into a waiting state, until any unit has completed a seek. This function is independent of the unit select code in the control word. Note that interrupt will be given when the heads of a unit are positioned at the beginning of the specified sector, and that this should be (at least) two sectors prior to the first of the sectors to be read or written.

M7: Return to zero seek
This will cause the selected disk to perform a seek to cylinder 0, and will also clear the seek error bit in the unit.

M8: Run ECC operation
This function will, when a data error has occurred, initiate the hardware operation that determines if the error is correctable or uncorrectable. If the error is correctable, the error pattern and its displacement within the data field are computed.

M9: Select/Release
This is implemented for dual channel drives only. All normal Load Control Word instructions from one channel will select the specified unit, until a Release command is issued. Attempts to select a reserved drive will only cause a delay in access time. A Priority Select command will unconditionally select, and absolutely reserve, the specified unit (interrupts the other channel during a transfer) until a Release command is issued. Attempting to select a priority selected drive will cause a astatus error (unit not ready)

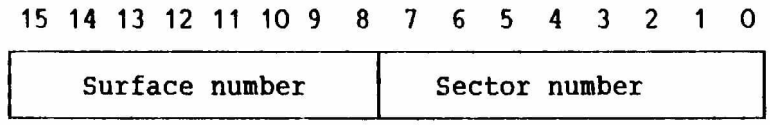
```
Release          : LDA (44020
                   IOX LCW
                   LDA (2010
                   IOX LCW

Priority select: LDA (44010 + Unit no.
                 IOX LCW
```

Bit 15 : This bit selects which register block on the controller the following IOX instructions shall activate.

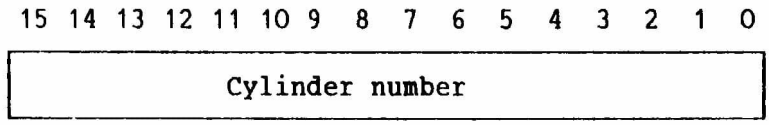
2.7 DEV.NO. + 6: Read Block Address I/II

Note that these registers will always show the last transferred sector address. If any error occurs during the transfer, the controller will stop, and the Block Address Register will show in which sector the error occurred. All the previous sectors are then transferred successfully; and, in the case of a data error (status bit 9), the whole failing sector will also be transferred. This means that an ECC operation or retry may be started immediately on this address.

Block Address Register I:



Block Address Register II:



2.8 DEV.NO. + 7: Load Word Count/Load ECC Control

Load Word Count: The Word Count register is increased from 16 to 24 bits, and is loaded by two successive instructions. The first loads the 8 upper bits (A-reg. 0-7 into Word Count bits 16-32), and the second one loads the lower 16 bits (A-reg. 0-15 into Word Count bits 0-15).

After a transfer, the upper/lower Word Count control bit (flip-flop) is reset. A Read Status instruction (DEV.NO. + 4) or a Device Clear will also reset this bit.

The controller is able to transfer a whole cylinder, or up to 16M words (24 bits), with a hardware increment of the head and sector addresses. For the 75 Mb disk, the maximum word count is 132000 (45k); starting with the head and cylinder address equal to 0.

The Word Count is set to an integer multiple of the number of words in a sector when device operation is M0-M3.

When executing M5 (Write Format), the interface is set in a special mode, and the Word Count is set to twice the number of sectors to be formatted. This special mode causes the data from memory to be written into the address part of the sector, instead of the data part. Data may also be written in the data fields during formatting by selecting a special format (see ECC control register).

Load ECC Control:

BIT	MEANING
0	Reset ECC
1	Force Parity Error
2	Long
3	Format A
4	Format B
5	Format C
6	Format D
7	
8	
9	
10	
11	→ Not used
12	
13	
14	
15	

Bit 0 : This bit will cause the ECC polynomials to be reset to the zero initial state. This function is only used when a data error has occurred, otherwise the polynomials automatically go to the zero state upon completion of a Read or Write. Device Clear function will also reset ECC and is preferred.

Bit 1 : Used for maintenance purposes only. This bit will force ECC parity error to be set.

Bit 2 : Used for maintenance purposes only. When a sector is read or written, the data field of the sector is extended by 64 bits (The length of the ECC pattern plus "End of Record" byte). The data and the extra bits are read into or written from the memory of the CPU. This function is used to diagnose the operation of the ECC circuits, and can be used with the following Device operations: M0, M1, M2, M3.

This bit is "echoed" in ECR bit 14.

Bits 3-6: Sector formats and sector length:

Format	A	B	Function:
	0	0	Old format, 1kb/sector, only the first address checked.
	1	0	Old format, 1kb/sector, all address fields checked.

0	1	New format, 1kb/sector, all address fields checked.
1	1	New format, 0.5kb/sector, all address fields checked.

Format 0 is identical to the old controller.
Format 2 should be selected when sector reallocation is used.

Note that it is not allowed to switch the format after formatting.

Format C: Used to write both the address and data during formatting, for faster track testing. Word count must then be two more than the number of data words multiplied by the number of sectors on a track. The memory layout must include the two address words between each sector data buffer.

Format D: Used to read the manufacturer's error information located at the beginning of each track. The word count must be 512 (1000 oct.), and the sector address is 0. Format A, B and C bits are not used (don't care). Only the first four defects on each track are logged. The memory content after transfer will be:

Memory
address + 0/ Cylinder number, bit 15 also tells if the track contains more than one error.
1/ Head number in upper 8 bits, lower 8 are zero.
2/ First defect position, in bytes from Index.
3/ First defect length, in bits.
4/ Second defect position.
5/ Third defect length.
6/ Third defect position.
7/ Third defect length.
10/ Fourth defect position.
11/ Fourth defect length.
12/ End of information, 170000 octal.
13-777/ Don't care.

Unused defect locations are all zeros. If the cylinder address, head address or end of information word do not match, the whole track should be considered defective and be real located. Note that status bit 9 (data error) may be set after this transfer.

This table shows the Format bits influence on the length (in bits) of the 8 phases that every sector is divided into:

Form.bit LongABCD	Phase1 length	Phase1 to RG	Phase1 to RCE	Phase2 length	Phase4 length	Phase4 to WG	Phase4 to RG	Phase4 to RCE	Phase5 length	Phase6 length
0 00X0	240	65	193	32	240	32	65	193	8192	56
1 00X0	240	65	193	32	240	32	65	193	8256	8
0 10X0	240	65	193	32	240	32	65	193	8192	56
1 10X0	240	65	193	32	240	32	65	193	8256	8
0 01X0	416	273	361	32	128	32	41	113	8192	56
1 01X0	416	273	361	32	128	32	41	113	8256	8
0 11X0	416	273	361	32	128	32	41	113	4096	56
1 11X0	416	273	361	32	128	32	41	113	4160	8
X XXX1	240	65	193	8192	240	--	--	--	8	56

Phase 3 is always 56 bits. Phase 7 is always 8 bits. Phase 8 is disk drive dependent. RG (Read Gate) and RCE (Read Clock Enable) are turned off at the beginning of Phase 4 and Phase 8. WG (Write Gate) is turned off at the end of Phase 8.

C H A P T E R 3

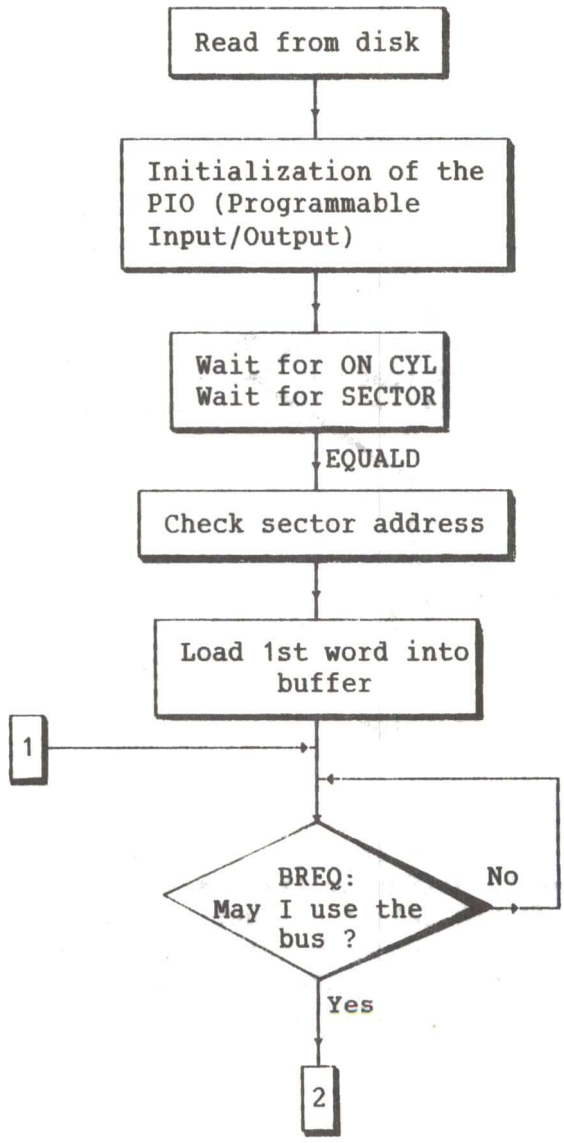
FUNCTIONAL DESCRIPTION

3 FUNCTIONAL DESCRIPTION

3.1 The DMA Transfer

The DMA transfer is divided into 3 parts (see figure 2):

1. Initialization
2. Transfer
3. Termination



Other users are:
- Refresh (first priority)
- CPU
- DMA (equal priority)

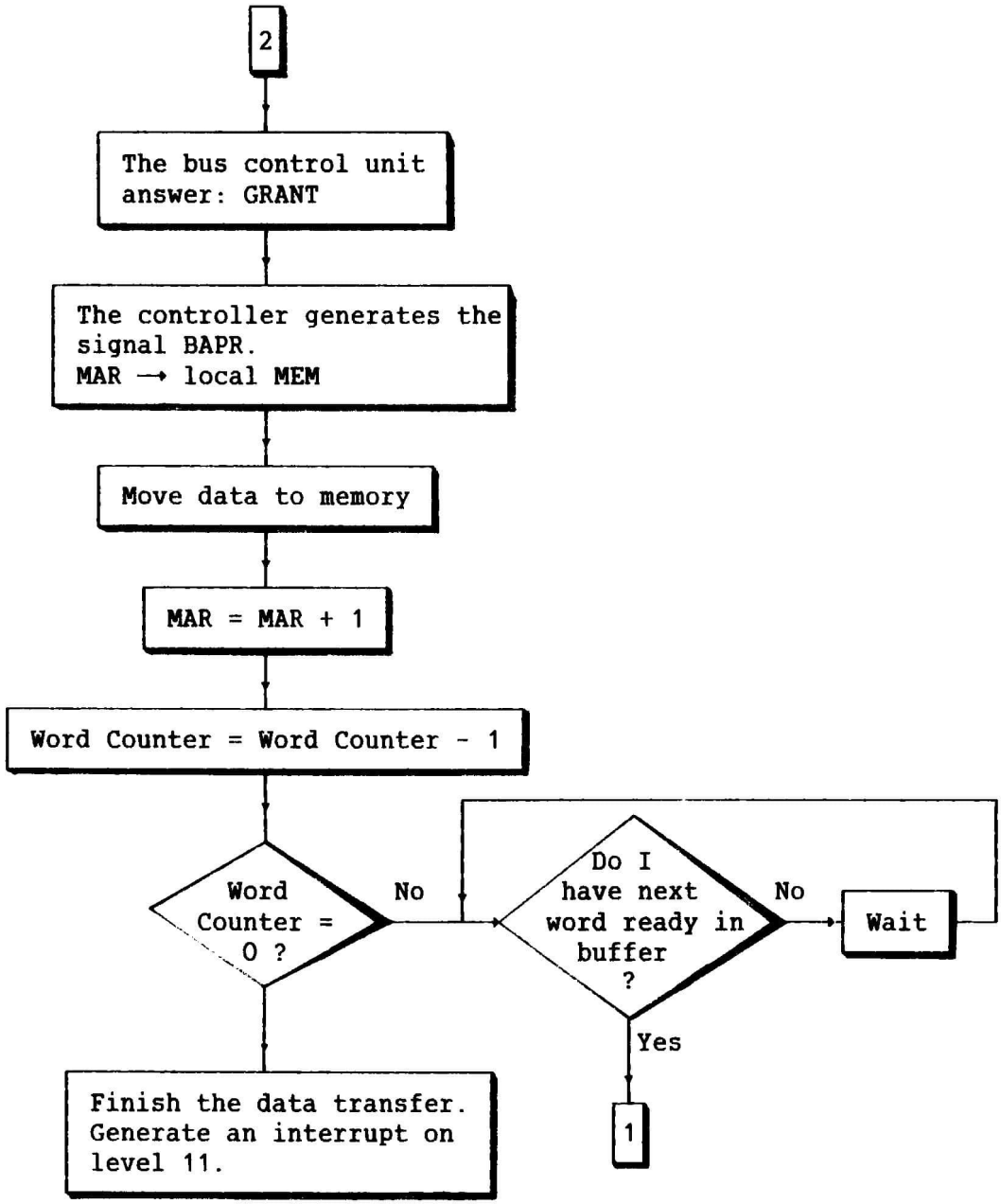


Fig. 2. The DMA Operation

An 8Kb FIFO (First In First Out temporary storage) acts as a buffer between the memory and the disk, due to different transfer rates. It is possible, in odd configurations, to select a lower transfer rate between the FIFO and the main memory, dependent on the quantity of the FIFO. This must be done by straps on the card. Data flow for write and read is illustrated in Figures 6 and 7 respectively.

3.2 The Interface Signals

In this section, the signals between the disk unit and the controller are listed and explained. The signals are transferred over two cables, the A- and B-cables.

In order to exchange signals between the controller and a disk unit over the A-cable, the unit must be selected.

On the B-cable, however, the signal exchange takes place without disk unit selection.

Figures 3 and 4 list the interface signals on the A- and B-cables.

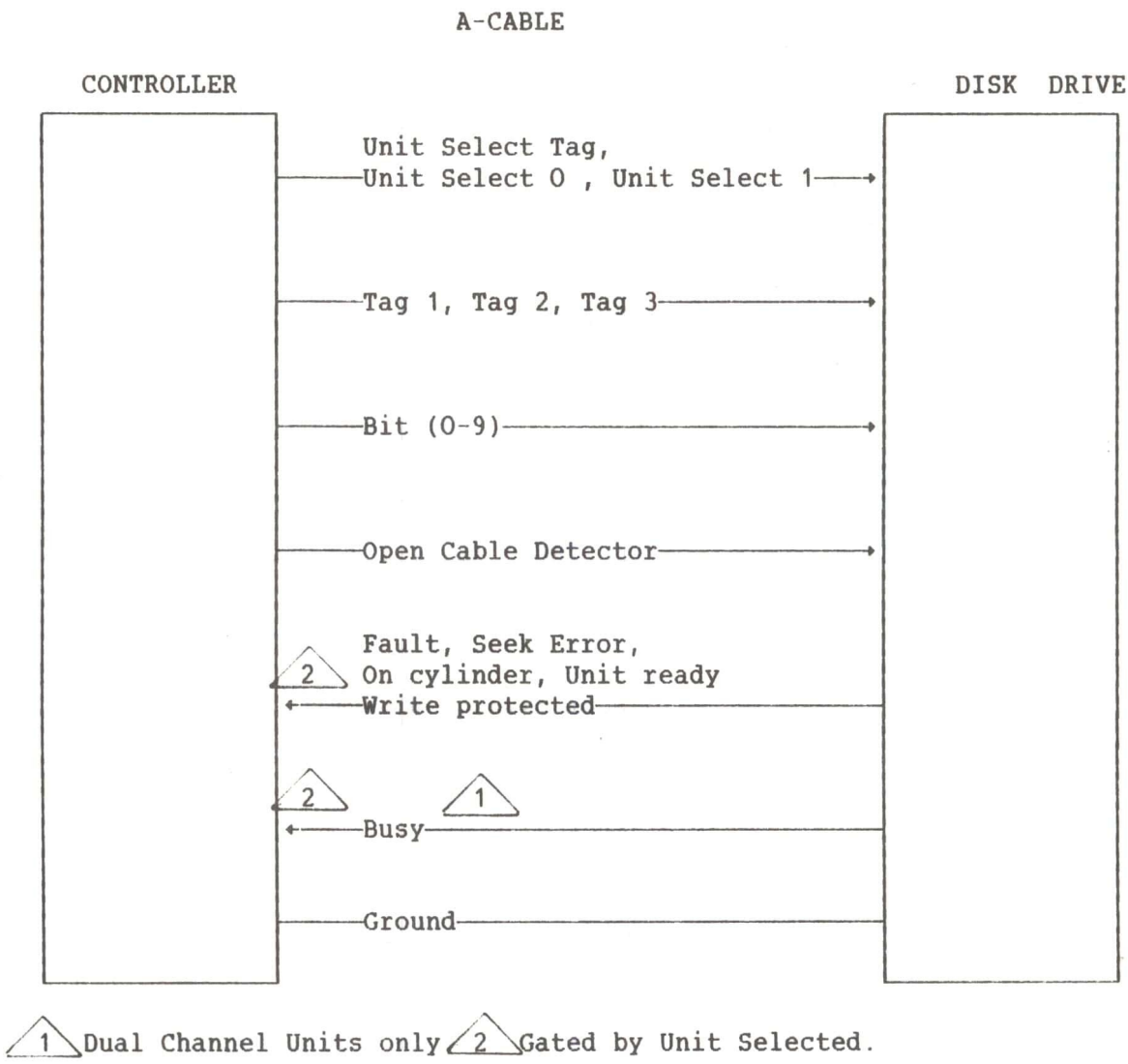


Fig. 3. Interface Lines - A-cable

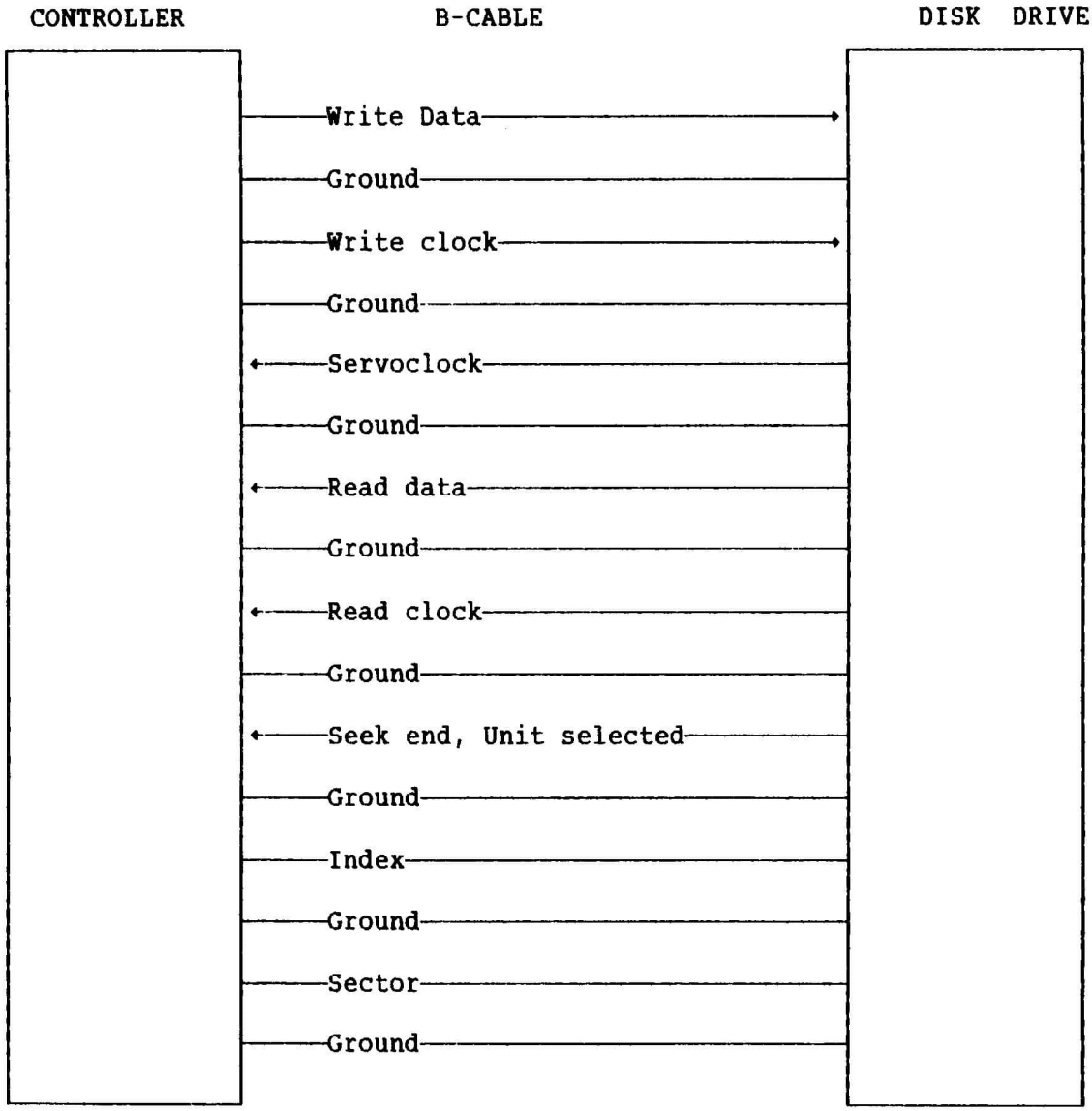


Fig. 4. Interface Lines - B-cable

3.2.1 Signal Explanation

This section is divided into 3 parts :

- bus bit usage
- the remaining A-cable lines
- the B-cable lines

3.2.1.1 Bus Bit Usage

The bus bits 0-9 are used for 3 purposes defined by the tag 1, tag 2 or tag 3 line.

Tag 1 line activated — The cylinder address, taken from the lower part of block address register II, is transferred over the bus bits and strobed into the cylinder address register in the selected unit.

Tag 2 line activated — The head select bits, taken from the upper byte of block address register I, are transferred over the bus bits and strobed into the head select register in the selected unit.

Tag 3 line activated — The various functions given in the table below are sent from the controller to the selected disk unit :

Bus bits:	Function :
0	Write Gate. Enable write drivers.
1	Read Gate. Enable the read circuits and data/clock separator circuits in the drive.
2	Servo-Offset Plus. Offsets the actuator (heads) from the center of a track position towards the spindle.
3	Servo-Offset Minus. Offsets the actuator (heads) from the center of a track position away from the spindle.
4	Fault Clear. Pulse sent to the drive to clear the fault summary latch.

:

5	Address Mark Enable (not used).
6	Return to Zero Seek (RTZ). Pulse sent to the drive, causing the actuator to seek back to track zero.
7	Data Strobe Early. Enables the data/clock separator (phased locked oscillator - PLO) to strobe the data at a time earlier than the optimum.
8	Data Strobe Late. Enable the data/clock separator (phased locked oscillator - PLO) to strobe the data at a time later than the optimum.

3.2.1.2 The Remaining A-Cable Lines

Open Cable Detect	Inhibits unit selection and any unwanted command, such as Write Gate, when the A-cable is disconnected or controller power is lost.
Unit Select Lines 2^0 - 2^3	Used to select the drive. The binary code on these lines must match the code of the drive's logical address plug, for the drive to be selected. These lines are used in conjunction with the unit select tag (refer to Unit Selection).
Unit Select Tag	Starts unit select sequence and is used in conjunction with Unit Select lines 2^0 - 2^3.
Fault	Indicates that one or more of these faults exist : - DC power fault - Head select fault - Write fault - Write or read while off cylinder - Write during a read operation Refer to Fault and Error Correction.

Seek Error	Indicates that the unit was unable to complete a move within 500 ms, or that the carriage has moved to a position outside the recording field. A seek error interrupt also occurs if an address greater than the maximum track is selected. Refer to Seek Functions for more information.
On Cylinder	Indicates that the drive has positioned the heads over a legal track (refer to Seek Functions).
Unit Ready	Indicates that the drive is : - selected - up to speed - heads are loaded - no fault exists
Write Protected	Gives status bit 13 if trying to write on a write protected disk.
Busy	Used for dual channel drives to inform the other channel that the unit is busy.

3.2.1.3 The B-Cable Lines

Write Data	Carries NRZ (Non Return to Zero) data to be recorded on the disk pack.
Write Clock	Synchronized to NRZ Write Data, it is a return of the servoclock. This signal is transmitted continuously.
Servoclock	9.677 MHz clock signals derived from the servotrack dibits.
Read Data	Carries NRZ data recovered from the disk pack (refer to discussions on Read/Write functions).
Read Clock	Clock signals derived from NRZ read data (refer to discussions on Read/Write functions).
Seek End	Seek End, which is a combination of ONCYL and/or SEEK ERROR, indicates that a seek operation has terminated.
Unit Selected	Indicates that the drive is selected. This line must be active before the drive can respond to any commands from the controller.
Index	Occurs once per revolution of the disk pack. Its leading edge is considered the leading edge of sector zero.
Sector	Derived from the servosurface of the disk pack. This signal can occur any number of times per revolution of the disk pack. The number of sector pulses occurring depends on the setting of the switches on the card in position in the logic chassis. Refer to chapter 7 for Switch Setting.

3.2.2 ND-100 Bus Signals

An Return	Separate ground line for analog circuits. Connected to logic ground return (GND) in power supply end. (15V Power Supply.)
BAPR	Bus Address Present in multiplexed data and address bus. Wired OR line.
BCRQ	Bus Control Request from source wanting full control over the bus (for future extensions). Wired OR line.
BDRY	Bus Data Ready signals that data is ready or has been accepted: given by the answering device. Wired OR line.
BD 0-23	Multiplexed data and address bus. Bit 0 is the least significant.
BERROR	Bus Error signals that an error was detected during a bus cycle, e.g., fatal memory error. Wired OR line.
BINACK	Bus Input Acknowledge signals that an interface requesting an input operation may enable data. Generated by the controlling unit.
BINPUT	Bus Input signalled by a unit which will transmit data. I/O interfaces must wait for BINACK before enabling data and BDRY. Wired OR line.
BINT 10-13,15	Interrupt lines. BINT10 has the lowest priority. Wired OR lines.
BDAP	Bus Data Present signals that data is present during DMA or memory cycles.
BIOXE	Input/Output Enable. A strobe to enable data transfer to or from an I/O interface. Generated by the controlling unit.
BLANK	Output Blanking signal for process interface. Wired OR signal generated by the monitoring device.
BMCL	Bus Master Clear for logic initialization at power-up, and when Master Clear button is pushed. Wired OR line.

BMEM	Bus Memory Cycle signals that a bus cycle accesses memory. Generated by the controlling unit.
BMINH	Bus Memory Inhibit used to inhibit memory accesses during power-down and power-up sequences in systems which only have battery backup for memory. Generated by the controlling unit.
BREQ	Request for a DMA cycle. Wired OR line.
CONTINUE	May be used to start a CPU that is in STOP mode. Wired OR line (only in CPU crate).
GND	Logical ground return.
INCONTR	Response to BCRQ indicating that a control over the bus is available. A unit which does not want to control the bus must issue OUTCONTR in response to INCONTR. INCONTR is generated as OUTCONTR by the nearest unit in a less significant board position.
INGRANT	Response to BREQ, indicating that the bus is available for DMA cycle. The interface which issued BREQ prior to the last leading edge of BMEM may use the bus for a single memory read or write cycle. Otherwise, INGRANT is passed onto OUTGRANT, which is connected to INGRANT of the next lower priority card position (further removed from the controlling unit). INGRANT, as OUTGRANT, originates from the controlling unit.
INIDENT	Response to BINT 10-13, together with address bits 0-5 which specify BINT number. The interface that issued BINT in the specified level prior to the last leading edge of BAPR, responds by enabling its IDENT CODE into the BD bus. Otherwise, IDENT is passed on to OUTIDENT, which is connected to INIDENT of the next lower priority card position (further removed from controlling unit). INIDENT originates in the OUTIDENT from the controlling unit.
PA 0-3	Define the card position code and the device numbers of the analog and digital process interfaces.
LOAD	Activates the load microprogram if the CPU is in STOP mode. Wired OR line (only in CPU crate).

OUTCONTR	See INCONTR.
OUTGRANT	See INGRANT.
OUTIDENT	See INIDENT.
RESTART	Starts program execution in location 20_8 if the CPU is in STOP mode. Wired OR line (only in CPU crate).
RUN	Indicates that the CPU is active and executing a program, i.e., not in STOP mode. Generated by the CPU (only in CPU crate).
SPARE	Not assigned.
STOP	Forces the CPU to enter STOP mode after completion of the current instruction. Wired OR line (only in CPU crate).
+ 5V	Main logic supply voltage.
+ 5V Standby	Logic supply voltage for memory retention during power fail.
+ 15V	Supply voltage for analog interface circuits. For customer use.
- 15V	Supply voltage for analog interface circuits. For customer use.
+ 12V Standby	Supply voltage for memory. Requires battery backup.

3.3 Track/Sector Format

A new track format is included, which allows the address field of each sector in a multisector transfer to be checked. Therefore, "head advance" may be used on disk drives with reallocated tracks.

This also makes it possible to have a spare sector on each track, which will give no additional seek or rotational time delays if a reallocated sector is found. The controller will just skip the bad sector and read the next one(s). The bad sector may be anywhere on the track, and the software driver will not see this at all. It only affects the formatting program. The capacity loss, compared to track reallocation, is typically only 5 Mb for 4-500 Mb drives, due to the much smaller spare track pool, which is now only for tracks containing more than one bad sector.

Half sector lengths are included, which gives sector sizes of 0.5 and 1 Kb. This is done mainly to handle disk drives with fixed sector sizes due to the embedded servo.

3.3.1 The Phases

This table shows the Format bits' influence on the length (in bits) of the 8 phases that every sector is divided into :

Form.bit LongABCD	Ph. 1 length	Phase1 to RG	Phase1 to RCE	Phase2 length	Phase4 length	Phase4 to WG	Phase4 to RG	Phase4 to RCE	Phase5 length	Phase6 length
0 00X0	240	65	193	32	240	32	65	193	8192	56
1 00X0	240	65	193	32	240	32	65	193	8256	8
0 10X0	240	65	193	32	240	32	65	193	8192	56
1 10X0	240	65	193	32	240	32	65	193	8256	8
0 01X0	416	273	361	32	128	32	41	113	8192	56
1 01X0	416	273	361	32	128	32	41	113	8256	8
0 11X0	416	273	361	32	128	32	41	113	4096	56
1 11X0	416	273	361	32	128	32	41	113	4160	8
X XXX1	240	65	193	8192	240	--	--	--	8	56

Phase 3 is always 56 bits.
Phase 7 is always 8 bits.
Phase 8 is disk drive dependent.
RG (Read Gate) and RCE (Read Clock Enable) is turned off at beginning of Phase 4 and Phase 8. WG (Write Gate) is turned off at end of Phase 8.

A sector is divided into 8 phases.

Phase 1 The purpose of this phase is :

- to compensate for sidewise mechanical skew between the read/write heads with respect to the servohead.
- to compensate for read circuits set up time.
- to allow the data/clock separation circuits phase lock oscillator to synchronize and lock to the address.

This phase is written during the formatting process.

Phase 2 — During formatting, the block address is written onto the disk pack. During read or write, the block address is checked.

Phase 3 — The block address, written onto the disk in phase 2 during formatting, at the same time generates a 56-bit error correction code (ECC - see section 3.3) which is written onto the disk in phase 3 during formatting.

Phase 4 — This phase is identical to phase 1. The purpose is to resynchronize the phase lock oscillator in the data/clock separation circuits.

Phase 4 is first written during the formatting process, but is rewritten for each normal write operation on the sector in question.

Phase 5 — Phase 5 represents the data capacity for the sector, and is equal to 512 16-bit words (1/2 K words). This data is taken from memory over a DMA channel during a write operation, and vice versa during a read operation. It is also possible to write data in the data fields of the sector during formatting - this makes track testing faster.

Phase 6 — When the data is written onto the disk in phase 5, an error correction code (ECC) is generated. The code will then be written onto the disk in phase 6.

Phase 7 — This phase consist of 8 1's, indicating the end of the sector.

Phase 8 — This phase consists of 0's, and its purpose is to compensate for sidewise mechanical skew between the read/write heads with respect to the servohead.

3.3.2 The Clock Counter

The clock counter works as an input to the phase generator, which in turn resets the clock counter when terminating each phase.

The clock pulses, which are counted, derive either from the write clock, read clock, or an internal clock oscillator used in test mode.

The circuits which perform the clock selection are located on the SMD Control (3043).

3.3.3 The Sector Counter

The sector counter in block address register I always shows the last transferred sector in the read back disk address.

The local sector counter for each unit is increased from 5 to 7 bits (max. 128 sectors). These counters are only used for a parallel seek of several units to include rotational optimization.

3.4 Error Correction Code Description

3.4.1 Features of the ECC Polynomial

Errors that occur to the data on the disk show up as error bursts. The burst-error processor is a hardware implementation of these codes. It can correct error bursts up to 11 bits long in a data stream being read from a disk. It does so by dividing the data stream by a fixed binary number, represented mathematically by a polynomial :

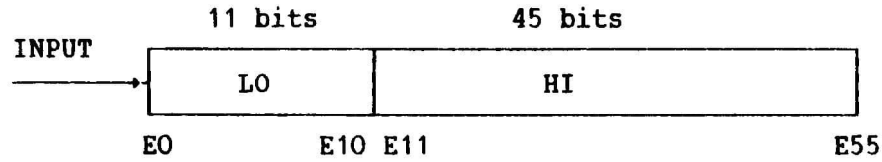
EXAMPLE :

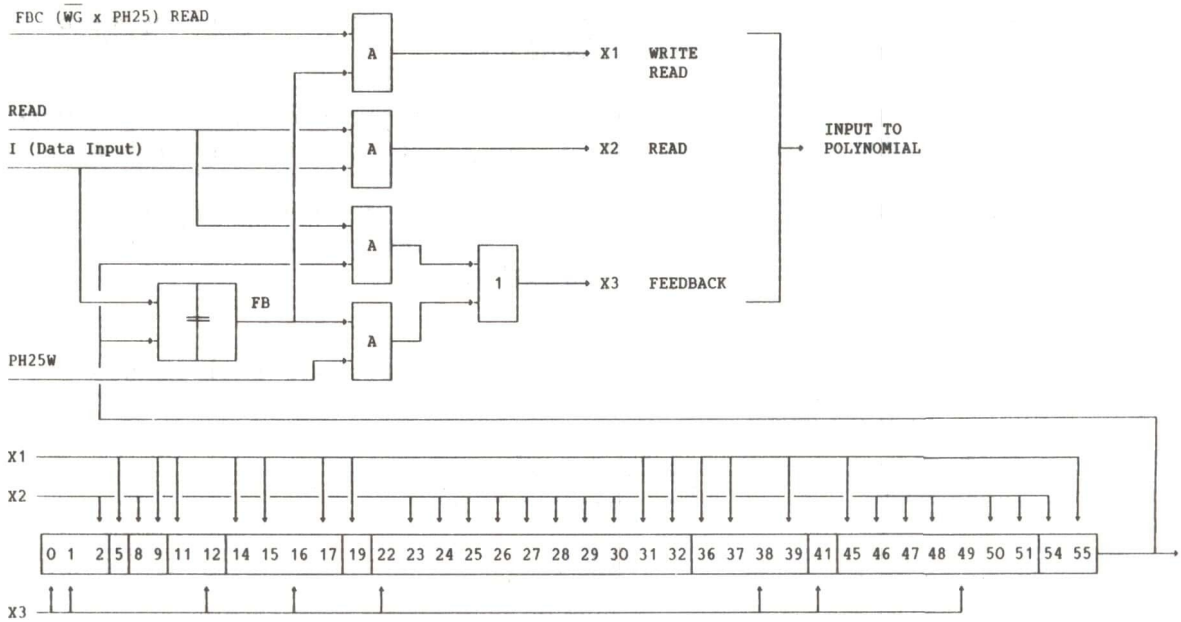
$X^0 + X^2 + X^5 + X^7$ stands for a binary 10100101 since each exponent indicates the position of a 1.

The polynomial is generated in a 56-bit special purpose shift register according to the formula :

$$G(X) = X^{56} + X^{55} + X^{49} + X^{45} + X^{41} + X^{39} + X^{38} + X^{37} + X^{36} + X^{31} + X^{22} + X^{19} + X^{17} + X^{16} + X^{15} + X^{14} + X^{12} + X^{11} + X^9 + X^5 + X + 1$$

The ECC polynomial is logically divided into two parts, one LO and one HI portion.





Write : Inputs X1 and X3 are open.
Data is excl. Ored with feedback, and fed into the network through inputs X1 and X3.

Read : All inputs are open.
Data is fed directly through input X2, feedback directly through X3, and data is excl. Ored with feedback in X1.

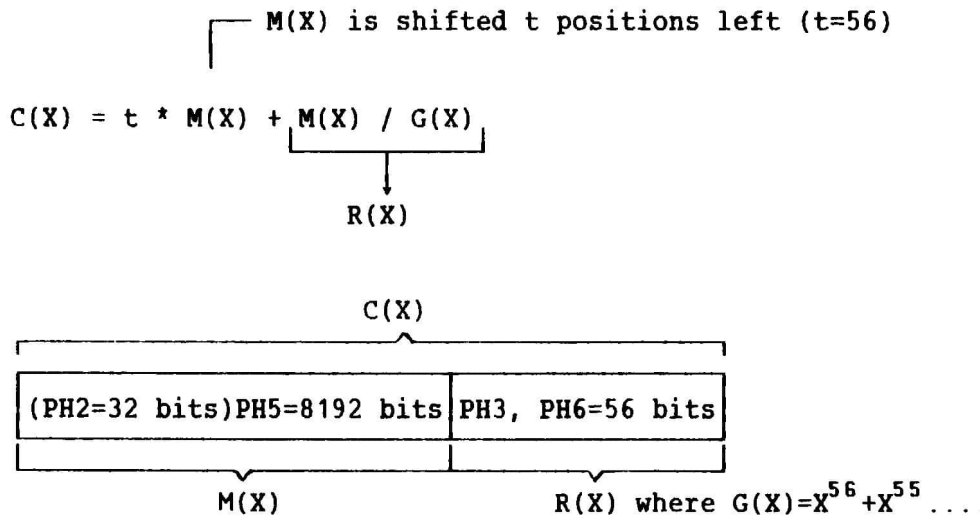
Fig. 5. ECC Polynomials

3.4.2 General Information About ECC

3.4.2.1 Write Data

Memory Data M(X) is serially written onto the disk as it is simultaneously divided with the polynom G(X). This happens by means of a shift register with different feedbacks.

After data is written onto the disk, the rest of the division, which is in the shift register, will be written onto the disk without feedbacks and input. Together this will make "the codeword" - C(X). A look at the code word (=8248 bits) shows that data written first (MSB) will be multiplied (=binary shifted) to the length of the shift register (=the rest) = 56 bits. Like this :



The result of the division is not used, only the rest.

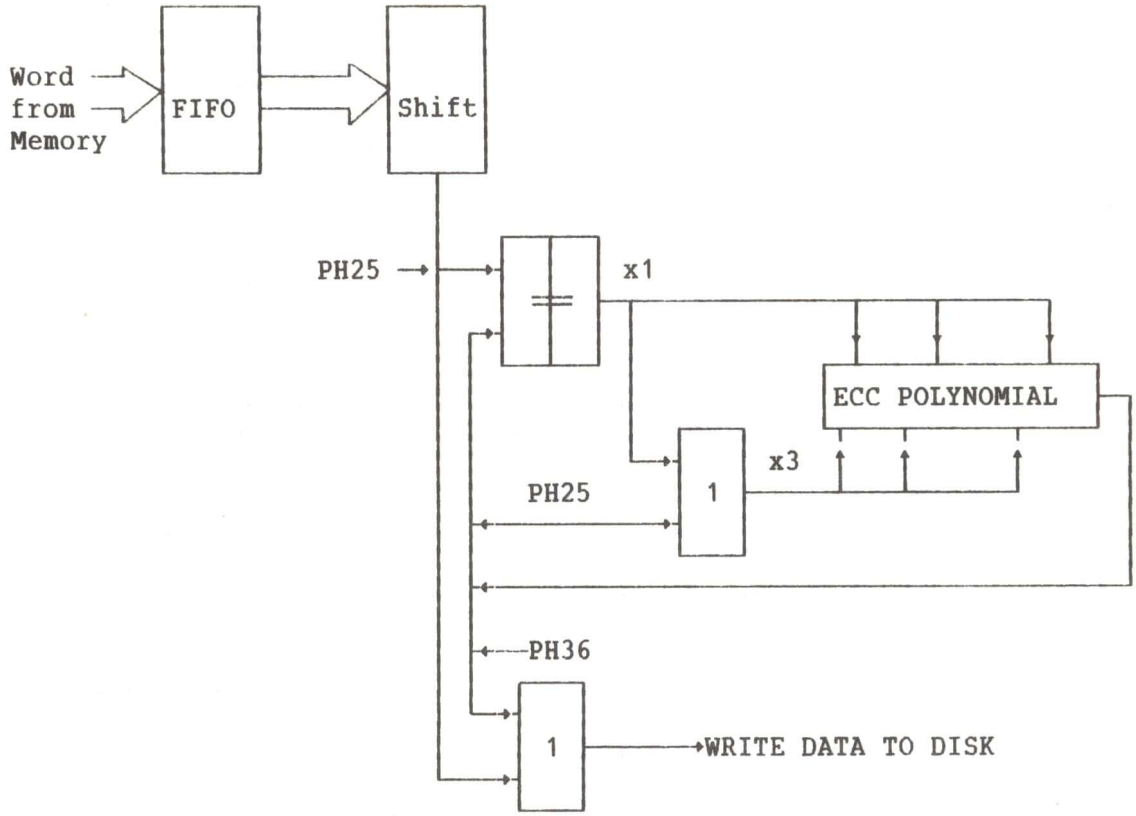


Fig. 6. Write Data

3.4.2.2 Read Data

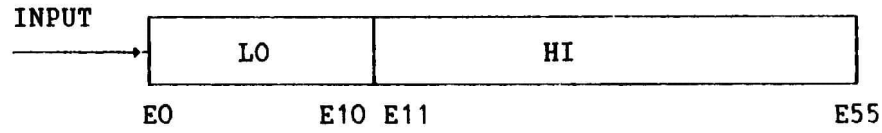
Data is serially read into the memory simulatneously as that in the shift register is divided to the polynom G(X). In addition, data is multiplied to X^{-n} N-n times. N is the period of the polynom = 585422, and n is the length of the code word = 8248.

If the data had notbeen premultiplied to X^{-n} , the shift register would have had to be shifted backward (hardware exacting), or it would have had to shift forward N-n times to get back to the starting-point (first data bit), because the contents of the shift register will repeat after N shifts one way (forward or backward).

N-n and N because we want to get back to the starting-point in order to go on shifting forwards.

When corrected, the input register will be closed, but gives feedback as during write data.

If HI is 0, it means that there is a correctable error LO.



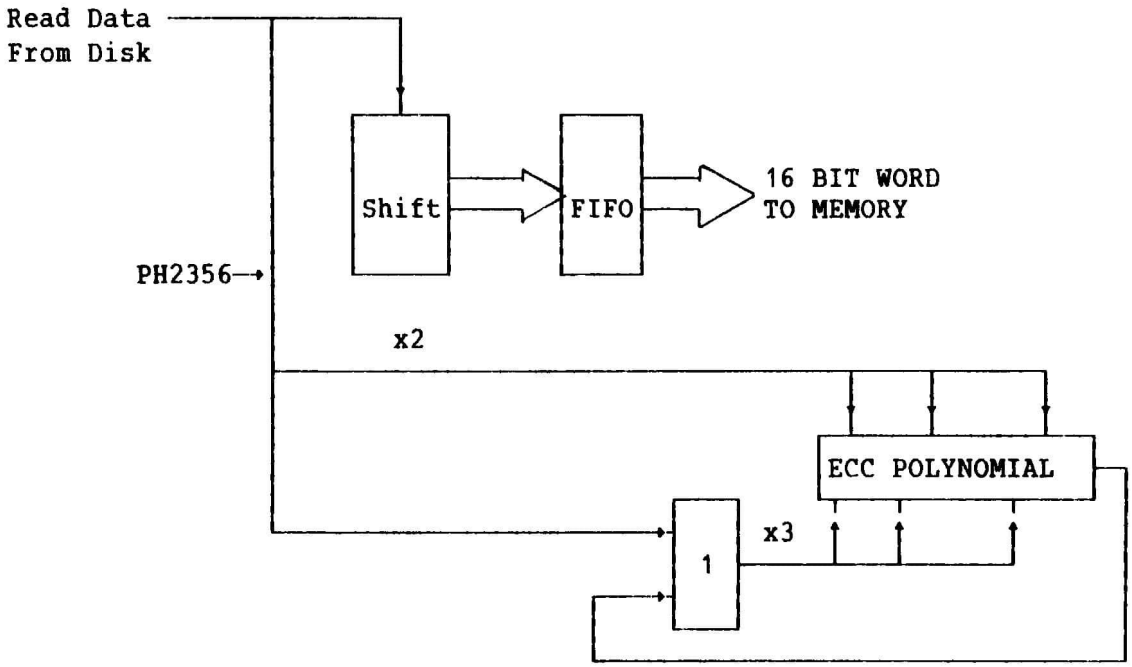


Fig. 7. Read Data

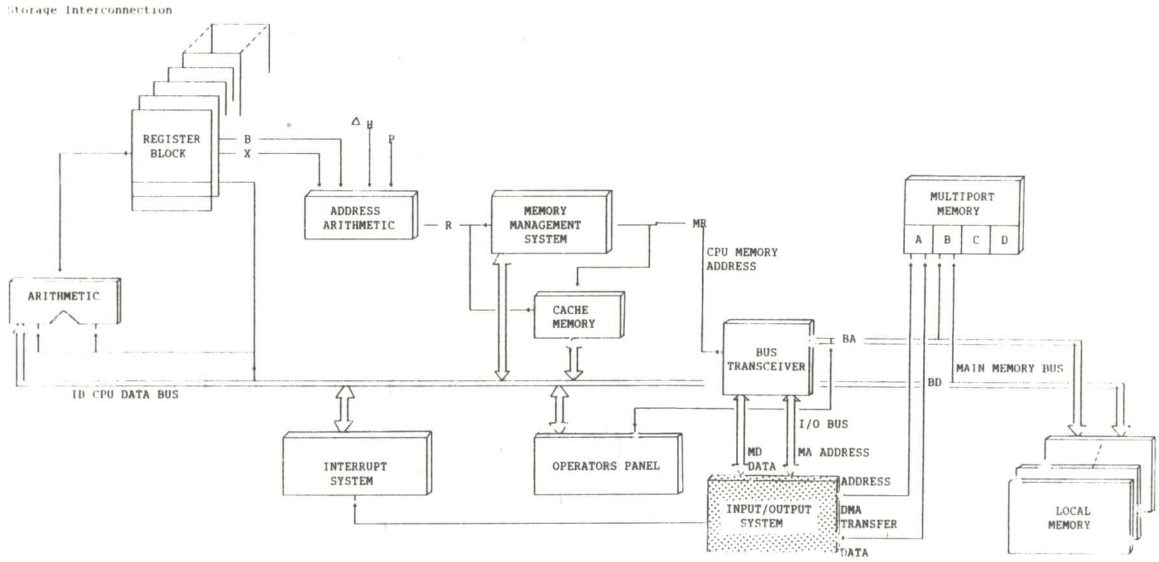


Fig. 8. Storage Interconnection

3.5 Timing Diagrams

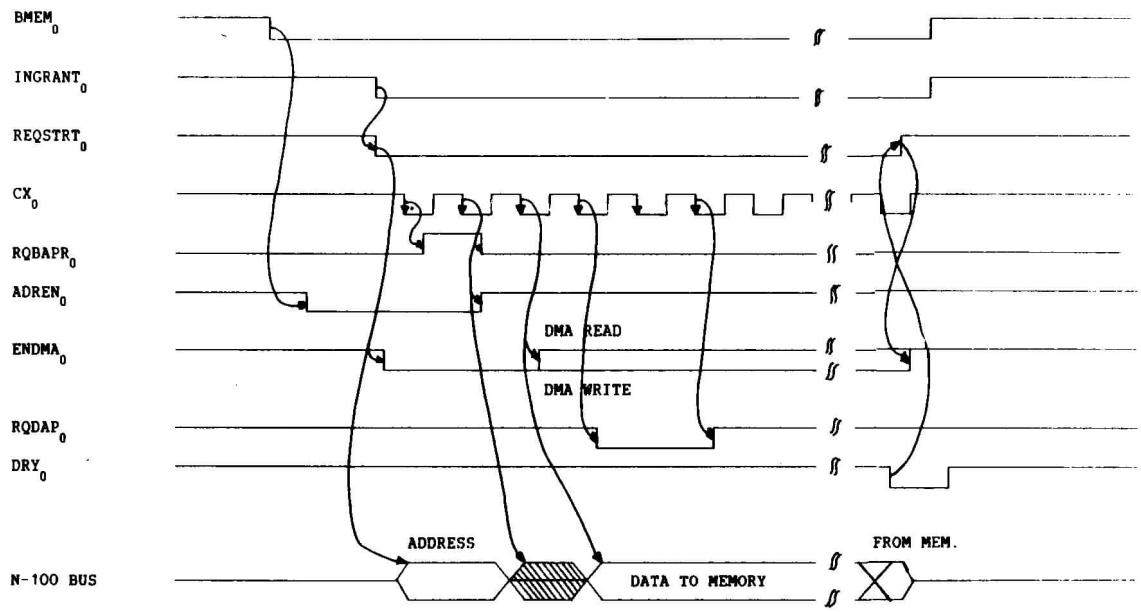


Fig. 9. DMA Timing

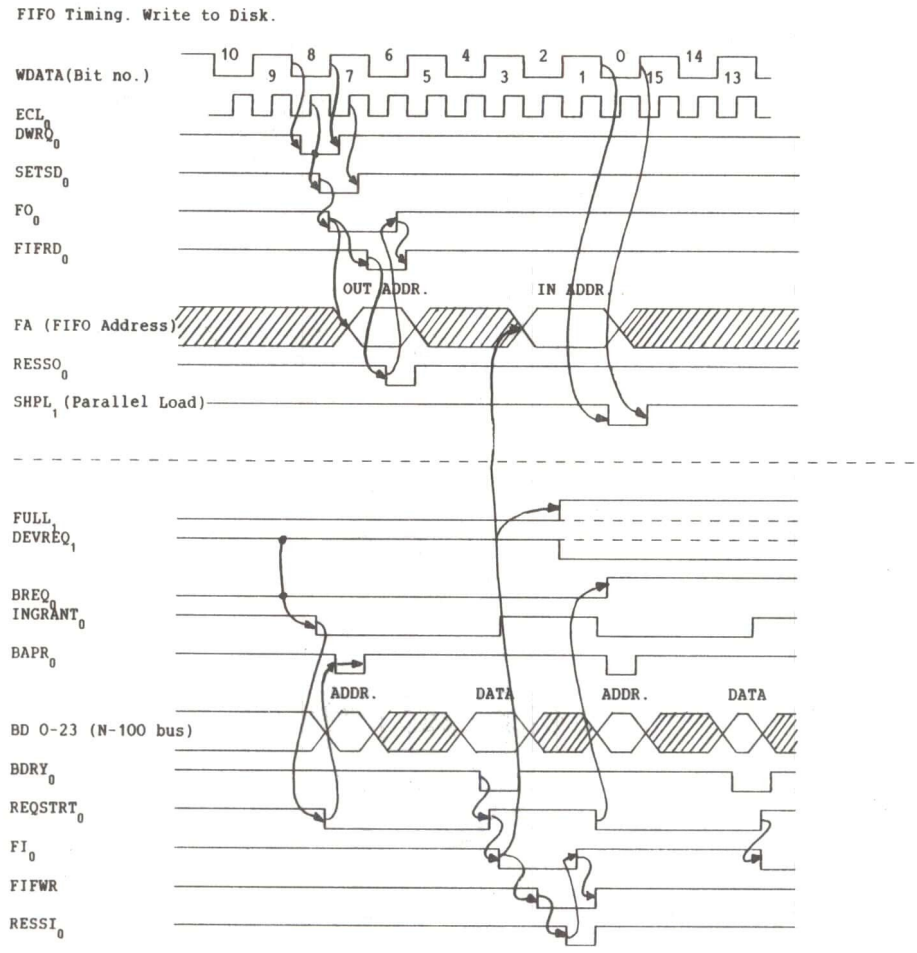


Fig. 10. FIFO Timing. Write From Disk

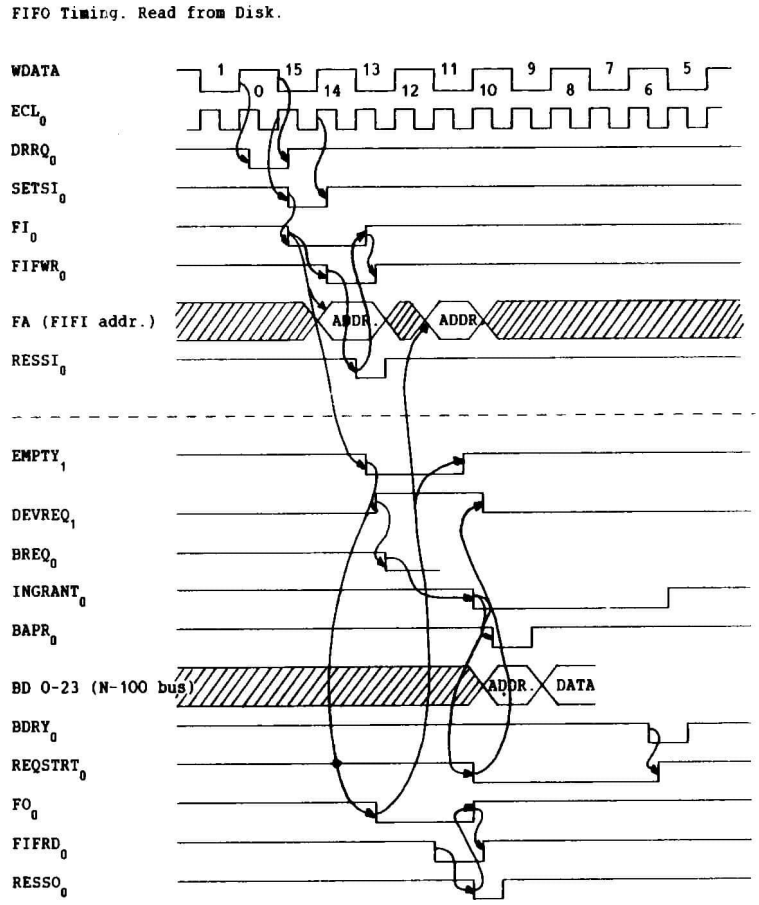


Fig. 11. FIFO Timing. Read From Disk

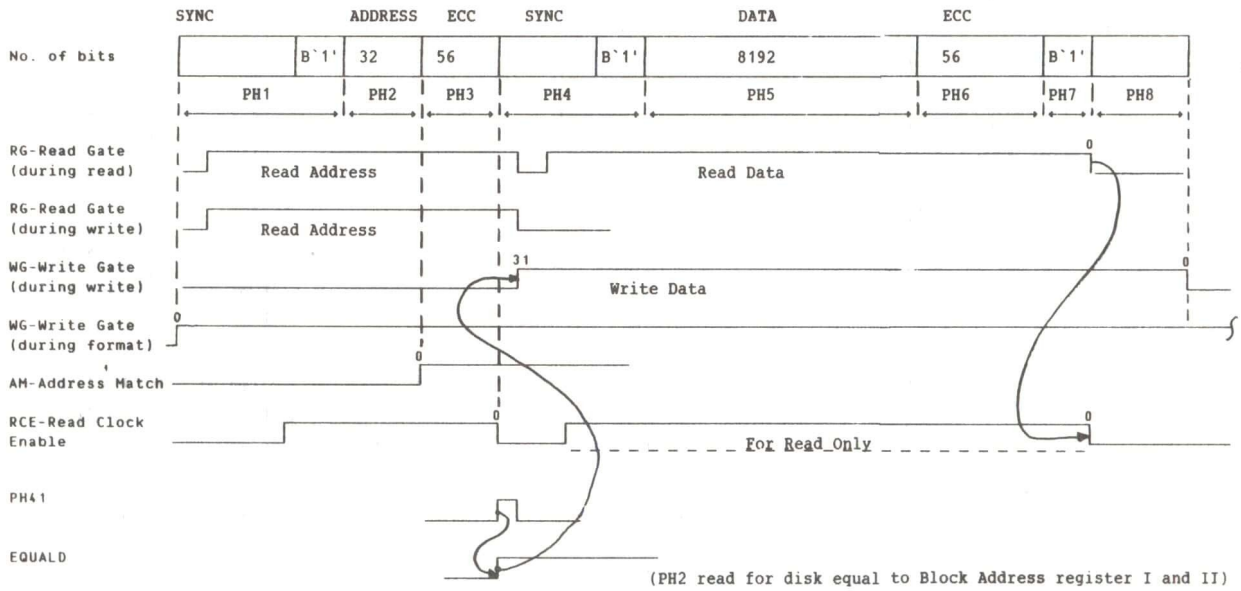


Fig. 12. Control Timing

3.6 Tag Timing

The tag timing generator is located on the SMD DATA (3044). For every function that is performed on the disk, tags 1,2, and 3 are issued in the listed sequence.

For more details, refer to figure 13.

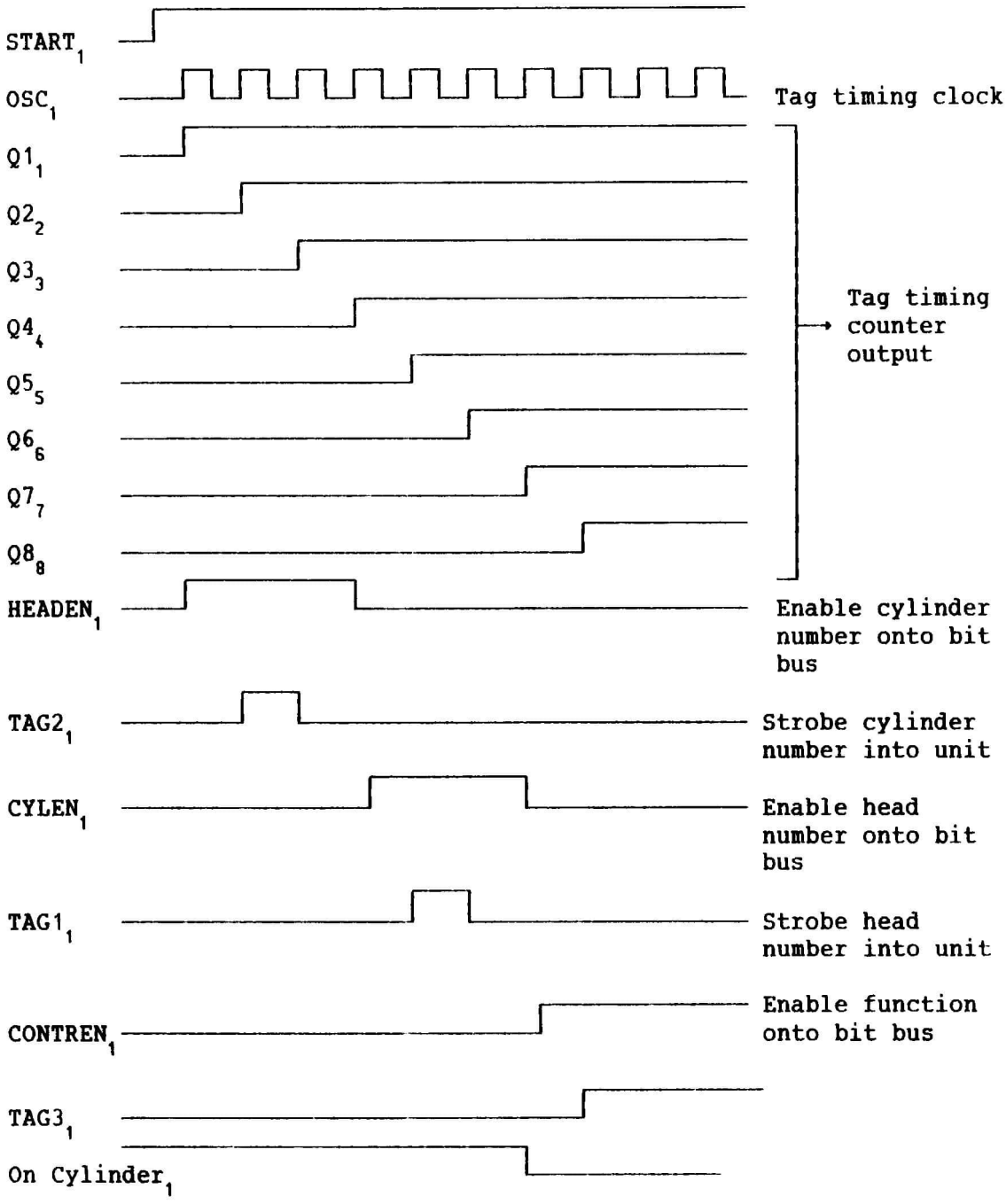


Fig. 13. Tag Timing

3.7 Interrupt Generation and Handling

The SMD disk controller is wired to interrupt level 11. The various sources for interrupt will be discussed here.

The interrupt sources can be divided into two groups (see figure 14):

- Error interrupts
- End of operation interrupts

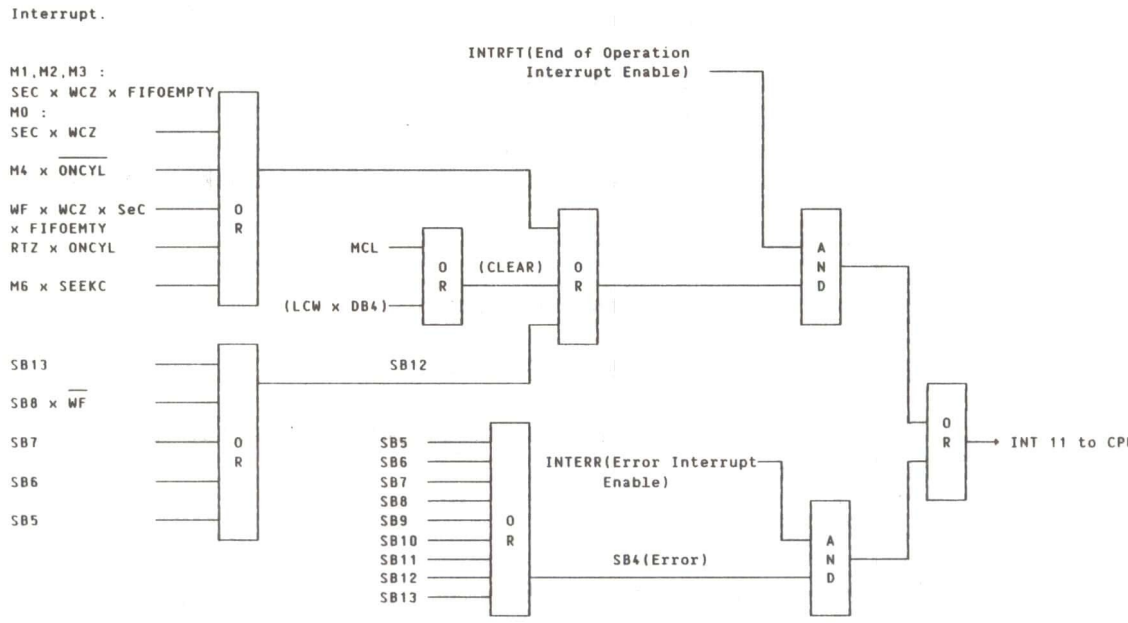


Fig. 14. The Interrupt Sources

Error interrupt is enabled by control word bit 1, and End of Operation interrupt is enabled by control word bit 0.

3.7.1 Error Interrupts

Error interrupt occurs when status bit 4 is forced on. Status bit 4 is inclusive OR of status bits 5,6,7,8,9,10,11,12, and 13.

3.7.2 End of Operation Interrupt

End of operation interrupt is generated when the START latch is reset. The START latch is reset in one of the following two ways :

- normal end of specified operation
- abnormal end of operation (SB 12)

Normal End of Operation

There are five different ways of generating Normal End of Operation. Refer to SMD Control.

1. Word counter has reached zero during a read or write operation (and FIFO empty).

   WRITE : SEC * WCZ * FIFOEMPTY
   READ : SEC * WCZ

2. On cylinder is deactivated upon an initiate seek command.

   (M4 * $\overline{\text{ON cyl}}$)

3. Completion of formatting one track.

   (WF * WCZ * SEC * FIFOEMPTY)

4. On cylinder on track 0 is reached upon completing a Return to Zero command.

   (RTZ * ON cyl)

5. Seek completion search positive.

   (M6 * SEEKC)

Abnormal End of Operation (SB 12)

There are five conditions that can set status bit 12, and thus interrupt.

1. Loss of Ready (SB13) condition from the selected unit during an operation.

2. Address mismatch (SB8) occurs when not formatting.

3. Fault line (SB7) from the selected unit is activated during an operation, or ECC parity error, or missing read clocks.

4. Illegal load (SB5) while controller is Busy.

5. Timeout (SB6).

CHAPTER 4

TROUBLESHOOTING

4 TROUBLESHOOTING

4.1 Debugging Guide

The normal procedure for checking out the ECC disk controller should be :

1. Check the operation of the IOX instructions.
2. Check the data channel by writing and reading a register in the disk controller.
3. Check the operation of the disk controller by running the controller in test mode.
4. Connect a disk drive to the controller and run test programs.

4.2 Check the Operation of the IOX Instructions

Refer to Programming Specifications in chapter 2.

A check should be made to ensure that all the controller registers can be accessed.

> NOTE !
>
> Control word register bit 15 selects the two banks of registers.

4.3 Check Data Channel

The data channel can be checked by writing and reading the same register in the controller, and then comparing the results. The Memory Address register is a register that can be accessed during read and write.

The following test loop tests the block address register I.

```
SAA 10          170 410         % Set bit 3 in A register
IOX CWR         165 545         % Set controller in test mode
COPY ST DA      146 165         % The contents of T-register
IOX BARI        165 543         % to block address register I
SAA 0           170 400         % Reset A register
IOX RBARI       165 546         % Read block address register
COPY SA DX      146 157         % and copy the contents to X
                                  register
JMP* - 7        124 371         % Repeat loop
```

Check that X-reg. equals T-reg. when changing T-reg.

Block address register II and the data channel are tested by the following test loop :

```
SAA 10          170 410         % Set bit 3 in A register
BSET ONE 170 DA 174 375         % Set bit 15 in A register
IOX CWR         165 545         % Set controller in test mode and
                                  select register bank I
COPY ST DA      146 165         % Transfer the contents of the
IOX BAR II      165 543         % T-reg to block addr. reg. II
SAA 0           170 400         % Reset A register
IOX RBAR II     165 546         % Read block addr.reg II and copy
                                  the contents to
COPY SA DX      146 157         % the X register
JMP* - 5        124 373         % Repeat loop
```

Check that X-reg. equals T-reg.

Testing MAR

```
                111             least sign MAR
                222             most sign MAR
            170 400             SAA 0 set block "0"
            165 545             LCW
            165 544             STS (MAR TOGGLE Reset)
             44 374             LDA
            165 541             LMAR most
             44 371             LDA
            165 541             LMAR least
            165 540             RMAR
            146 157             COPY SA - DX
            165 540             RMAR
            146 156             COPY SA - DT
            124 367             JMP* - 11
```

Check that X-reg. equals the least significant MAR, and that T-reg. equals the most significant MAR.

The contents of the memory buffer after the transfer is complete should be :

```
First location  :     125 252
Second location :     052 525
Third location  :     125 252
etc.
```

The easiest way of checking data transfer from memory to the disk controller is using compare mode while the controller is in test mode.

The data buffer, which was built up during read in test mode, is used as the output data under compare mode. The control word register is set to 014 014, to execute a compare test in test mode.

The block address register in test mode should be set as for a normal read, and the result in the status register should also be the same.

4.4.1 Test Loop

The following loop reads data in test mode and stores the data in memory, starting at the address given by MARL and MARU. The number of words to be transferred is given by WCL and WCU. The drive address is set to a special pattern used only in test mode. The loop tests for correct contents of the status register, and it also checks for proper operation of the memory address register and the word count register. In case of incorrect operation of the controller, the loop will stop at oneof seven WAIT instructions. The contents of the data buffer in memory must be checked manually.

If you want to change the operation of the controller, you may change the parameters listed from

MARU,

to

ACTIV,

```
044120   START,   LDA        SBLOCK
165545            IOX        LCO          % SELECT REG.BLOCK II
170401            SAA        1
165547            IOX        LWC          % CLEAR ECC
170430            SAA        30

165545            IOX        LCO          % CLEAR DEVICE
044114            LDA        INIT
004115            STA        STEST        % INITIATE SOFTWARE TIMEOUT
170410            SAA        10
165545            IOX        LCO          % TEST MODE

044100            LDA        MARU
165541            IOX        LMAR         % LOAD MEM.ADDR. BITS 16-23
044077            LDA        MARL
```

```
165541            IOX       LMAR        % LOAD MEM.ADDR. BITS 0-15
044076            LDA       WCU

165547            IOX       LWC         %LOAD WORD-COUNT BITS 16-23
044075            LDA       WCL
165547            IOX       LWC         % LOAD WORD-COUNT BITS 0-15
044074            LDA       DA1
165543            IOX       LDAD        % LOAD DISK ADDR.REG. I

044074            LDA       SBLOCK
165545            IOX       LCO         % SELECT REG.BLOCK II
044071            LDA       DA2
165543            IOX       LDAD        % LOAD DISK ADDR.REG. II
044071            LDA       ACTIV

165545            IOX       LCO         % LOAD CONTROL WORD
165544            IOX       RSR         % READ STATUS
175035            BSKP      ZRO 30 DA
151001            WAIT      1           % NOT ACTIVE AFTER ACTIVATE
165544  READS,    IOX       RSR         % READ STATUS

146151            COPY      SA DD
175235            BSKP      ONE 30 DA
124043            JMP       STIME
146115            COPY      SD DA
070063            AND       (177773

146153            COPY      SA DB
044055            LDA       ACTIV
107754            AND       (10
131005            JAZ       *+5         % JUMP IF NOT TEST MODE
050060            LDT       (41030

140036            SKP       SB EQL DT
151002            WAIT      2           % TEST MODE STATUS ERROR
124004            JMP       *+4
050055            LDT       (40010
140036            SKP       SB EQL DT

151003            WAIT      3           % DISK STATUS ERROR
170777            SAA       -1
165540            IOX       RMAR
064033            SUB       MARL
064034            SUB       WCL

131002            JAZ       *+2
151004            WAIT      4           % WRONG MEM.ADDR. BITS 0-15
170777            SAA       -1
165540            IOX       RMAR
070043            AND       (377

064023            SUB       MARU
064024            SUB       WCU
131002            JAZ       *+2
151005            WAIT      5           %WRONG MEM.ADDR. BITS 16-23
165544            IOX       RSR         % RESET FLIP-FLOP
```

```
044024          LDA     SBLOCK
165545          IOX     LCO         % SELECT REG.BLOCK II
170777          SAA     -1
165540          IOX     RMAR
131002          JAZ     *+2

151006          WAIT    6           % WORD COUNT NOT ZERO
124276          JMP     START
054020  STIME,  LDX     BUSY
150006          TRA     PID         % KEEP CPU BUSY
132777          JNC     *-1

040016          MIN     STEST
124326          JMP     READS
151007          WAIT    7           % SOFTWARE TIMEOUT
124267          JMP     START
000000  MARU,   0

001000  MARL,   1000
000000  WCU,    0
001000  WCL,    1000
125252  DA1,    125252
052525  DA2,    052525

100010  SBLOCK, 100010              % UNIT NUMBER MUST BE
                                      SPECIFIED
000014  ACTIV,  14                  % BOTH IN SBLOCK AND ACTIV
170000  INIT,   170000
177770  BUSY,   -10
000000  STEST,  0
177773  )FILL

000010
041030
040010
000377
```

C H A P T E R 5

TEST PROGRAMS

5 TEST PROGRAMS

The following test programs may be used :

- PASCAN
- Super-Rand
- ECC Test
- BIGFUNC
- Disc Tema

If you want more detailed information about test programs, the Test Program Description manual (ND-30.005) is recommended.

5.1 PASCAN Test Program - 2226

This is a stand-alone "PACK-SCAN" program for disk controllers with ECC. The program reads through the entire pack sequentially and reports "hard" and "soft" errors.

A "hard" error is defined as any error not recoverable by retries or ECC.

A correctable error in the read data istermeda "soft" error, i.e., recoverable through the use of retries or the ECC system.

The intended primary use of the program is for pack surface analysis.

There is an option to be specified prior to running the program :

"Address and Data" means that all address fields and data fields are read and verified.

"Data only" means that all data fields, but not all address fields, within each track are read and verified.

Error Reporting :

Hard Error Displays :

1. the current logical (octal) sector address
2. the controller status register

Soft Error Displays :

1. the current logical (octal) sector address
2. the address in main memory where error correction was applied
3. the two error correction pattern words to be exclusively OR'ed with data at the main memory address to correct the data

When an error is encountered and reported, the test continues the scan until the entire pack is read. "Scan Completed" is then reported.

5.2 Super-Rand Test Program-2222

This is a stand-alone random data, controller, and disk read/write test. The write data is generated by a pseudo-random number generator, and the disk address is generated in the following sequence :

0, n-1, 1, n-2, 2, n-3, ...

n is the number of sectors on the disk pack.

Example of Operation :

1. At disk address A, a random data pattern (i) is written from main memory.

2. At disk address B, a random data pattern (i) is written from main memory.

3. The written data at disk address A is read back and verified (against i).

4. The written data at disk address B is read back and verified (against i).

The process continues in the outlined fashion.

Errors and data mismatches are reported as specified by the test at runtime.

Options to be specified at runtime.

Retries active ?	When retries are specified, errors are not reported if they are recoverable by the retry and recovery procedure of the test.
ECC active ?	If active, correctable data errors are not reported.
RT clock ?	Prints out the time of day associated with each error reported.

The test runs continuously. Four disk units may be specified per controller, and the test runs simultaneously against all specified units.

This is a diagnostic program for the disk controller with ECC. The test does read and write functions to test the functions of the error correction. It is therefore required that an online drive with a disk scratch pack is attached to the controller.

The test completely diagnoses the 3043/3044 card of the controller, and associated control circuitry on other boards. Data records with correctable errors are written, read back, and verified. The process is repeated many times, varying the error pattern and its displacement within the data record.

Errors are reported as they occur, and a brief description is displayed with status word information.

5.3 Disc Tema

This test enables you to format, dump contents, change single words, or check parity on disks. It can also copy, compare, and verify the contents of two disks. Starting the program causes some tests to be run. The disk status is read, and errors are reported.

The test program is written so as to make it easy to run with the modes that are assumed to be the most common ones.

Almost all of the commands are written the same way. The errors are also printed in the same way. The description of the various commands covers only what is special to each command.

For details, refer to the Test Program Description Manual: ND-30.005.

The following is a description of the BIGFUNC Test Program, which is part of Disc Tema.

5.4 BIGFUNC

BIGFUNC is a stand-alone test program, intended to test the disk status word and some of the disk operations. Reading and writing is done on a track not used by the SINTRAN III operating system, but it might still be wise to use a scratch pack when running BIGFUNC.

The program is self-documenting. The following tests are done :

1. The memory address register is written and read 131072 times.

2. Each of the block address registers are written and read 131072 times.

3. Data is read from the interface in test mode. The status word, the data read, and the memory address register are checked. Word count is in the range 1-2000B.

The status bits are then checked 8 times, in different sequences :

4. Status bit 0 is loaded and read twice.

5. Status bit 1 is loaded and read twice.

6. Status bit 2 is checked after device clear and read.

7. Status bit 5 is checked by loading :

   - the memory address register
   - the block address register I
   - the word count register
   - the control word

   when parity check operation is active; and by loading block address register I when the disk arm is not on-cylinder.

8. Status bit 6 is checked by doing a short parity check and a very long formatting operation.

9. Status bit 7 is checked by reading from a non-specified unit (see below). 8 read/writes are done in case of error.

10. Status bit 8 is checked by formatting a track with incorrect formating data, and reading it back.

11. Status bit 9 is checked by reading with word count 1004B and bit 2 in ECC control loaded (long bit).

12. Status bit 20 is checked by doing read, compare, change one bit in the disk buffer, compare.

13. Status bit 11 is checked by doing read with the instructions IOX 0 three times in the waiting loop, and by doing write with the instruction IOX 0 twice in the waiting loop.

14. Status bit 13 is checked by the selection of specified units and by reading from non-specified units (see below).

15. Status bit 14 is checked by doing return-to-zero-seek and initiate-seek.

16. Status bit 15 is loaded and read twice. Status bits 3, 4, and 12 are not checked separately. All units not specified to be tested should be turned off (stop the disk pack and turn off the power at the back of the disk unit).

17. Read and write are checked by reading and writing from different buffers. Seek-complete-search is checked with no previous seek.

18. Read-seek-condition is checked by doing return-to-zero-seek, initiate-seek, and by reading from an illegal block address.

The test repeats itself indefinitely.

All errors are reported as error messages on the terminal.

C H A P T E R 6

INSTALLATION

6 INSTALLATION

6.1 I/O Configuration Example

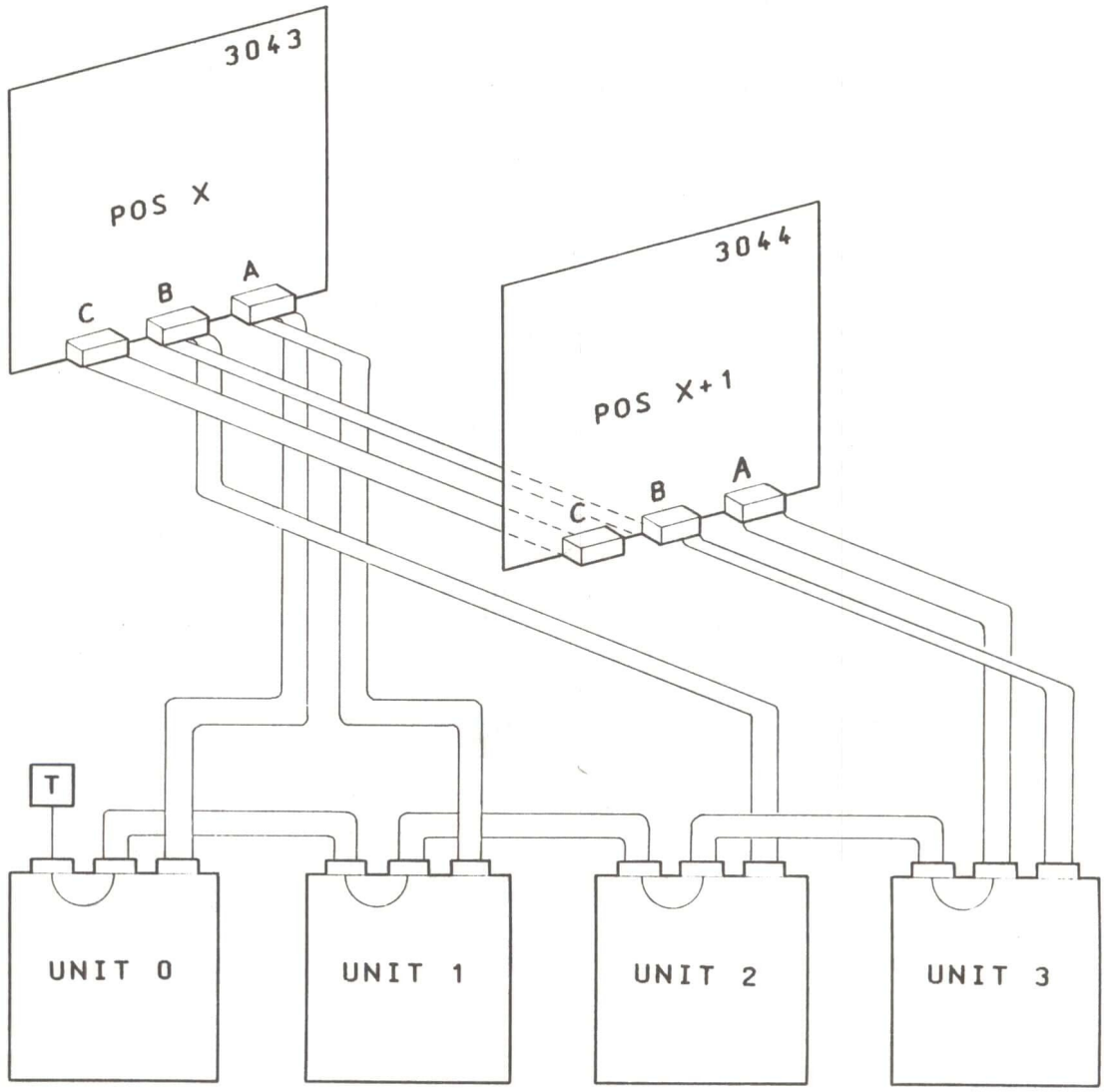


Fig. 15. I/O Configuration Example

6.2 ND-100 Plug Panel

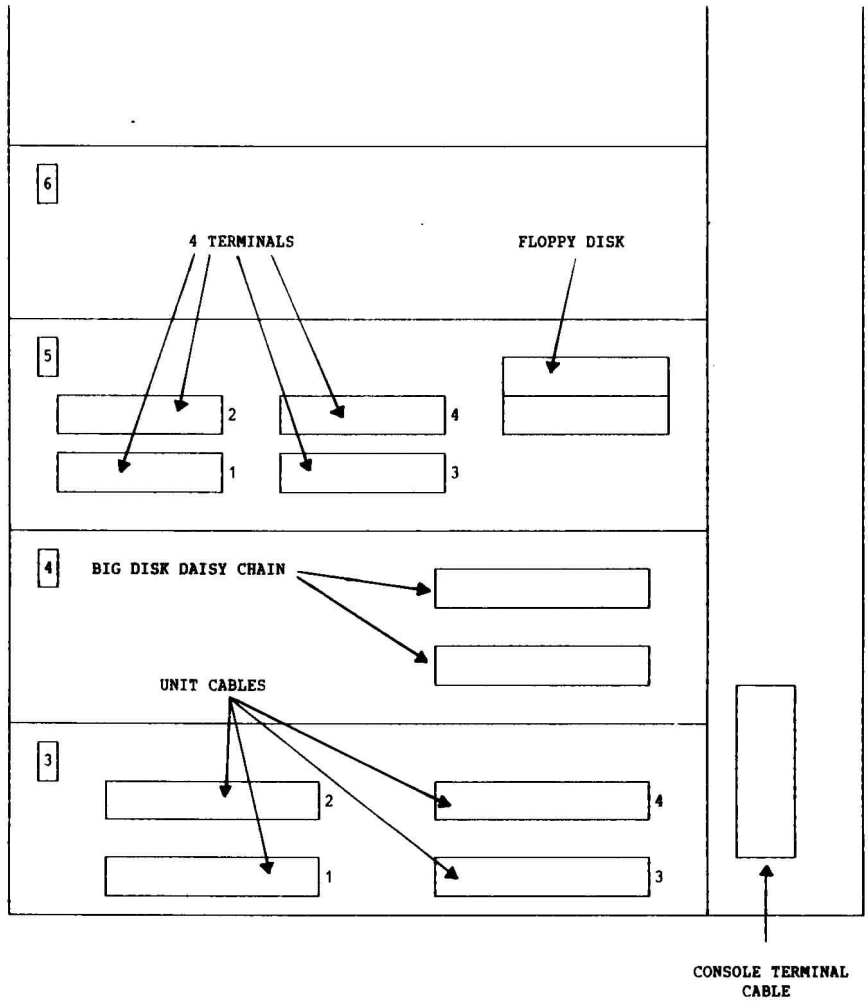


Fig. 16. ND-100 Plug Panel for External Device Connection

6.3 Switches and Indicators on Card no. 3043

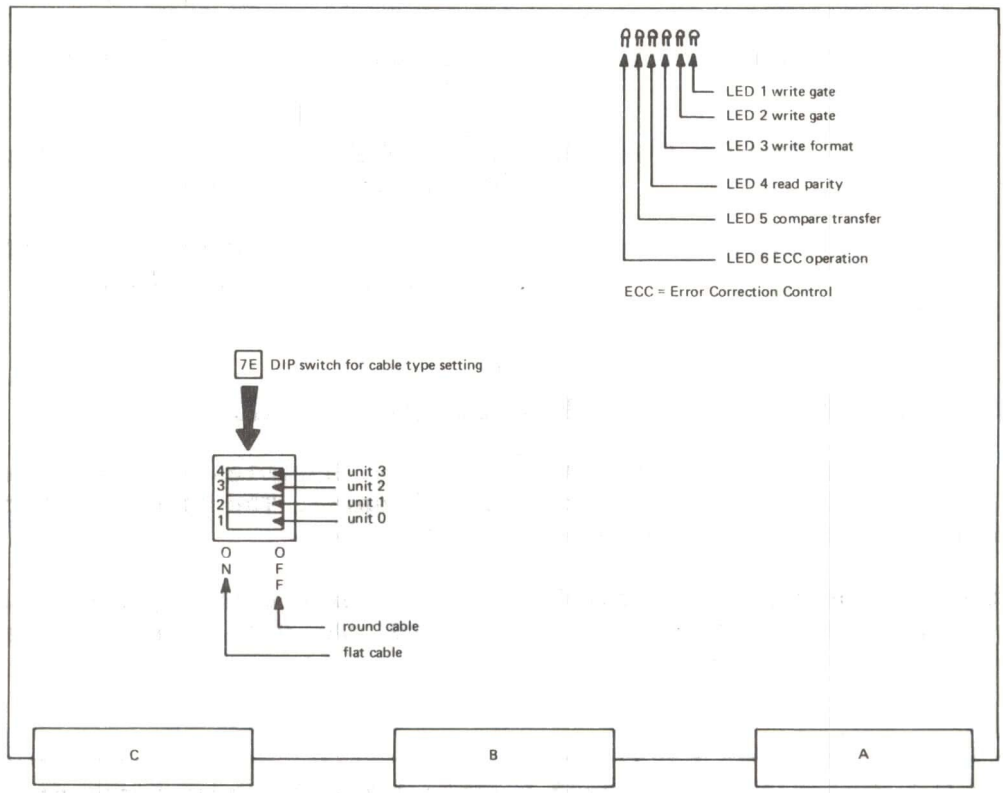


Fig. 17. Switches and Indicators on Card no. 3043

6.3.1 Indicators - LED 1 - LED 6

All indicators are yellow LEDs, with the following meanings :

LED 1	Write gate.	Is lit when the disk heads write.
LED 2	Read gate.	Is lit when the disk heads read.
LED 3	Write format.	Is lit when the controller formats.
LED 4	Read parity.	Is lit when the controller checks parity.
LED 5	Compare transfer.	Is lit when the controller compares data after a read/write.
LED 6	ECC Operation.	Is lit when the controller performs error correction calculation.

6.3.2 Cable Type Setting (DIP Switch in Position 7E)

The switch setting concerns B-cables only (B-cables are cables which go directly from the computer to the disk unit). The daisy chain cable (A-cable) may be a flat cable or a round cable.

Switch 7E consists of 4 switches, one for each disk unit. The switch must be OFF when the B-cable is round, and ON when the B-cable is flat.

Unit 0	Switch 1	OFF	Round B-cable between computer and disk unit 0.
		ON	Flat B-cable between computer and disk unit 0.
Unit 1	Switch 2	OFF	Round B-cable between computer and disk unit 1.
		ON	Flat B-cable between computer and disk unit 1.
Unit 2	Switch 3	OFF	Round B-cable between computer and disk unit 2.
		ON	Flat B-cable between computer and disk unit 2.
Unit 3	Switch 4	OFF	Round B-cable between computer and disk unit 3.
		ON	Flat B-cable between computer and disk unit 3.

6.4 Switches and Indicators on Card no. 3044

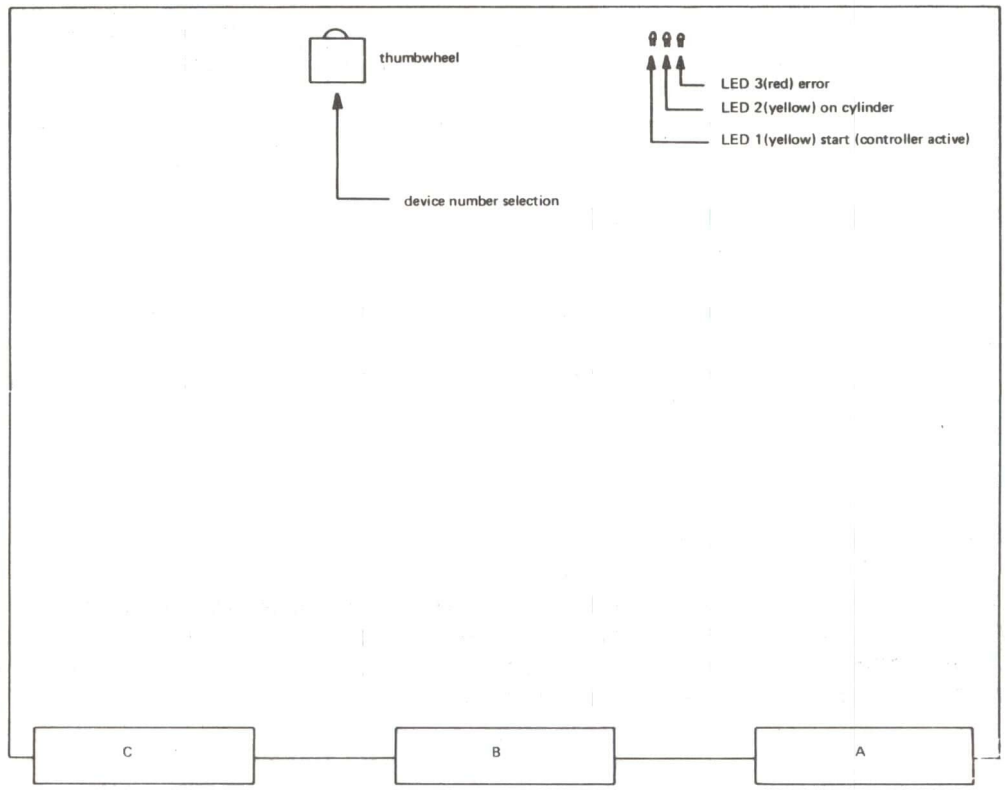


Fig. 18. Switches and Indicators on Card no. 3044

6.4.1 Device Number Selection (Thumbwheel)

Thumbwheel Setting	Device Register Address Range (Octal)	Ident. Code (Octal)	Device name
1-7	not used		
8	1540-1547	17	Big Disk System 1
9	1550-1547	20	Big Disk System 2
10-15	not used		

6.4.2 Indicators - LED 1 - LED 3

LED 1	(Yellow)	Start	Controller active.
LED 2	(Yellow)	On Cylinder	Read/write head on cylinder.
LED 3	(Red)	Error	

6.5 Connecting a Disk Drive

When the controller runs without problems in test mode, a unit can be connected. The initial start-up procedure is given in the maintenance manual accompanying the disk. The disk pack to be used must be formatted, preferably on another machine.

C H A P T E R 7

CONNECTOR LIST

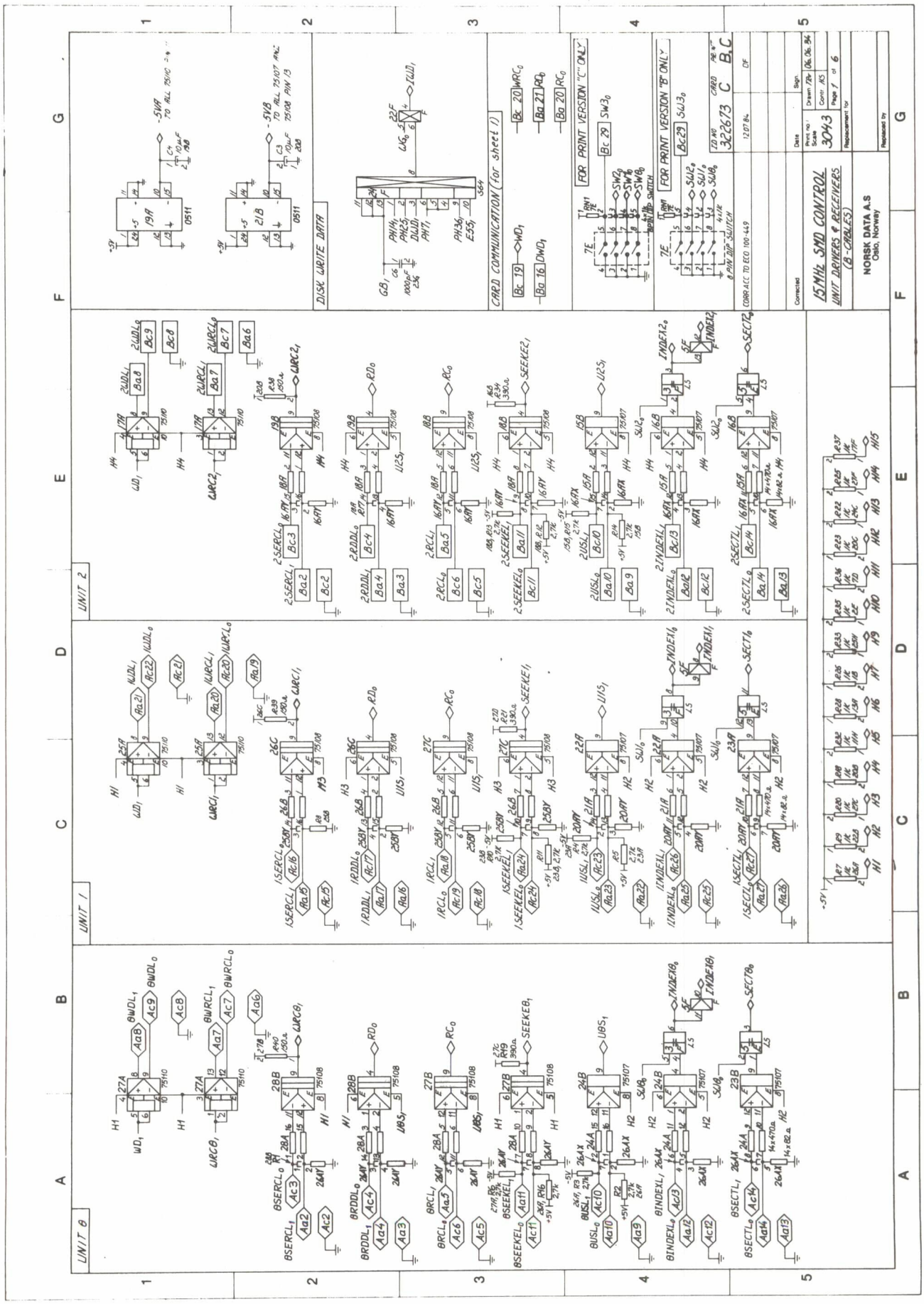
7 CONNECTOR LIST

Card communication signals 3043 - 3044

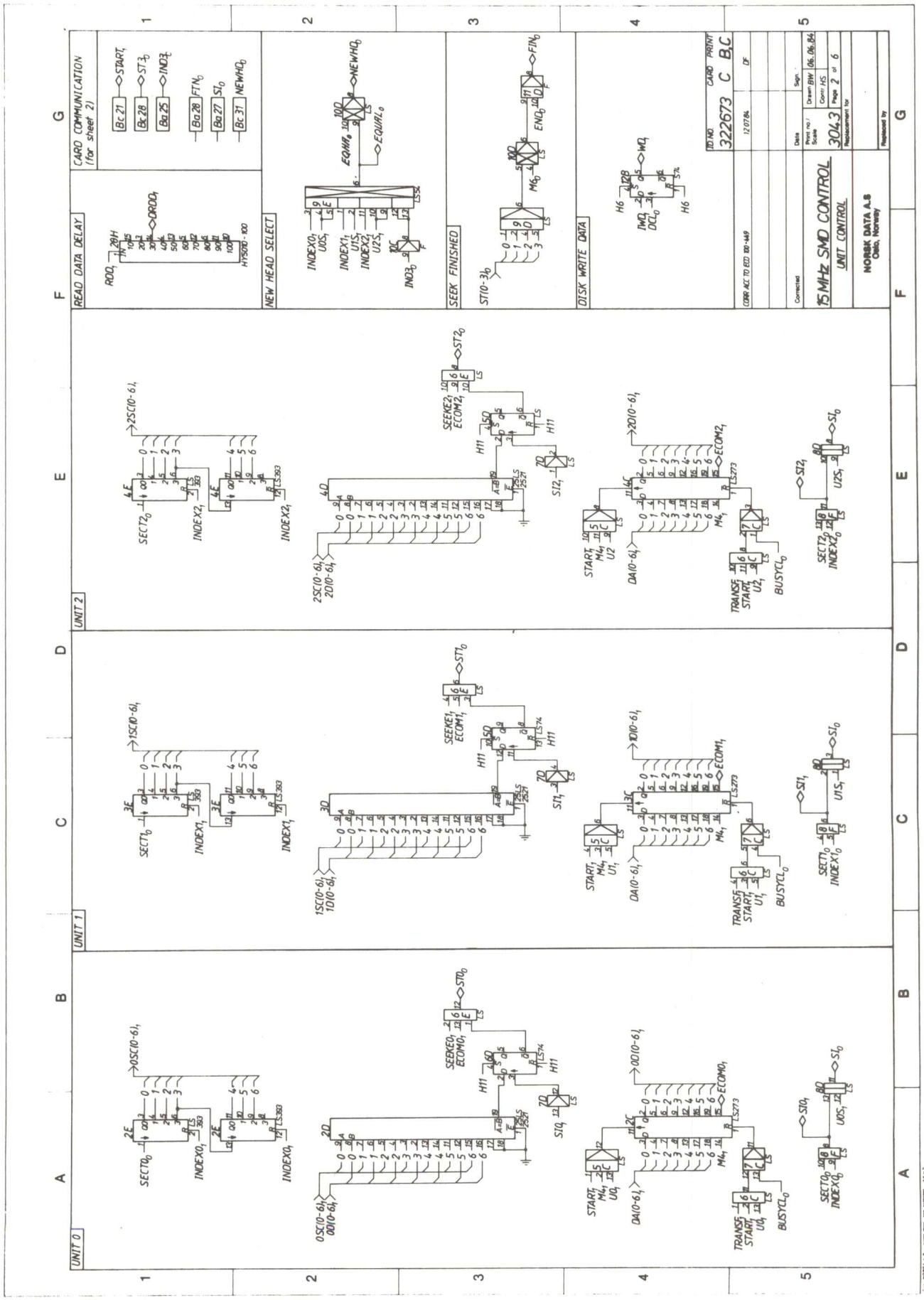
		"3043"		"3044"
c	15	WG_0	→	Write Gate
a	15	RG_0	→	Read Gate
c	16	$SB10_0$	→	Status bit 10 (Compare Error)
a	16	DWD_1	←	Disk Write Data from shift register
c	27	$RSECT_0$	←	Read Seek Condition
a	27	ME_0	←	Master Enable
c	18	$LBLOCK_0$ 1	←	Load Block address register I
a	18	SEC_0	→	Sector Pulses
c	19	WD_1	←	Write Data to disk
	19	LCW_0	←	Load Control Word
c	20	WRC_0	→	Write clock from disk (servoclock)
a	20	RC_0	→	Read clock from disk
c	21	$START_1$	←	Controller active
a	21	RD_0	→	Read Data from disk
c	22	$DRRQ_0$	→	Disk Read Requests
a	22	ECL_1	→	Disk Serial data clock
c	23	$SB9_0$	→	Status bit 9 (Data Error)
a	23	$SB8_0$	→	Status bit 8 (Address Mismatch)
c	24	$WRITE\ VL_1$	←	Write clock to disk
a	24	$SB7_0$	→	Status bit 7 (ECC parity error or missing clocks)
c	25	$EC2_0$	→	Enable Block Address shift in phase 2
a	25	$IND3_0$	←	Index pulses from unit 3
c	26	RDD_1	→	Read Data from disk or test mode generator
a	26	BA_1	←	Serial Block Address
c	27	$U3_1$	→	Select Unit 3
a	27	SI_0	→	Sector or Index pulses from disk
c	28	$ST3_0$	←	Seek Terminated on unit 3
a	28	FIN_0	→	M6 og M8 finished
c	29	$EQUAL_0$	→	Equal sector
a	29	REP_0	←	Read ECC Pattern
c	30	$ECCC_0$	←	Load ECC Control register
a	30	REC_0	←	Read ECC Count
c	31	$NEWHD_0$	→	Select new head (crossing index mark)
a	31	$DWRQ_0$	→	Disk Write Requests
c	32	GROUND		
a	32	GROUND		

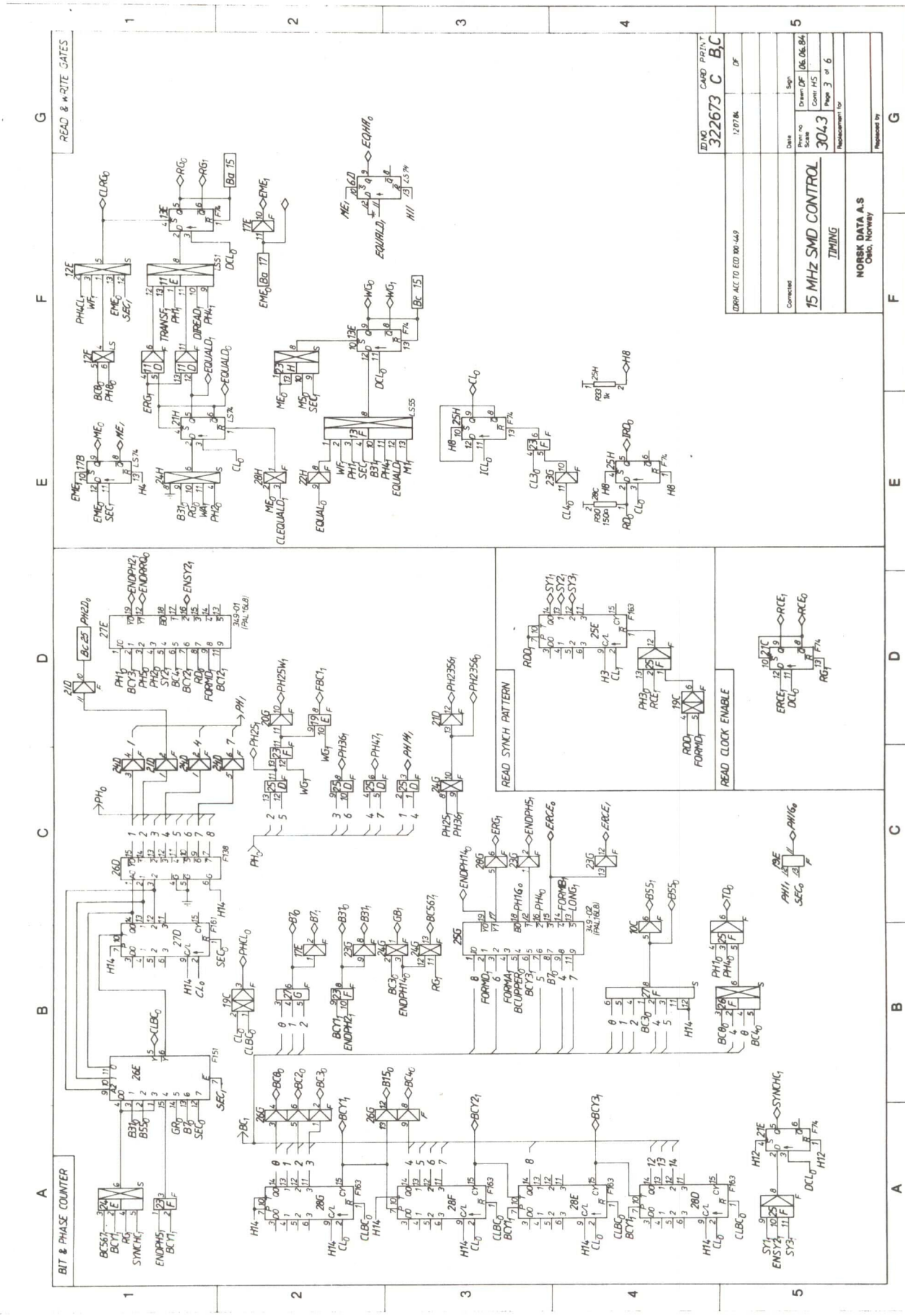
A P P E N D I X A

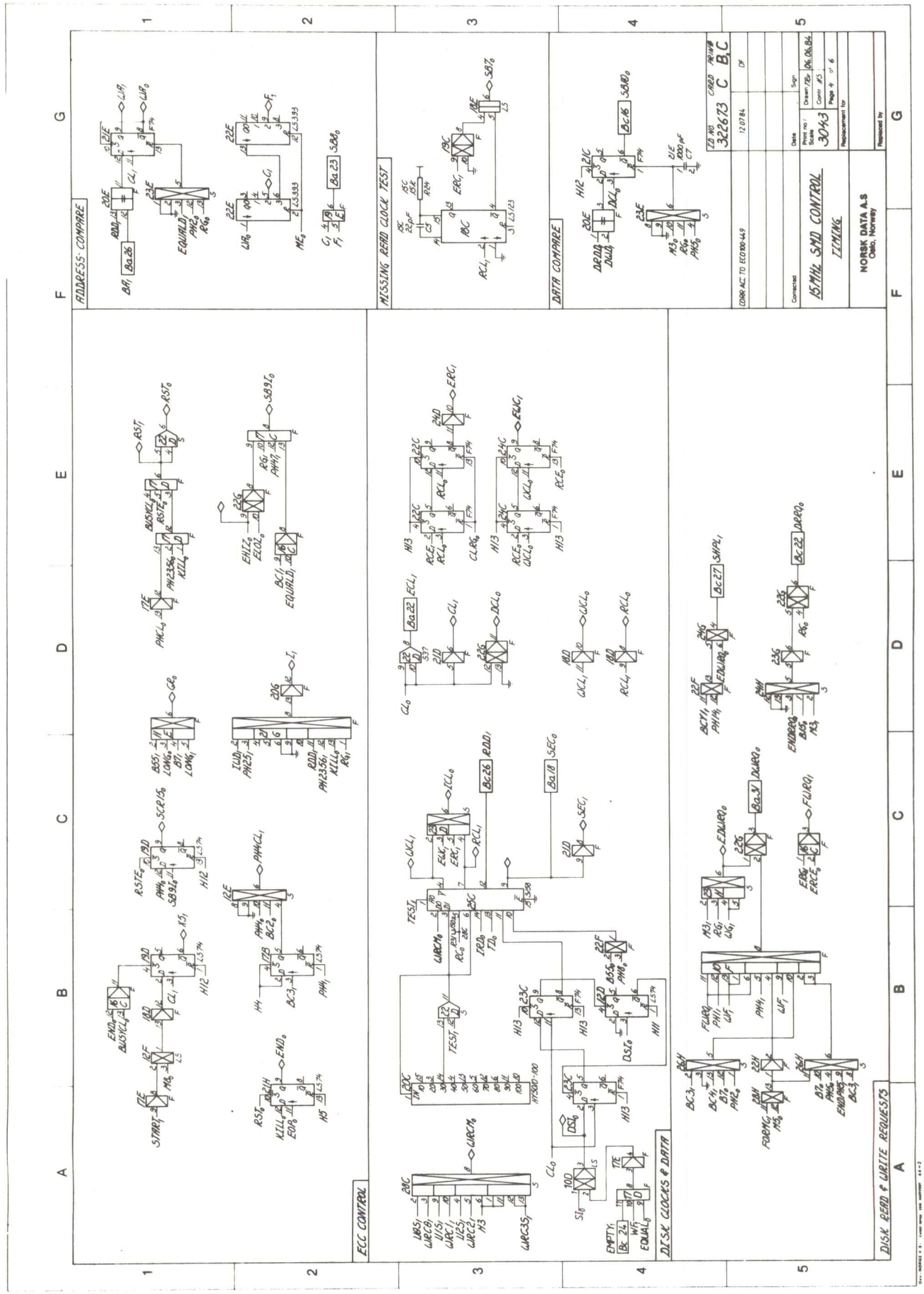
LOGIC DIAGRAM CARD NO. 3043


UNIT 0
UNIT 1
UNIT 2
DISK WRITE DATA
CARD COMMUNICATION (for sheet 1)
FOR PRINT VERSION "C" ONLY
FOR PRINT VERSION "B" ONLY
15MHz SMD CONTROL
UNIT DRIVERS & RECEIVERS
(B-CABLES)
3043
NORSK DATA A.S
Oslo, Norway
CARD NO 326173 C B.C
CORR ACC TO ECO 100-449
Drawn ZBr 06.06.84
Contr AKS
Page 1 of 6
Replacement for
Replaced by
Date
Sign
Checked
Corrected

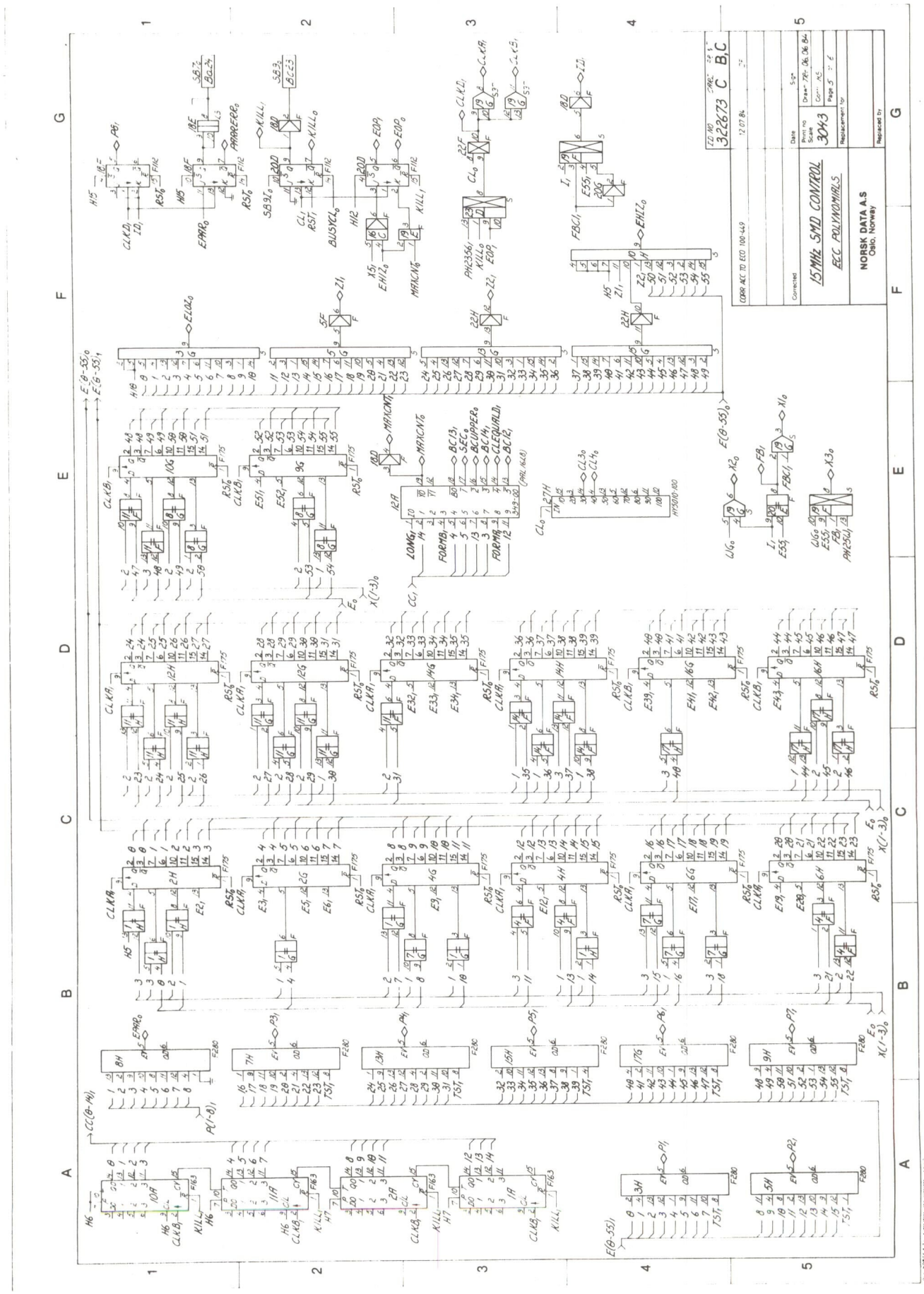
15MHZ SMD DISK CONTROLLER
LOGIC DIAGRAM CARD NO. 3043


UNIT 0
UNIT 1
UNIT 2
CARD COMMUNICATION (for sheet 2)
READ DATA DELAY
NEW HEAD SELECT
SEEK FINISHED
DISK WRITE DATA
15MHz SMD CONTROL
UNIT CONTROL
NORBIK DATA A.S
Oslo, Norway
3043
3226/3 C B.C
Page 2 of 6

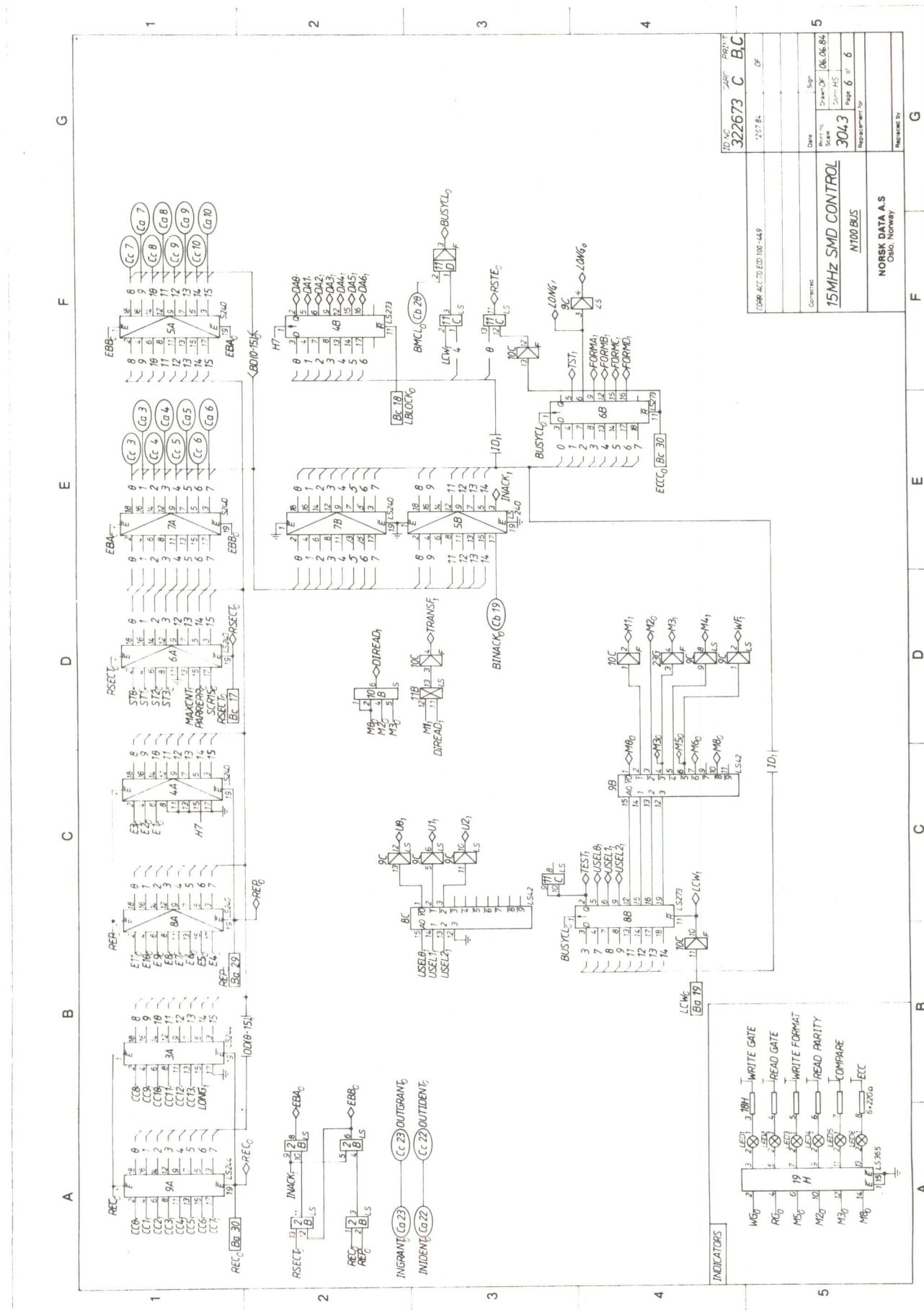

BIT & PHASE COUNTER
READ & WRITE GATES
READ SYNCH PATTERN
READ CLOCK ENABLE
IDNO 322673 C B,C
15 MHz SMD CONTROL
TIMING
3043
NORSK DATA A.S
Oslo, Norway


ADDRESS COMPARE
MISSING READ CLOCK TEST
DATA COMPARE
ECC CONTROL
DISK CLOCKS & DATA
DISK READ & WRITE REQUESTS
15 MHz SMD CONTROL
TIMING
NORSK DATA A.S
Oslo, Norway
3043
3226/73
Page 4 of 6

15MHZ SMD DISK CONTROLLER
LOGIC DIAGRAM CARD NO. 3043



15MHZ SMD DISK CONTROLLER
LOGIC DIAGRAM CARD NO. 3043


15MHz SMD CONTROL
N100 BUS
3043
NORSK DATA A.S
Oslo, Norway
322673 C B.C
INDICATORS
WRITE GATE
READ GATE
WRITE FORMAT
READ PARITY
COMPARE
ECC

A P P E N D I X B

DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043

GENERAL DESCRIPTION

As explained in the manual, the 15 MHz SMD data card handles all the disk A-cable signals, plus the B-cable signals for one disk unit (no. 3). The 15 MHz SMD control card handles the B-cable signals for the remaining 3 disk units (0, 1 and 2). Both cards also communicate with each other and also with the NORD-100 bus. The following applies to the 15 MHz SMD data card.

PLUG CONNECTIONS

Plug A is used for the A-cable signals. B-cable signals are connected via plug B, which is also used for communication with the 15 MHz SMD control card. Plug C is used for communication with the NORD-100 bus.

ND-100 BUS SIGNALS

These signals are connected via plug C to/from :

- Block 1/1 (top left of FBD)
- Block 5/9 (lower left)
- Blocks 1/2 and 1/3 (upper center)

INTERNAL DATA BUS (DB)

The main data bus internal to the card (DB 0-23) is shown passing across theupper part of the FBD, and connecting down the right-hand side.

DISK ADDRESS BUSSES

The two disk address busses, DA 0-15 and A 0-15, originate in block 2/2 to the left of center of the FBD and are distributed to blocks 5/1, 4/1, 5/4 and 4/3 at FBD center.

A-CABLE SIGNALS

All the card outputs to the A-cable originate in block 4/2 (to the right of FBD center), and all signals from the A-cable enter block 4/3 at FBD bottom center.

The A-cable bus (B 0L-11L) originates in block 4/2 (to the right of FBD center). The least significant ten bits of the bus are fed to block 4/2 from block 4/1 as B 0-9. The most significant bits arrive at block 4/2 as A 10-11 from block 2/2.

The TAG bus signals (TAG 1-3) originate in block 4/1 and are fed out of the card via block 4/2.

B-CABLE AND INTER-CARD SIGNALS

The B-cable signals, which are concerned with disk unit 3, are connected to block 5/5 at the bottom left of the FBD. The plug B signals that enter or leave block 5/5, and also are prefixed by (3), are those belonging to the B-cable. The remaining plug B signals are connected to the 15 MHz SMD control card (3043).

Note that on the logic diagram, the B-cable signals are not prefixed by (3), but they should have been in order to be consistent with the B-cable signals on card 3043, which are prefixed by 0, 1 or 2.

The data signals on the B-cable are as follows. WD, which enters block 5/5, is the Write Data for disk unit 3. The Write Data has originated in the FIFO on this card (see the next paragraph.), but has passed through the 15 MHz SMD control card before returning as WDL, to go directly to disk unit 3.

The RD output from block 5/5 is the buffered version of RDDL, which is the data read directly from disk unit 3. RD goes to card 3043 before returning to this card as RDD (at FBD mid-left) and entering the FIFI (see the next paragraph.).

FIFO DATA FLOW

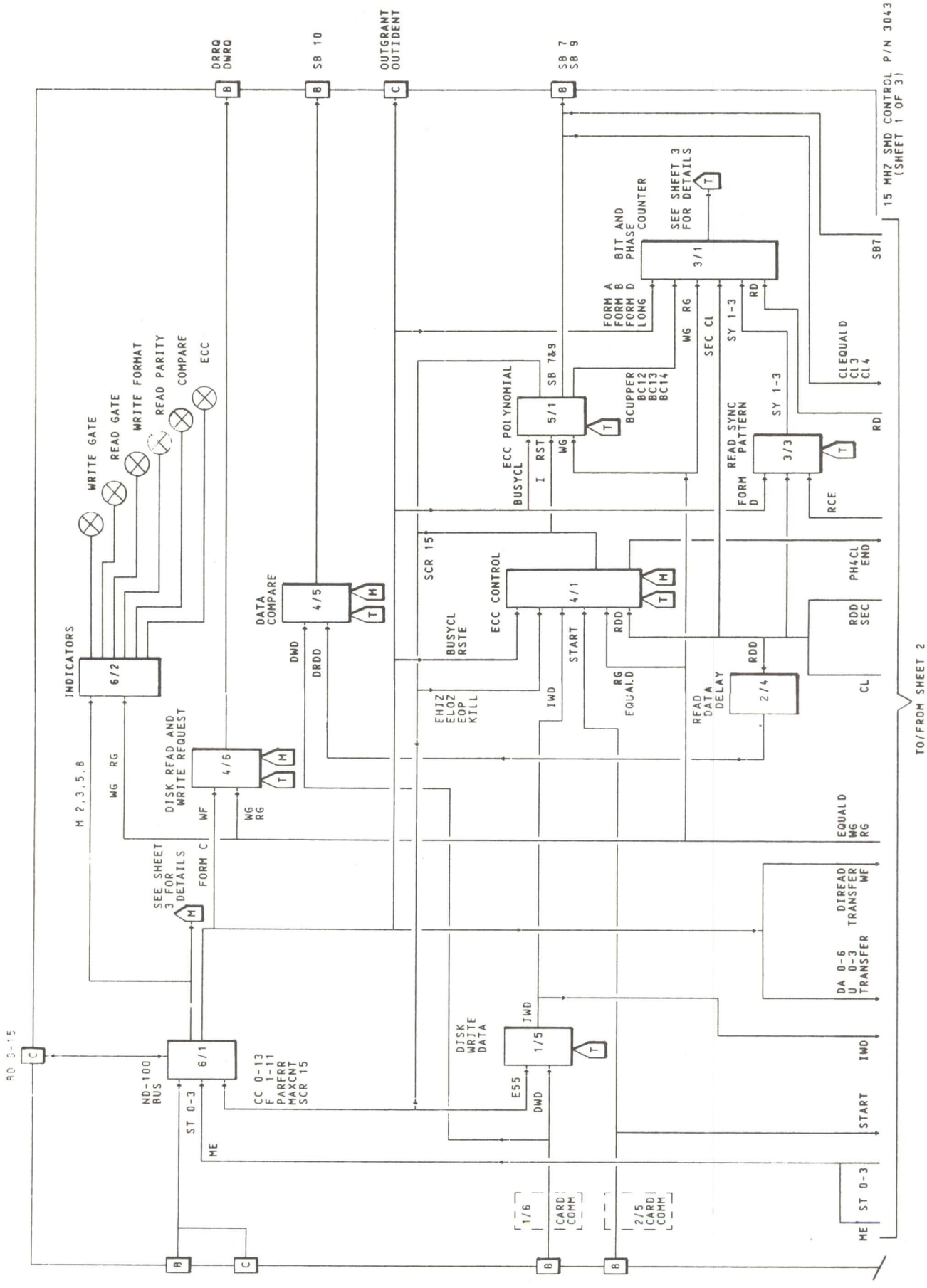
All data transferred between the disk units and the computer memory passes through the FIFO register block (3/2 at the top left of the FBD). The memory data is transferred to/from the FIFO block via the BD 0-15 lines. The disk data input to the FIFO is signal RDD (at FBD mid-left), which comes from card 3044. The data output form FIFO to a particular disk unit is signal DWD leaving the FBD at bottom right, and which also goes to card 3043 before being passed on to a disk unit.

MODE CONTROL SIGNALS

The card operates in various modes according to the content of the control word loaded into block 2/2 (at FBD upper left). This block generates 10 mode control signals (M0-M9), which are not shown on the FBD but whose destinations are as follows :

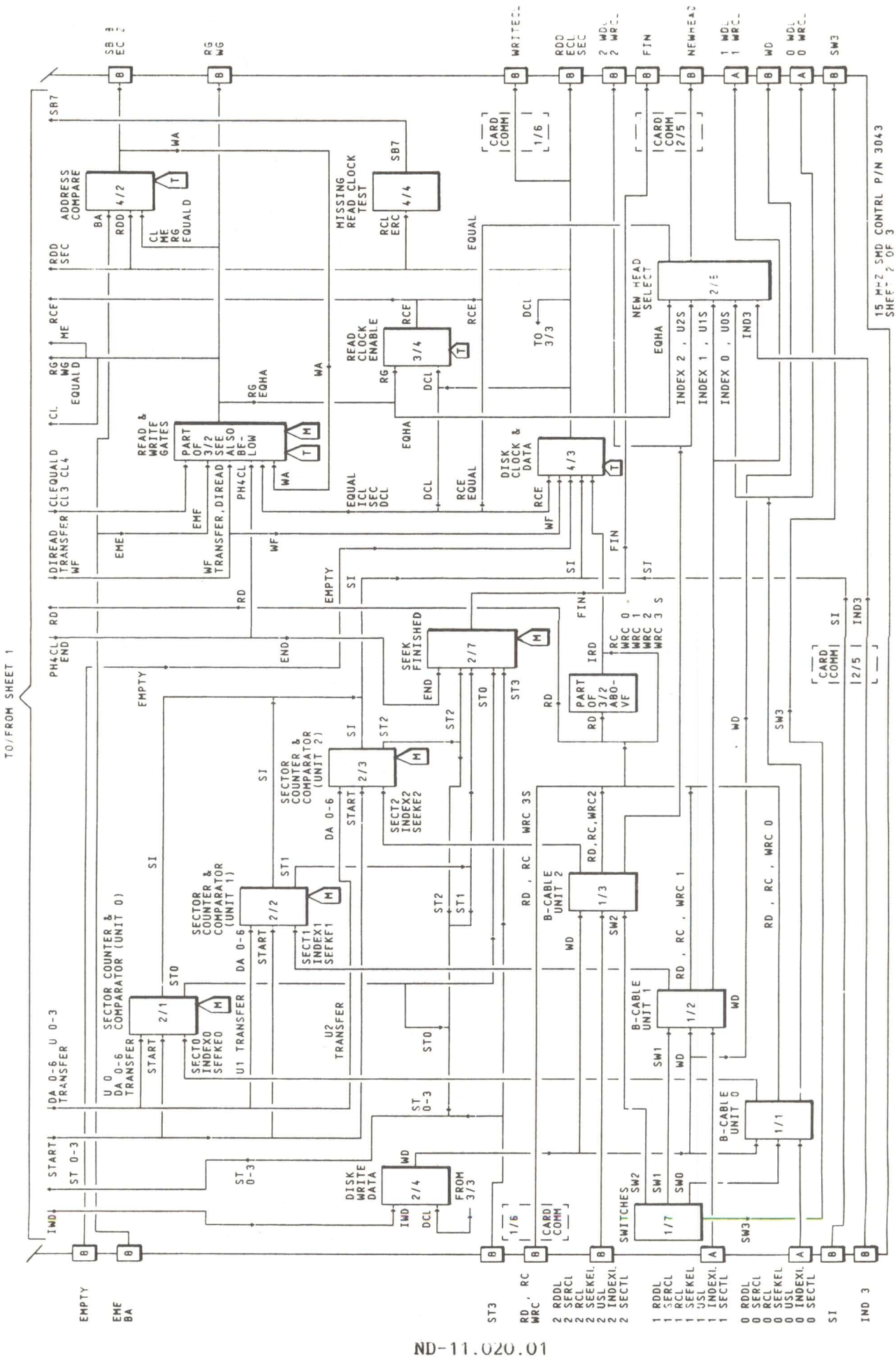
Signals	Destination Block	Function
M0	1/2, 1/3, 3/2, 5/2	Read Transfer
M1	(used in block 2/2)	Write Transfer
M2	1/3, 3/2, 5/2	Read Parity Transfer
M3	(used in block 2/2)	Compose Transfer
M123	5/2	Sum of M1, M2 and M3
M4	5/2, 5/4	Initiate Seek
M5	2/3, 2/4, 5/2	Write Format
M7	5/2	Return to Zero Seek
M8	4/1	Run ECC Operation
M9	4/1	Select Release

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043



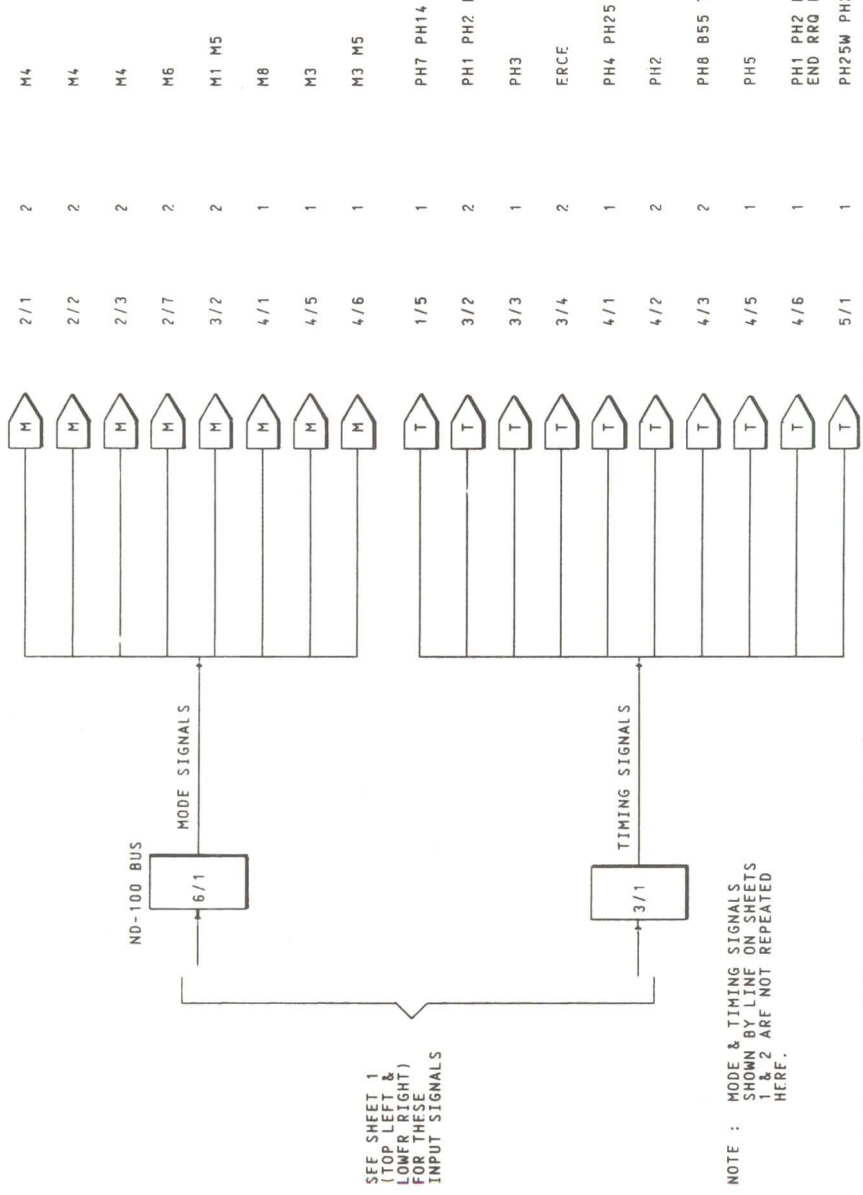
ND-11.020.01

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043


TO/FROM SHEET 1
15 MHZ SMD CONTRL P/N 3043
SHEET 2 OF 3
ADDRESS COMPARE
MISSING READ CLOCK TEST
READ CLOCK ENABLE
READ & WRITE GATES
DISK CLOCK & DATA
NEW HEAD SELECT
SECTOR COUNTER & COMPARATOR (UNIT 0)
SECTOR COUNTER & COMPARATOR (UNIT 1)
SECTOR COUNTER & COMPARATOR (UNIT 2)
SEEK FINISHED
B-CABLE UNIT 0
B-CABLE UNIT 1
B-CABLE UNIT 2
DISK WRITE DATA
SWITCHES SW2
U2 TRANSFER
U1 TRANSFER
INDEX 0 , U0S
INDEX 1 , U1S
INDEX 2 , U2S
EMPTY
EME
BA
ST3
RD , RC
SI
IND 3
ND-11.020.01

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043

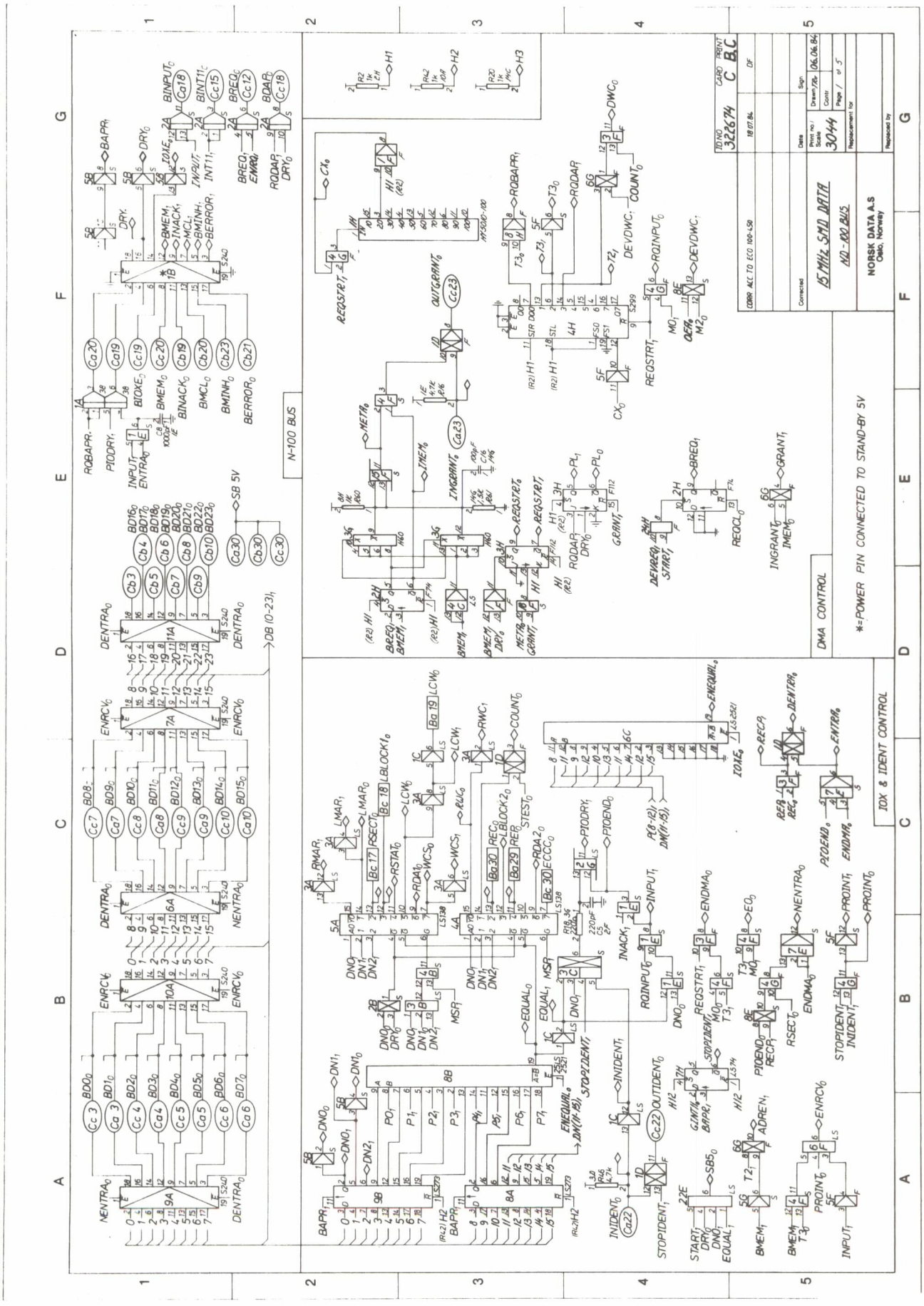


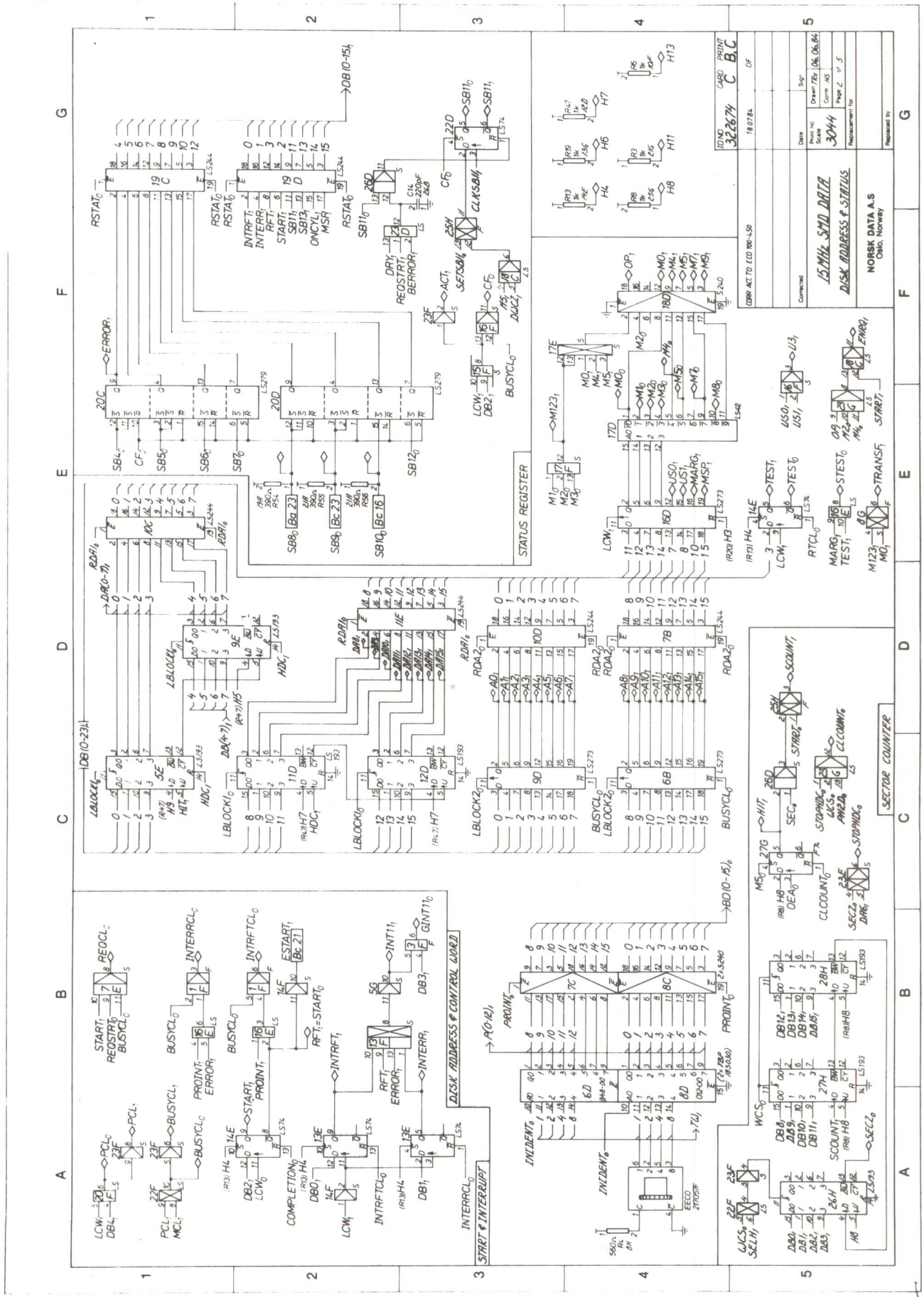
15 MHZ SMD CONTROL P/N 3043
(SHEET 3 OF 3)

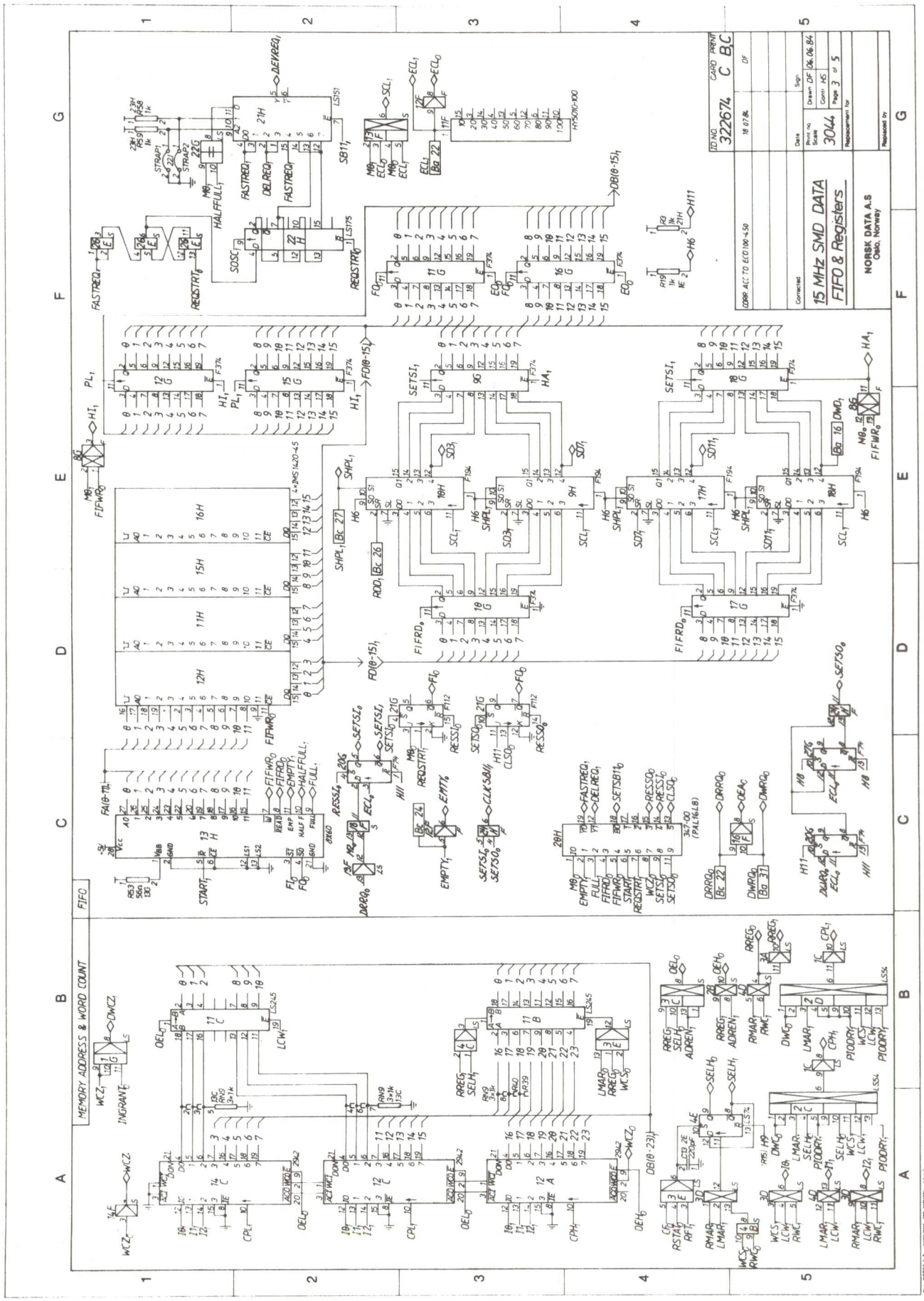
15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3043

A P P E N D I X C

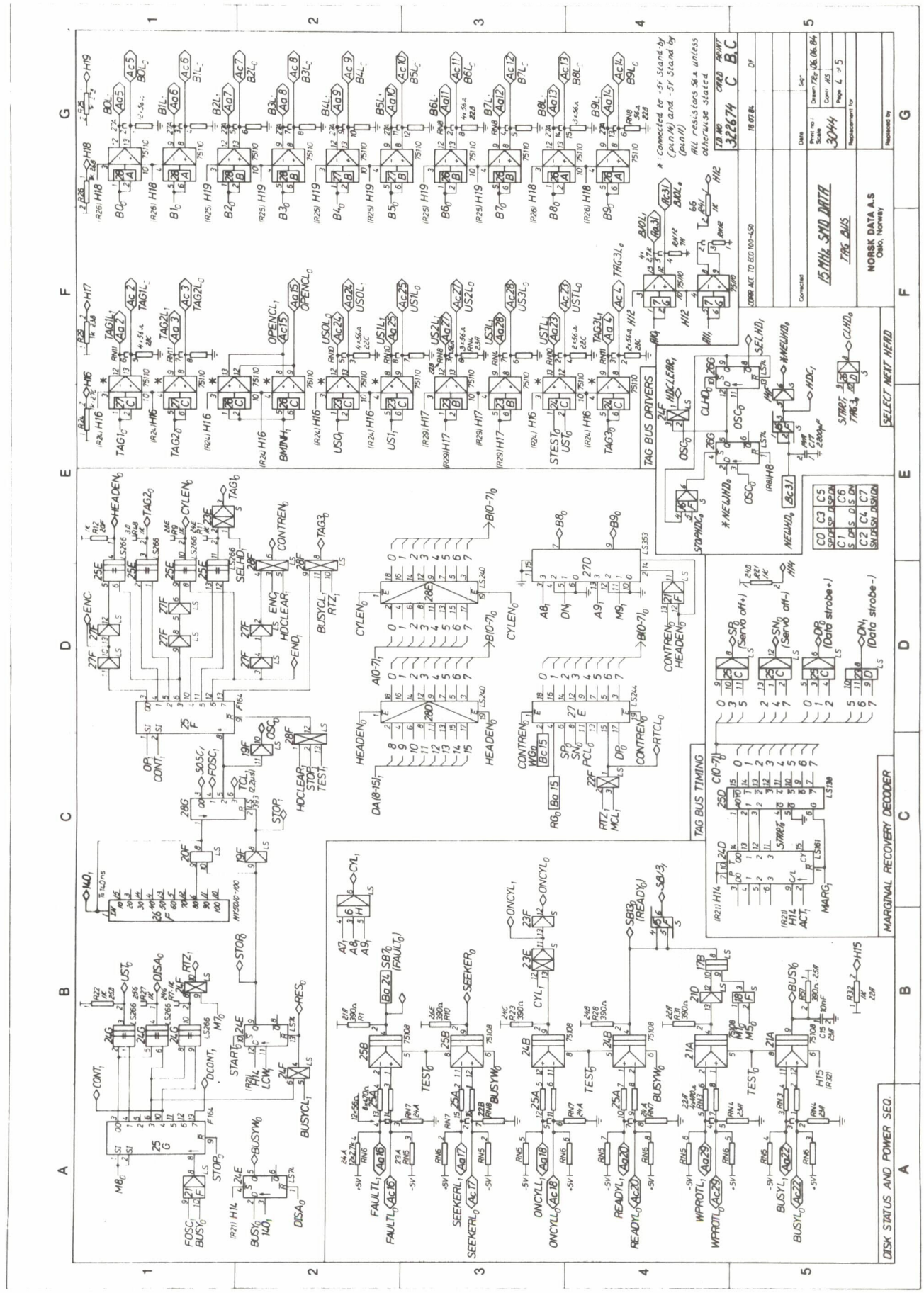
LOGIC DIAGRAM CARD NO. 3044


15 MHz SMD DATA
ND-100 BUS
NORSK DATA A.S
Oslo, Norway
3044
DMA CONTROL
IOX & IDENT CONTROL
*=POWER PIN CONNECTED TO STAND-BY 5V
N-100 BUS
>DB (0-23)1
>SB 5V

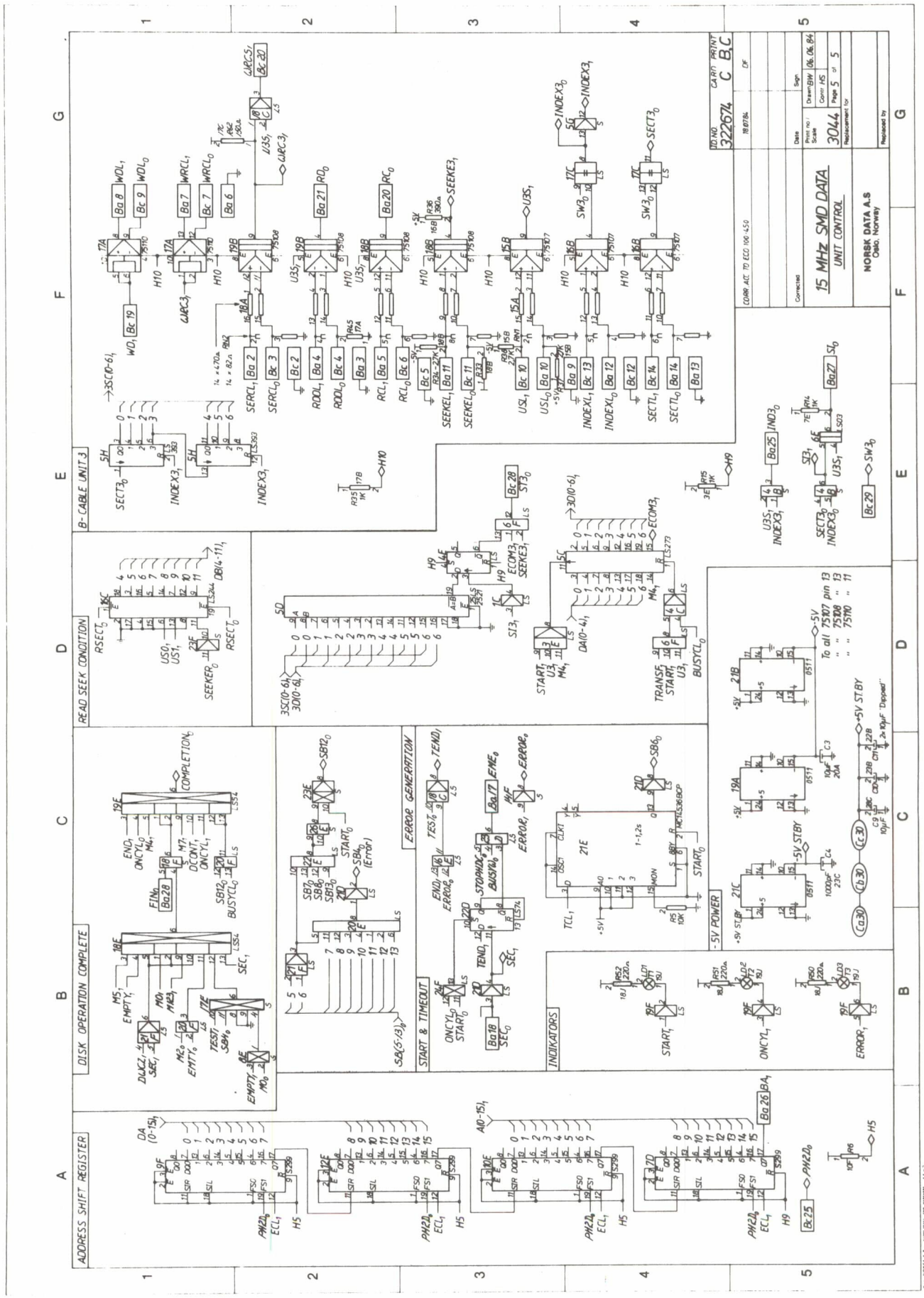

15 MHz SMD DATA
DISK ADDRESS & STATUS
NORSK DATA A.S
Oslo, Norway
3044
STATUS REGISTER
DISK ADDRESS & CONTROL WORD
SECTOR COUNTER
START & INTERRUPT


MEMORY ADDRESS & WORD COUNT
FIFO
15 MHz SMD DATA
FIFO & Registers
NORSK DATA A.S
Oslo, Norway
3044
322674
C BC

15MHZ SMD DISK CONTROLLER
LOGIC DIAGRAM CARD NO. 3044


15MHz SMD DATA
TAG BUS
3044
NORSK DATA A.S
Oslo, Norway
DISK STATUS AND POWER SEQ
TAG BUS DRIVERS
TAG BUS TIMING
MARGINAL RECOVERY DECODER
SELECT NEXT HEAD

15MHZ SMD DISK CONTROLLER
LOGIC DIAGRAM CARD NO. 3044


ADDRESS SHIFT REGISTER
DISK OPERATION COMPLETE
B-CABLE UNIT 3
READ SEEK CONDITION
ERROR GENERATION
START & TIMEOUT
INDIKATORS
-5V POWER
15 MHz SMD DATA
UNIT CONTROL
3044
NORSK DATA A.S
Oslo, Norway
3226674
C.B.C

A P P E N D I X D

DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3044

GENERAL DESCRIPTION

As explained in the manual, the 15 MHz SMD data card handles all the disk A-cable signals, plus the B-cable signals for one disk unit (No. 3). The 15 MHz SMD control card handles the B-cable signals for the remaining three disk units (0, 1, and 2). Both cards also communicate with each other and also with the NORD-100 bus. The following applies only to the 15 MHz SMD control card.

PLUG CONNECTIONS

Plug A is used for the 3-cable signals for disk units 0 and 1. The signals for unit 2are connected via plug B, which is also used for communication with the 15 MHz SMD Data card. Plug C is used for communication with the NORD-100 bus.

GENERAL LAYOUT OF THE FBD

The FBD is spread over 3 sheets, whose contents are summarized as follows :

Sheet 1 :

- o ND-100 Bus communication (block 6/1 at top left).
- o ECC Polynomial (5/1 at mid-right).
- o ECC Control (4/1 at center).
- o Bit & Phase Counters (3/1 at lower right).
- o Indicator Lamps (6/2 top center).
- o Data Compare (4/5 upper center).
- o Disk Read & Write Requests (4/6 at top center).

Sheet 2 :

- o The B-cable buffer circuits (for units 0, 1, and 2) at lower left of the sheet.
- o The 3 sector counters and comparators (for units 0,1 and 2) at upper left of the sheet.
- o Seek Finished Logic (2/7 at center).
- o Read and Write Gates (3/2 at upper right).
- o New Head Select (2/6 at bottom right).
- o Address Compare (4/2 at top right).

Sheet 3 :

- Connections of Mode Control Signals.
- Connections of Timing Signals from Bit Counter and Phase Counter.

Sheets 1 and 2 contain all the function blocks shown on the logic diagrams. Sheet 3 repeats 2 of the blocks on sheet 1 that generate the Mode Control signals (M....) and the Timing signals (mainly B.... & PH....). It also shows their connections, because it was impractical to represent these signals by lines on the FBD.

A block on sheet 1 or sheet 2 which receives Mode or Timing signals is marked with an input arrow and a letter `M' for Mode or `T' for Timing. Because the relevant block numbers on sheet 3 are in numerical order, it is easy to locate a particular block number and find out what signals the block receives.

B-CABLE AND INTER-CARD SIGNALS

All the card inputs and outputs that are connected to the B-cables (for Units 0, 1, and 2) enter or leave their corresponding B-cable logic blocks (1/1, 1/2, and 1/3 at lower left of FBD sheet 2). The B-cable signal names also end in `L', and are preceded by a number corresponding to the unit they are connected to. For example, 2 WDL (leaving block 1/3) is the Write Data for unit 2.

All other signals on plug B are connected to the 15 MHz SMD data card (3044).

ND-100 BUS SIGNALS

These signals are connected between block 6/1 (top left of Sheet 1) and plug C.

WRITE DATA PATHS

The data for writing on the disks arrives as card input DWD at the mid-left of FBD sheet 1. This data has come from the computer memory via the FIFO on the 15 MHz SMD data card (3044).

The data is gated through block 1/5, then passes down to sheet 2 as IWD. On sheet 2, it passes through block 2/4 (at mid-left) before being distributed, as WD, to each of the 3 B-cable blocks (1/1, 1/2, and 1/3) which pass it on to the appropriate disk units as XWDL (where X is 0, 1, or 2)

Note that WD also exits the card (at bottom right of sheet 2) for transmission to Unit 3 via card 3044.

Write data is also fed from block 1/5 on sheet 1 (as IWD) to the ECC polynomial via the ECC control logic (block 4/1), which it leaves as signal `I' to be checked in the polynomial for errors.

READ DATA PATHS

Data read from a disk unit enters its respective B-cable block (1/1, 1/2, or 1/3) at the bottom left of FBD sheet 2 as XRDDL (where X is 0, 1, or 2).

The read data output from blocks 1/1, 1/2, and 1/3 (which are just buffers) is combined into one signal line (RD), because data will be read from only one unit at a time.

Similarly, the data read from unit 3, which is buffered in the 15 MHz SMD data card (3044), arrives at this card (3043) also as RD, and joins the other 3 RD signals as a single input to block 3/2 (at lower center of FBD).

The read data exits block 3/2 as IRD, which passes through block 4/3 before leaving these cards as RDD, to go to card 3044 where it is transferred to memory via the FIFO.

RDD also goes to FBD sheet 1 of 3043, where it enters the ECC control block (4/1), after having been delayed in block 2/4. The read data leaves block 4/1 on signal line `I,' which enters the ECC polynomial (5/1) to be checked for errors.

ECC POLYNOMIAL

The ECC polynomial (block 5/1 at mid-right of FBD sheet 1) receives either write data or read data for error checking. This data enters 5/1 on signal line `I', and the gating of either write data (IWD) or read data (RDD) onto line `I' is done on the ECC control block (4/1 on sheet 1).

The output from the ECC polynomial consists of :

- Data outputs
- Status outputs
- Control Signal outputs

which are related to the 2 card FBDs as follows :

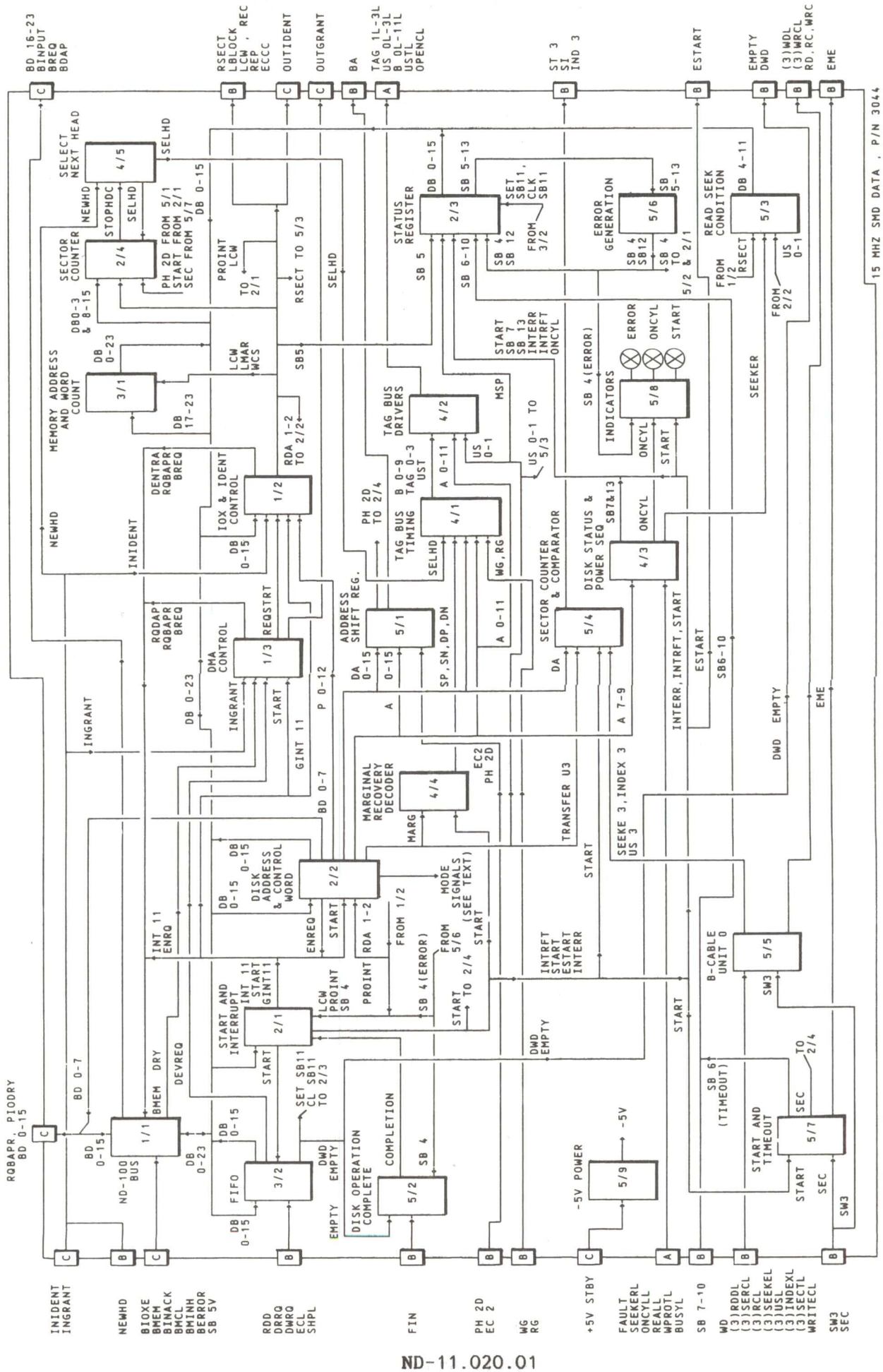
The data outputs (CC 0-13 and E 1-11) are fed to block 6/1 (on sheet 1, 3043), from which they can be read into computer memory via the BD 0-15 lines.

Two status outputs (SB7 and SB9) go out of the card and are transmitted via plug B to card 3044, where they can be read together with the other 2 SB signals from 3043 (SB 8 from sheet 2, and SB 10 from sheet 1) in the status register on card 3044.

The remaining signal outputs from 4/1 are handled on card 3043 as follows :

Two status signals (PARERR and MAXCNT) go to block 6/1 (on sheet 1), from which they can be read into memory via the BD lines, together with the Seek Complete status bits (ST 0-3) from sheet 2. The control signals from 5/1 go to blocks 1/5, 4/1 and 6/1 on sheet 1.

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3044



ND-11.020.01

15MHZ SMD DISK CONTROLLER
DESCRIPTIVE BLOCK DIAGRAM CARD NO. 3044

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Manual number: ND-11.020.01

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