Norsk Data

MPM 5
Technical Description

ND-10.004.01

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Preface:

THE PRODUCT

The Multiport Memory 5 modules described in this manual are the Twin 16-Bit Port module, the Dynamic RAM module and the Line Driver module.

The Twin 16-Bit module is the channel's entrance to the memory bank. The Dynamic RAM module is the physical storage. The Line Driver module drives signals between memory banks.

THE READER

The information in this manual is primarily intended for service personnel, system designers, hardware designers and others who require a detailed explanation of the MPM-5 modules and their functions.

PREREQUISITE KNOWLEDGE

The reader of this manual ought to be familiar with the hardware side of the ND-100 and the ND-500. It is also necessary that the reader knows the general multiport memory channel specifications.

THE MANUAL

The manual contains a hardware description of the Twin 16-Bit Port module, the Dynamic RAM module and the Line Driver module. It also contains a programming guide for the MPM-5 systems, start-up and initialization instructions and information on error messages and fault-finding.

RELATED MANUALS

ND-100 Functional Description ND-06.015 describes how the Multiport Memory Systems are integrated in the ND-100 computer systems.

ND-500 Hardware Description ND-05.011 describes the integration into the ND-500 computer systems.

Multiport Memory Channel Specifications ND-10.006 gives an introduction to the multiport memory concept, and contains interface specifications for all three multiport models.

Multiport Memory 5 Bus Description ND-10.005 describes the controller module and the internal bus in the MPM-5 systems.

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CHAPTER 1

HARDWARE DESCRIPTION

1 HARDWARE DESCRIPTION

1.1 GENERAL

This chapter describes the TWIN 16-BIT PORT module, the DYNAMIC RAM module and the LINE DRIVER module in the Multiport 5 Memory Systems, from a hardware point of view. Chapter 2 contains a programming guide for the MPM-5 Test and Maintenance Program, from which all initialization and testing of the modules are made. The program is operated from the console terminal which is connected to the maintenance processor on the controller module.

1.2 THE TWIN 16-BIT PORT

The memory port module is called a 'twin 16-bit port' because it is 2 x 16 bits wide and can be connected to both 16-bit and 32-bit width data channels. The module accepts one address cable with up to 29 address bits (addressing 32-bit words). Interface specifications are given in the Multiport Memory Channel Specifications manual (ND 10.006).

Two versions of the twin port module have been made, one with printed circuit board (PCB) number 5152 and the other with PCB number 5155. The difference between the two versions lies in the address handling.

The module is divided into two parts, described here as the ADDRESS part and the DATA part. The block diagram in Fig. 1 gives an overview of the organization of the module.

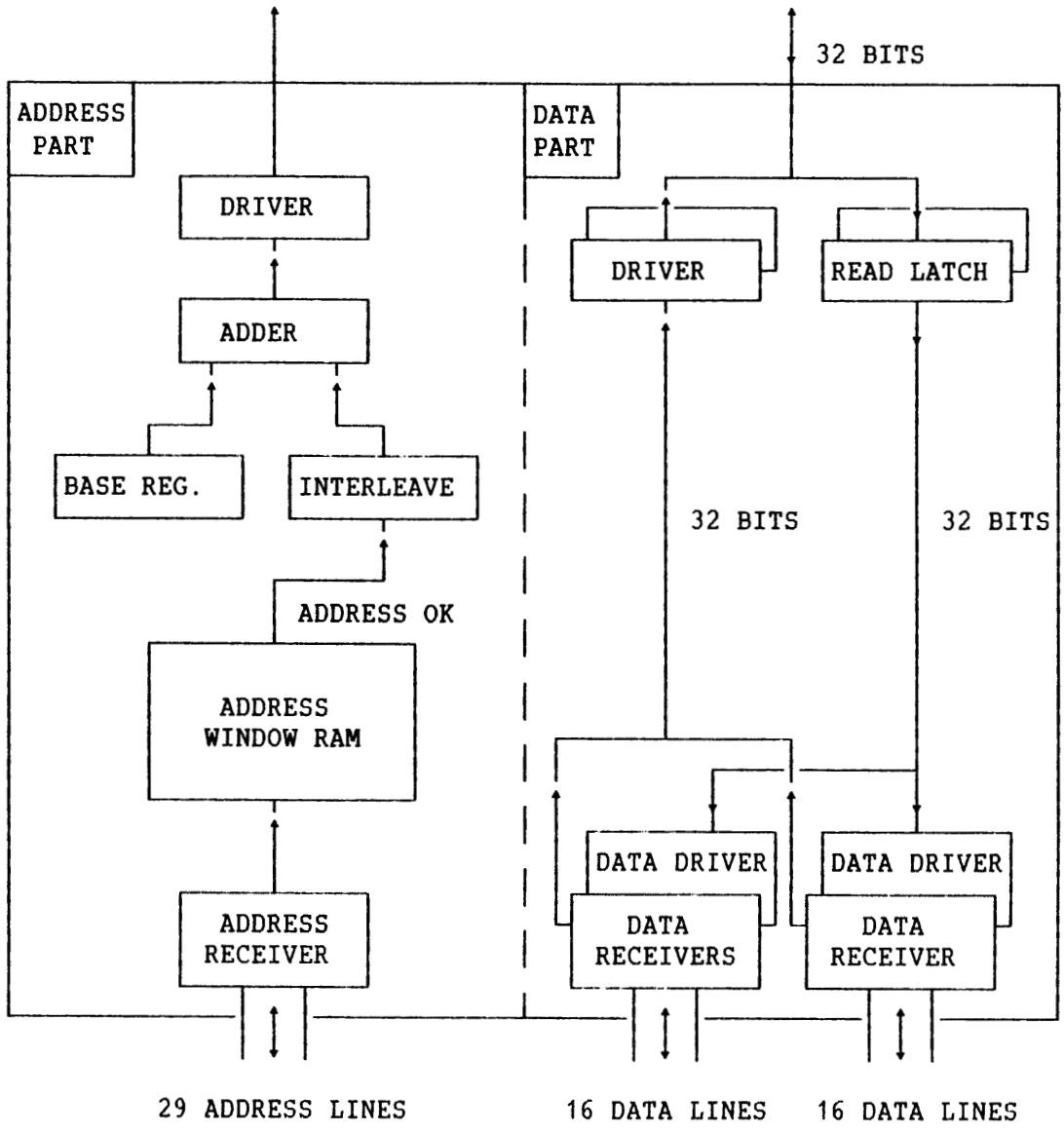


Fig. 1. Block Diagram Twin 16-Bit Port

1.3 DATA PART

The port module accepts two data cables of 16 bits each (+ 2 parity bits each). During a memory write operation, the 16 (18) or 32 (36) bits receivedare latched into a write buffer. The DATA READY signal is generated instantly, and sent back to the requesting source.

During a memory read operation, 32 bits are read from memory. 16 bits (+ 2 parity bits) are forwarded to the 16-bit sources. The ND-500 gets 32 (+ 4) bits at a time from the twin port module.

1.4 ADDRESS PART

When the source looks at the memory, it sees the total memory range of the system. The address seen from the source is called the channel address. The bank, however, has its own local address range. A conversion from channel address to physical bank address is then needed.

When 16-bit and 32-bit sources are to communicate, the 16-bit data words have to be stored as 32-bit words which can be read directly to the 32-bit sources. The interleave technique is used to manage this problem.

The differences between the two versions, 5152 and 5155, of the twin 16-bit port module are the address-window handling and the interleave possibilities. The address-window handling for the 5152 is described on page 8, and the interleave for the 5152 is described on page 13. The address-window handling for the 5155 is described on page 9, and the interleave for the 5155 is described on page 11.

The flowchart in Fig. 2 illustrates how the address handling in general is sequenced on the port module.

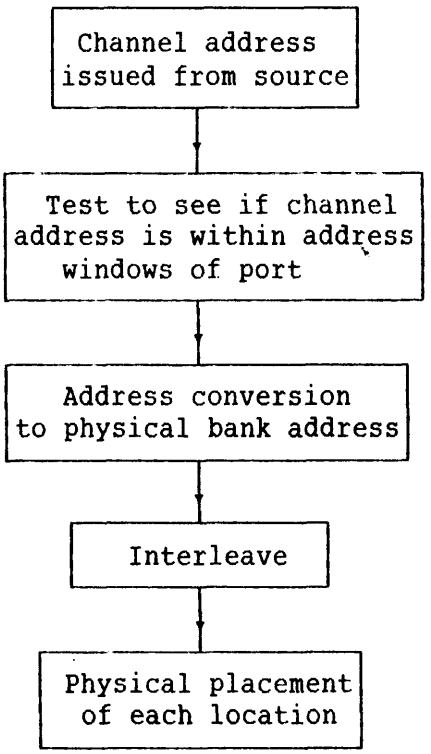


Fig. 2. Address-handling on Port Module

1.4.1 Address Windows

The address windows are used to test if the channel address is within the address range of the port. A memory port is assigned its own address range within the total range of the memory system. The addresses specified define the address range that the source sees in a memory bank. This is done by setting a lower and an upper address limit on the port with the test and maintenance program on the controller module.

The address limits define one or more address windows in the memory area of the bank. How you program the desired limits is described in Chapter 2. An illustration of how the address windows appear in the memory is shown in Fig. 3.

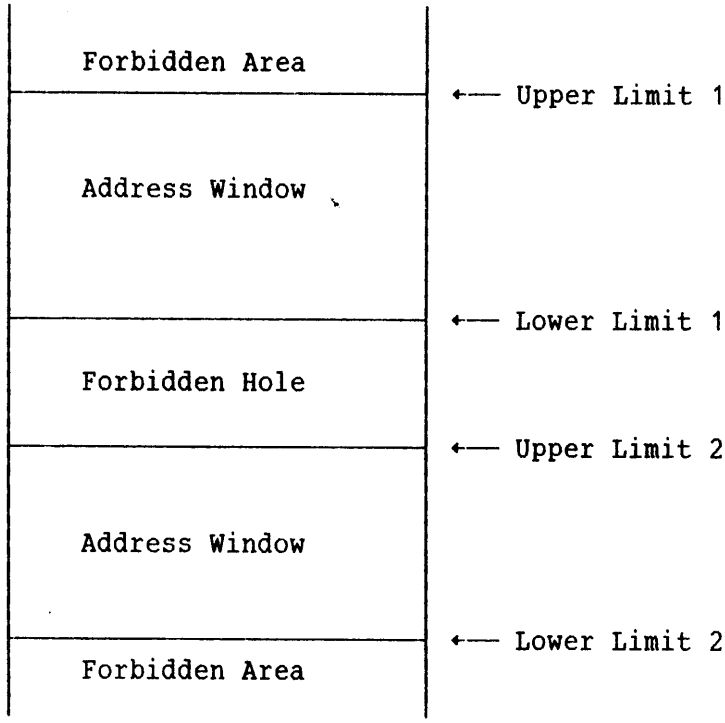


Fig. 3. Address Windows within Memory

When an address is received by the port from the memory channel, the port tests the address against its address windows. The port will respond only if the channel address is within the address range of the port. An illustration of this is given in Fig. 4.

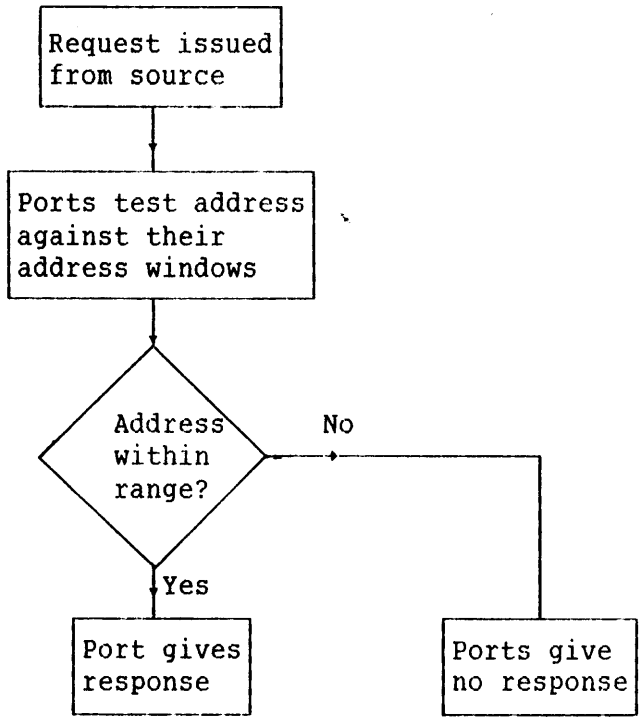


Fig. 4. Port Response to Channel Address

The way the address windows are decoded differs somewhat between the two versions 5152 and 5155. This is explained in section 1.4.2 and section 1.4.3.

1.4.2 Address Windows Decoding on the 5152

Four 4 Kbit RAMs are used to decode the address windows. The windows are contained in a look-up table giving a resolution in memory of 128 Kbyte. By keeping the addresses in a memory, it is possible to implement holes within the memory area.

Bits 17-28 in the channel address are used to find the right bit in the RAMs. Bit 29 and 30 select which of the 4 RAMs shall be used. The right RAM will respond with a '1' if the channel address is within the windows. Bit 31 in the address is not present on the channel, and therefore not decoded.

The RAMs have stand-by power, and do not need to be initiated after a power fail if the stand-by power has been on all the time.

The 16-bit data that is written into the RAMs is decoded as a 12-bit address, and a 4-bit data word. Bits 0, 13, 14, and 15 are data, and bits 1-12 are address. The address bits correspond to bits 17-28 in the 32-bit address. The four RAMs may be seen as a 16 K 1 bit memory, where each address on the channel corresponds to one bit under decoding. When the RAMs are loaded, 4 bits are written each time, with address separation 10000 octal seen from the channel. This means that when bits 1-12 (of the 16-bit data word) are all zero, bit 13 will be the content of location 0 in the 16 K 1 bit memory, bit 14 location 10000 octal, bit 15 location 20000 octal and bit 0 location 40000 octal. Example:

Lower limit = 00 004 000 000
Upper limit = 00 010 000 000

This means that locations 10, 11, 12, 13, 15, 15, 16, 17 and 20 (in the 16 K 1 bit memory) shall have content '1'. All other locations are set to '0'. When the RAMs are loaded, the 16 data bits must be:

access no.	location to be loaded (module 10000 octal)	contents of 16-bit data word
1	0	0
2	1	2
3	2	4
n	n-1	2(n-1)
6	7	16
7	10	20020
10	11	20022
11	12	20024
12	13	20026
13	14	20030
14	15	20032
15	16	20034
16	17	20036
17	20	20040
20	21	42
n	n-1	2(n-1)
10000	7777	17776

1.4.3 Address Windows Decoding on the 5155

On the 5155, two 16 K x 1 bit RAMs are used to decode the address limits. One RAM is used for decoding of LOCAL access, ie., within the MPM-5 bank, and the other RAM is used for decoding of GLOBAL access, ie., through a line driver module to other banks.

The address windows are contained in a look-up table giving a resolution in memory of 128 Kbyte. The resolution used when the port acts as a 16-bit data port is 64 Kbyte, because this is the address resolution when using 16-bit words. The LOCAL and/or GLOBAL accesses are defined in the address windows look-up table.

By keeping the addresses in a look-up table it is possible to implement holes inside the windows. Fig. 5 illustrates how the look-up table is organized.

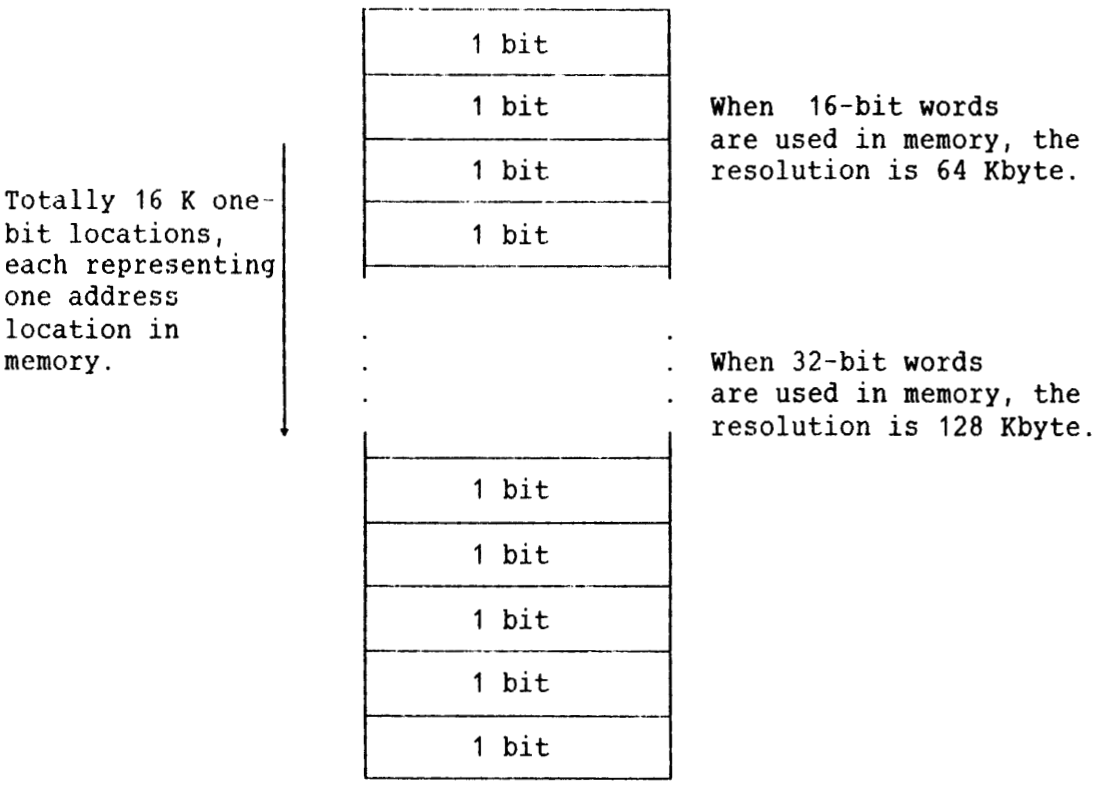


Fig. 5. Address Windows Look-up Table on the 5155

Bits 17-30 in the channel address are used to find the right bits in the RAMs. The RAMs will respond with a '1' if the channel address is within the address windows. Bit 31 in the address is not present, and therefore not decoded.

The 16-bit data that is written into the RAMs is decoded as a 14-bit address and a 2-bit data word. Bit 0 and bit 15 are data, and bits 1-14 are address. The address bits correspond to bits 17-30 in the 32-bit channel address. The RAMs may be seen as two 16 K 1-bit memories, where each address on the channel corresponds to one bit under decoding. When the RAMs are loaded, 2 bits are written each time.

1.4.4 Address Conversion

The base is essential in the address conversion. A bank has its own internal physical memory range. To convert the channel address into bank address, a base register is added to the channel address. It is the upper 16 bits of the channel address that will be justified.

It is important to distinguish between the base and the base register. The base is the start address, which means the first physical address in the bank, and it has an increment of 128 Kbyte. When programming the port, the start address is the parameter that has to be used. But the value which is placed in the base register by the program, is 2's complement of the base subtracted from lower limit. Example:

Lower limit = 00 004 000 000
Base = 00 000 400 000

use only 16 bits means

Lower limit = 000020
Base = 000002

Lower limit - base = 000016

2's complement of 000016 gives

Value of the base register = 377762

1.4.5 Interleave

The purpose of the interleave is to site subsequent channel addresses in different hardware parts. This makes the bandwidth increase, because a new request can be issued before the preceding one is served. It also enables for wide-channel (more than 16 bits) communication, because the whole width can be read at a time.

The interleave is performed by shifting the channel address bits a number of positions to the right. The bits shifted are compared to registers at the port module. The channel address locations are directed to separate hardware parts, depending on the valueof the shifted address bits. There are several interleave types, with a different number of address bits shifted, as shown in Fig. 6.

Interleave type:	Address bits shifted:
0 way	(not shifted)
2 way	one position to the right
4 way	two positions to the right
8 way	three positions to the right

Fig. 6. Interleave Types

If we consider two-way interleave, the interleave function has to work so that subsequent addresses enter alternating ports. When one address is let through in port 0, the next address is let through in port 1, the subsequent address in port 0, and so on. When the address has been accepted by the port, the port has to decide in which half of the 32-bit memory the 16-bit word is to be placed. This is done by checking the least significant bit in the address. Odd addresses are placed in one part, even addresses in the other. This is illustrated in Fig. 7.

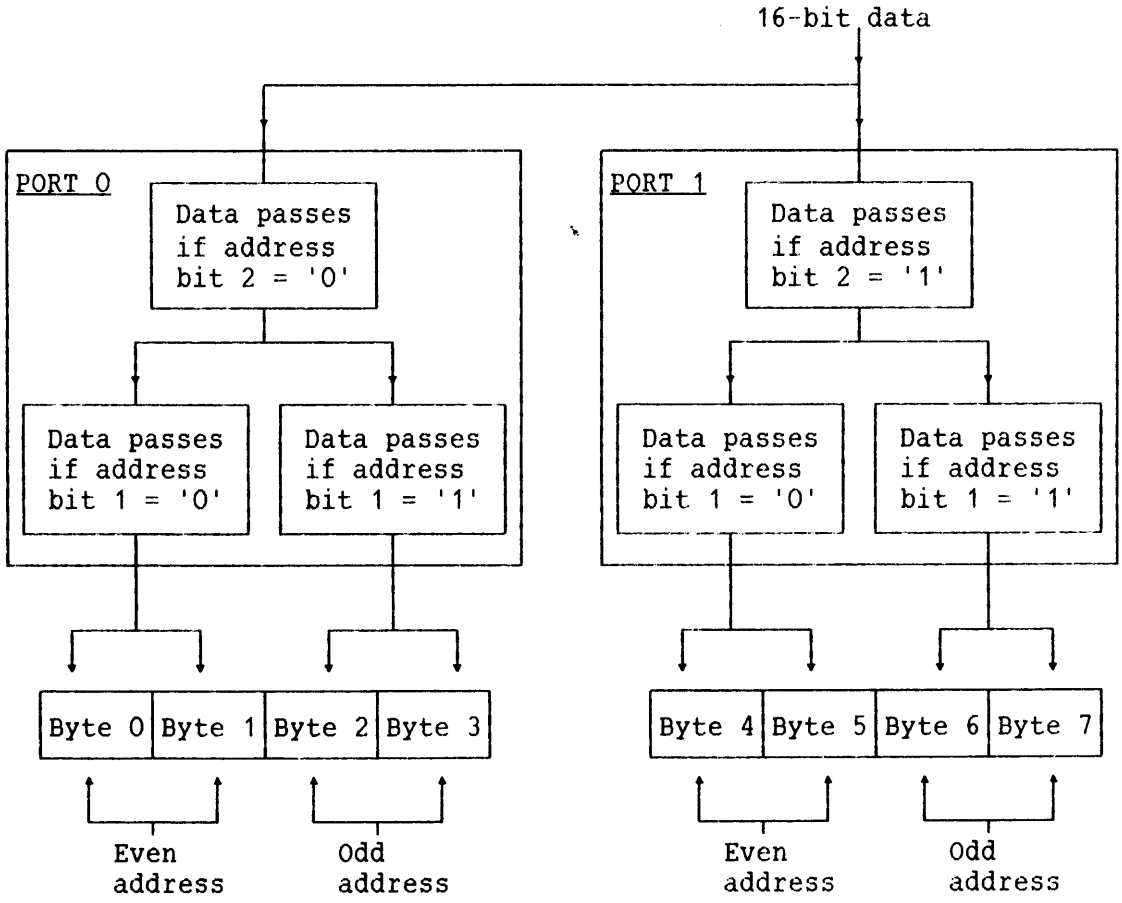


Fig. 7. Port Action with Two-way Interleave

The interleave organization depends upon the computer system configuration. In an ND-570 system with a 64-bit wide cache memory and with the twin-port version 5152, the standard interleave PROM on the 5152 has to be replaced by a special interleave PROM. The PROM has position 21H on the printed circuit board.

In an ND-570 system with a 32-bit wide cache memory, and in all other systems with the 5152 version, the standard interleave prom is kept.

Systems may also have the twin-port version 5155 instead of the 5152 version. The 5155 has a special ALLOW bit in the master control register, which is described in page 16. With this bit it is possible to change from 32-bit interleave (ND-570 with 64-bit wide cache) to 16-bit interleave (all other systems). It is then not necessary to change the interleave PROM.

The interleave configurations possible are shown in Fig. 8. The three bits in the two leftmost columns refer to the port control register described in page 17. The interleave type refers to the shifting of address bits. The bank interleave refers to the physical placement of each location.

Port Control Reg.		INTERLEAVE CONFIGURATIONS		
Bit 1 0	Bit 6	Interleave Type	Configuration with Standard PROM (34200)	Configuration with Special PROM
0 0	0	0 way	Not used.	Not used.
0 1	0	2 way	16-bit channel, 1-bank interleave.	16-bit channel, 1-bank interleave.
1 0	0	4 way	16-bit channel, 2-bank interleave.	16-bit channel, 2-bank interleave.
1 1	0	8 way	16-bit channel, 4-bank interleave.	16-bit channel, 4-bank interleave.
0 0	1	0 way	32-bit channel, 1-bank, no bank interleave.	
0 1	1	2 way	32-bit channel, 2-bank interleave.	64-bit channel, 2-bank, no bank interleave.
1 0	1	4 way	32-bit channel, 4-bank interleave.	64-bit channel, 4-bank interleave.
1 1	1	8 way	32-bit channel, 8-bank interleave.	

Fig. 8. Interleave Configurations on the Twin 16-Bit Port

1.5 CONTROL AND TEST REGISTERS

The port has several registers that may be programmed from the MP-bus controller, or from another device that generates control signals for I/O functions on the MP-bus. The registers are used in control and test procedures and can be divided in two groups, one used in WRITE operations and the other in READ operations on the MP-bus. The registers are as follows:

WRITE COMMANDS

Register	Meaning	Bits
Test request	Starts a test request. Test bit in status register must be set if a request is to be generated.	-
Master Control	General control information.	8
Port Control	Specific control information on each port.	8
Base	Address for generation of physical bank address from the channel.	16
Windows	Windows that define the address range of a port.	16
Display	For display of windows, base and, if interleave, port number.	16
Test address	Address indicating which address	
lower part	in the memory the test request	16
upper part	is to activate.	16
Test data	Data to put into the memory	
lower part	during a test request.	16
upper part		16

READ COMMANDS

Register	Meaning	Bits
Slot identification	Information on the module in the slot.	16
Master status	General status information.	8
Port status	Specific status information on each port.	8
Test data	Data read by a test request. Same	32
Test data	data in both registers.	32

A more detailed description of the registers is given in section 1.5.1 through section 1.5.6.

1.5.1 Test Request

A write access on this address starts a request to the MP-bus from the port. The address on the MP-bus is the one that is put into the test address register. The cycle will be a read/write cycle, and the write data is taken from the test data register. Read data is placed in the same register. Only one test request will be executed after access on this address.

NOTE! The test bit (bit 3) in the master control register must be set to '1' before the desired test request, otherwise the request will not be executed.

1.5.2 Master Control Register

The bits of the master control register have the following meaning:

Bit 0 If = '0', inhibits all requests from the port on the MP-bus. If the request is coming from the channel, no address ready or data ready signals will be returned.

1 If = '1', super test is performed.

2 If = '1', disables address bits 24 through 28, ie., the address bits not supplied by old ND equipment.

3 Test, - must be set before a desired test request and before loading the address windows. When normal operation is wanted, the test bit must be set to '0'.

4 This bit has different functions on 5152 and on 5155.

On 5152: Local bit under request, '1' indicates if local access is wanted. At least one of the bits 4 and 5 must be set to '1'.

On 5155: ALLOW bit. When = '1', it allows for access from an ND-500 with a 32-bit wide cache memory. When it = '0' it allows for access from an ND-500 with a 64-bit wide cache memory.

5 This bit is not used on 5155. On 5152: Global bit under request, '1' indicates if global access is wanted.

6 Inverted write parity check, '1' means no parity check on write.

7 Not used.

1.5.3 Port Control Register

The bits of the port control register have the following meaning:

Bit 0 Interleave type bit 0.

1 Interleave type bit 1.

2 Bank number if interleave, bit 0.

3 Bank number if interleave, bit 1.

4 Speed-up bit 0.

5 Speed-up bit 1.

6 If = '1', 32-bit (ND-500) data channel. If = '0', 16-bit (ND-100) data channel.

7 Wait, disable write queue (buffered write).

Bits 0 and 1 generate the desired interleave type. The effect of the bit settings is shown in the table in Fig. 9, which is the same figure as Fig.8.

Effect of Interleave Type Bit Settings				
Bit 1 0	Bit 6	Interleave Type	Configuration with Standard Prom	Configuration with Special Prom
0 0	0	0 way	Not used.	Not used.
0 1	0	2 way	16-bit channel, 1-bank interleave.	16-bit channel, 1-bank interleave.
1 0	0	4 way	16-bit channel, 2-bank interleave.	16-bit channel, 2-bank interleave.
1 1	0	8 way	16-bit channel, 1-bank interleave.	16-bit channel, 4-bank interleave.
0 0	1	0 way	32-bit channel, 1-bank, no interleave.	
0 1	1	2 way	32-bit channel, 2-bank interleave.	64-bit channel, 2-bank, no interleave.
1 0	1	4 way	32-bit channel, 4-bank interleave.	64-bit channel, 4-bank interleave.
1 1	1	8 way	32-bit channel, 8-bank interleave.	

Fig. 9. Effect of Interleave Type Bit Settings

Bits 2 and 3 decode and enable the right bank. With 2-bank interleave, bit 2 decodes the bank that has access. With 4-bank interleave bits 2 and 3 decode the bank that has access. This is illustrated in Fig.10.

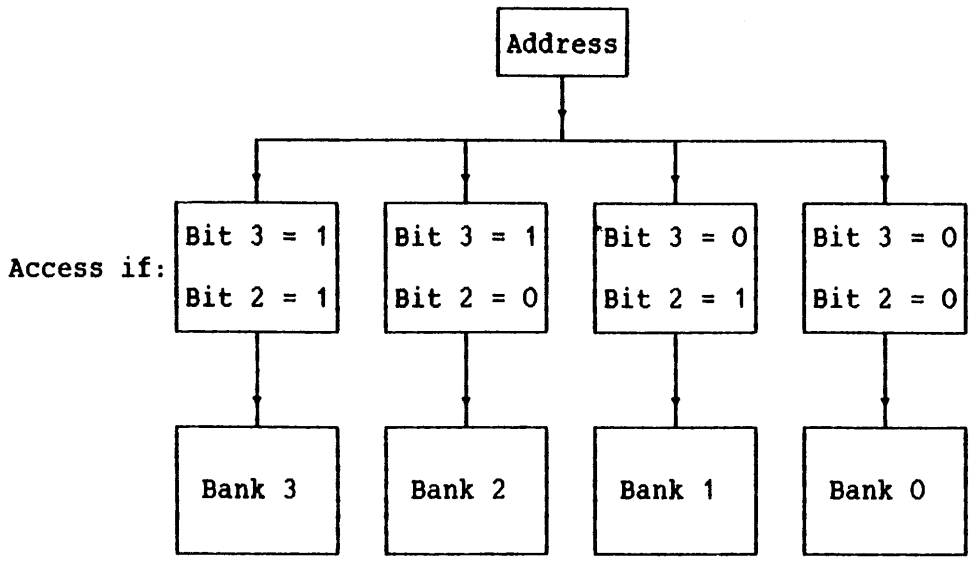


Fig. 10. Decoding of Interleave Bank Number

Bits 4 and 5 are called 'speed-up'. They may be used if the addresses from the channel sources are stable before request is sent. The table in Fig.11 shows the effect of the different speed-up bit settings.

Bit 5 4	Delay (ns)	Address stable before Request (ns)	Typical Channel Source Type
0 0	10	30	ND-100 CPU without DMA
0 1	30	10	
1 0	40	0	ND-100, ND-500
1 1	60	-20	MPM-5 Line Driver

Fig. 11. Effect of Speed-up Bit Settings

Bit 6 must be '0' when a 32-bit channel is connected and '1' when a 16-bit channel is connected.

Bit 7 is called 'wait', and must be used if the channel source makes a pulsed request (which is not found on ND equipment). With the wait bit set, the channel waits until the port has access to the MP-bus during a write cycle. This is not necessary if the request is turned off after an address ready.

1.5.4 Test Address

The address used during a test request may be written into the test address register. The address has a length of 32 bits, and is read from the MP-bus controller. It must be written in two steps, 16 bits each time.

1.5.5 Test Data

The write data that has to be used during the test request must be placed in this register before the request. After a test request a 32-bit word can be read out. The test request is a read/write cycle.

1.5.6 Base

The base for calculating the physical bank address on the MP-bus must be placed in this register.

1.5.7 Address Windows

For 5152: Four 4 Kbit RAMs are used in decoding the address windows. 16-bit data is written into the RAMs, and decoded as a 12-bit address and a 4-bit data word. The four RAMs may be considered as a 16K x 1 bit memory, where each address on the channel corresponds to one bit in the memory.

For 5155: Two 16 K x 1 bit RAMs are used in decoding the limits, one for global access and the other for local access. Each channel address corresponds to one bit in memory.

1.5.8 Display

The display register is used to load 16 different 7-segment displays at the card edge. All 16 displays are loaded with the same address. In the necessary 8-bit data word, bits 0 - 3 describe the value to

be displayed and bits 4 - 7 indicate which display to load.

NOTE! Bits 0-3 are in 1's complement representation.

The displays are listed in the table in Fig.12.

Display No.	Meaning (all values are octal)
0	Lower limit, most significant digit
1	Lower limit
2	Lower limit
3	Lower limit
4	Lower limit, least significant digit
5	Upper limit, most significant digit
6	Upper limit
7	Upper limit
8	Upper limit
9	Upper limit, least significant digit
10	Base, most significant digit
11	Base
12	Base
13	Base, least significant digit
14	Set 15 octal (will blank the display)
15	Port number when interleave is used

Fig. 12. Displays loaded through the Display Register

NOTE! The displayed base value is not the value of the base register, but that which was used to calculate the value of the base register.

1.5.9 Slot Identification

This register gives information on slot position and module type. The different bits have the following meaning:

Bits 0 - 3	Give the model of the module
4	Always '1'
5 - 10	Give the module type
11 - 15	Give the slot position

1.5.10 Master Status Register

The different bits of the master status register have the following meaning:

Bit 0	Inhibit, read-back from write register
1	Master request
2	Bus ready
3	Test, read-back from write register
4	Local, read-back from write register
5	Global, read-back from write register
6	WCHK, read-back from write register
7	Not used.

Bit 1 indicates that the port is waiting to execute.

Bit 2 is set to '1' when the port is reading data from the bank. If you try to write to the port from the MP-bus, an error will be the result. Read is allowed.

Bits 0, 3, 4, 5 and 6 are read-back from the same bits in the write register.

1.5.11 Port Status Register

All bits in this register are read-back from the port control register.

1.5.12 Test Data

The 32-bit test data is read on both addresses.

1.6 THE DYNAMIC RAM MODULE

The Dynamic RAM module (print number 5411) can be equipped to give 2 different models:

1) 1 Mbyte (4 rows with 64 K x 1 bit memory chips)

2) 4 Mbyte (4 rows with 256 K x 1 bit memory chips)

The module has 32-bit data width plus 7 correction bits. The correction code is a modified hamming code, which is able to correct single errors and detect multiple errors. When errors occur, the maintenance processor updates an EEPROM (the error memory) on the memory module. The error memory is a non-volatile 2 K x 8-bit memory that contains a log of the errors occurring on the specific memory module.

The module accepts single bytes during a write operation. A read-modify-write cycle is then performed internally on the module, because the correction code is different when single bytes are written.

The memory range of the module is defined by a lower address limit and an upper address limit, which together give the size of the module. The lower address limit and the size of the module are supplied from the maintenance processor.

The start address, which is the lower address of the module, is programmed from the maintenance processor. The upper address is calculated by the module itself. The lower address and the size of the module are displayed on the card.

1.7 DYNAMIC RAM REGISTERS

The dynamic RAM module has several registers which are programmed from the maintenance processor. The registers are as follows:

- Slot Identification
- RAM Control
- Lower Limit
- Display Memory
- Error Memory Address
- Error Memory Data
- Suppress Error Table

1.7.1 Slot Identification

This register is used in read operations. The different bits have the following meaning:

Bits 0 - 10: Type and Model Code

Bits 11 - 15: Slot Code

1.7.2 RAM Control Register

This register determines the special modes in which the module can be operated. The different bits have the following meaning:

Bit 0 = '1' means disable error correction.

Bit 0 = '0' means enable error correction if manual disable switch is also turned off. Green LED is lighted.

Bit 1 = '1' means enable suppression of error reporting. When pression is active, previously detected single bit errors are not reported.

Bit 1 = '0' means report all errors detected.

Bit 2 = '1' means disable memory access to this module without

regard to the limit register.

Bit 2 = '0' means enable memory access from this module.

Bit 3 = '1' means disable writing into correction bits. Used for maintenance only, to check operation of error correction network.

Bit 3 = '0' means normal operation.

1.7.3 Limit

This register contains the lower address limit of the module, and must be programmed according to the module size which is 1 Mbyte or 4 Mbyte. The different bits have the following meaning:

1 Mbyte: Bits 0 - 3 = '0', Bits 4 - 15 = Limit in 1 Mbyte units.

4 Mbyte: Bits 0 - 5 = '0', Bits 6 - 15 = Limit in 4 Mbyte units.

1.7.4 Display Memory

The display always shows the lower limit in 256 Kbyte units. The limit will therefore range from 0 to 37777, placed in the five rightmost digits of the display. The left digit shows the size of the module in 256 Kbyte units:

1 Mbyte module ⟶ left digit shows 4

4 Mbyte module ⟶ left digit shows 6

The format of the display memory is as follows:

Bit 0 - 3: Digit value, octal format is default, any format is possible.

NOTE! The value must be inverted before it is written out!

Bit 4 - 6: Digit number. The leftmost is number 0, the rightmost is number 5.

1.7.5 Error Memory Address

The address of the desired memory byte can be loaded into this register. Note that the register is reset to 0 after about 1 second, because the contents of the slot identification register have to be displayed as status information. The different bits have the following meaning:

Bits 0 - 10: Address bits.

Bit 11: = '1' means write enable. Prepares the contents of the Error Memory Data register to be written into the chip. To do the actual transfer, a programming pulse must be sent separately from the universal timer of the maintenance processor.

= '0' means normal read operation.

1.7.6 Error Memory Data

This data register contains the value to be written into the error memory.

Bits 0 - 8: One byte of data.

1.7.7 Suppress Error Table

This table is loaded with the errors detected by the error code. This means that a specific error is only reported the first time it is detected. This of course only concerns single-bit correctable errors. Fatal errors have to be reported each time (although it is possible to suppress them).

The different bits have the following meaning:

Bits 0 - 6: Error code (syndrome code) 0-127 (decimal). The significance of the codes is listed on page 69.

Bits 7 - 8: Section number showing for which of the four memory rows the error code is valid .

Bit 9: When = '1': Suppress error messages from chip pointed out by bits 0 - 8.

When = '0': Report error messages in chip pointed out by bits 0 - 8.

1.8 THE LINE DRIVER MODULE

The line driver module has printed circuit (PCB) number 5154. The function of the module is to drive signals between banks. It is thus only used in multibank configurations. The transmitters and receivers have differential lines conforming to the RS 422 standard. Fig. 13 shows the main principles of the module.

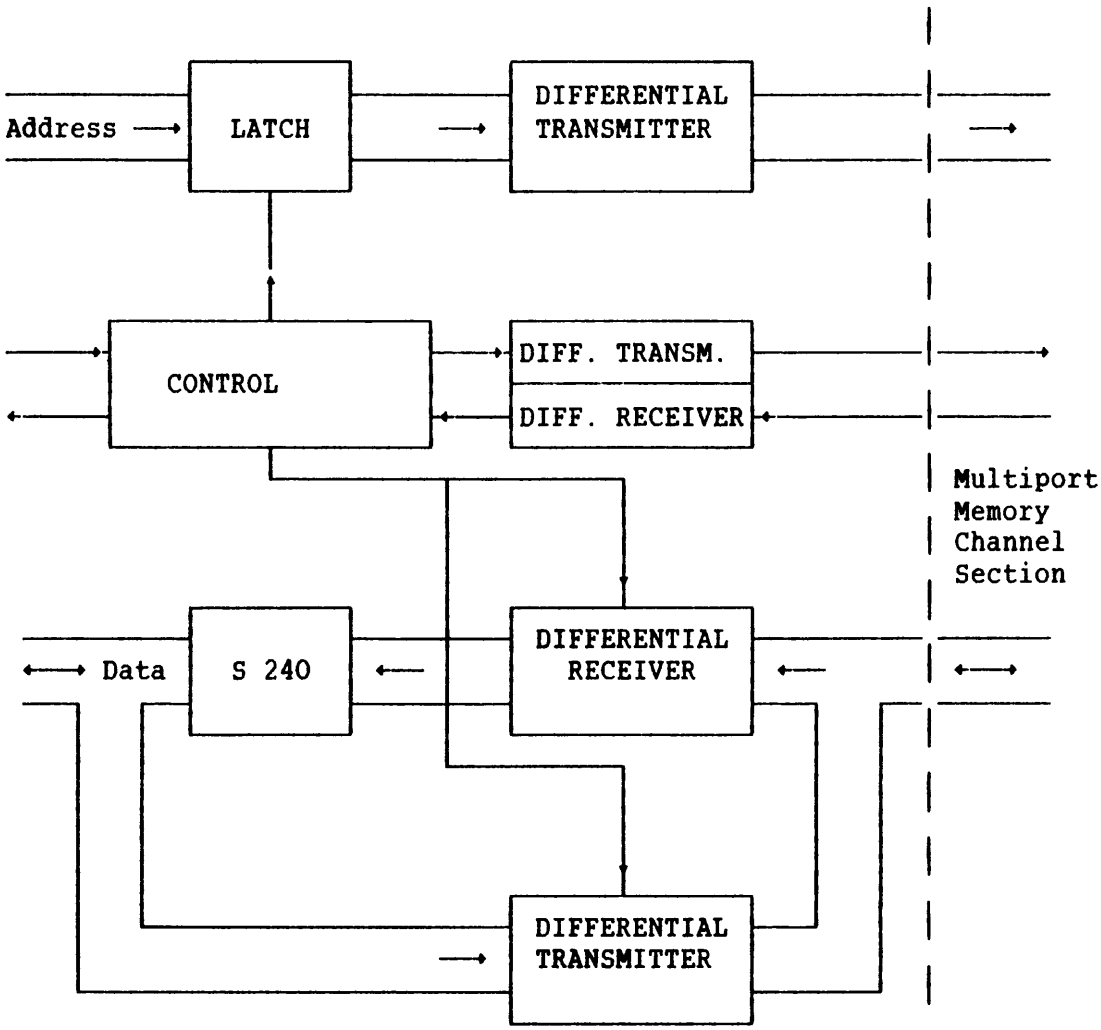


Fig. 13. The main Principles of the Line Driver Module

CHAPTER 2

PROGRAMMING GUIDE FOR THE MPM-5 SYSTEM

2 PROGRAMMING GUIDE FOR THE MPM-5 SYSTEM

2.1 GENERAL

All the registers on the port module and the dynamic RAM module are programmed from the Multiport-5 Test and Maintenance Program. This program appears at the console terminal connected to the controller module.

The Test and Maintenance Program is always present at the console terminal. If the console is a CRT-terminal and the screen is empty, push the return key and the prompt > will appear. When you see the prompt >, you can give commands to the program.

The program has 22 different commands, which are explained in this chapter. The commands can be abbreviated in the same way as SINTRAN commands. The parameters can be separated by space or comma. If the commands are not followed by parameters, the parameters will be prompted.

NOTE! The MPM-5 Test and Maintenance Program requires UPPER CASE position on the console terminal.

Control characters can be used for command editing. They are as follows:

CTRL A: Delete one character.

CTRL C: Copy one character.

CTRL D: Copy rest of line including RETURN.

CTRL S: Stop print-out on screen (only XON/XOFF terminals)

CTRL Q: Start a new empty line where the old command can be edited

After CTRL S: Start print-out on screen (only on XON/XOFF terminals)

If you want to perform a software reset on the program, type

CTRL X

The MPM-5 memory will then be initiated, as after a WARM start.

In the following, all inputs to the program are underlined. Carriage return/line feed is illustrated with ↵.

The format of the communication between the controller module and the console terminal is 7 data bits and 2 stop bits.

The following sections explain all the commands and their parameters. Examples are given when necessary.

2.2 HELP

This command lists all commands with parameters. Just type:

>HELP↵

2.3 CONFIGURATE-SLOT

Parameter: Slot number

With this command, it is possible to configurate the MPM-5 system. The parameters conform to the registers described in Chapter 1. When the command is given, the program answers with a list of the modules in the bank and in what slot they are sited. Then SLOTNO is prompted, and the desired slot number may be entered. The configuration can now be performed. The example below shows exactly how the program will respond on the console terminal when the command CONFIGURATE-SLOT is given. In addition, comments to the program are given in separated areas.

Example:

```
>CONFIGURATE-SLOT↵

   M O D U L E S   I N   T H I S   B A N K
==========================================================================
SLOT NO.   05  :  DYNAMIC RAM -  1 MB (64KB DEVICES)
SLOT NO.   12  :  TWIN 16-BIT PORT (5155)
SLOT NO.   13  :  MPM-5 BANK CONTROLLER

SLOTNO:5↵

SLOT NO.   05  :  DYNAMIC RAM - 1 MB (64KB DEVICES)

           Comment: This module is described on page 24.

LOWER LIMIT (256 KBYTE INCREMENT (OCTAL)):0↵

RAM CONTROL REG.:0↵

           Comment: Refer to the bit explanation on page 25.
                    The value 00B means that
                  - error correction is  enabled,
                  - suppression of error reporting is disabled,
                  - memory access to this module without regard
                    to the limit registers is  enabled and
                  - writing into correction bits is enabled.

SAVE(YES/NO):YES↵

           Comment: If the answer is YES, the configuration
                    parameters are saved both in the non-volatile
                    memory in the backplain and in the registers
                    on the specified module. If the answer is NO,
                    they are stored only on the module.

- WRITING TO NONVOLATILE MEMORY, PLEASE WAIT -

SLOTNO:12↵

SLOT NO.   12  :  TWIN 16-BIT PORT (5155)

EXPLAIN PORT PARAMETERS (YES/NO):YES↵
Memory areas are opened for access by giving LOWER and UPPER
LIMITS. Several non-overlapping areas are allowed.
START ADDRESS is the first physical address in the MPM-memory.
LIMITS and START ADDRESS are in modules of 128 KByte (0=0B,
1=400000B, 2=1000000B,..., n=n*400000B).
```

```
DATALENGTH is 16 or 32 bits.
INTERLEAVE TYPE is 0, 2, 4 or 8.

LOWER LIMIT:0↵

UPPER LIMIT:000020B↵
```

Comment: These values for lower and upper limits mean that the address window starts from address 0 and ends at address 000017B, inclusive.

```
ACCESS (LOCAL=1, GLOBAL=2, BOTH=3):1↵
```

Comment: Local means only within the bank. Global means outside the bank.

```
MORE LIMITS (YES/NO):N↵
```

Comment: If holes inside the memory are wanted, add more limits.

```
START ADDRESS:0↵
```

Comment: The start address conforms to the base, described on page 11.

```
DATALENGTH (16, 32):16↵
```

Comment: The data length refers to bit 6 in the port control register, described on page 17.

```
INTERLEAVE TYPE (0, 2, 4, 8):2↵
```

Comment: Interleave type 1 means that you have a 16-bit channel and 1-bank interleave. The interleave type refers to bit 0 and bit 1 in the port control register, described on page 17.

```
INTERLEAVE PORT NUMBER (0-3):0↵
```

Comment: The interleave port number refers to bit 2 and bit 3 in the port control register, described on page 17.

```
REQUEST DELAY IN NS (10, 30, 40, 60):40↵
```

Comment: The request delay refers to bit 4 and bit 5 in the port control register, described on page 17.

```
BUFFERED WRITE (YES/NO):YES↵
```

Comment: Buffered write means that, when doing a write cycle, data ready is sent back as soon as the data is latched into the port, but before the MPM-5 cycle is finished.

```
MASTER CONTROL REG. (RETURN = DEFAULT):↵
```

Comment: The master control register is described on page 16.

```
SAVE (YES/NO):YES↵

- WRITING TO NON-VOLATILE MEMORY, PLEASE WAIT -

SLOTNO:13↵

SLOT NO.    13   : MPM-5 BANK CONTROLLER
```

Comment: This module is described in the manual MPM-5 Bus Description (ND-10.005)

```
TIMEOUT (2-40 MIC. SEC.):3↵

MAINTENANCE CONTROL REG.(RETURN = DEFAULT):↵

ERROR INVESTIGATOR ON? (YES/NO):YES↵

REPORT 1-BIT ERRORS? (YES/NO):YES↵

NEW BAUD RATE? (YES/NO):NO↵

- WRITING TO NON-VOLATILE MEMORY, PLEASE WAIT -
```

The configuration is now finished.

2.4 LIST-CONFIGURATION

Parameter: Slot number

This command lists the contents of a specified slot in the bank. When the command is given, the program responds as in the following example. The configuration is the same that was created in the CONFIGURATE-SLOT example.

Example:

```
>LIST-CONFIGURATION↵

SLOTNO:5↵

SLOT NO.  05 : DYNAMIC RAM -  1 MB (64KB DEVICES)

LOW LIMIT OF RAM      : 000000B

RAM CONTROL REGISTER : 000000B
```

Comment: This register is described on page 25.
When RAM control register = 00B it means that
- error correction is enabled,
- suppression of error reporting is disabled,
- memory access to this module, without regards to the limit register, is enabled and
- writing into correction bits is enabled.

```
SLOTNO:12↵

SLOT NO.  12 : TWIN 16-BIT PORT (5155)

PORT BASE REGISTER      : 000000B
```

Comment: This register is described on page 11.

```
PORT CONTROL REGISTER    : 000140B

          Comment: This register is described on page 17.
                   When port control register = 140B, it means
                   that
                 - there is no interleave,
                 - the bank has number 0,
                 - there is 40 ns request delay,
                 - this is a 16-bit channel and
                 - the write queue is not disabled


MASTER CONTROL REGISTER : 000025B

          Comment: This register is described on page 16.
                   When the master control register = 25B, it
                   means that
                 - requests are not inhibited,
                 - supertest is not performed,
                 - address bits not supplied by ND-100 are
                   disabled,
                 - test request is not desired,
                 - local access is wanted,
                 - global access is not wanted and
                 - parity check on write is performed.


LIMITS THAT DEFINE ACCESS AREAS FOR THE PORT.

LOW LIMIT : 000000B      HIGH LIMIT: 000020B


SLOTNO:13<-|

SLOT NO.  13 : MPM-5 BANK CONTROLLER

          Comment: This module is described in the manual
                   MPM-5 Bus Description (ND-10.005)


MAINTENANCE CONTR. REG.: 000435B

TIMEOUT ON MPM-BUS     : 000003

BAUD RATE ON CONSOLE    : 000600

ERROR INVESTIGATOR ENABLED

REPORT ALL CORRECTED ERRORS
```

2.5 INVESTIGATE-BANK

This command lists all the modules in the bank, and indicates in which slot they are sited.

2.6 AUTOINITIATE-BANK

After this command, the bank will automatically be initiated with parameters found in the EEPROM.

2.7 MEMORY-DUMP

Parameters: Start Address

End Address

This command displays windows of 20 x 86 bytes in the MPM-5 memory, specified by the parameters START-ADDRESS and END-ADDRESS. The parameters are prompted if they are not given immediately after the command. There are also four subcommands available under MEMORY-DUMP. These are:

- N (= NEXT) displays the next window.
- P (= PREVIOUS) displays the previous window.
- C (= CONTINUOUS) displays the same window continuously (can only be used on a screen).
- E (= EXIT) takes you back to > (prompt) level.

2.8 MEMORY-TEST

Parameters: Start Block (128 Kbyte)

Number of blocks

Number of runs

Suppress error report? (Yes/No)

This command performs a statical pattern test on the MPM-5 memory.

Example:

```
>MEMORY-TEST↵
START-BLK (128KB):0↵
NO. OF BLK:2↵
NO. OF RUN:1↵
          Comment: Octal values are default input.

SUPPRESS ERR. REPORT (YES/NO):YES↵
          Comment: The memory test will now be performed on the
                   first 256 Kbyte of the MPM-5 memory. The test
                   is run once, and reporting of errors will be
                   suppressed during the test.
```

2.9 LOOK-AT-MPMMEMORY

Parameter: Address

This command lists the contents of an address location in the MPM-5 memory specified by the parameter ADDRESS. There are ten subcommands available:

- HELP: lists all subcommands.
- EXIT: takes you back to > (prompt) level.
- PERMIT-DEPOSIT: permits writing to the memory.
- DOUBLEWORD: gives double word as size of displayed value.
- WORD: gives word as size of displayed value.
- BYTE: gives byte as size of displayed value.
- PREVIOUS: looks at previous location.
- ADDITIONAL-FORMAT <FORMAT (HEX, DEC, ASCII)>, gives the value of the location in the desired format.

- LOOP-ON: Starts a continuous read of the location. The command may be used in test and debug operations. Values may also be read continuously if the PERMIT-DEPOSIT command has been given.

- LOOP-OFF: Stops the LOOP-ON.

2.10 ENABLE-ERROR-INVESTIGATOR

This command activates the error investigator. When the error investigator is active, the maintenance processor continuously scans the memory to detect possible errors.

2.11 DISABLE-ERROR-INVESTIGATOR

This command inactivates the error investigator. The activity on the console terminal will then not be disturbed by error messages.

2.12 ENABLE-INTERRUPT

Parameter: Channel number

When this command is given, the interrupt from the specified channel number is enabled. The channels are listed in Fig. 14.

Channel Number	Signal Name	Meaning
0	ETIME	Detects end of byte-erase pulse, and writes it to the EEPROM 2816.
1	SINT	Message bus has finished transmission.
2	RTCLK	Pulse from real time clock
3		Not used.
4	INTL	Information received in error-log.
5	TIMINT	Timeout on the MPM-5 bus.
6	INTX	Message received on the message bus.
7	TELLIN	Triggers the TIMINT.

Fig. 14. Channel Numbers

2.13 DISABLE-INTERRUPT

Parameter: Channel number

When this command is given, the interrupt from the specified channel number is disabled. The channel numbers are the same as for the ENABLE-INTERRUPT command, see Fig.14.

2.14 DUMP-ERROR-LOG

Parameter: Slot number

This command dumps the error log of a dynamic RAM module specified by slot number. The table in Fig. 15 shows a section of the error log display. The POSITION refers to the same position on the physical RAM module. One position contains one memory chip. The errors can occur as

- soft errors, ie., the error will disappear if the correct contents are written back to the memory

- hard errors, ie., there is not possible to change the contents of the memory

These two types of errors can again occur as

- single bit errors, or

- multiple bit errors.

If thereare hyphens in the error log, no error is detected in the memory chip in the corresponding position on the memory module. If there is a number there, the number indicates how many errors have been detected since the last reset of the error log. The letter H after the number indicates a HARD error, and no letter indicates a SOFT error.

The error reporting can be suppressed by setting bit 1 in the RAM control register to '1'. When this is done, previously detected single-bit hard errors are not reported. This means that, if the value 5H is found in a position in the error log, there has been 4 soft errors and 1 hard error. Identical hard errors are not subsequently reported. When the reporting of single-bit hard errors is suppressed, the error codes of detected errors are loaded in the suppress error table on the RAM module. See page 27.

If bit 1 in the RAM control register is '0', all hard errors are reported. If a memory chip has a hard error, this error is then reported very often. This is not always desirable.

Example:

Fig. 15 shows a section of the error log display on the console terminal. You can see that there is an error in the chip in position E2. The error has occurred 6 times, and it is a soft error. In position L3, there is a hard error. If the error reporting is suppressed, position 20D contains 4 soft errors and 1 reported hard error.

```
POSITION :     D       E       F        . . .       L
-------------------------------------------------  ---------
       1 :     -       -       -                    -
       2 :     -       6       -                    -
       3 :     -       -       -                    1H
       4 :     -       -       -                    -

         .
         .
         .

      20 :     5H      -       -                    -

H=HARD-, S=SOFT-ERROR.    NO. OF MULTIBIT ERRORS:   00000
```

Fig. 15. A Section of the Error Log Display

2.15 LOOK-AT-68MEMORY

Parameter: Address

This command lists the contents of an address location in the memory of the M68000 on the controller module. The location is specified by the parameter ADDRESS.

There are ten subcommands available:

- HELP: Lists all subcommands.
- EXIT: Takes you back to > (prompt) level.
- PERMIT-DEPOSIT: Permits writing to the memory.
- DOUBLEWORD: Gives double word as size of displayed value.
- WORD: Gives word as size of displayed value.
- BYTE: Gives byte as size of displayed value.
- PREVIOUS: Looks at previous location.
- ADDITIONAL-FORMAT <FORMAT (HEX, DEC, ASCII)>: Gives the value of the location in the desired format.
- LOOP-ON: Starts a continuous read of the location. The command may be used in test and debug operations. Values may also be read continuously if the PERMIT-DEPOSIT command has been given.
- LOOP-OFF: Stops the LOOP-ON.

2.16 VALUE

Parameter: Number

With this command, it is possible to give a value in one of the radixes octal, decimal or hexadecimal and convert the value to the other two radixes. Default input radix is octal. Decimal input can be achieved by typing D after the value, and hex. input by typing H.

Example:

```
>VALUE↵
NUMBER:16↵
          16B          14          EH
```

Comment: The octal value here is 16, 14 is the decimal value, and E is the hexadecimal value.

2.17 INITIATE-EEPROM

Parameters: Slot number

Date (Year, Month, Day (YYMMDD))

Old contents will be lost - continue? (Yes/No)

This command is only used when an EEPROM is replaced by a new one. There is one EEPROM on each memory module, and one in the backwiring. To initiate the one in the backwiring, you have to give the slot number of the controller module.

2.18 LOOK-AT-EEPROM

Parameters: Slot Number

Address

This command lists a location in the EEPROM.

2.19 IO-FORMATS

Parameters: Input (Oct, Hex, Dec)

Address

Data

Size (Byte, Word, Double word)

This command may be used to format the command MEMORY-DUMP. Data can then be displayed as octal, decimal or hexadecimal values and as bytes, words or double words.

2.20 LOOK-AT-IO

Parameter: Word Address

This command may be used to perform I/O read/write on the MPM-5 bus. The commands are listed in Fig. 16, Fig. 17 and Fig. 18. To find the word address, you have to:

- Take the octal value of the slot number of the port or RAM modules and multiply by 2.
- Place the calculated value in the position marked xx in in the word address.

Example:

If you want to read the contents of the slot identification on the RAM module in slot position 17(decimal), you do as follows:

- 17(decimal) X 2 = 34(decimal)
- 34(decimal) = 42B
- From Fig. 18 you find that 'read slot identification' has the word address xx0000.
- The complete word address is then 420000.

PORT WRITE COMMANDS:

Word Address	Meaning
xx0500	Test Request
xx0504	Master Control Register
xx0520	Port Control Register
xx0540	Test Address, lower part
xx0544	Test Address, upper part
xx0550	Test Data, lower part
xx0554	Test Data, upper part
xx0524	Base
xx0532	Limit
xx0534	Display

Fig. 16. Port Write Commands

PORT READ COMMANDS:

Word Address	Meaning
xx0000	Slot Identification
xx0504	Master Status Register
xx0520	Port Status Register
xx0550	Test Data
xx0554	Test Data

Fig. 17. Port Read Commands

RAM COMMANDS:

Word Address	Meaning
xx0000	Read Slot Identification
xx2120	Write RAM Control Register
xx2130	Write Lower Limit Register
xx2134	Write Display Memory
xx2140	Write Error-Memory Address
xx2150	Write Error-Memory Data
xx2150	Read Error-Memory Data
xx2160	Write Suppress Error Table

Fig. 18. RAM Commands

2.21 SYNDROME-TEST

This command performs a test on the logic circuitry which is used to detect errors in memory. The test simulates all possible 1-bit and 2-bit (multiple) errors, and makes sure that error message signals are generated. The test is performed on address zero on each memory module in the bank.

2.22 CHANGE-PASSWORD

Parameter: Old password

New password

With this command, it is possible to change the system password. When the password is changed, the keyboard can be locked with the command LOCK-CONSOLE-KEYBOARD. The Test and Maintenance Program is then only available when the password is given.

2.23 LOCK-CONSOLE-KEYBOARD

After this command is given the Test and Maintenance Program can only be entered with the password.

CHAPTER 3

START-UP AND INITIALIZATION OF THE MPM-5 SYSTEMS

3 START-UP AND INITIALIZATION OF THE MPM-5 SYSTEMS

> NOTE! When boards are moved in and out of the crate, always first disable the error investigator with the command DISABLE-ERROR-INVESTIGATOR.

3.1 The very first Start-up

A special procedure has to be completed prior to starting up the MPM-5 for the very first time. The procedure implements several commands in the Test and Maintenance program, described in chapter 2. The procedure is as follows:

- >INITIATE-EEPROM
- >CONFIGURATE-SLOT
- >LIST-CONFIGURATION
- >MEMORY-TEST
- >SYNDROME-TEST
- >AUTO-INITIATE-BANK

The MPM-5 is now ready for normal operation.

3.2 Initialization after COLD Start or WARM Start

After COLD start or WARM start, the MPM-5 is automatically initialized with the information contained in the EEPROM in the backwiring.

3.3 System Expansion

When you want to expand the MPM-5 system, you have to configurate the new modules with the CONFIGURATE-SLOT command.

When new RAM-boards are added, remember to raise the upper address limit.

3.4 Termination

The termination chips on the port module are numbered 16-1-151, which means that the termination resistance is 150Ω. On page 57 you find a list of how you terminate in different MPM-5 configurations. The functions and the card positions of the termination chips are:

Chip Position	Function
19A	OFF-termination, do not remove this chip
18A 18C 22C 26C	Terminate the address lines (on the B-connector)
12C 14C 16C	Terminate the data lines (on the C-connector)
2A 5A 8A	Terminate the data lines (on the D-connector)

MPM-5 Configuration	Action with Termination Chips
Any configuration with end-termination	Remove all termination chips, except the one in position 19A.
1-bank, no end-termination	Keep all chips.
16-bit channel, 2-bank, no end-termination	Remove all chips on the first port in the daisychain, except the one in position 19A. Keep all chips on the last port.
16-bit channel, 4-bank	Keep all chips on the last port in the daisychain. Remove all other chips except the one in position 19A.
32-bit channel, 2-bank	Remove all chips on the first port in the daisy chain, except the one in position 19A. Keep all chips on the second port.
64-bit channel, 2-bank	Remove the chips in positions 18A, 18C, 22C and 26C on the first port in the daisy-chain. Keep all other chips.
64-bit channel, 4-bank	Remove the chips in positions 2A, 5A, 8A, 12C, 14C, 16C, 18A, 18C, 22C, 26C on the first three ports in the daisy-chain. Keep all other chips.
128-bit channel	Remove the chips in positions 18A, 18C, 22C and 26C on all ports, except the last port in the daisy-chain. Keep all other chips

CHAPTER 4

ERROR MESSAGES AND FAULTFINDING

4 ERROR MESSAGES AND FAULTFINDING

> NOTE! When boards are moved in and out of the crate, always first disable the error investigator with the command DISABLE-ERROR-INVESTIGATOR.

4.1 Error Messages

Any error during normal operation of the MPM-5 systems makes one of eight different error messages appear on the console terminal. The error messages contain information from which the error source can be decoded.

The error-logs are updated for every memory cycle. When errors occur, the error logs are locked, and will not be opened before their contents are read. Thus the information on the error-causing cycle is saved.

The information in the error-logs is a great help in locating the error source, but the information has to be decoded in order to be understandable.

The error messages for occurring bus errors are:

* MPM-5 BUS ERROR (MEMORY CYCLE) - TIMEOUT - *

* MPM-5 BUS ERROR (MEMORY CYCLE) - FATAL - *

* MPM-5 BUS ERROR (MEMORY CYCLE) - WRITE PARITY - *

* MPM-5 BUS ERROR (IO CYCLE)

* MPM-5 BUS ERROR (MEMORY CYCLE) - CORRECTED ERROR - *

* MPM-5 BUS ERROR (MEMORY CYCLE) *

Two lines of standard information always follow these six error messages.

Example:

```
* MPM-5 BUS ERROR (MEMORY CYCLE)  - C O R R E C T E D  E R R O R -  *
MAINT.STAT:147122 ERRLOG 1:000001B ERRLOG 2:031460B ERRLOG 3:015222B
MASTER:    000016 SLAVE:   000019  ADDRESS: 000001B SYNDROME:000122B
```

The upper line contains the value of the maintenance status register and the values of the error logs. The lower line contains information that is decoded from the upper line, but this is not sufficient to find the error source. The different codes in both lines are therefore explained in detail in the following part of this section. After all the codes have been explained, some examples are given to show you how all this information is used.

MAINT.STAT:

This code represents the contents of the maintenance status register on the controller module. The different bits have the following meaning:

Bit 1	Non-volatile memory write ready
2	Not used
3	Not used
4	Log error detected. This means that the error message is written out after the error interrupt has been received.
5	Not used
6	Not used
7	Not used
8	Slot number bit 0 ┐
9	Slot number bit 1 ├→ These bits give the slot
10	Slot number bit 2 ├→ These bits give the slot
11	Slot number bit 3 ├→ number of the controller
12	Slot number bit 4 ┘ module.
13	Not used
14	Not used
15	Inverted COLD start. When POWER-FAIL interrupt has occurred, bit 15 has the following meaning: Bit 15 = 0 - COLD start Bit 15 = 1 - WARM start

ERRLOG 1:

This code represents the contents of the error-log 1. The meaning of the different bits in the error-log 1 is shown in the table in Fig. 19.

BIT	SIGNAL NAME	MEANING
15	Not used	
14	Not used	
13	Not used	
12	Not used	
11	BREF	Bus refresh
10	BARYERROR	Bus address ready error, timeout
9	BDRYERROR	Bus data ready error, timeout
8	BDREQERROR	Bus data request error, timeout
7	Not used	
6	Not used	
5	Not used	
4	BA22	Bus address bit 22
3	BA21	Bus address bit 21
2	BA20	Bus address bit 20
1	BA19	Bus address bit 19
0	BA18	Bus address bit 18

Fig. 19. Error-log 1

ERRLOG 2:

This code represents the contents of the error-log 2. The meaning of the different bits in the error-log 2 is shown in the table in Fig. 20.

BIT	SIGNAL NAME	MEANING
15	BCYCLE2	Bus cycle bit 2
14	BCYCLE1	Bus cycle bit 1
13	BCYCLE0	Bus cycle bit 0
12	BSCOD4	Bus slave code bit 4
11	BSCOD3	Bus slave code bit 3
10	BSCOD2	Bus slave code bit 2
9	BSCOD1	Bus slave code bit 1
8	BSCOD0	Bus slave code bit 0
7	LOGALL	Log all errors on bus
6	BGLOBAL	Bus global access
5	BLOCAL	Bus local access
4	BMCOD4	Bus master code bit 4
3	BMCOD3	Bus master code bit 3
2	BMCOD2	Bus master code bit 2
1	BMCOD1	Bus master code bit 1
0	BMCOD0	Bus master code bit 0

Fig. 20. Error-log 2

Bits 13, 14 and 15 in error-log 2 define in what type of cycle the error has occurred. The cycle types arelisted in Fig. 21.

BCYCLE BITS 2 1 0	MEANING
0 0 0	Not used
0 0 1	Memory cycle
0 1 0	I/O cycle
0 1 1	Not used
1 0 0	Not used
1 0 1	Broadcast to memory
1 1 0	Broadcast to I/O
1 1 1	Not used

Fig. 21. Cycle Types decoded from the BCYCLE Bits

ERRLOG 3:

This code represents the contents of the error-log 3. The meaning of the different bits in the error-log 3 is shown in Fig. 22.

BIT	SIGNAL NAME	MEANING
15	LOCK	Semaphore cycle, ie., test and set
14	BWCHK	Bus write parity check
13	BDERR1	Bus data error 1, error type
12	BDERR0	Bus data error 0, error type
11	BERROR	Bus errors, inclusive or of errors
10	BFATAL	Fatal error, ie., multipple error
9	BSYN6	Syndrome code bit 6
8	BSYN5	Syndrome code bit 5
7	BSYN4	Syndrome code bit 4
6	BSYN3	Syndrome code bit 3
5	BSYN2	Syndrome code bit 2
4	BSYN1	Syndrome code bit 1
3	BSYN0	Syndrome code bit 0
2	Not used	
1	BWRITE	Bus write, data to memory module
0	BREAD	Bus read, data from memory module

Fig. 22. Error-log 3

Bits 10, 11 12 and 13 in error-log 3 define the type of error that has occurred from a memory module during a memory cycle. The error types are listed in Fig. 23.

BFATAL	BERROR	BDERROR0	BDERROR1	MEANING
0	1	1	0	Corrected error
0	1	X	1	Write parity error
1	1	X	X	Multippel error

Fig. 23. Error Types from Memory Module during Memory Cycle

MASTER:

The MASTER code gives the slot number of the module that was master during the error-causing cycle.

Modules can be either masters or slaves. In general, modules that 'ask' on the multiport bus are masters, and modules that 'answere' are slaves. But this also depends on what the master asks for, and when it appears on the bus. Finally, it also depends on the physical design of the system.

SLAVE:

This code gives the slot number of the module that was slave during the error-causing cycle. When you have the slot number of both the master and the slave involved, you know that the error has occurred in one of these modules.

The SLAVE code may also be zero. This means that no slaves have answered the request from the MASTER.

ADDRESS:

The address code is decoded from bits 0-4 in the error-log 1 and represents the MPM5-bus address bits 18-22. With these bus address bits it is possible to locate the rows of chips on the memory board where the faulty chip is sited. When you have both the SYNDROME code and the address code, it is possible to locate the single chip.

You can find the rows of chips on the memory board by using the table in Fig. 24. Note that the decoding is different for the 1 Mbyte memory module and for the 4 Mbyte memory module.

Address bits 18-22 cover only the first 8 Mbyte of your memory. If you have more than 8 Mbyte, the address code will start at zero for the next 8 Mbyte. The decoding of chips then goes as for the first 8 Mbyte. To be sure, you can check the SLAVE code to see which RAM module is failing.

ADDRESS code (using 1 Mb)	ADDRESS code (using 4 Mb)	Rows of chips on module
0	0, 1, 2, 3	L and K
1	4, 5, 6, 7	J and H
2	10, 11, 12, 13	G and F
3	14, 15, 16, 17	E and D

Fig. 24. Row of Chips decoded from Address Bits

SYNDROME:

The SYNDROME code is decoded from bits 3-9 in the error-log 3. After you have located the two rows of chips, you can find the faulty chip by using the syndrome code. The table in Fig. 25 shows which syndrome codes refer to the specific chips. The chip number refers to the number found in Fig. 26 on page 70.

SYNDROME CODE	CHIP NUMBER
46	0
144	1
43	2
142	3
141	4
54	5
51	6
150	7
26	8
124	9
122	10
121	11
130	12
64	13
61	14
160	15
67	16
165	17
127	18
25	19
45	20
135	21
117	22
15	23
16	24
13	25
112	26
153	27
52	28
136	29
133	30
32	31
1	32
2	33
4	34
10	35
20	36
40	37
100	38
166	ALL 0
111	ALL 1

Fig. 25. Single Chips decoded from the Syndrome Code

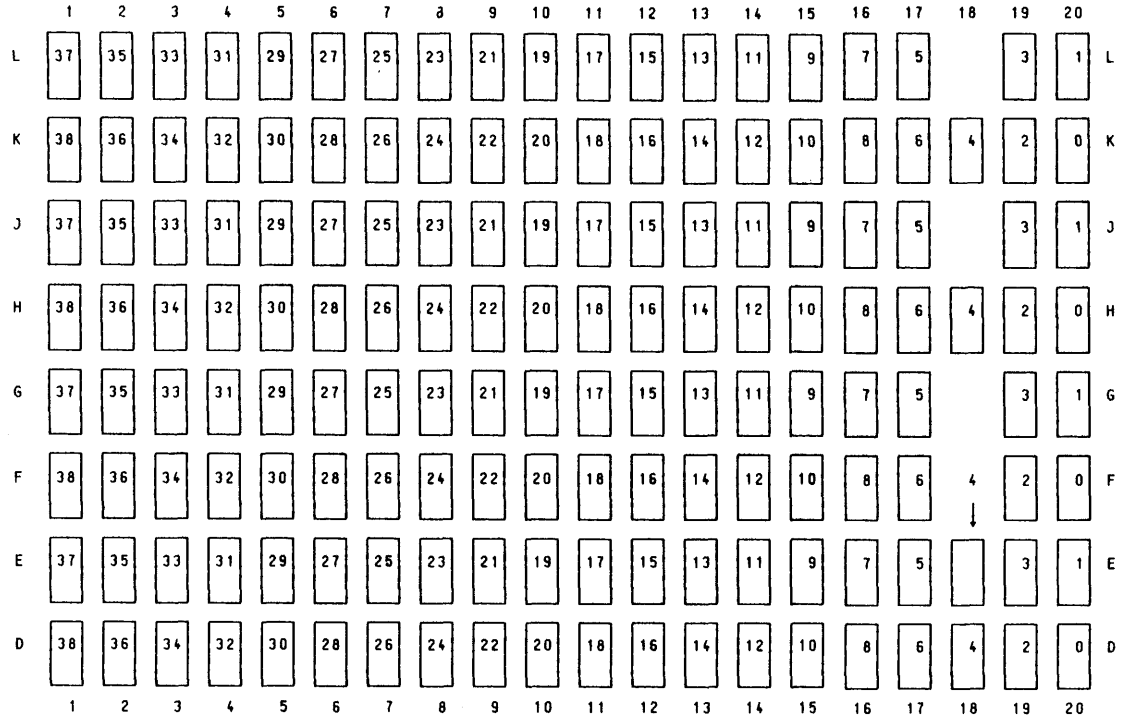


Fig. 26. Memory Chips on the Memory Module

EXAMPLE 1:

You are now going to decode the error message

```
* MPM-5 BUSERROR (MEMORYCYCLE) - C O R R E C T E D  E R R  O  R  -  *
MAINT.STAT:147122  ERRLOG 1:000001B  ERRLOG 2:031460B ERRLOG 3:015222B
MASTER:    000016  SLAVE:   000019   ADDRESS: 000001B SYNDROME:000122B
```

Since this is a corrected error, you know that a memory module is involved. The memory modules can only be slaves, so slot number 19 contains the possible failing memory module.

To find the faulty chip you first have to look at the ADDRESS code, which here is 1. If you look at Fig.24 on page 68, you will find the chip in one of the rows J or H on the memory module, if you assume that this is a 1 Mbyte module.

Now you have to look at Fig.25 on page 69 to decode the SYNDROME code. In this case the SYNDROME code is 122B. From the table you can see that the code 122 refers to chip number 10 in position 15H on the memory module. You have then found the faulty chip.

EXAMPLE 2:

You are now going to decode the error message

```
*   MPM-5   BUSERROR   (MEMORYCYCLE)   -   T I M E O U T   -   *
MAINT.STAT:147122  ERRLOG 1:003037B  ERRLOG 2:020056B ERRLOG 3:004001B
MASTER:    000014  SLAVE:   000000   ADDRESS: 000037B SYNDROME:000000B
```

The MASTER here is the controller module in position 14. This you can see from bits 8-12 in the maintenance status register described on page 62.

The SLAVE code is zero, which means that no module has answered the request from the MASTER.

To find out what sort of timeout has occurred, you have to look at bits 8-10 in error-log 1. In this case, error-log 1 has the value 003037B, which means that bits 9 and 10 are set. If you now look at these bits in the table in Fig.19 on page 64, you will see that the controller has not received ADDRESS READY and DATA READY from any memory module.

The value of the ADDRESS code is 37B, which means that all the bus address bits in error-log 1 are set. Possible error causes can be:

- missing answer from a memory module
- the controller has sent wrong address

If the MASTER had been a port, possible error causes could have been:

- the limits on the port do not conform to the limits on the memory modules
- error in cabling

Two other error messages can also appear during normal operation of the MPM-5 system:

MPM-5 CORRECTED ERROR (SOFT), SLOT: <slot number>

MPM-5 CORRECTED ERROR (HARD), SLOT: <slot number>

These error messages only occur if the error investigator is on. This means that they only come up if the controller module discovers the error. The EEPROM on the memory board will be updated and the DUMP-ERROR-LOG command will show memory matrix with the position of the faulty chip.

APPENDIX A

DEFAULT VALUES FOR PROGRAM PARAMETERS

Interleave Port Number.....0

Interleave Type.....0

Lower Limit.....0

Maintenance Control Register.....435B

Master Control Register (16 bit channel).....125B

Master Control Register (32 bit channel).....25B

RAM Control Register.....0

Request Delay... .....40ns

Start Address.....0

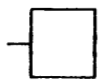
Timeout on MPM-bus.....2µs

APPENDIX B

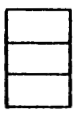
INDICATORS AND SWITCHES

NOTATION USED IN THIS APPENDIX:

* LD — means Light Emitting Diode



means switch



means display

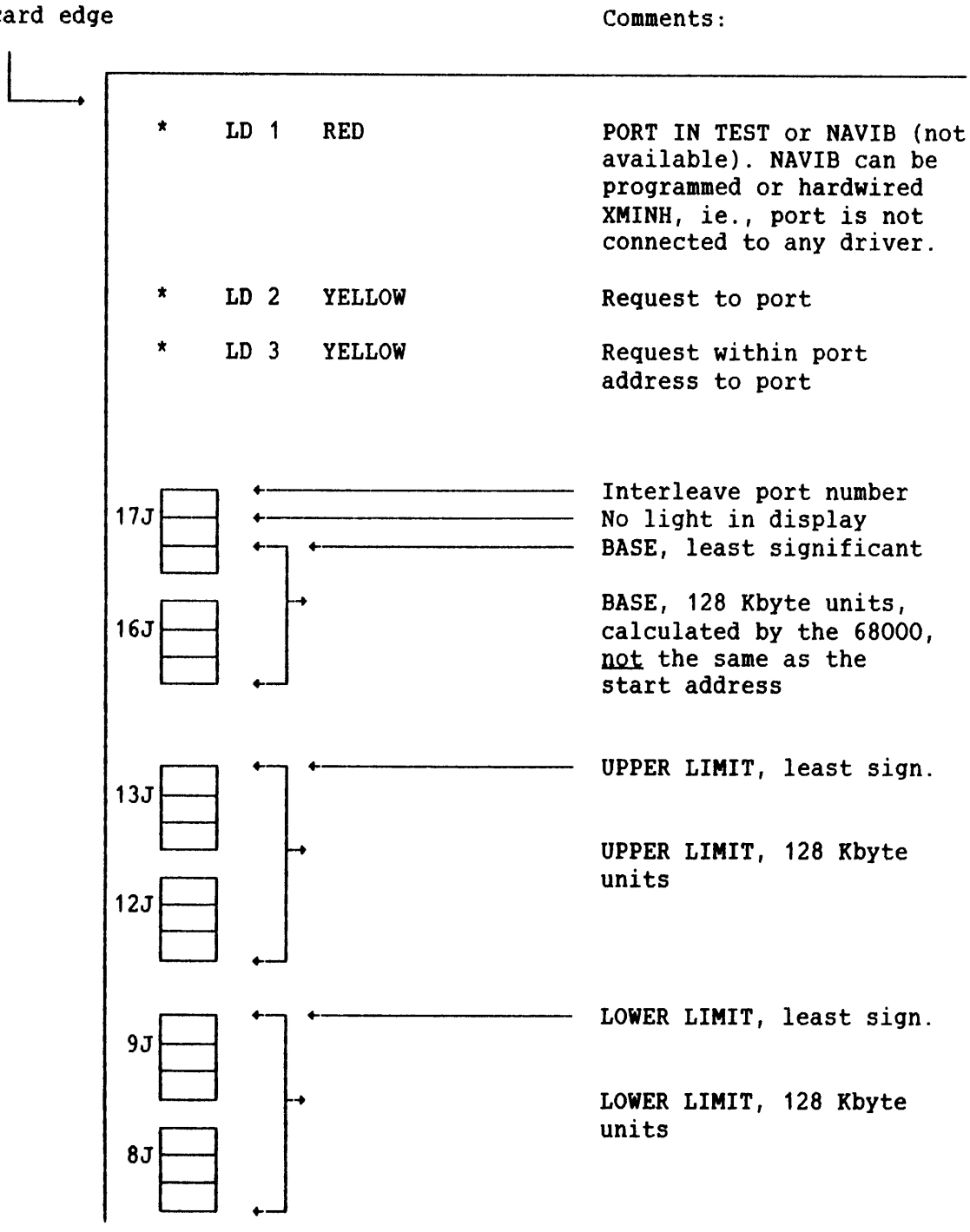
17J
9J
28L
etc.

digit(s) and letter mean position on the card

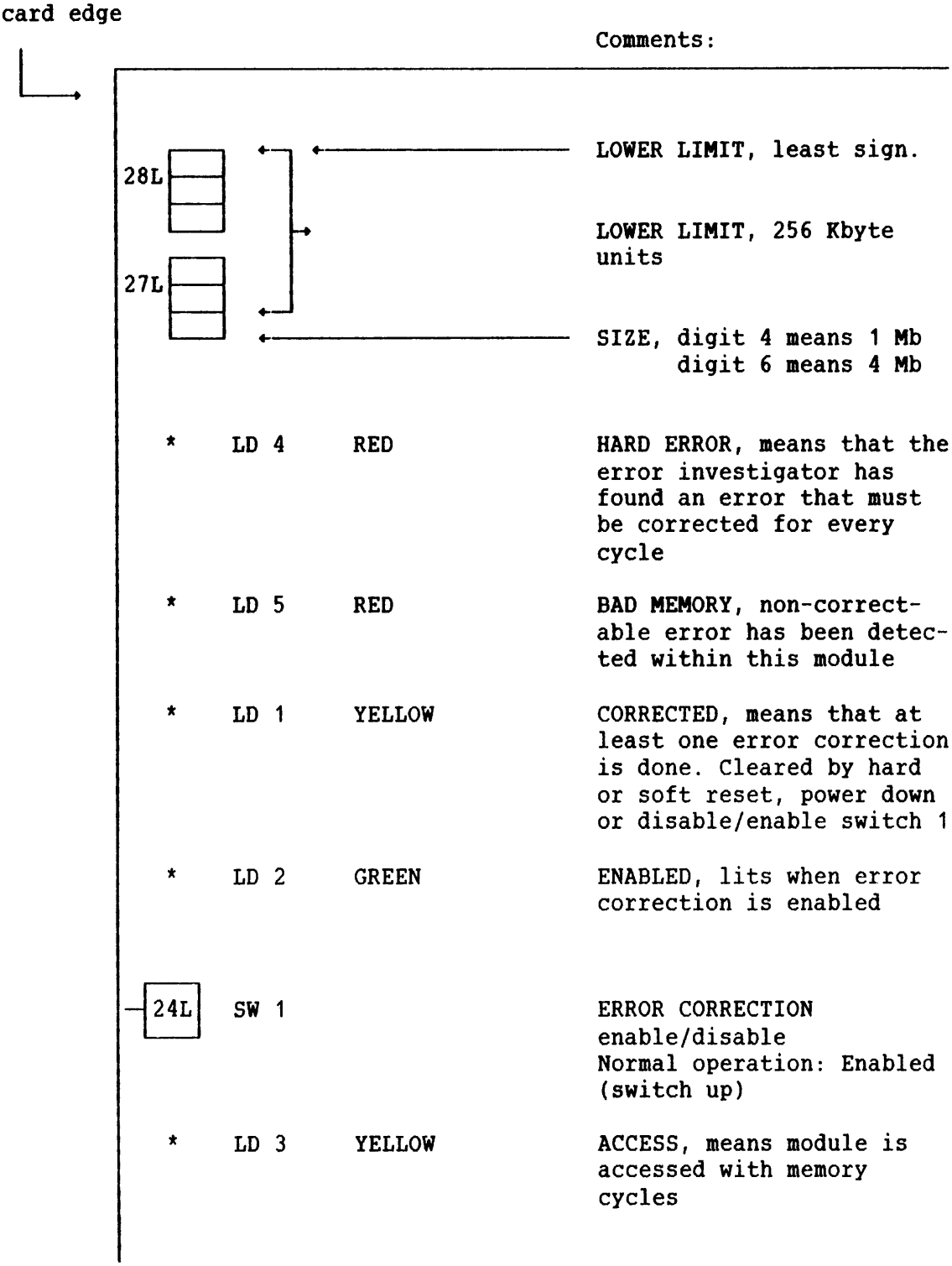
LD 4
LD 3
SW 1
etc.

letters and digit mean that these are printed on the card

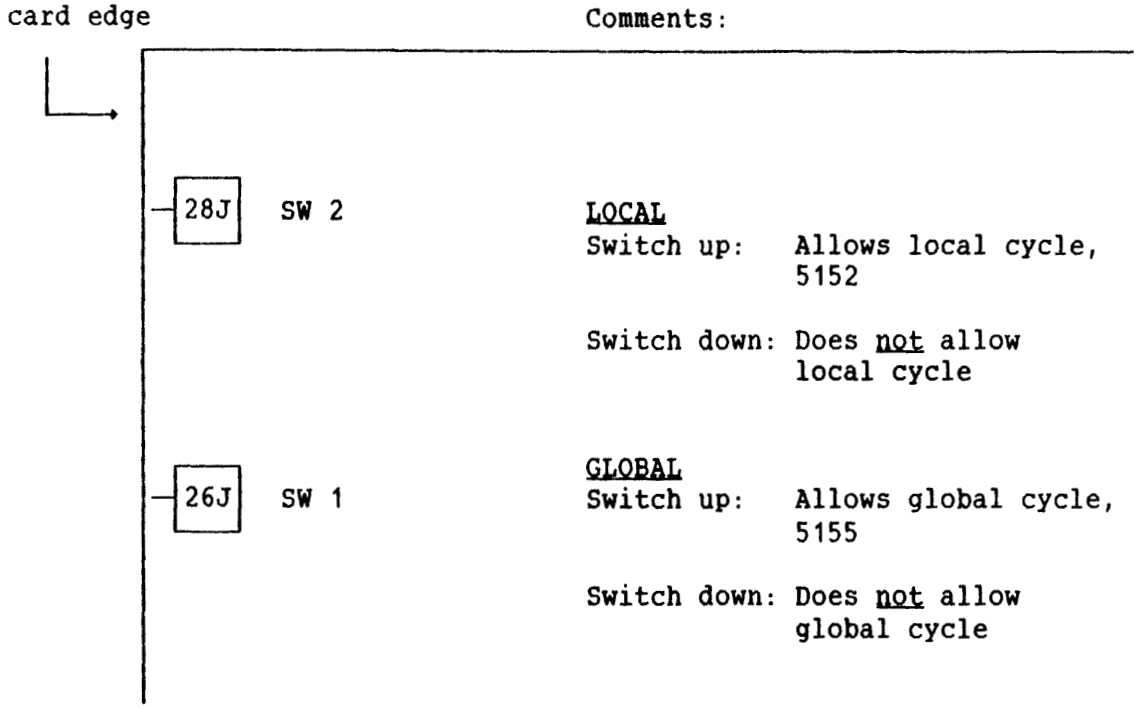
MPM-5 PORT INDICATORS



MPM-5 DYNAMIC RAM INDICATORS AND SWITCH



MPM-5 32 BIT LINE DRIVER SWITCHES



APPENDIX C

MPM-5 IDENT. PRINT AND ND NUMBERS

MPM-5 IDENT, PRINT AND ND NUMBERS

NAME	ID NO.	PRINT NO.	ND NO.	READ/ INVEST.
MPM-5 Controller	324351	5151	381	
MPM-5 Twin 16 Bit Port	324352	5152	383	120
MPM-5 Twin 16 Bit Port	324355	5155	383	121
MPM-5 Dynamic RAM 1 Mb	324211	5411	382	423
MPM-5 Dynamic RAM 4 Mb	324158	5411	387	427
MPM-5 32 Bit Line Driver	324354	5154	384	384
Backwirings:				
Single MPM-5 A	324421	5321		
Single MPM-5 B	324431	5331	386	
Single MPM-5 C	324251	5331		
Single MPM-5 D	324432	5332		
Dual MPM-5	324422	5322		
Dual MPM-5	324433	5322	380	
Dual MPM-5	324252	5333		
Dual MPM-5	324434	5334		

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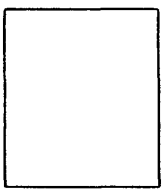

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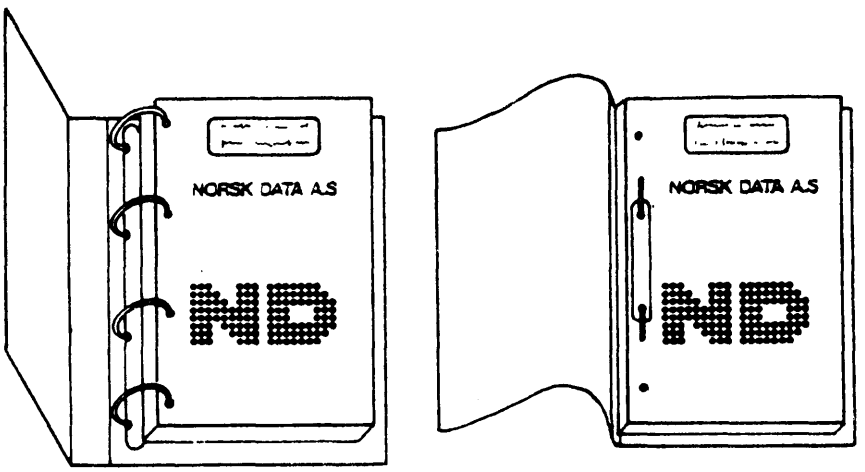

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