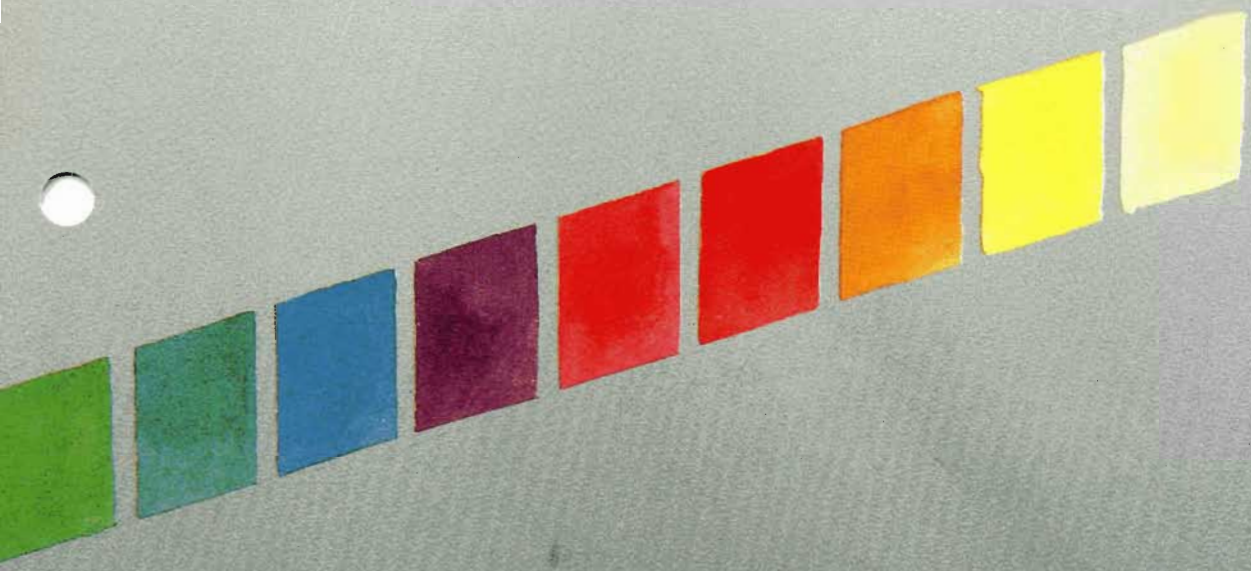

TECHNICAL INTRODUCTION TO MULTIPORT 4

ND-10.003

Norsk Data

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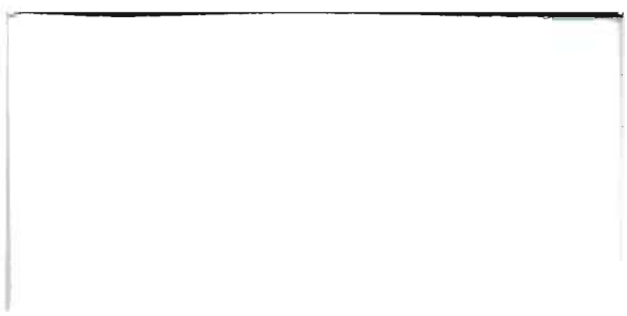

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TECHNICAL INTRODUCTION TO MULTIPORT 4

ND-10.003

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Preface:

THE PRODUCT

This manual describes the multiport memory system used in ND-100 and ND-100/ND-500 multiprocessor configurations.

THE READER

Personnel configuring and maintaining NORSK DATA multi processor systems.

PREREQUISITE KNOWLEDGE

Familiarity with the ND-100 architecture and physical implementation. Knowledge of the principles of the BIG multiport memory system is an advantage.

THE MANUAL

This manual starts by defining terms used in the manual. Followed by MPM 4 features, the new MPM 4 modules and examples of configurating with the new MPM 4 backplanes. The appendices defines the specifications for accessing the MPM 4 system via a memory port.

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TABLE OF CONTENTS

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1. Introduction

The MULTIPORT MEMORY 4 (MPM 4) is the successor to the multiport memory system which has served NORSK DATA since 1974 (The BIG multiport). MPM 4 expands the memory capacity from 4 Mbytes, where the BIG MPM stops, to 32 Mbytes.
ND-100 size memory modules can now be used in a multiport memory system. In addition to being a multiport memory system the MPM 4 also serves as an expansion of the ND-100 bus accommodating I/O and DMA controllers.

MULTIPORT MEMORY 4:

New hardware based on well-established and well proven concepts.

The "old" concepts include:

* The BIG multiport memory system.
* The ND-100 bus system.
* The ND-100 bus-extender (the BEX module)

The "new" hardware includes:

* Three ND-100 size modules
  - BUS-MASTER (BUSM)
  - BUS-CONTROLLER (BUSC)
  - MEMORY PORT (PORT)

* New backplane types making the ND-100 bus available in various units of 5, 6 or 10 positions.

Combining the new modules and the new backplanes makes a powerful tool for configuring the desired system.

Before the new modules and typical configurations are described. some of the terms will be explained.

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2. Definition of terms

ND-100 BUS — This bus is a backplane bus accessible via a 96 pins Euroboard connector. The ND-100 bus timeshares the address and the data lines (24bits) while the control and interrupt signals (35) have a unique pin assignment. The bus may accommodate one control unit such as the ND-100 CPU or the BUSC, passive units like I/O controllers, the memory and the BUSM and active requesting units like DMA controllers or ports.

BANK — In the MPM 4, a bank is defined as an ND-100 BUS. A bank consists of a storage section . a control section and port(s). An ND-100 bus with no memory or ports will also be referred to as a bank. The control section will administer the ND-100 bus and refresh the local memory.
All banks may be supplied from their own power supply. The importance of the bank is determined with a VITAL switch on the control module. A power failure with the VITAL switch ON will be reported to the master ND-100 on interrupt level 14 and the master will enter a save routine before making a controlled stop.
A power failure with the VITAL switch OFF will be reported to level 13, and that program will take the proper action. The system might continue even if the bank is not functioning.

PORT — A port is characterized as the interface between the storage section of the bank and the requesting source. Each port defines the address range of the source in the bank.

SOURCE — The logical unit able to request the memory.
16 bits sources will be the ND-100 via the BUS Master or via the MULTIPORT DRIVER module or DMA devices branched in a separate BUSC.
32 bits sources will be the ND 520 or ND 540.
64 or 128 bits sources will be the ND 560.

MEMORY — All memory modules in MPM 4 will be 128 Kb(ND 115), 256 Kb(ND116) or 512 Kb(ND117). All modules provide single bit error correction and multiple memory error detection. This is accomplished by 6 bits generated and checked within the memory module.

ND 520 * — ND-100/500 configuration with no ND-500 cache.

ND 540 * — ND-100/500 configuration with 1 DATA and 1 INSTRUCTION CACHE module (1 module = 16 Kb.)

ND 560 ** — As ND 540 with either 2 or 4 CACHE modules.

* = 1 Cabinet processor system.
**= Multi-cabinet processor system.

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3. MPM 4 highlights

IT IS MORE THAN A MULTIPORT MEMORY SYSTEM

The MPM 4 makes it possible to extend the ND-100 bus and insert more I/O controllers.

ND-100 MODULES

MPM 4 makes use of all present and future ND-100 CPU. memory. I/O and DMA controller modules.

1/2 MEGA BYTES MEMORY MODULES

Will use the new 1/2 Mbytes ECC memory modules with 64K x 1 bit memory chips.

32 Mbytes LIMIT

Will have a maximum memory limit of 32 Mbytes.

COMPATIBLE

The port access is compatible with the BIG multiport memory system on signal level. (Not plug-compatible)

PORT

The port will only occupy one slot in the bank.

PORT IN THE CPU RACK

The PORT module may be installed in the CPU bus of the existing ND-100. This opens for common memory in smaller configurations.

PORT PARITY CHECK

The port can be set to check the parity of the data during a write operation. It always checks on read.

SEMAPHORE CYCLES

A special LOCK signal has been introduced as a port control signal. If this signal is active it will guarantee the port two consecutive memory accesses.

FLEXIBLE

The MPM 4 modules can be installed in a standard 22 position ND-100 bus providing 19 ports to access 1/2 Mbytes of memory or 1 port with access to 8 Mbytes of memory or any desired combination.

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ACCESSIBLE FROM SOURCES OF VARIABLE WIDTH

16, 32 , 64 or 128 bits sources may access the MPM 4.
The source will access 16 bits in each of the banks with the same address supplied to all banks.
When combining sources of different widths the widest source will access all banks simultaneously while other sources will access the banks sequentially.
The bank access will be controlled on the BUSC or the PORT modules providing a 2, 4 or 8 way interleave.
In a 2-way interleave system subsequent addresses will be directed to 2 banks, in a 4-way to 4 banks etc.....

BANK ACCESS CONTROLLED BY SWITCHES

Shifting of the address bits for achieving the desired interleave effect and the control of the least, the 2 least or the 3 least significant address bits will be set up by switches.
No special print or cables are required.

IMPROVED THROUGHPUT

The ND-100 I/O throughput is improved because the mass storage controller has direct memory access.
The DMA accesses the memory without interfering (cycle stealing) with the CPU.

EASY TO ASSEMBLE

Due to daisy-chaining in the backplanes and the installed plug panels no special cabels are required and the interconnections are made with standard cables.

PERFORMANCE

The ND-100 or the port will during a memory access occupy the ND-100-bus for 500 nanoseconds. This gives a bandwiths or bus transfer rate of 4 Mbytes per second.
With 8 banks and a sufficent number of ports the total bandwidth to memory = 32 Mbytes.

The access time of the port (from request to data-ready) = 550 ns for READ and 320 ns for WRITE.

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4. The MPM 4 concept

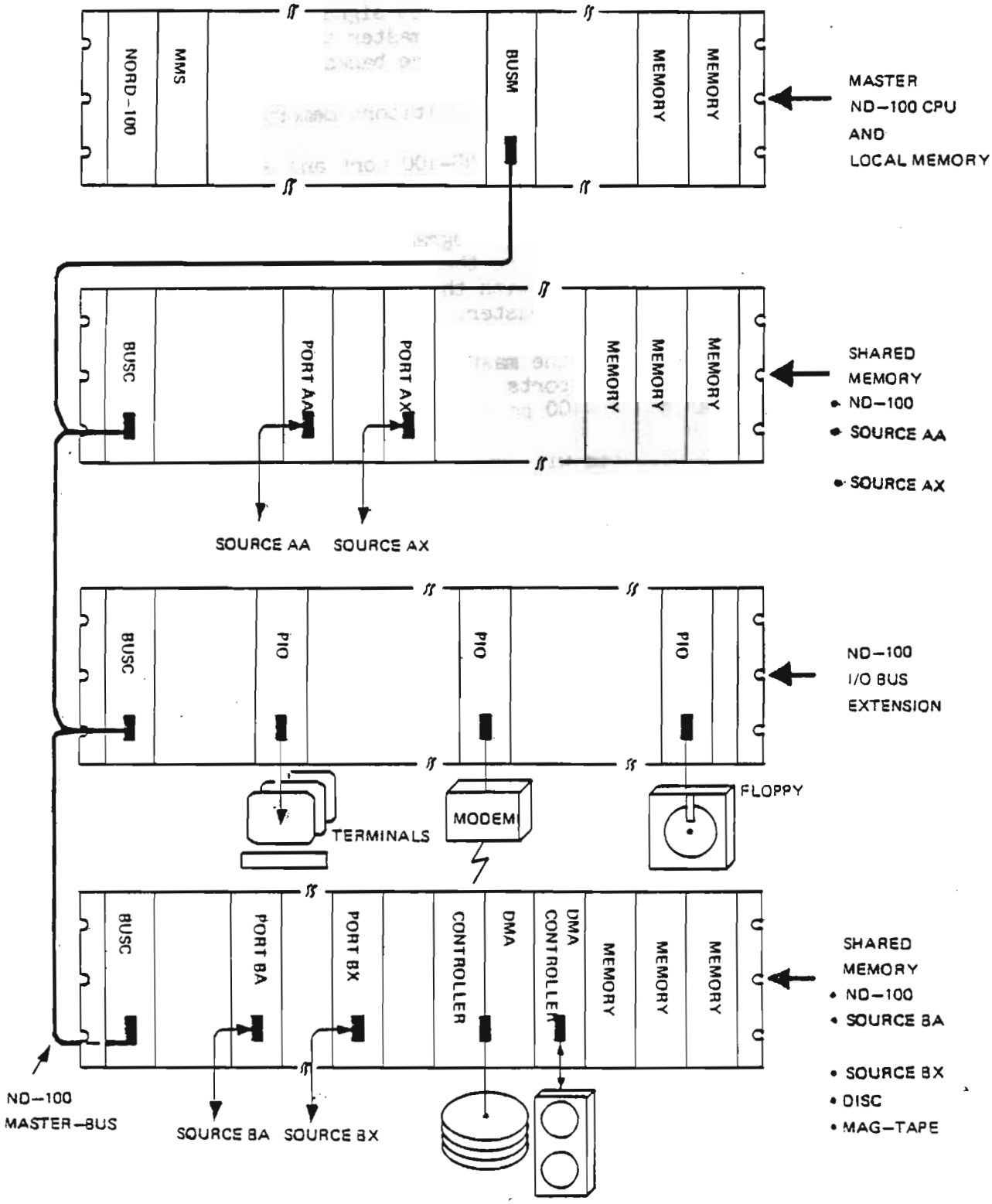

Fig. 1. MPM 4 CONCEPT

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Refer to figure 1.

This figure shows the flexibility of the MPM 4.
A Bus Master module is installed in bus of the master ND-100.
This BUSM module converts the ND-100 bus signals into differential signals on the ND-100 master bus. The master bus is connected to the BUS Controller module present in all the banks.

The first bank serves as a typical multiport memory system with ports and memory.
The BUSC module serves here as an ND-100 port and a control module for the bank.

In the next bank containing only Programmed Input Output control modules the BUSC converts the master bus into a local ND-100 bus. All communication with this bank will be routed through the A-register of the ND-100 master.

The last BUSC connected to the master bus is connected in a bank containing memory, ports and DMA controllers.
The BUSC serves as the ND-100 port, the bus expander and as the bus controller.
Note that the DMA requests will only be accepted by the local memory in the bank.

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5. Module highlights

5.1. ND-100 BUS MASTER (BUSM 3030), ND number 395

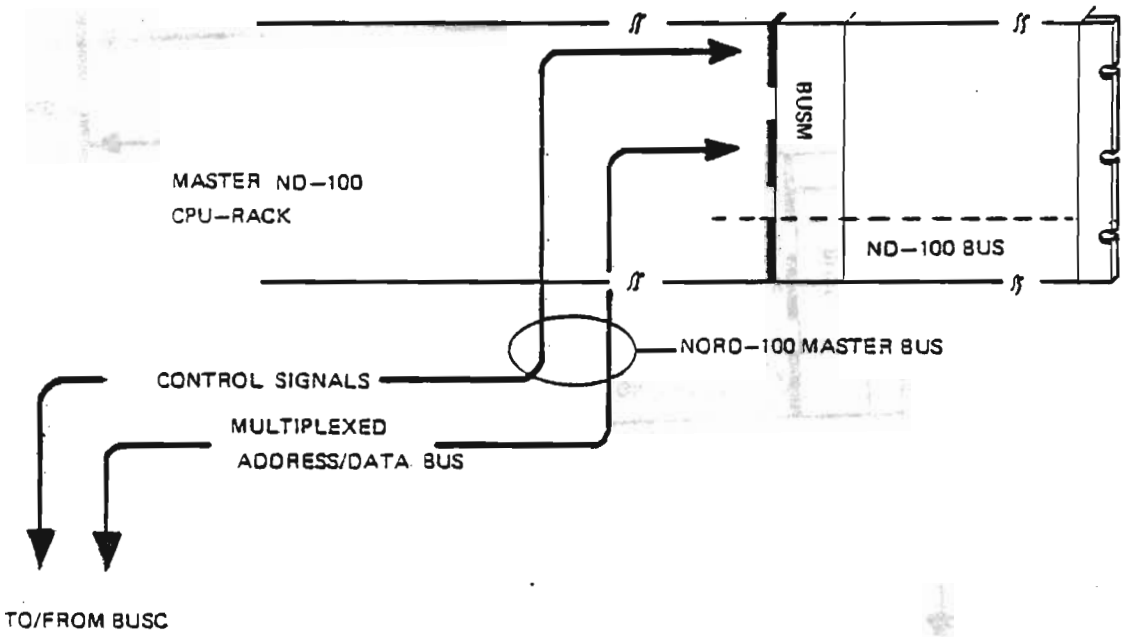

Fig. 2. BUS MASTER

* The ND-100 BUS Master module is located in the master ND-100 CPU rack and contains line receivers/drivers for extending the ND-100 bus.

* The BUSM module always communicates with a BUS Controller module (BUSC).

* Up to 9 BUSC modules can be connected to one BUSM module.

* Multiple BUSM modules can be installed in the main ND-100 bus.

* The total number of BUSC modules in a system is set to 32.

* The BUSM module refreshes the memory installed via the BUSC module of the bank.

* The control signals are supplied through the A connector and multiplexed address and data lines through the B connector.
  The C connector forms the ND-100 bus.

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5.2. BUS CONTROLLER (BUSC 3031), ND number 390

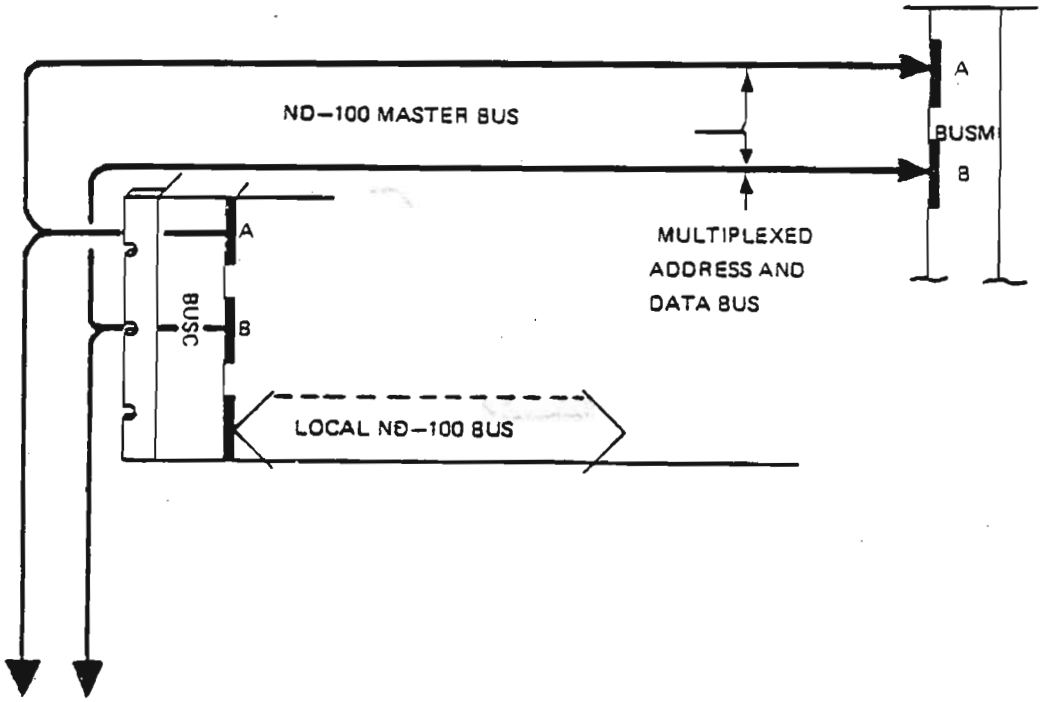

Fig. 3. BUS Controller

When only I/O modules are installed in the bus the BUSC module will serve as an ND-100 bus extension.

When memory is installed in the local bus, the BUSC module will:

* Serve as a multiport memory controller including:

  -> Bus allocation,administration.

  There will be two request sources to the BUSC for accessing the local memory, the BUSM (with a GLOBAL request) and DMA or PORT requests originated in the local bus (with a LOCAL request).
  The priority between them is rotating or toggling. The DMA controller or PORT located closest to the BUSC will be serviced first.

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-> Local memory refresh when there is no master ND-100 refresh. This can occur when the ND-100 master loses its power.

The BUSC will continue to function in the event of a collapse of the master ND-100.

* Serve as the master ND-100 port, including the following switch setting:
  - -> Interleave. Used with various ND-500 cache configurations.
  - -> Vital. Power failure interrupt to level 13 or 14.
  - -> Lower address.
  - -> Upper address.
  - -> Base address.

The setting of the lower, upper and base address is also displayed.

Correct setting of the lower, upper and base limit switches enables the master ND-100 to see all or part of the local memory.

* Contains the Parity Error Address (PEA) and the Parity Error Status registers (PES), updated when local memory cycles malfunction. These errors can be disabled or reported to interrupt level 13 of the ND-100 master.

* The following information may be obtained by the master ND-100 (IOX read)
  - -> PES register
  - -> PEA register
  - -> Limit registers
  - -> Test mode register
  - -> Status register

* The Write Control Word and a Data register(for test) are set with an IOX write instruction.

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5.3. MEMORY PORT (PORT 3032), ND number 391

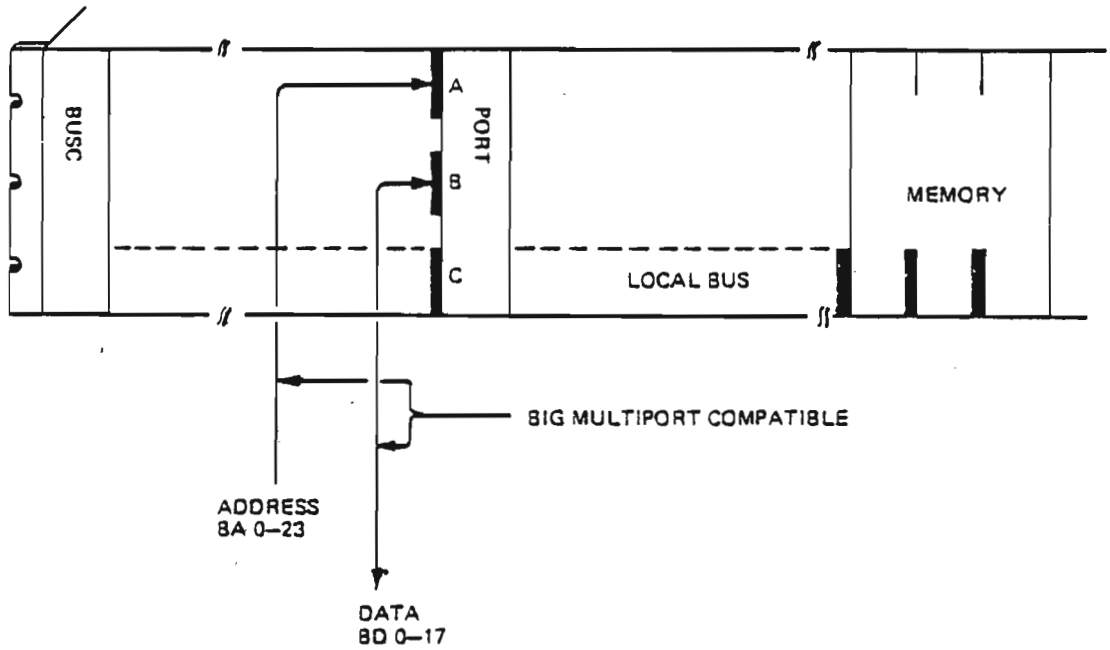

Fig. 4. MEMORY PORT

The memory port module serves as the communication link between the requesting source and the memory.

The PORT module contains:

* Address range switch setting (lower and upper) **
* Base address switch. **
* Interleave switch setting.
* Address range compare logic.
* Write parity check. (Switch settable)
* Read parity check for generating parity error to the source in the event of multiple errors.
* The A connector receives the 24 address lines.
* The 18 data bits are received/transmitted via the B connector.

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* The control signals are duplicated on both the A and the B connectors.

* The new LOCK signal (Pin 23 of the B connector) will prevent the bus arbiter (bus administration circuit) from reallocation during two subsequent cycles. With this signal active the port will have two memory cycles without any other source being able to change the memory content in between. This feature may be used for inter processor signalling.

** Correct setting of the lower, upper and base limit switches enables the PORT to see all or part of the local memory.

6. The address range of the memory modules

The first memory module installed in a bank will normally be set from address 0. This address is referred to as the local address of the bank. The first module installed will display its upper address, and this address will be set as the lower address of the next module, etc.

The local address in the bus is obtained by taking the input address to the port , subtracting the lower limit and adding the base limit.

LOCAL ADDRESS = SOURCE ADDRESS - LOWER LIMIT + BASE LIMIT.

BASE LIMIT: See section 7.

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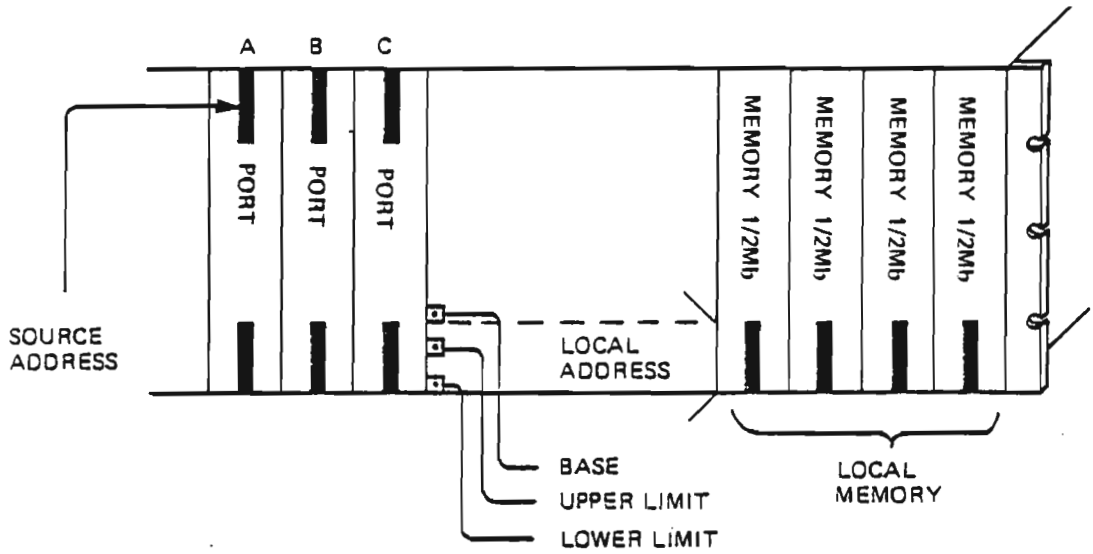
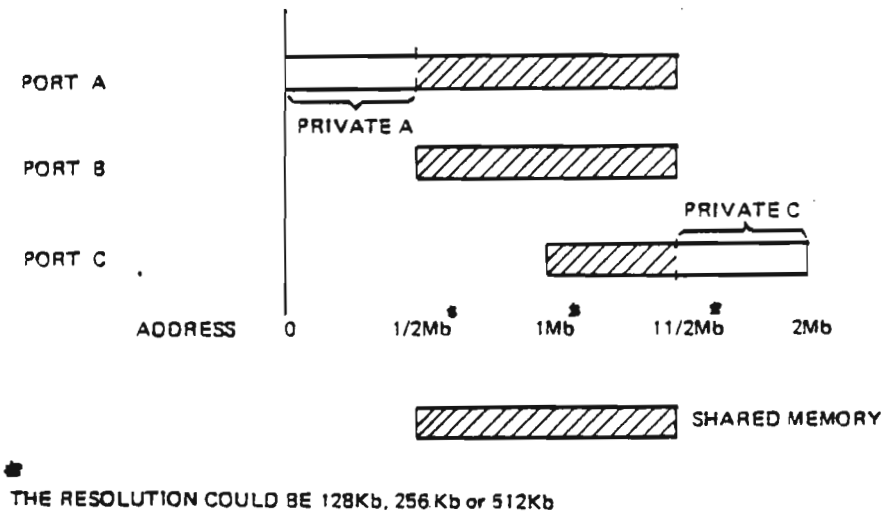
7. BASE limit register

The effect of the introduced BASE limit register.



Local address = Source address − Lower limit + Base limit

Fig. 5. Thumbwheel switches



* THE RESOLUTION COULD BE 128Kb, 256 Kb or 512Kb

Fig. 6. Example of address range set-up.

Correct setting of the lower, upper and base limit switches enables the PORT and the BUSC to see all or part of the local memory.
By introducing the BASE switch the local address of the PORT or the ND-100 can be offset by the BASE switch setting.
This feature is valuable in multiprocessor configurations such as the ND-500, where part of the memory is shared and part of the memory is private.
The number of card crates and power supplies is drastically reduced.

The increment of the BASE switch is 64 Kwords or 128 Kbytes.

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8. Introduction to the new backplanes

In addition to the hardware modules described, the MPM 4 has 4 new backplane types. (Backplane = module interconnection)

An outline of the backplanes is given in the following table:

NAME:	CAPASITY: (Number of positions)	USAGE:
MPM4-4 BANK (ND 393)	4x6	This backplane of 4 banks each with 6 slots is the most compact but the least flexible of the new backplanes. It is intended as a ND-500 configuration backplane. (ND-560)
MPM4-2 BANK (ND 392)	2x10	This backplane of 2 banks each with 10 slots is intended to be used in ND-100 and ND-560 configurations.
MPM4-1 BANK	5	This backplane of 5 positions provides one half of the shared memory in ND-520 and ND-540 configurations. It replaces the 5 first positions of the standard ND-500 backplane.
MPM4 ND-100	15 + 6	The 15 positions make a standard ND-100 bus, while the 6 positions form the other half of the shared memory in ND-520 and ND-540 configurations. The 6 positions backplane can also be used for accommodating ND-100 DMA controllers and multiport drivers.
ND-100 STANDARD 1 BANK	22	The standard 22 positions ND-100 backplane may now, by the introduction of the MPM 4 modules. be used as a one bank multiport memory system.

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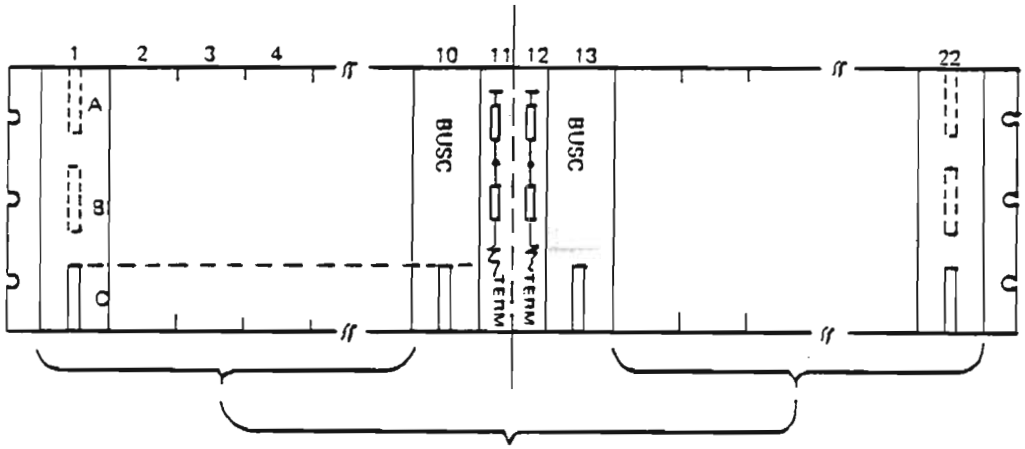
9. Examples of ND-100 configurations

This section covers the following backplanes:

* MPM4-2 BANK
  and
* MPM4 ND-100

9.1. MPM4-2 BANK backplane



These positions may house

- I/O modules
- PORT modules
- DMA controller modules
- Memory modules

Fig. 7. 2-bank backplane

The positions 10 and 13 are prewired for the BUSC modules, while the bus-termination takes place in the positions 11 and 12.

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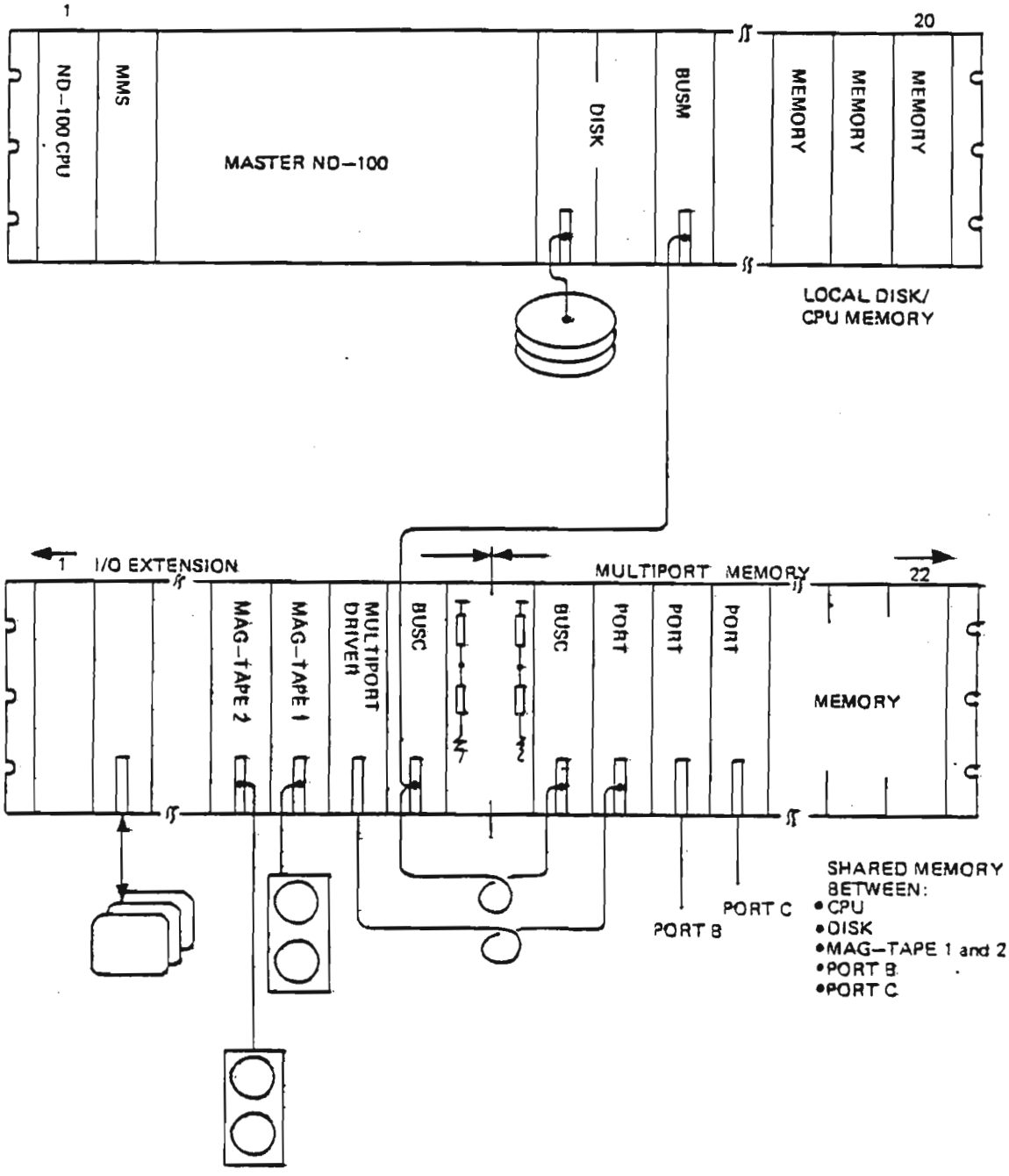

Fig. 8. Example of configuration with 2 BANK backplane

In this configuration the left bank (position 1 to 10) serves as a bus-extension while the right bank (position 13 to 22) serves as a multiport memory system.

These two card-crates fit into one 11 module (big) cabinet. (Refer to figure 10)

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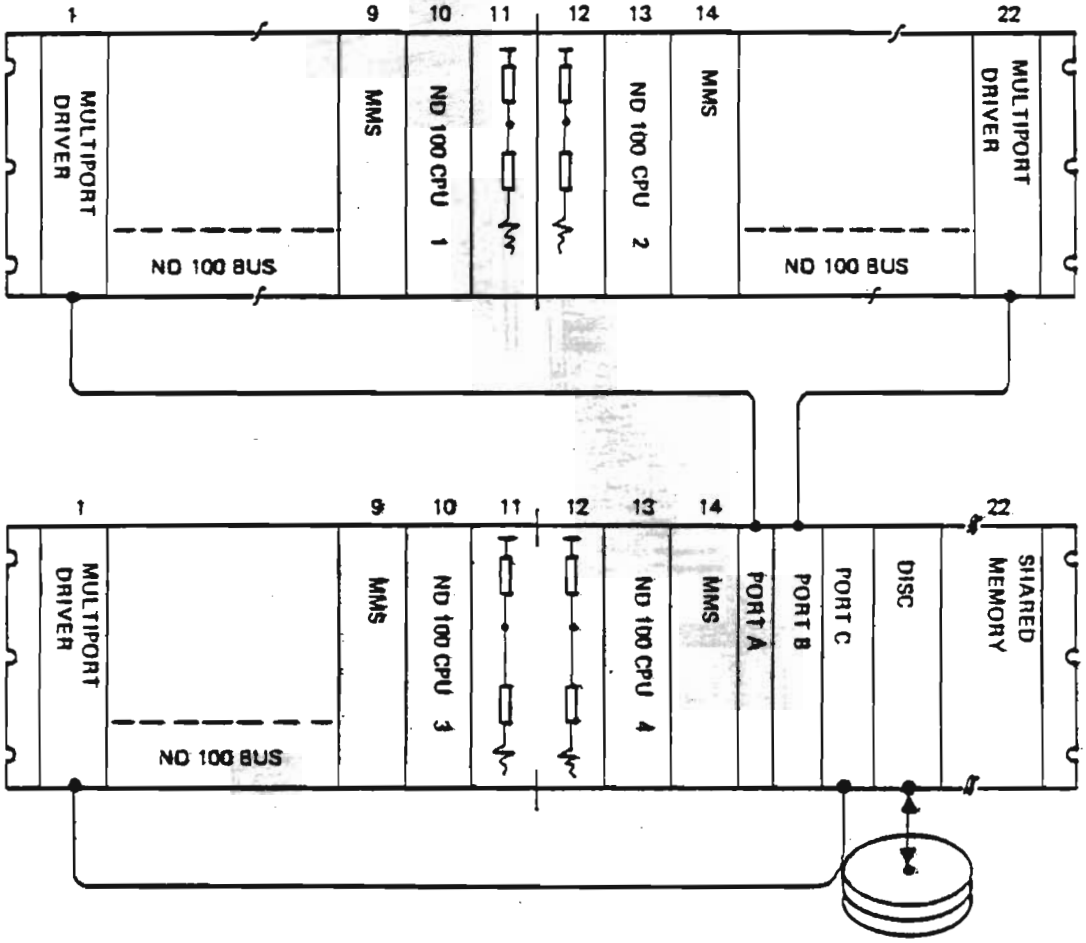

Fig. 9. Example of configuration with 2 BANK backplane

In this multi processor configuration the 2 BANK backplane is used to hold one ND-100 in each bank.
Only standard ND-100 modules are used, no MPM 4 modules except for the PORT module.

These two card-crates fit into one 11 module cabinet.
(Refer to figure 10)

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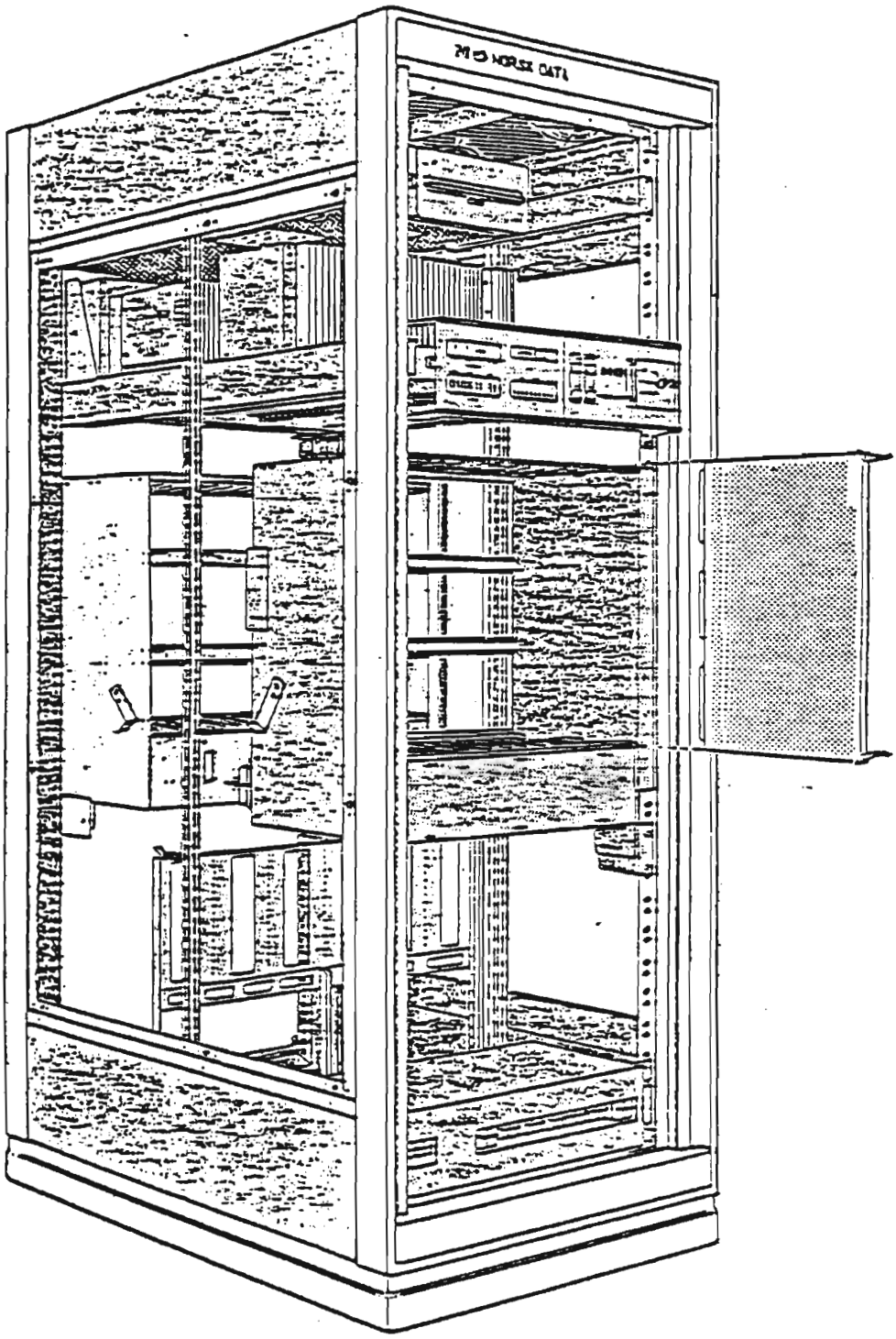

Fig. 10. 11 module cabinet with 2 ND-100 card-crates.

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9.2. MPM4 ND-100 backplane

This 15 + 6 position backplane will normally be used in ND-520 or ND-540 configurations.
The 15 positions will be a normal ND-100 bus while the 6 positions could either be used as shared memory (including ports) or as slots for I/O or DMA controllers.

Figure 11 shows a configuration where the 6 positions with DMA controllers and one multiport driver form a separate source accessing the shared memory.

In configurations demanding a high DMA transfer rate this could be a suitable solution.

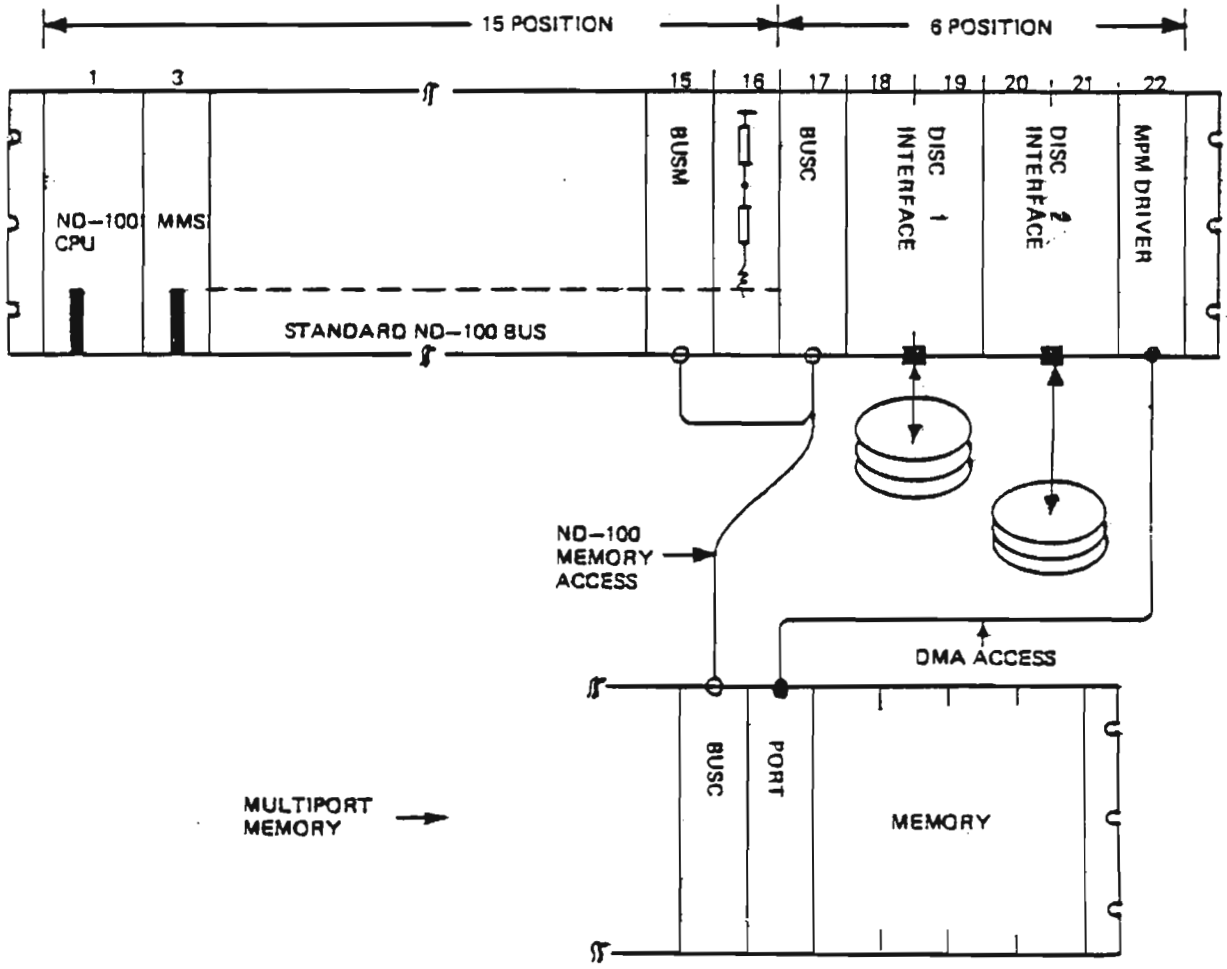

Fig. 11. MPM4 ND-100 backplane

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10. Examples of ND-500 configurations

10.1. ND-500 attachment to memory in general

The ND-500 will communicate with the memory via two separate channels, one channel for instructions and one for data.
The physical memory connection takes place via the CACHE modules.
ND-520 with no CACHE will only use the memory communication facilities on the module.
ND-540 with CACHE will use both the CACHE and the memory communication facilities.
ND-560 will have 1, 2 or 4 CACHE modules in the configuration for data and the same number for instructions.
The number of Cache modules in the ND-560 does not have to be symmetrical.
32 bits of data or instructions will pass through one CACHE module.

As the MPM 4 concept is based on memory banks of 16 bits, one ND-500 CACHE module will be connected to two 16 bits banks via two ports. one in each bank.

In most cases the data and instruction CACHE will see the same physical memory, via ports connected to the same bus. Due to flexibility in the ND-500 concept, the data and instruction channels need not overlap, but may have their own private memory.

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10.2. MPM4 2 BANK system

Figure 12 depicts an ND-560 configuration with 16 Kbytes of instruction and 16 Kbytes of data CACHE connected to a MPM4 2 BANK system. Total shared memory = 7 Mbytes (14 memory modules).

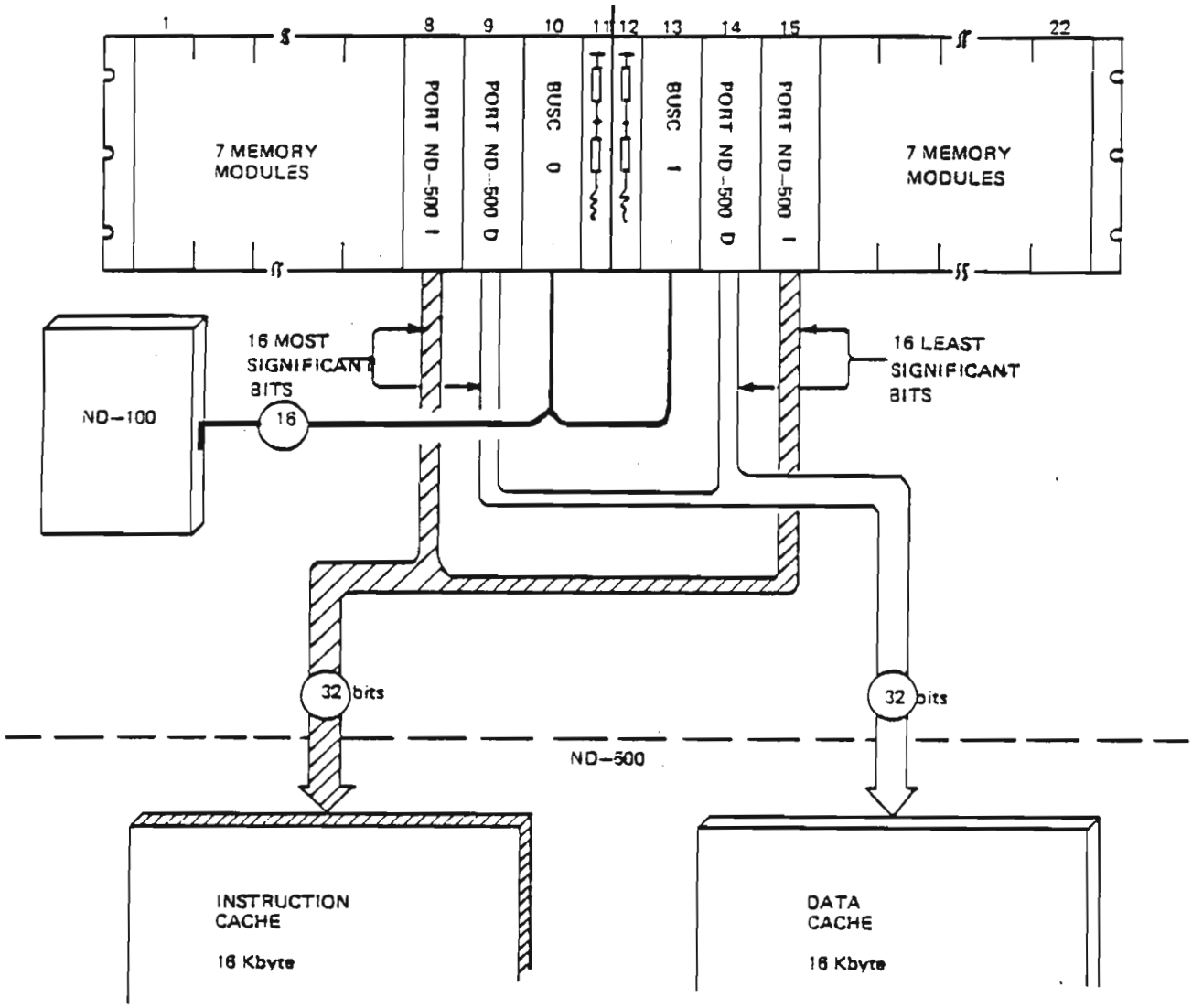

Fig. 12. MPM4 2 BANK configuration.

With 2 x 32 Kbytes CACHE (1/2 CACHE), 2 MPM4 2 BANK systems are required; this makes room for 14 Mbytes.

With 4 x 32 Kbytes CACHE (1/1 CACHE), 4 MPM4 2 BANK systems are required; this makes room for 32 Mbytes. (Maximum memory)

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10.3. MPM4 4 BANK system

Figure 13 depicts an ND-560 configuration with 32 Kbytes of instruction and 32 Kbytes of data CACHE connected to a MPM4 4 BANK system. Total shared memory = 6 Mbytes (12 memory modules).

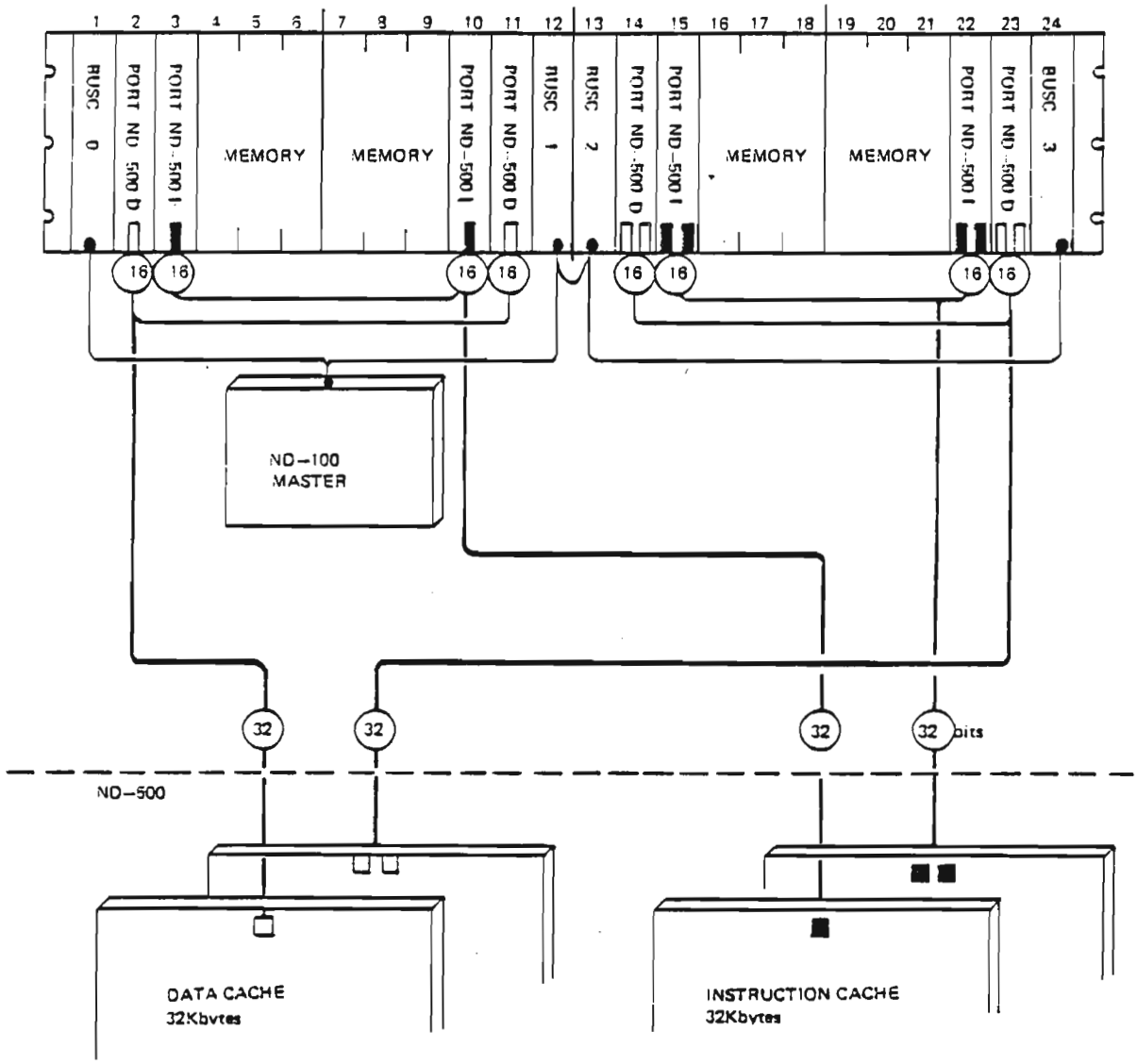

Fig. 13. MPM4 4 BANK configuration

With 2 x 4 CACHE modules 2 MPM 4 4 BANK crates are needed; this will make room for 12 Mbytes of shared memory.

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11. ND-520 and ND-540, The MINI SUPER-MINI

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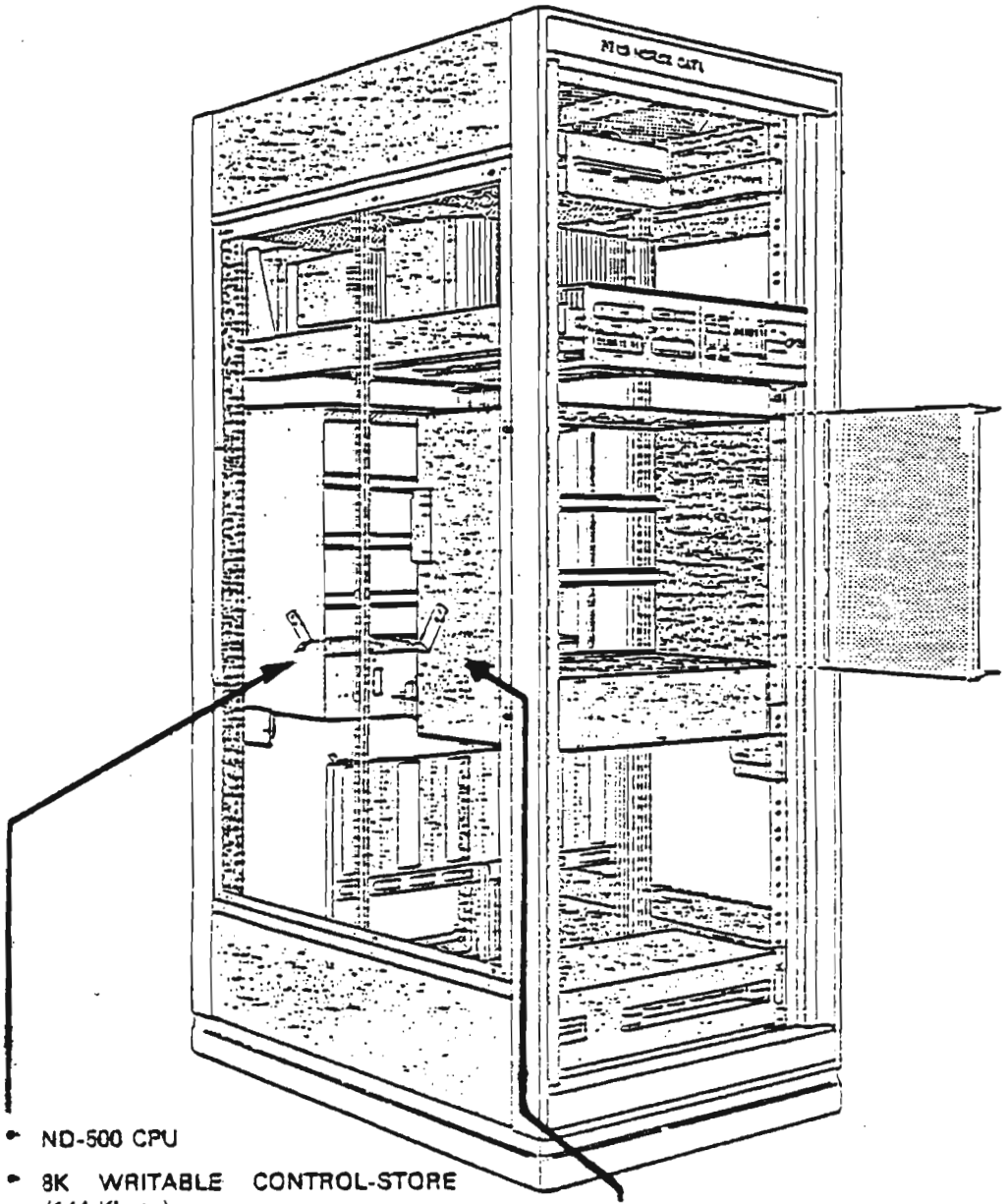

- ND-500 CPU
- 8K WRITABLE CONTROL-STORE (144 Kbyte)
- HARDWARE ARITHMETIC FOR ALL FLOATING POINT AND MPY-DIV INSTRUCTIONS
- MEMORY MANAGEMENT SYSTEM FOR DATA
- MEMORY MANAGEMENT SYSTEM FOR INSTRUCTIONS
- 16 Kbyte DATA-CACHE ND-540
  ND-520 = NO CACHE
- 16 Kbyte INSTRUCTION-CACHE ND-540
  ND-520 = NO CACHE
- LEAST SIGNIFICANT PART OF SHARED MEMORY (MAX 1Mbyte)

- ND-100 CPU
- MEMORY MANAGEMENT SYSTEM
- 2 Kbyte INSTRUCTION/DATA CACHE
- DISC CONTROLLER (2 MODULES)
- ND-500 CONTROLLER
- DMA FLOPPY CONTROLLER (DUAL DENSITY ON DUAL SIDE)
- ND-100 LOCAL MEMORY STANDARD = 1/4 Mbyte
- 6 SLOTS FOR I/O OR DMA CONTROLLER MODULES
- MOST SIGNIFICANT PART OF SHARED MEMORY (MAX 1 Mbyte)

Fig. 14. ND-520 and ND-540 cabinet

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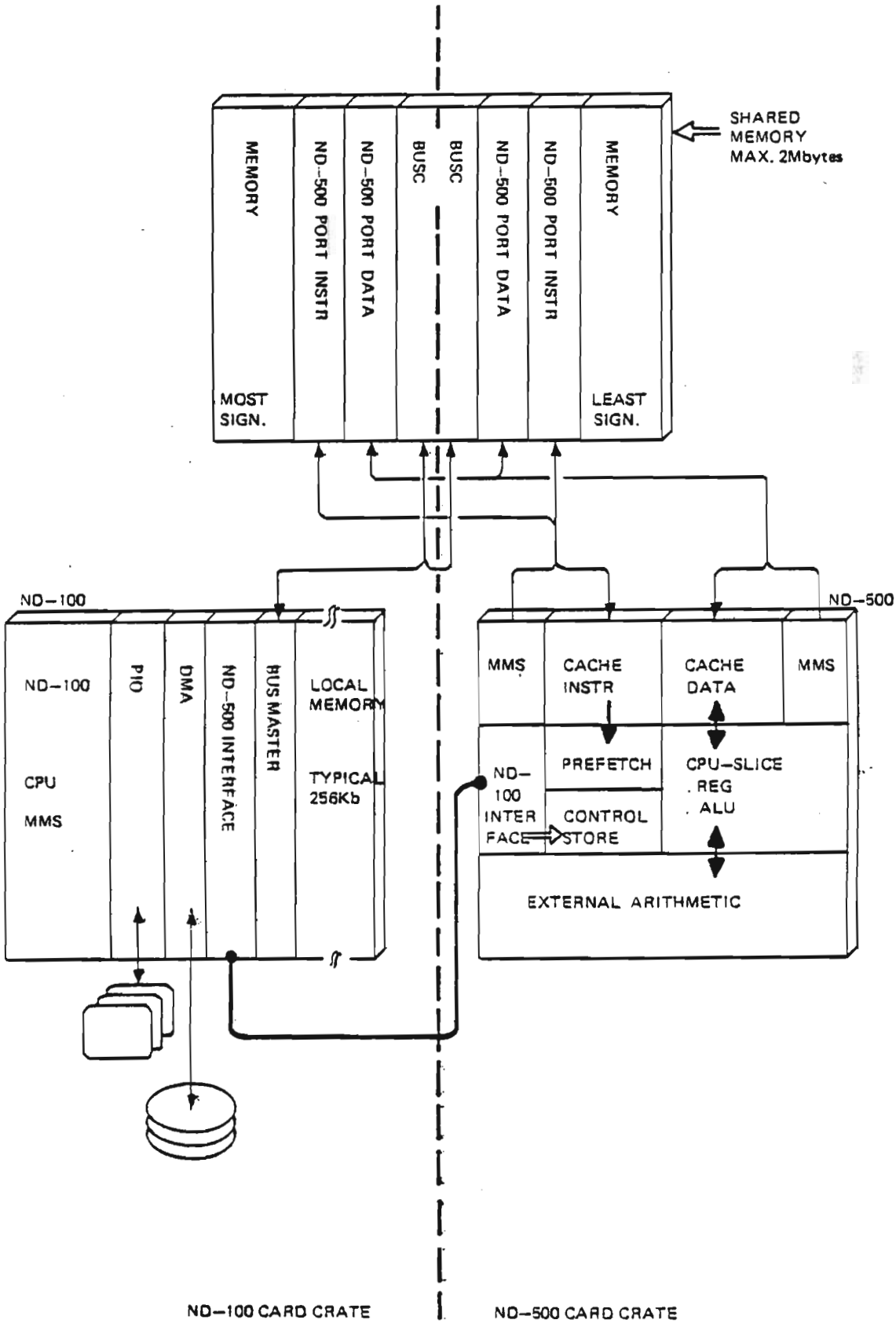

Fig. 15. ND-540 BLOCK DIAGRAM

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MPM4 ND-100 backplane.

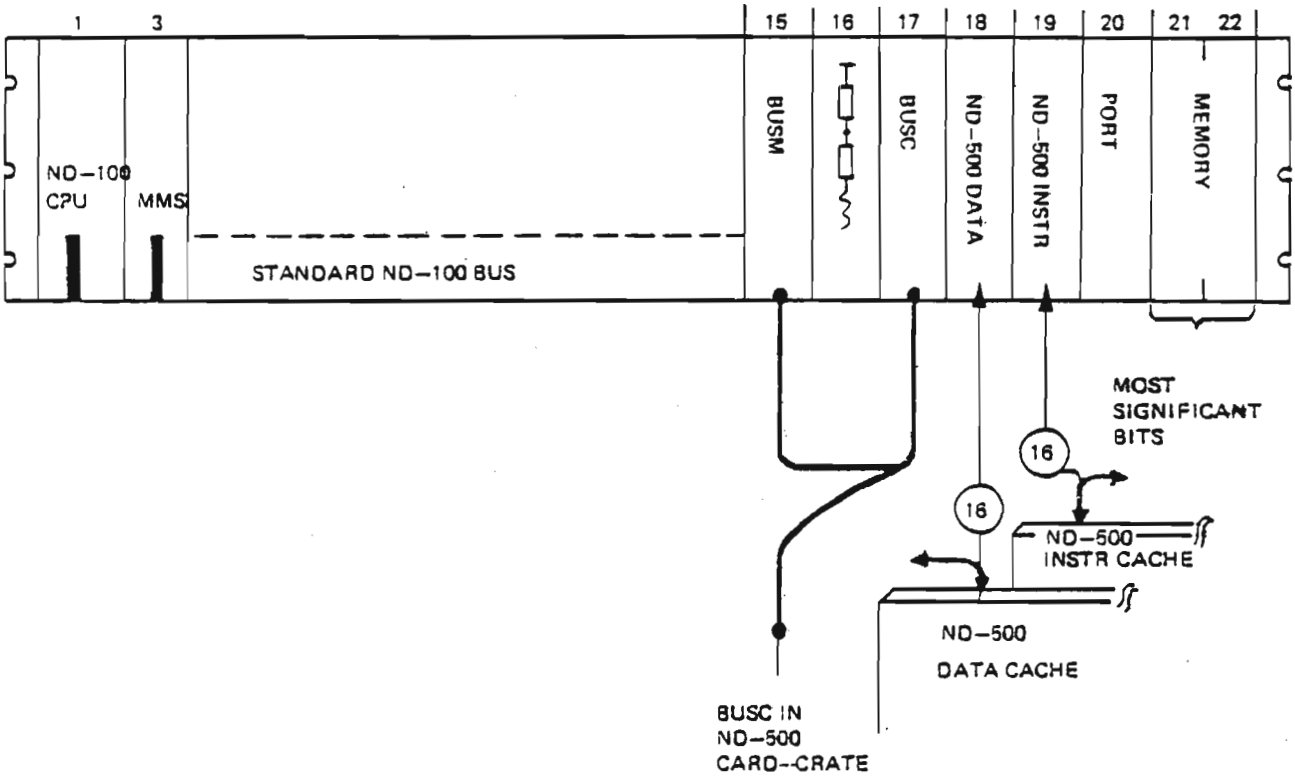

Fig. 16. MPM4 ND-100 backplane

The MPM4 ND-100 is a special backplane used in the ND-520 and ND-540 configurations.
The backplane will consist of 15 standard ND-100 bus positions plus 6 positions prewired to form the most significant part of the shared memory.

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MPM4-1 BANK backplane.

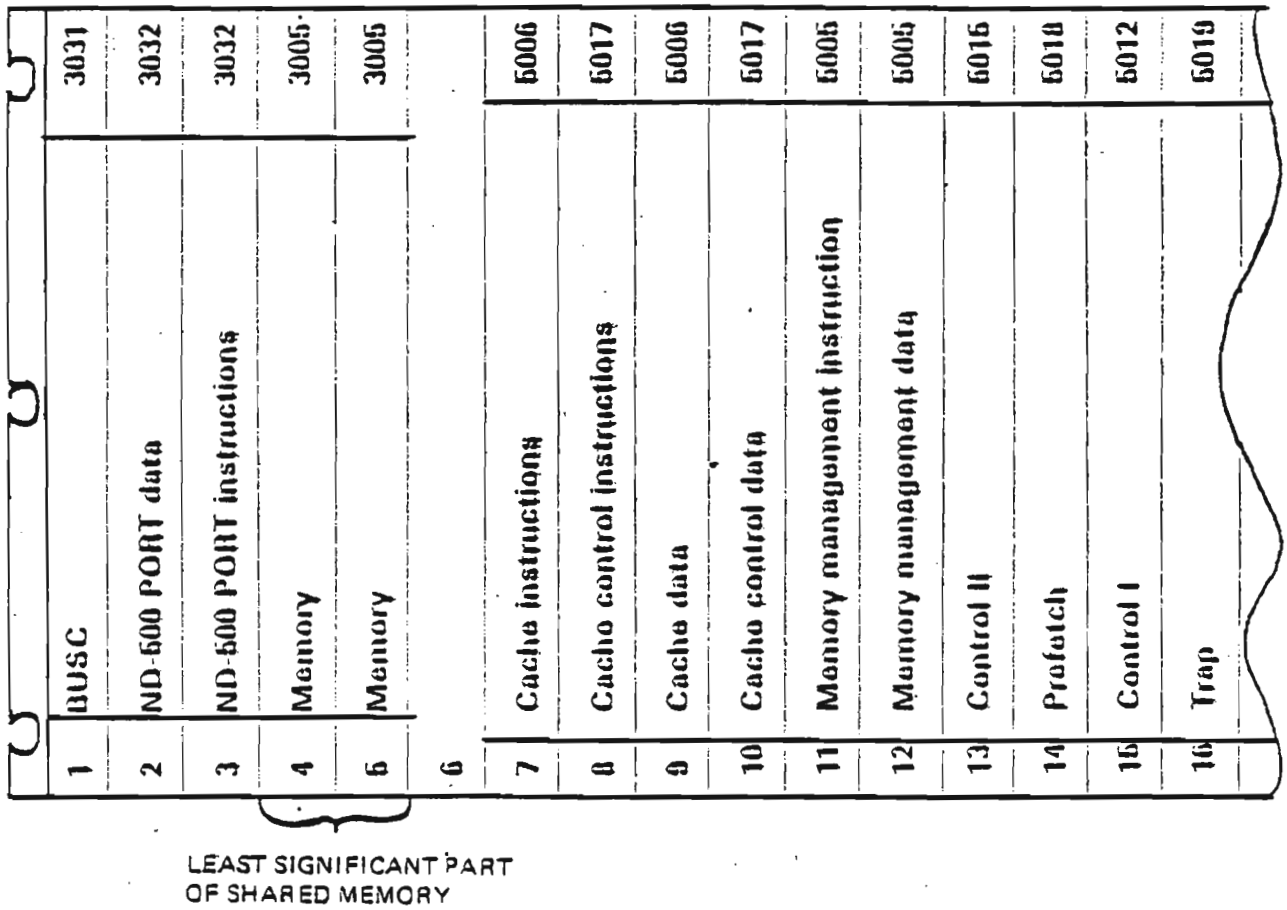

Fig. 17. MPM4-1 BANK backplane

The MPM4-1BANK is a special backplane used in the ND-520 and ND-540 configurations in the ND-500 card crate.
The backplane will consist of 21 ND-500 backplane positions (positions 7 to 27) plus 5 positions prewired to form the least significant part of the shared memory.

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A P P E N D I X A

BUS MASTER 3030 BLOCK DIAGRAM

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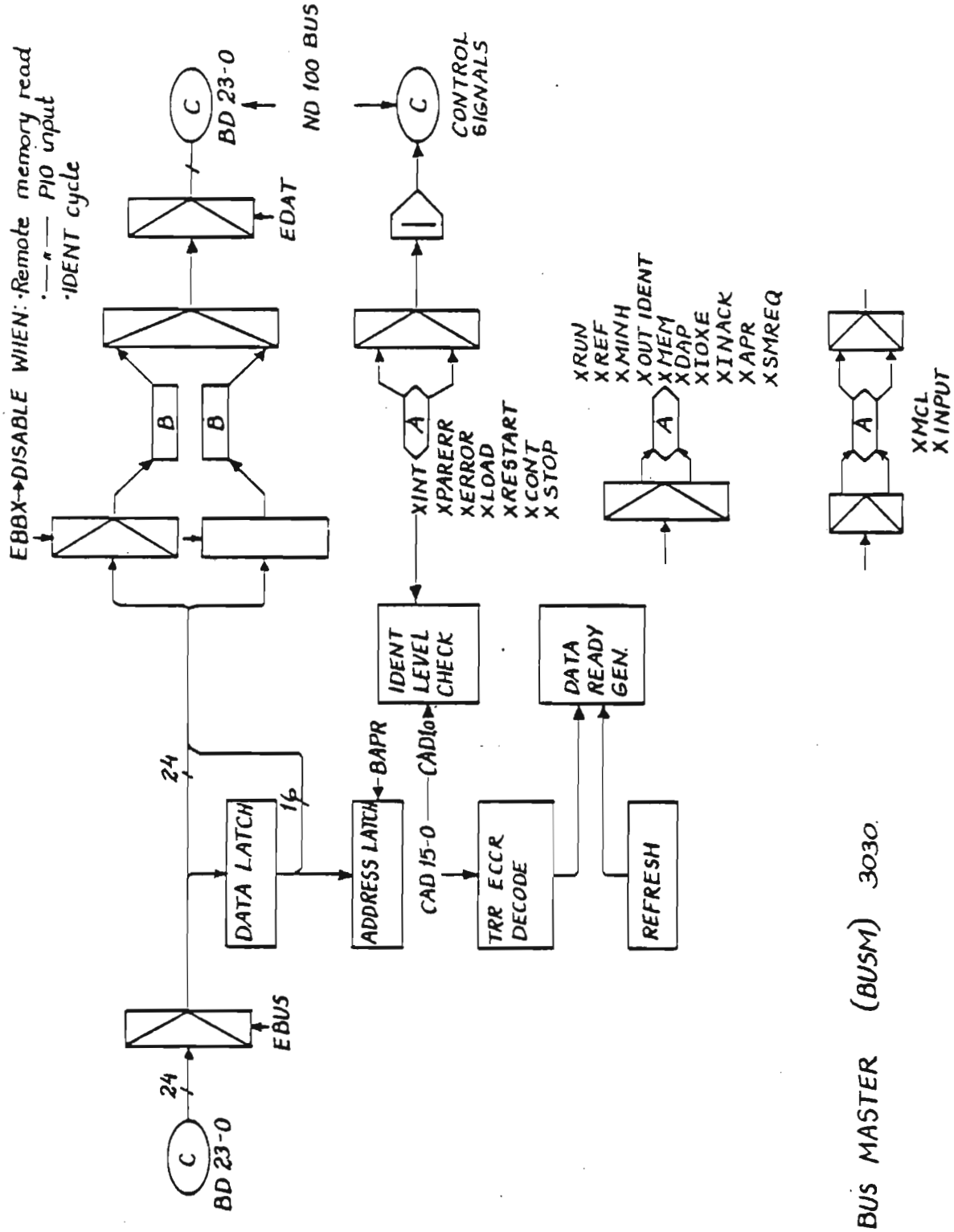

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APPENDIX B

BUS CONTROLLER 3031 BLOCK DIAGRAM

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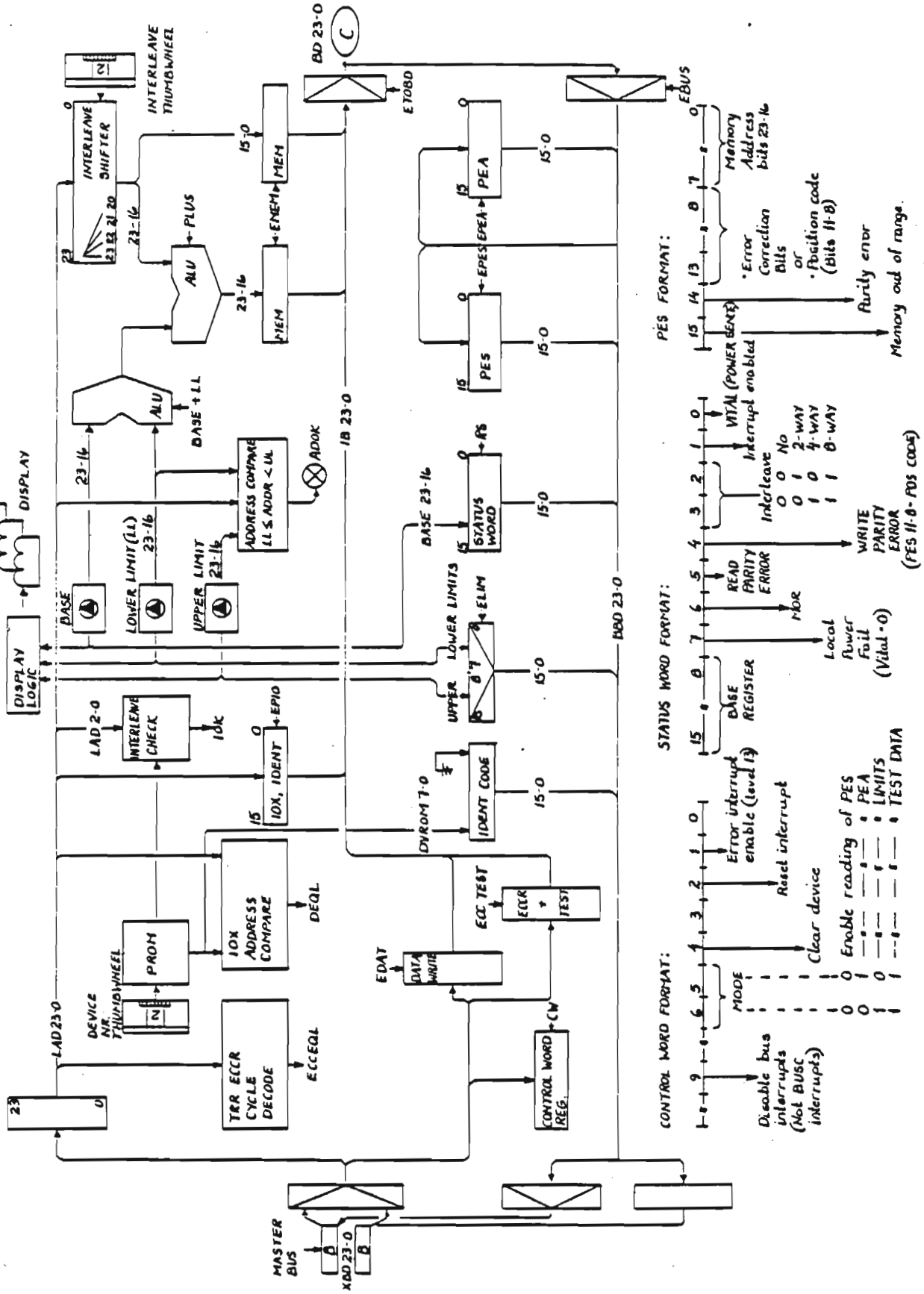
Appendix.B
BUS CONTROLLER 3031 BLOCK DIAGRAM



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APPENDIX C

MEMORY PORT 3032 BLOCK DIAGRAM

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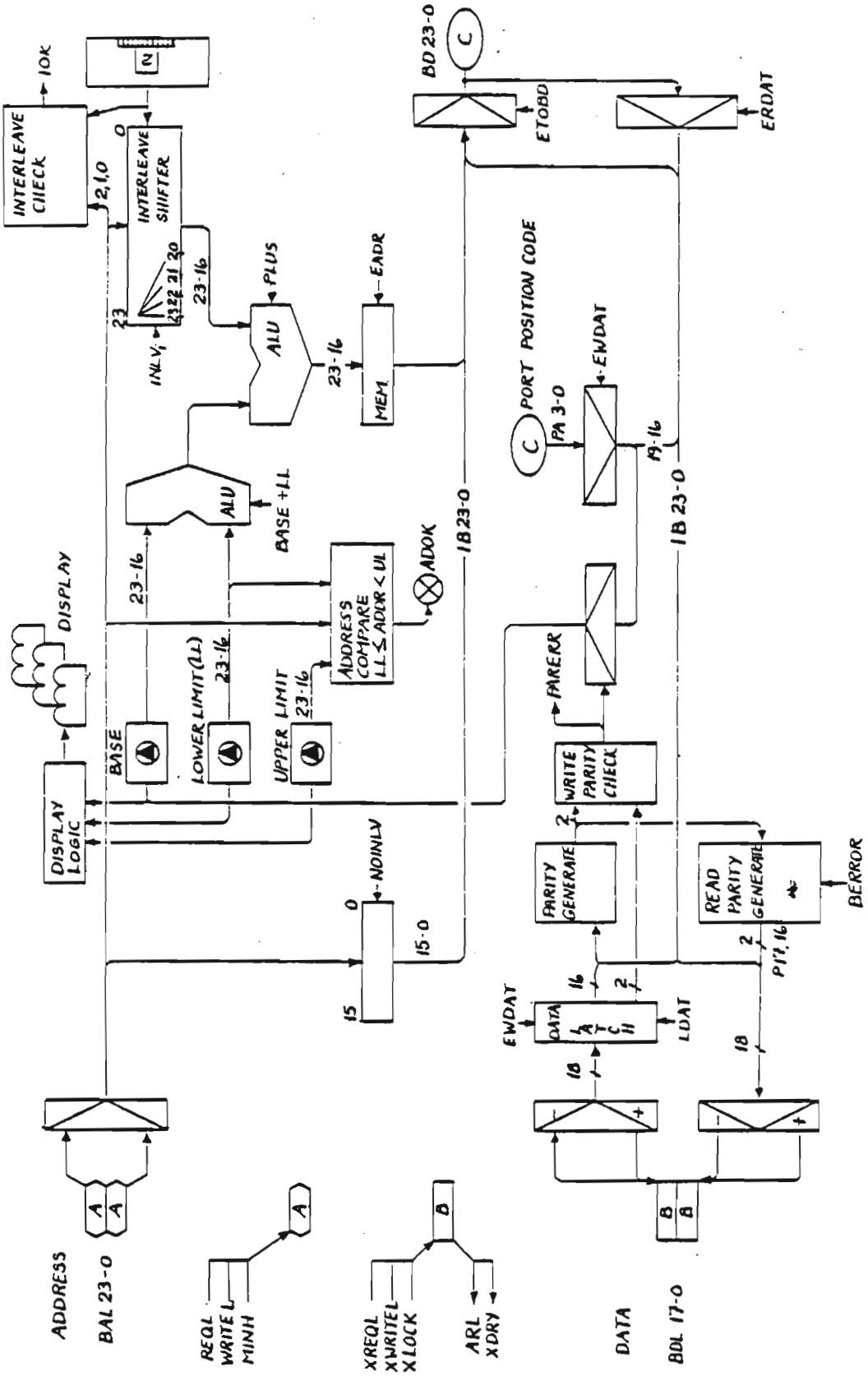

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A P P E N D I X D

MEMORY CHANNEL Signal desciption

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Below is a description of signals between the PORT and the SOURCE as seen from the SOURCE.

Address cable signals:

BA 0-23	:24 output address signals.
REQ	:Output signal for requesting a memory access.
WRITE	:Output signal indicating data direction. WRITE = 1 : Write to memory WRITE = 0 : Read from memory
XMINH	:Output signal indicating Memory Inhibit. Used to inhibit request during power down periods.

Data cable signals:

BD 0-15	:16 bidirectional data signals.
BD 16-17	:2 bidirectional signals indicating odd parity of lower and upper byte respectively.
AR	:Input signal, Address ready. Indicates that the address is accepted by a bank and that another address may be generated.
DR	:Input signal, Data ready. Indicates that write data is accepted by a bank, or that read data from memory is valid on the data lines.
LOCK	:Output signal. Used to obtain semaphore request, i.e. two consecutive cycles in a memory cell without allowing any other source to access memory.

Signal Standard

The channel signals are transmitted over differential lines conforming to CCITT-V.11 or RS-422 standard.

Cable

Cables may be 120 ohm twisted pairs or flat cables. Maximum total length of one channel is 15 meter. This limitation is due to requirement of signal quality at 10 Mbaud.

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A P P E N D I X E

MEMORY CHANNEL timing

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Timing diagrams and requirements are shown in Figures 18.

Access and Cycle Times

Access time at the port, measured as time between REQ and DR, assuming no latency.

Write: 320 ns maximum

Read: 550 ns maximum if data is good
600 ns maximum if data is corrected

Description:	Name:	Min.:	Type:	Max.:	Unit:
Address set-up time	t_{AS}	0			
Write data set-up time	t_{DS}	−75			ns
Write command before write data enabled	t_{WS}	70			ns 1)
Write data hold time	t_{DH}	0			
Write command hold time	t_{WH}	0			
Address hold time	t_{AH}	0			
Address ready pulse width	T_{ARP}	60	90		ns
Request pulse width	t_{RP}	50		∞	ns
Data ready pulse width	T_{DRP}	70	100		ns
End of address ready to next request	t_{RAR}	0			
Access time from Request to Address Ready	T_{AACC}		320		ns 2)
Write data access time	T_{WACC}		320		ns 2)
Write cycle time	T_{WCYC}		420		ns
Read command set-up time	t_{RS}	−30			ns
Read data disabled after Read Command false	T_{RDIS}	25		70	ns 1)
Read data valid before Data Ready	T_{DVAL}	0			
Read data access time (no error)	T_{RACC}		550		ns 2)
Read data access time (1 bit corrected)	T_{RACC}		600		ns 2)
Read cycle cycle time	T_{RCYC}	380	420		ns

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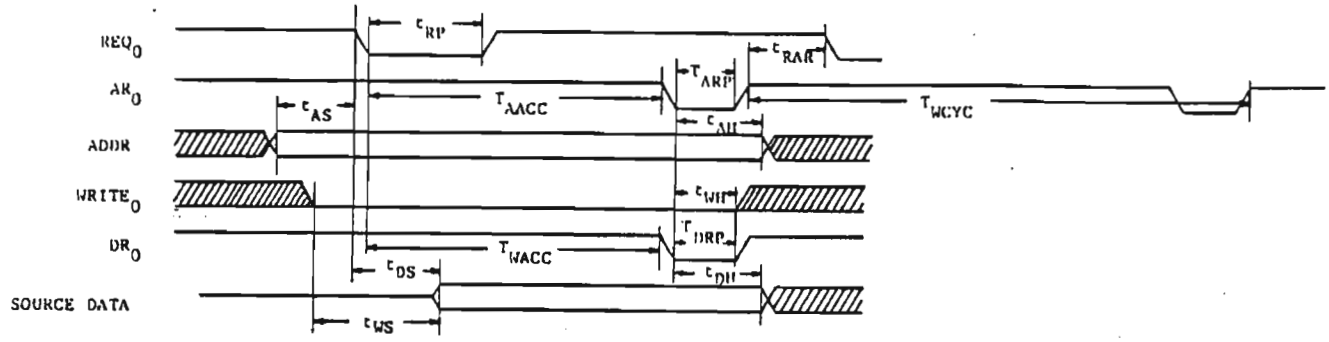
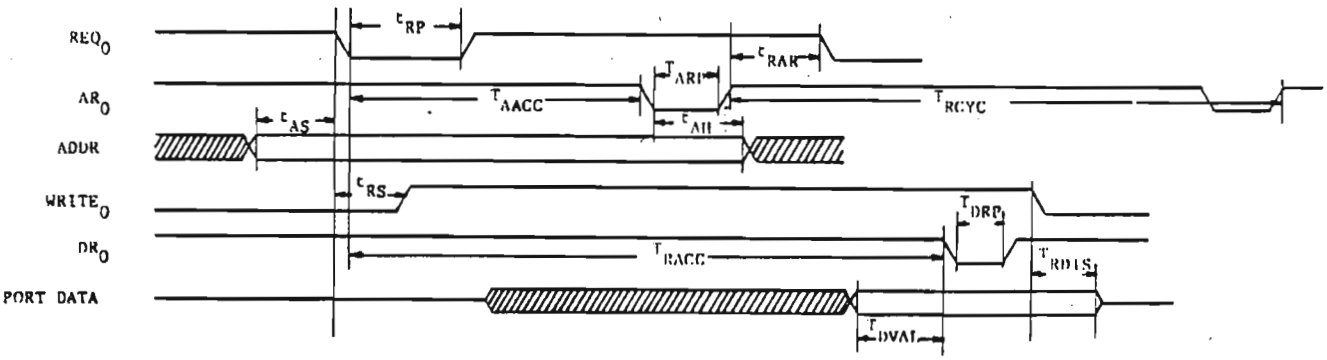


Memory Channel Write Access Timing



Memory Channel Read Access Timing

Fig. 18. Memory channel timing specifications measured at port terminals

1) Write signal should be put true as soon as possible after each read access in order to disable data driver at port.

2) Access times in case there is no waiting time due to previous accesses in the bank.

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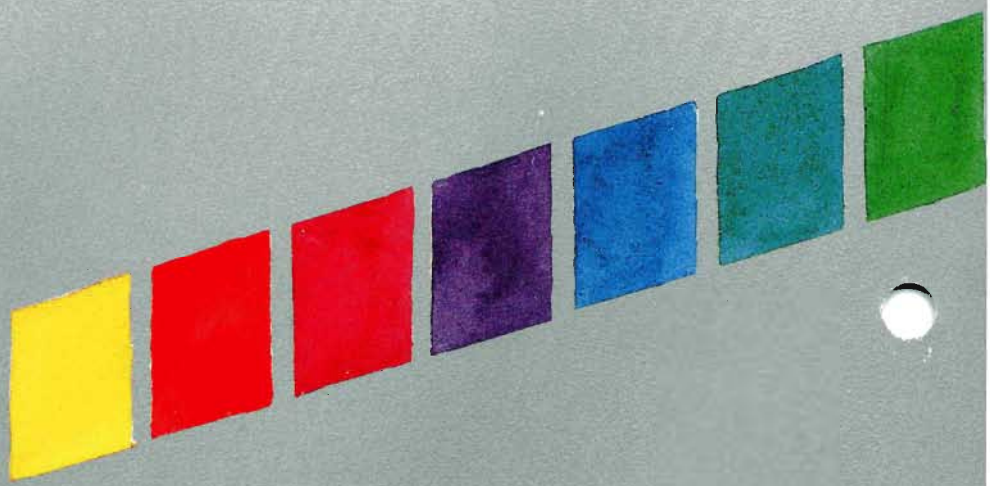

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