PROGAM SPECIFICATIONS AND SWITCH - SETTING FOR I/O CONTROL MODULES IN NORD 10 - 10/S AND COMPATIBLE I/O SYSTEMS

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TELETYPE AND DISPLAY CODING

On the NORD-10 1020/II Teletype Buffer Card there are three select functions to be set.

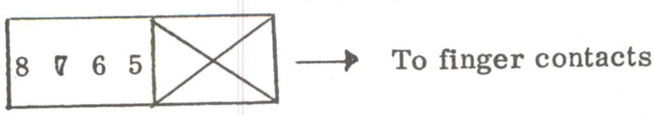
Select 1: Teletype number

Position 11A

Device number	Teletype number	(Octal)	11A1	11A2	11A3	11A4
300	1	0	OFF	OFF	OFF	OFF
310	2	1	OFF	OFF	OFF	ON
320	3	2	OFF	OFF	ON	OFF
330	4	3	OFF	OFF	ON	ON
340	5	4	OFF	ON	OFF	OFF
350	6	5	OFF	ON	OFF	ON
360	7	6	OFF	ON	ON	OFF
370	8	7	OFF	ON	ON	ON
1300	9	10	ON	OFF	OFF	OFF
1310	10	11	ON	OFF	OFF	ON
1320	11	12	ON	OFF	ON	OFF
1330	12	13	ON	OFF	ON	ON
1340	13	14	ON	ON	OFF	OFF
1350	14	15	ON	ON	OFF	ON
1360	15	16	ON	ON	ON	OFF
1370	16	17	ON	ON	ON	ON

Select 2: Frequency

Position 11A



FQ	11A5	11A6	11A7	11A8	
75 baud	ON	ON	ON	ON	
100 baud	ON	OFF	ON	ON	
110 baud	ON	OFF	ON	OFF	
150 baud	OFF	ON	ON	ON	
300 baud	OFF	OFF	ON	ON	
600 baud	OFF	OFF	OFF	ON	
1200 baud	ON	ON	ON	ON	STRAP
2400 baud	OFF	ON	ON	ON	STRAP
4800 baud	OFF	OFF	ON	ON	STRAP
9600 baud	OFF	OFF	OFF	ON	STRAP

STRAP means break connection between Q9 and Q10. Connect Q8 to Q9.

24/9/75/TU/bp

Select 3: Ident Code

Position 1E

6 5 4 3 2 1	→ To finger contacts

Teletype number	(Octal)	Ident Code	1E1	1E2	1E3	1E4	1E5	1E6
1	0	1	OFF	ON	ON	ON	ON	ON
2	1	5	OFF	ON	OFF	ON	ON	ON
3	2	6	ON	OFF	OFF	ON	ON	ON
4	3	7	OFF	OFF	OFF	ON	ON	ON
5	4	44	ON	ON	OFF	ON	ON	OFF
6	5	45	OFF	ON	OFF	ON	ON	OFF
7	6	46	ON	OFF	OFF	ON	ON	OFF
8	7	47	OFF	OFF	OFF	ON	ON	OFF
9	10	50	ON	ON	ON	OFF	ON	OFF
10	11	51	OFF	ON	ON	OFF	ON	OFF
11	12	52	ON	OFF	ON	OFF	ON	OFF
12	13	53	OFF	OFF	ON	OFF	ON	OFF
13	14	54	ON	ON	OFF	OFF	ON	OFF
14	15	55	OFF	ON	OFF	OFF	ON	OFF
15	16	56	ON	OFF	OFF	OFF	ON	OFF
16	17	57	OFF	OFF	OFF	OFF	ON	OFF

NORD-10 ASYNCHRONOUS MODEM PROGRAMMING SPECIFICATION

1046

1 ASYNCHRONOUS MODEM ADDRESSES

The codes below are relevant for the first asynchronous modem . (Modem no. 0.) The codes for the first eight modems are found by adding $10_8 \cdot N$ to the codes given. N=modem number (0, 1, 2......, 7). For the next eight modems the codes are found by adding $(1000 + 10(N-10))_8$. N=modem number $(10, 11, 12, \ldots\ldots 17)_8$.

2 INPUT CHANNEL (INTERRUPT LEVEL 12)

2.1 Read Data Register

IOX 200

The number of data bits read into the A-register is specified by bits 11 and 12 in the input channel control register. (See section 5.2). The received character is right justified. (From bit 0 and upwards).

2.2 Read Status Register

IOX 202

See section 5.1 for the specification of status bits.

2.3 Write Control Register

IOX 203

See section 5.2 for the specification of control bits.

3 OUTPUT CHANNEL (INTERRUPT LEVEL 10)

3.1 Connect Data Set to Line

IOX 204

This IOX instruction will connect the modem to the line in the same way as an external call, dependent on the input channel control register (Section 5.2).

3.2 Write Data Register

IOX 205

The number of bits specified by bits 11 and 12 in the input channel control register is written to the output data register, starting with bit 0 and counting upwards.

3.3 Read Status Register

IOX 206

See section 6.1 for the specification of status bits.

3.4 Write Control Register

IOX 207

See section 6.2 for the specification of control bits.

4 IDENT CODE

The ident code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel responding to level 10.

5 INPUT CHANNEL

5.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Framing error
	6	Parity error
	7	Overrun
	8	Carrier error
	9	Carrier error enabled
	10	Frequency status
	11	Carrier missing
	12	Connect missing
	13	Data Set Ready missing
	14	Not used
	15	Half duplex

Notes: Additional explanation to status bits.

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occured while working in parity generating/checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Bit 8: Carrier error means that the line signal (Carrier) is missing in a period where input control (and status) bit 9, Carrier error enable, is set to 1.

Bit 9: See section 5.2, bit 9 for meaning of this bit.

Bit 10: This is the status of the control signal frequency select. (Section 5.2, Bit 10.)

Bit 11: Carrier missing gives the status of receive line signal detector, or carrier on the line.

0 indicates Carrier present
1 indicates Carrier missing.

Bit 12: Connect missing gives the status of Connect Data Set to Line.

0 indicates that Connect is ON
1 indicates that Connect is OFF.

Bit 13: Data Set Ready missing gives the status of the Data Set Ready signal from the modem.

0 indicates that the modem is ready
1 indicates that the modem is not ready.

Bit 15: 0 indicates that the terminal is operated in full duplex mode
1 indicates that the terminal is operated in half duplex mode.

5.2 Control Register

Bit		
	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5-6	Not used
	7	6 sec. timeout disable
	8	2 bits timeout disable
	9	Carrier error enable
	10	Transmission frequency select
	11-12	Character length
	13	Number of stop bits
	14	Parity generation/checking
	15	Half duplex

Notes:

Bit 2: After a Master Clear or a Device Clear (bit 4), the device has to be activated by writing a 1 into bit 2 of the control register. The modem will not be connected to the line if bit 2 in the input control and status register is 0.

Bit 3: Test mode will loop transmitted data back to received data, if the other terminal is connected to the line, transmitted data will also be transferred to this terminal.

Bit 4: Gives a clear pulse to the buffer card. Disconnects modem from the line. After a Device Clear, the buffer card must be initialized.

Bit 7: 6 seconds timeout disable.
If no Carrier is received within 6 seconds after a Connect Data Set to Line signal is given to the modem, a 6 seconds timing circuit will normally turn off the Connect signal. If a 1 is written into bit 7 of the input control register, the Connect signal can only be turned off by clearing the input Activate device bit. Bit 7 is set to 0 by Master Clear and Device Clear.

Bit 8: 2 bits timeout disable.
This control signal has only meaning when the buffer is used in half duplex mode. (Control bit 15.) In that case it will cause the Request to Send signal to be turned off at the time of two bits after the last character is transmitted to the line.
If a 1 is written into this control bit, the Request to Send signal can be turned off by writing 0 into either output channel control register bit 2 or input channel control register bit 2 (which also turns off Connect Data Set to Line), or by giving a Master Clear or Device Clear. In full duplex operation, Request to Send and Connect Data Set to Line are identical. Bit 8 is set to 0 by Master Clear and Device Clear.

Bit 9: When set to 1, this signal will cause an error condition if input status bit 11 is 1. If IC means input channel control register, an IS means input channel status register, then

$$IS8=IS11 \cdot IC9$$

and

$$IS4=IS5+IS6+IS7+IS8$$

Bit 9 is set to 0 by Master Clear and Device Clear.
Note: This can give you a temporary interrupt, which can give you an interrupt on level 14 if not handled in time.

Bit 10: Selects transmission frequency when used with full duplex modem.

0 selects frequency for called station
1 selects frequency for calling station

Master Clear and Device Clear set the control bit to 0.

Bit 11-12: The content of these bits gives the following character lengths, both for the input channel and the output channel:

Bit 12	11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is added to the number given in this table.

Bit 13: The number of stop bits will be two if the control bit is 0, and one if the control bit is 1.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

Bit 15: 0 selects full duplex operation. In this case Request to Send is identical to Connect Data Set to Line.

1 selects half duplex operation. In this case Request to Send is blocked by Carrier on the line.

Master Clear and Device Clear set the Control bit to 0.

6 OUTPUT CHANNEL

6.1 Status Register

Bit	
0	Ready for transfer interrupt enabled
1	Not used
2	Device active
3	Device ready for transfer
4-9	Not used
10	Frequency status
11	Carrier missing
12	Request to Send missing
13	Ready for Sending missing
14	Not used
15	Half duplex

Notes:

Bit 2: This status bit will be 1 as long as the device is busy transmitting characters.

Bit 3: This bit indicates that the output data buffer is ready to receive a new character. This will be a 1 if bit 2 is 0, but may as well be a 1 when bit 2 is 1 due to the double buffer.

Bits 10-11: Same as for input channel (Section 5.1).

Bit 12: Gives the status of the Request to Send control signal to the modem.

0 means that Request to Send is ON.
1 means that Request to Send is OFF.

Bit 13: Gives the status of the Ready for Sending status signal from the modem.

0 means Ready for Sending.
1 means NOT Ready for Sending.

Bit 15: Same as for input channel (Section 5.1).

6.2 Control Register

Bit		
	0	Enable interrupt on device ready for transfer
	1	Not used
	2	Activate device
	3-15	Not used

Notes:

Bit 2: When operated in half duplex mode a 1 in bit 2 gives Request to Send if there is no Carrier on the line. If there is a Carrier on the line, Request to Send will go ON when the Carrier goes OFF.

7 CONTROL AND STATUS WORDS

7.1 Input

Bit	Status	Control
0	RFT en	Enable RFT
1	ERR en	Enable ERR
2	Dev. act	Activate
3	Dev. RFT	Test
4	ERR OR	Device clear
5	Framing	
6	Parity	
7	Overrun	6 sec. timeout disable
8	Carrier error	2 bits timeout disable
9	Carrier error en	Carrier error en.
10	Frq. stat	Frq. select
11	Carr. missing	Char. length
12	Conn. missing	Char. length
13	DSR missing	Stop bits
14		Parity gen/check
15	Half duplex	Half duplex

7.2 Output

Bit	Status	Control
0	RFT en	Enable RFT
1		
2	Dev. act	Activate
3	Dev. RFT	
4		
5		
6		
7		
8		
9		
10	Frq. stat	
11	Carr. missing	
12	RQTS missing	
13	RFS missing	
14		
15	Half duplex	

ASYNCHRONOUS MODEM CODING

On the NORD-10 1046 Asynchronous Modem Buffer Card there are three select functions to be set.

Select 1: Terminal number

Position 13B

[4 3 2 1] → To finger contacts

Device number	Terminal number	(Octal)	13B1	13B2	13B3	13B4
200	1	0	OFF	OFF	OFF	OFF
210	2	1	OFF	OFF	OFF	ON
220	3	2	OFF	OFF	ON	OFF
230	4	3	OFF	OFF	ON	ON
240	5	4	OFF	ON	OFF	OFF
250	6	5	OFF	ON	OFF	ON
260	7	6	OFF	ON	ON	OFF
270	8	7	OFF	ON	ON	ON
1200	9	10	ON	OFF	OFF	OFF
1210	10	11	ON	OFF	OFF	ON
1220	11	12	ON	OFF	ON	OFF
1230	12	13	ON	OFF	ON	ON
1240	13	14	ON	ON	OFF	OFF
1250	14	15	ON	ON	OFF	ON
1260	15	16	ON	ON	ON	OFF
1270	16	17	ON	ON	ON	ON

Select 2: Frequency

Position 1B

[4 3 2 1] → To finger contacts

FQ	1B1	1B2	1B3	1B4	
75 baud	ON	ON	ON	ON	
100 baud	ON	OFF	ON	ON	
110 baud	OFF	ON	OFF	ON	
150 baud	ON	ON	ON	OFF	
300 baud	ON	ON	OFF	OFF	
600 baud	ON	OFF	OFF	OFF	
1200 baud	ON	ON	ON	ON	STRAP
2400 baud	ON	ON	ON	OFF	STRAP
4800 baud	ON	ON	OFF	OFF	STRAP
9600 baud	ON	OFF	OFF	OFF	STRAP

STRAP means break connection between terminal 4 and C1. Connect C1 to C2.

Select 3: Ident Code

Position 1C

6	5	4	3	2	1	→ To finger contacts

Terminal number	(Octal)	Ident Code (Octal)	1C1	1C2	1C3	1C4	1C5	1C6
1	0	60	ON	ON	ON	ON	OFF	OFF
2	1	61	OFF	ON	ON	ON	OFF	OFF
3	2	62	ON	OFF	ON	ON	OFF	OFF
4	3	63	OFF	OFF	ON	ON	OFF	OFF
5	4	64	ON	ON	OFF	ON	OFF	OFF
6	5	65	OFF	ON	OFF	ON	OFF	OFF
7	6	66	ON	OFF	OFF	ON	OFF	OFF
8	7	67	OFF	OFF	OFF	ON	OFF	OFF
9	10	70	ON	ON	ON	OFF	OFF	OFF
10	11	71	OFF	ON	ON	OFF	OFF	OFF
11	12	72	ON	OFF	ON	OFF	OFF	OFF
12	13	73	OFF	OFF	ON	OFF	OFF	OFF
13	14	74	ON	ON	OFF	OFF	OFF	OFF
14	15	75	OFF	ON	OFF	OFF	OFF	OFF
15	16	76	ON	OFF	OFF	OFF	OFF	OFF
16	17	77	OFF	OFF	OFF	OFF	OFF	OFF

NORD-10 SYNCHRONOUS MODEM PROGRAMMING SPECIFICATION

+‡+ 1050

1 SYNCHRONOUS MODEM ADDRESSES

The codes below are relevant for the first synchronous modem. (Modem no. 0). The codes for the first eight modems are found by adding $10_8 \cdot N$ to the codes given. N=modem number (0, 1, 2,......., 7). For the next eight modems the codes are found by adding $(1000+10(N-10))_8$. N=modem number $(10, 11, 12, ...17)_8$.

2 INPUT CHANNEL (INTERRUPT LEVEL 12)

2.1 Read Data Register

IOX 100

The number of data bits read into the A-register is specified by bits 11 and 12 in the input channel control register. (See section 5.2). The received character is right justified. (From bit 0 and upwards). Resets Device Ready for Transfer.

2.2 Write into input and/or output SYN-character register.

IOX 101

The eight least significant bits in A-register are written into the SYN-character registers specified by A-register bits 8 and 9.

A 1 in bit 8 prevents writing into the input SYN-character register. A 1 in bit 9 prevents writing into the output SYN-character register.

The program sequence

```
LDA     (26          %     octal
IOX 101
```

makes the content of both input and output SYN-character registers 26_8.

The program sequence

```
LDA     (777
IOX 101
```

makes all bits in the output SYN-character register 1.

2.3 Read Status Register

IOX 102

See section 5.1 for the specification of status bits.

2.4 Write Control Register

IOX 103

See section 5.2 for the specification of control bits.

3 OUTPUT CHANNEL (INTERRUPT LEVEL 10)

3.1 Write Data Register

IOX 105

The number of bits specified by bits 11 and 12 in the input channel control register is written to the output data register, starting with bit 0 and counting upwards.

Resets device ready for transfer.

3.2 Read Status Register

IOX 106

See section 6.1 for the specification of status bits.

3.3 Write Control Register

IOX 107

See section 6.2 for the specification of control bits.

4 IDENT CODE

The ident code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel responding to level 10.

Serviced ident resets proper interrupt enabling flip-flops. The ident code for synchronous modem 0 is 4.

5 INPUT CHANNEL

5.1 Status Register

Bit	
0	Ready for transfer interrupt enabled, reset
1	Error interrupt enabled
2	Device active
3	Device ready for transfer
4	Inclusive OR of errors
5	SYN-character received
6	Parity error
7	Overrun
8	Carrier error
9	Carrier error enabled
10	Request to Send missing
11	Carrier missing
12	Connect missing
13	Data Set Ready missing
14	Ready for Sending missing
15	Half duplex

Notes: Additional explanation ot status bits.

Bit 5: SYN-character received is one of the receiver error bits, but can be separately enabled/disabled. See section 5.2, bit 8. If SYN-character error is enabled, bit 5 will be set to 1 each time a SYN-character is received, and be a 1 until disabled or the first character unequal to SYN is received.

Bit 6: Parity error means that a parity error has occured while working in parity generating/checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Bit 8: Carrier error means that the line signal (Carrier) is missing in a period where input control (and status) bit 9, Carrier error enable, is set to 1.

Bit 9: See section 5.2, bit 9 for meaning of this bit.

Bit 10: Gives the status of the Request to Send signal.

0 means that Request to Send is ON
1 means that Request to Send is OFF

Request to Send is turned ON in full fuplex mode by activating output, and in half duplex mode when output is activated and no carrier is present. Request to Send is turned OFF either programmable (writing 0 into output control register bit 2) or when connect data set to line is turned OFF.

Bit 11:	Carrier missing gives the status of receive line signal detector, or carrier on the line. 0 indicates Carrier present 1 indicates Carrier missing.
Bit 12:	Connect missing gives the status of Connect Data Set to Line. 0 indicates that Connect is ON. 1 indicates that Connect is OFF. The Connect signal is set by activating input or by a calling and is reset by a 6 sec. timeout, Master Clear and Device Clear.
Bit 13:	Data Set Ready missing gives the status of the Data Set Ready signal from the modem. 0 indicates that the modem is ready. 1 indicates that the modem is not ready.
Bit 14:	Gives the status of the Ready for Sending signal from the modem. 0 means Ready for Sending. 1 means NOT Ready for Sending.
Bit 15:	0 indicates that the terminal is operated in full duplex mode. 1 indicates that the terminal is operated in half duplex mode.

5.2 Control Register

Bit		
	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device, Connect Data Set to Line
	3	Test mode
	4	Device clear
	5-6	Not used
	7	6 sec. timeout disable
	8	SYN-character error enable
	9	Carrier error enable
	10	Receiver Reset
	11-12	Character length
	13	Odd/even parity
	14	Parity generation/checking
	15	Half duplex

Note:

Bit 2: After a Master Clear or a Device Clear (bit 4), the device has to be activated by writing a 1 into bit 2 of the control register. This also sets the Connect Data Set to Line signal.

Bit 3: Test mode will loop transmitted data back to received data at a rate of 19200 bit/s.

Bit 4: Gives a clear pulse to the buffer card. Disconnects modem from the line. After a Device Clear, the buffer card must be initialized.

Bit 7: 6 seconds timeout disable. If no Carrier is received or programmed Request to Send is given within 6 seconds after a Connect Data Set to Line signal is given to the modem, a 6 seconds timing circuit will normally turn off the Connect signal. If a 1 is written into bit 7 of the input control register, the Connect signal can only be turned off by clearing the input Activate device bit. Bit 7 is set to 0 by Master Clear and Device Clear.

Bit 8: SYN-character error enable gives a possibility to detect received SYN-characters without bit-pattern recognition in software. If enabled, a received SYN-character gives error interrupt. If bit 8 is set to 0, received SYN-characters will NOT give error interrupts. Master Clear and Device Clear disables SYN-character error.

Bit 9: When set to 1, this signal will cause an error condition if input status bit 11 is 1. If IC means input channel control register, an IS means input channel status register, then

$$IS8 = IS11 \cdot IC9$$

and

$$IS4 = IS5+IS6+IS7+IS8$$

Bit 9 is set to 0 by Master Clear and Device Clear.

Note: This can give you a temporary interrupt, which can give you an interrupt on level 14 if not handled in time.

Bit 10: A 1 in this bit gives a Receiver Reset pulse. This causes the receiver to be set in a SYN-character searching mode. If Ready for transfer an/or any of the error conditions except carrier error are set, they will be reset.

In the search mode the serielly received data bit stream is examined on a bit by bit basis until a SYN-character is found. A SYN-character is found, by definition, when the contents of the receiver SYN-character register and the receiver shift register are identical. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register, and at the same time device ready for transfer is given.

Bit 11 - 12: The content of these bits gives the following character lengths, both for the input channel and the output channel:

Bit 12	11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is added to the number given in this table on the transmission side, and checked and removed a parity bit on the receiving side.

Bit 13: If the interface is in a parity generating/checking mode (bit 14), then

0 is used for odd parity, and
1 is used for even parity.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an odd or even parity bit to the character on the output channel, and give an error indication if the received character has wrong parity. (See bit 13.)

Bit 15: 0 selects full duplex operation.

1 selects half duplex operation.

Master Clear and Device Clear set the bit to 0.

6 OUTPUT CHANNEL

6.1 Status Register

Bit		
	0	Ready for transfer interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	SYN-character transmitted
	6-9	Not used
	10-15	Identical to input channel status register

Note:

Bit 2: This status bit will be 1 as long as the modem is ready to transmit characters.

Bit 3: This bit indicates that the output data buffer is ready to receive a new character. This will be a 1 if bit 2 is 0, but may as well be a 1 when bit 2 is 1 due to the double buffer.

Bit 4 - 5: These bits are identical, and is set to 1 if the transmitted character is taken from the transmitter SYN-character register. This is done only when the transmitter buffer register is empty. If output error interrupt is enabled, this will cause an error interrupt on level 10.

6.2 Control Register

Bit	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device, Request to Send
	3-15	Not used

Note:

Bit 2: When operated in half duplex mode a 1 in bit 2 gives Request to Send if there is no Carrier on the line. If there is a Carrier on the line, Request to Send will go ON when the Carrier goes OFF. In full duplex mode, Request to Send is independed of Carrier.

7 CONTROL AND STATUS WORDS

7.1 Input

Bit	Status	Control
0	RFT en	Enable RFT
1	ERR en	Enable ERR
2	Dev. act	Activate, Connect
3	Dev. RFT	Test
4	ERR OR	Device clear
5	SYN received	
6	Parity	
7	Overrun	6 sec. timeout disable
8	Carrier error	SYN err en
9	Carrier error en	Carrier error en.
10	RQTS missing	Receiver Reset
11	Carr. missing	Char. length
12	Conn. missing	Char. length
13	DSR missing	Odd/Even parity
14	RFS missing	Parity gen/check
15	Half duplex	Half duplex

7.2 Output

Bit	Status	Control
0	RFT en	Enable RFT
1	ERR en	Enable ERR
2	Dev. act	Activate, RQTS
3	Dev. RFT	
4	ERR OR	
5	SYN transmitted	
6		
7		
8		
9		
10	RQTS missing	
11	Carr. missing	
12	Con. missing	
13	DSR missing	
14	RFS missing	
15	Half duplex	

SYNCHRONOUS MODEM CODING

On the NORD-10 1050 Synchronous Modem Buffer Card there are two select functions to be set.

Select 1: Terminal number. Position 15E
Select 2: Ident code. Position 1E.

15E [4 3 2 1] To finger contacts   1E [4 3 2 1] To finger contacts

Device Number	Modem number	Octal	Ident Code	15E1	15E2	15E3	15E4	1E1	1E2	1E3	1E4
100	1	0	4	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
110	2	1	14	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
120	3	2	20	OFF	OFF	ON	OFF	ON	ON	OFF	ON
130	4	3	24	OFF	OFF	ON	ON	OFF	ON	OFF	ON
140	5	4	30	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
150	6	5	34	OFF	ON	OFF	ON	OFF	OFF	OFF	ON
160	7	6	40	OFF	ON	ON	OFF	ON	ON	ON	OFF
170	8	7	10	OFF	ON	ON	ON	ON	OFF	ON	ON

NORD-10 TERMINAL BUFFER PROGRAMMING SPECIFICATION

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1 TERMINAL BUFFER ADDRESSES

The codes below are relevant for the first terminal. The codes for the first sixteen terminals are found by adding $10_8 \cdot N$ to the codes given. N= terminal number $(0, 1, 2........, 17)_8$. For the next sixteen terminals the codes are found by adding $(1000 + 10(N-20))_8$. N=terminal number $(20, 11, 12,......37)_8$. Further information in section 11.

2 INPUT CHANNEL (INTERRUPT LEVEL 12)

2.1 Read Data Register

IOX 200

The number of data bits read into the A register is specified by bits 11 and 12 in the input channel control register. (See section 6.2). The received character is right justified. (From bit 0 and upwards).

2.2 Read Status Register

IOX 202

See section 6.1 for the specification of status bits.

2.3 Write Control Register

IOX 203

See section 6.2 for the specification of control bits.

3 OUTPUT CHANNEL (INTERRUPT LEVEL 10)

3.1 Write Data Register

IOX 205

The number of bits specified by bits 11 and 12 in the <u>input</u> channel control register is written to the output data register, starting with bit 0 and counting upwards.

3.2 Read Status Register

IOX 206

See section 7.1 for the specification of status bits.

3.3 Write Control Register

IOX 207

See section 6.2 for the specification of control bits.

4 DATARATE SELECTION

IOX 201

See section 9 for baud rate selection, using either external or internal oscillator. A change in the data rate selection must be followed by a programmed device clear.

5 IDENT CODE

The ident code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel responding to level 10. The selection of different ident codes are given by the section 10.

6 INPUT CHANNEL

6.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Not used
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Framing error
	6	Parity error
	7	Overrun
	8 9 10	Not used
	11	Carrier missing
	12	Request to Send missing
	13	Ready for Sending missing
	14	Not used
	15	Half duplex

Notes: Additional explanation to status bits.

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occured while working in parity generating/checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Bit 11: Carrier missing gives the status of the Received Line Signal Detector (circuit 109), or carrier on the line.

0 indicates carrier present.

1 indicates carrier missing.

In the case of current loop terminals, the bit is always 0.
For direct connected terminals using V-24 or EIA RS-232C interface levels, this bit gives the status of the Request to Send line in the terminal (circuit 105).

Bit 12: Request to Send missing gives the status of the Request to Send interface signal (circuit 105) from the Terminal Buffer to the Data Set or Terminal.

0 indicates that RQTS is ON.

1 indicates that RQTS is OFF.

For current loop terminals, the bit is always 0. When the interface is directly connected to a terminal using V-24 or EIA RS-232C signal levels, this signal is connected to circuit 109, Received Line Signal Detector in the terminal.

Bit 13: Ready for Sending missing gives the status of the Ready for Sending signal (circuit 106) to the Terminal Buffer.

0 indicates that the modem or terminal is ready to receive data.

1 indicates that no data should be send, and this is prevented in hardware by holding the transmitter clock.

For current loop terminals, this bit is always 0. For direct connected V-24 or EIA RS-232C terminals this signal is connected to circuit 108/2, Data Terminal Ready.

Bit 15: Half Duplex

0 indicates full duplex communication.

1 indicates half duplex communication.

The status of this bit will be as written into the control register.

6.2 Control Register

Bit		
Bit	0	Enable interrupt on device ready for transfer
	1	Not used
	2	Activate device
	3	Test mode
	4	Device clear
	5-6	Not used
	7	Carriage return delay enable
	8, 9, 10	Not used
	11-12	Character length
	13	Number of stop bits
	14	Parity generation/checking
	15	Half duplex

Notes:

Bit 2: After a Master Clear or a Device Clear (bit 4), the device has to be activated by writing a 1 into bit 2 of the control register. If not, received data will not be clocked into the receiver data buffer. The control bit will be 1 until 0 is written into it, or it is cleared by Master Clear or Device Clear.

Bit 3: Test mode will loop transmitted data back to received data, and if the other terminal is connected to the line, transmitted data will also be transferred to this terminal.

Bit 4: Gives a clear pulse to the buffer card. After a Device Clear, the buffer card must be initialized.

Bit 7: Carriage return delay enable. If set to 1, this bit will cause a delay of 200-250 milliseconds each time an ASCII carriage return (octal value 15) is transmitted to the terminal. (Useful for Silent 700 terminal with data rate 300 bits/second) Characters with octal values 14, 16 and 17 (form feed, shift out and shift in) will also cause the same delay. (The parity bit is not checked.)

Bit 11-12: The content of these bits gives the following character lengths, both for the input channel and the output channel:

Bit 12	Bit 11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is added to the number given in this table.

Bit 13: The number of stop bits will be two if the control bit is 0, and one if the control bit is 1.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

Bit 15: This bit has only meaning when the V-24 (EIA RS-232C) part of the interface is used.

If full duplex (bit 15=0) is selected, Request to Send will be constant in ON position. If half duplex (bit 15=1) is selected, Request to Send will be turned ON when the output character register is loaded, and automaticly turned OFF when the output character register is empty.

7 OUTPUT CHANNEL

7.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Not used
	2	Device active
	3	Device ready for transfer
	4-10	Not used
	11	Carrier missing
	12	Request to Send missing
	13	Ready for Sending missing
	14	Not used
	15	Half duplex

Notes:

Bit 2: This status bit will be 1 as long as the device is busy transmitting characters.

Bit 3: This bit indicates that the output data buffer is ready to receive a new character. This will be a 1 if bit 2 is 0, but may as well be a 1 when bit 2 is 1 due to the double buffer.

Bits 11-15: Same as for input channel (section 6.1).

7.2 Control Register

Bit	0	Enable interrupt on device ready for transfer
	1-15	Not used

Notes:

The device is activated when a character is loaded into the output character register (section 3.1). There is no need for separat activation.

8 CONTROL AND STATUS WORDS

8.1 Input

Bit	Status	Control
0	RFT en	Enable RFT
1		
2	Dev. act.	Activate
3	Dev. RFT	Test
4	ERR OR	Device clear
5	Framing	
6	Parity	
7	Overrun	Carriage return delay enable
8		
9		
10		
11	Carr. missing	Char. length
12	Request to Send missing	Char. length
13	Ready for Sending missing	Stop bits
14		Parity gen./check
15	Half Duplex	Half Duplex

8.2 Output

Bit	Status	Control
0	RFT en	Enable RFT
1		
2	Dev. act.	
3	Dev. RFT	
4		
5		
6		
7		
8		
9		
10		
11	Carr. missing	
12	RQTS missing	
13	RFS missing	
14		
15	Half duplex	

9 DATA RATE SELECTION

There are several possibilities to control the data rate for input and output serial data.

The data rate can be selected by:

a) EXTERNAL OSCILLATOR (16 x the bit rate), common for both input and output. The external oscillator is connected to card terminal 81 with a TTL or CCITT - V.24 (EIA RS-232C) signal level.

In this case a high signal has to be connected to terminal 80 (select external oscillator). Switches as for 9600 baud.

b) SWITCH SETTING on card. Independant speed for input and output. The switch in position 9B6 must be in the ON position, and the switch setting is sensed each time Master Clear is pressed. The selectable baud rates are: 9600, 4800, 2400, 1200, 600, 300, 200, 150, 110, 100, 75 and 50. In this case, no high signal must be connected to terminal 81. A high signal to terminal 80 will stop both input and output as long as the signal is high (BUSY).

Switch settings for the different baud rates are given in table 9.1.

c) IOX INSTRUCTION. The baud rate selection by software corresponds much to the switch setting referred to under b).

Input and output are independant, and are selected by the same IOX instruction (Group device number + 1). The content of the A register before the IOX instruction is executed determines the baud rate. The 4 least significant bits (0-3) are used for the input channel, and the next 4 (bits 4-7) are used for the output channel. Table 9.1 gives the bit pattern and corresponding baud rate.

The BUSY signal (terminal 80) will, as mentioned under b), stop the feeding of input and output data.

If the switch in position 9B6 is ON, pressing of the Master Clear button will select the baud rate given by the switches (15E1-15E8). If the switch in position 9B6 is OFF, the baud rate setting is only due to the IOX instruction, and is not changed by pressing Master Clear.

Note: A programmed device clear has no influence on the baud rate setting, but must always be given after the baud rate has been changed.

Table 9.1

INPUT CHANNEL (TO THE COMPUTER)

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REG.								
	15E4	15E3	15E2	15E1	Bit 7							Bit 0	Octal
9600	ON	ON	ON	ON	X	X	X	X	0	0	0	0	0
4800	ON	ON	ON	OFF	X	X	X	X	0	0	0	1	1
2400	ON	ON	OFF	ON	X	X	X	X	0	0	1	0	2
1200	ON	ON	OFF	OFF	X	X	X	X	0	0	1	1	3
600	OFF	ON	ON	ON	X	X	X	X	1	0	0	0	10
300	OFF	ON	ON	OFF	X	X	X	X	1	0	0	1	11
200	OFF	OFF	ON	OFF	X	X	X	X	1	1	0	1	15
150	OFF	ON	OFF	ON	X	X	X	X	1	0	1	0	12
110	OFF	OFF	ON	ON	X	X	X	X	1	1	0	0	14
100	OFF	OFF	OFF	ON	X	X	X	X	1	1	1	0	16
75	OFF	ON	OFF	OFF	X	X	X	X	1	0	1	1	13
50	OFF	OFF	OFF	OFF	X	X	X	X	1	1	1	1	17

OUTPUT CHANNEL (FROM THE COMPUTER)

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REG.								
	15E8	15E7	15E6	15E5	Bit 7							Bit 0	Octal
9600	ON	ON	ON	ON	0	0	0	0	X	X	X	X	000
4800	ON	ON	ON	OFF	0	0	0	1	X	X	X	X	020
2400	ON	ON	OFF	ON	0	0	1	0	X	X	X	X	040
1200	ON	ON	OFF	OFF	0	0	1	1	X	X	X	X	060
600	OFF	ON	ON	ON	1	0	0	0	X	X	X	X	200
300	OFF	ON	ON	OFF	1	0	0	1	X	X	X	X	220
200	OFF	OFF	ON	OFF	1	1	0	1	X	X	X	X	320
150	OFF	ON	OFF	ON	1	0	1	0	X	X	X	X	240
110	OFF	OFF	ON	ON	1	1	0	0	X	X	X	X	300
100	OFF	OFF	OFF	ON	1	1	1	0	X	X	X	X	340
75	OFF	ON	OFF	OFF	1	0	1	1	X	X	X	X	260
50	OFF	OFF	OFF	OFF	1	1	1	1	X	X	X	X	360

Note: Input and output baud rates are selected by the same IOX instruction. If the A register is set to octal value 14 before the IOX instruction is executed, 110 baud will be selected for input, and 9600 baud will be selected for output. To get 110 baud on both input and output channel, the octal value 314 should be placed in the A register before the IOX instruction is executed.

10 IDENT CODES AND INTERRUPT MECHANISM

10.1 Ident Codes

The ident codes are binary coded by the switches in position 1E, with 0 corresponding to ON and 1 corresponding to OFF.

Examples:

Ident code	1E7	1E6	1E5	1E4	1E3	1E2	1E1
0_8	ON	ON	ON	ON	ON	ON	ON
1_8	ON	ON	ON	ON	ON	ON	OFF
2_8	ON	ON	ON	ON	ON	OFF	ON
60_8	ON	OFF	OFF	ON	ON	ON	ON
77_8	ON	OFF	OFF	OFF	OFF	OFF	OFF
155_8	OFF	OFF	ON	OFF	OFF	ON	OFF

All ident codes from 0 to 177_8 can be selected.

10.2 Interrupt Mechanism

What is needed for a device to give an interrupt?

First of all the device must be ready for a transfer, i.e. status bit 3 must be on. For input this means that a whole character is received by the input buffer, and is ready to be read into the A register. For output it means that it is possible to place at least one more character in the output buffer. Secondly, interrupt on ready for transfer must be enabled. It means that a 1 is written into the control register bit 0 (which also is status register bit 0). The AND function of Ready for Transfer and Ready for Transfer Interrupt Enabled is gated to "wire-or" lines, separate for input and output. Input is connected to interrupt level 12 (terminal 35) and output is connected to interrupt level 10 (terminal 27).

When an interrupt is detected (dependant on the status in CPU and the program), the CPU usually responds by executing an IDENT instruction for the interrupting level. The level shift an interrupt mechanism in the CPU will not be described here. What is usually seen on the card is that sooner or later the INIDENT signal (terminal 7) will occur with the correct level code (determined by Bus Address bits 0 and 1 (terminals 32 and 33). The timing here is that the Bus Address bits occur before INIDENT, giving the INT signal (11C8) time to go on before the INIDENT signal occurs. Now, one part of the schotky data selector/multiplexer (74S157) in position 13A is used as a latch, freezing the status of the INT signal at the moment INIDENT occurs. If it is a 1, TINT will be a 1. This in turn results in INPUT and CONNECT back to the CPU, and the interrupt enable flip-flop for the selected level is cleared by CLINT (13A7) gated through the 74157circuit in position 11A. (11A4 or 11A7.) As the interrupt flag is AND function of the enable flip-flop and the Ready for Transfer status, the flag is cleared when the enable flip-flop is cleared.

Together with CONNECT and INPUT back to the CPU,the Ident Code is gated to the Data Bus (DB 0-7).

The ident code is identical for input and output channel.

11 DEVICE NUMBER SELECTION

Device numbers are selected by the switches in position 9B. The combinations are:

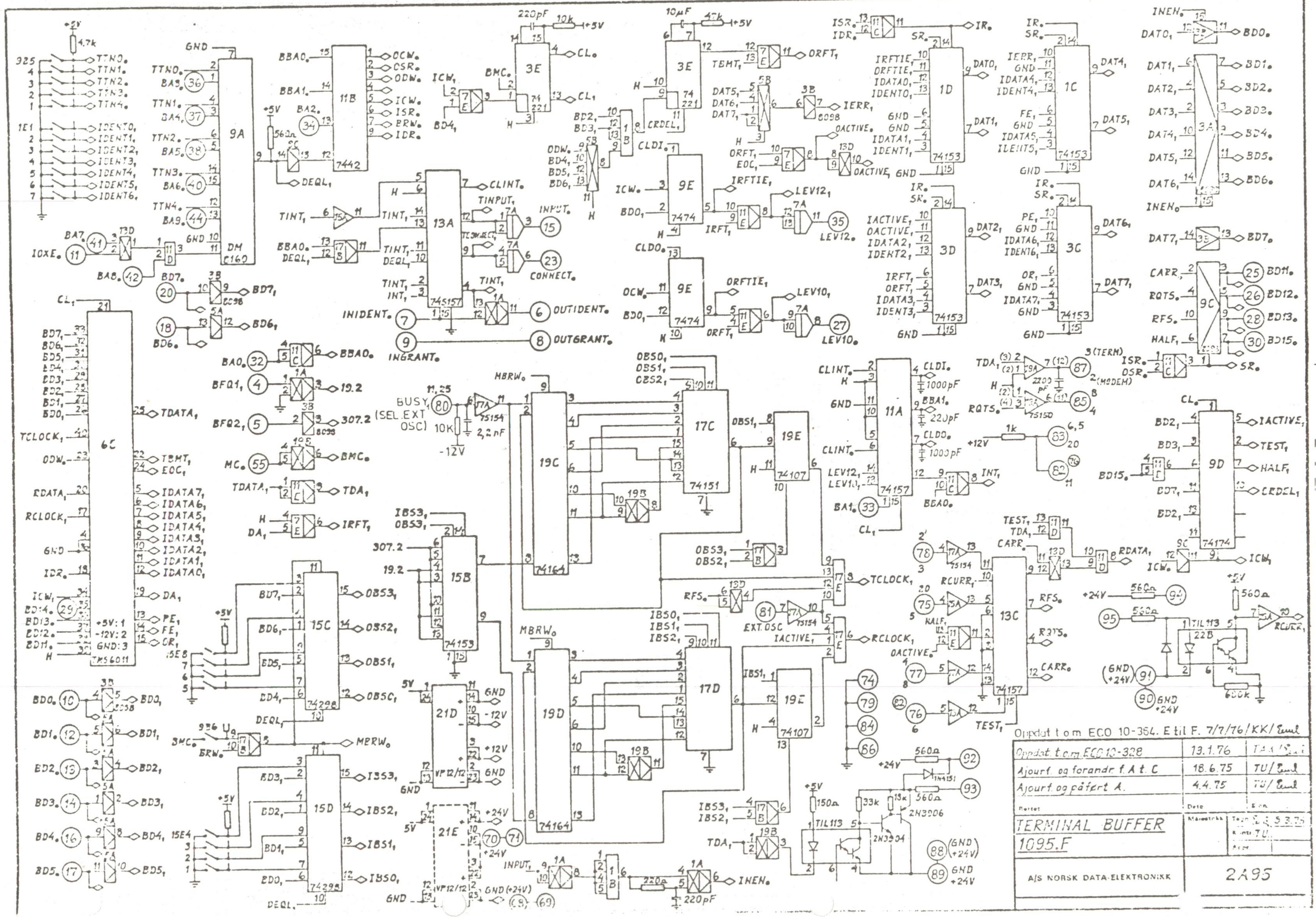
	9B1	9B2	9B3	9B4	9B5
200	OFF	OFF	OFF	OFF	OFF
210			OFF	OFF	ON
220			OFF	ON	OFF
230			OFF	ON	ON
240			ON	OFF	OFF
250			ON	OFF	ON
260			ON	ON	OFF
270			ON	ON	ON
300		ON	OFF	OFF	OFF
310			OFF	OFF	ON
320			OFF	ON	OFF
330			OFF	ON	ON
340			ON	OFF	OFF
350			ON	OFF	ON
360			ON	ON	OFF
370			ON	ON	ON
1200	ON	OFF	OFF	OFF	OFF
1210			OFF	OFF	ON
1220			OFF	ON	OFF
1230			OFF	ON	ON
1240			ON	OFF	OFF
1250			ON	OFF	ON
1260			ON	ON	OFF
1270			ON	ON	ON
1300		ON	OFF	OFF	OFF
1310			OFF	OFF	ON
1320			OFF	ON	OFF
1330			OFF	ON	ON
1340			ON	OFF	OFF
1350			ON	OFF	ON
1360			ON	ON	OFF
1370			ON	ON	ON

Note: The use of the switch in position 9B6 is described in section 9.

12 SWITCHES ON THE CARD

There are 3 groups of switches on the card. The functions of the switches are short listed below:

1E1	Ident code bit 0	OFF=1, ON=0
1E2	Ident code bit 1	" "
1E3	Ident code bit 2	" "
1E4	Ident code bit 3	" "
1E5	Ident code bit 4	" "
1E6	Ident code bit 5	" "
1E7	Ident code bit 6	" "
9B1	Device number bit 9 (4)	OFF→0, ON→1
9B2	Device number bit 6 (3)	" "
9B3	Device number bit 5 (2)	" "
9B4	Device number bit 4 (1)	" "
9B5	Device number bit 3 (0)	" "
9B6	Master Clear baud rate setting	OFF=NO, ON = YES
15E1	Baud rate selection, see table 9.1	
15E2	"	
15E3	"	
15E4	"	
15E5	"	
15E6	"	
15E7	"	
15E8	"	


Oppdat t o m ECO 10-364. E til F. 7/7/76/KK/
Oppdat. t.o.m ECO 10-328
13.1.76
Ajourf. og forandr. f. A t. C
18.6.75
Ajourf. og påført A.
4.4.75
TERMINAL BUFFER
1095.F
A/S NORSK DATA-ELEKTRONIKK
2A95

APPENDIX B :

DATASHEETS for LM 323, LM 340 - 05, HP 5082 - 4371

LM123/LM223/LM323 3 amp-5 volt positive regulator

general description

The LM123 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The 3 amp regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1 amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1μF solid tantalum capacitor should be used on the input. A 0.1μF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature, and power dissipation ensure that the LM123 will perform satisfactorily as a system element.

Operation is guaranteed over the junction temperature range −55°C to +150°C. An electrically identical LM223 operates from −25°C to +150°C and the LM323 is specified from 0°C to +125°C junction temperature. A hermetic TO-3 package is used for high reliability and low thermal resistance.

features

- 3 amp output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5 minimum input voltage
- 30W power dissipation

absolute maximum ratings

Input Voltage	20V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM123	−55°C to +150°C
LM223	−25°C to +150°C
LM323	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

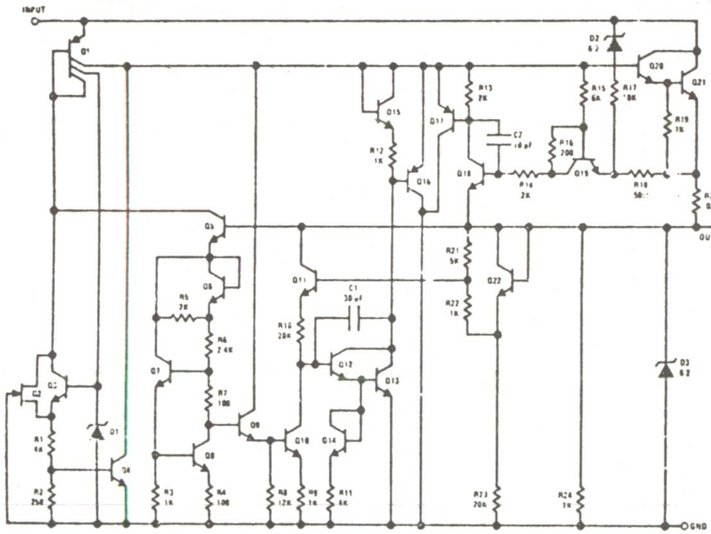
PARAMETER	CONDITIONS	LM123/LM223 MIN	LM123/LM223 TYP	LM123/LM223 MAX	LM323 MIN	LM323 TYP	LM323 MAX	UNITS
Output Voltage	$T_j = 25°C$ $V_{IN} = 7.5V$, $I_{OUT} = 0$	4.7	5	5.3	4.8	5	5.2	V
Output Voltage	$7.5V \leq V_{IN} \leq 15V$ $0 \leq I_{OUT} \leq 3A$, $P \leq 30W$	4.6		5.4	4.75		5.25	V
Line Regulation (Note 3)	$T_j = 25°C$ $7.5V \leq V_{IN} \leq 15V$		5	25		5	25	mV
Load Regulation (Note 3)	$T_j = 25°C$, $V_{IN} = 7.5V$, $0 \leq I_{OUT} \leq 3A$		25	100		25	100	mV
Quiescent Current	$7.5V \leq V_{IN} \leq 15V$, $0 \leq I_{OUT} \leq 3A$		12	20		12	20	mA
Output Noise Voltage	$T_j = 25°C$ $10 Hz \leq f \leq 100 kHz$		40			40		μVrms
Short Circuit Current Limit	$T_j = 25°C$ $V_{IN} = 15V$ $V_{IN} = 7.5V$		3 4	4.5 5		3 4	4.5 5	A A
Long Term Stability				35			35	mV
Thermal Resistance Junction to Case (Note 2)			2			2		°C/W

Note 1: Unless otherwise noted, specifications apply for $-55°C \leq T_j \leq +150°C$ for the LM123, $-25°C \leq T_j \leq +150°C$ for the LM223, and $0°C \leq T_j \leq +125°C$ for the LM323. Although power dissipation is internally limited, specifications apply only for $P \leq 30W$.

Note 2: Without a heat sink, the thermal resistance of the TO-3 package is about 35°C/W. With a heat sink, the effective thermal resistance can only approach the specified values of 2°C/W, depending on the efficiency of the heat sink.

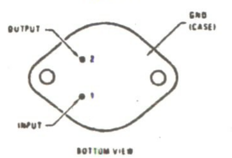
Note 3: Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1 ms and a duty cycle ≤ 5%.

schematic diagram



connection diagram

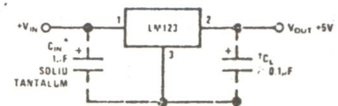
TO-3 (K)



Order Number LM123K, LM223K or LM323K
See Package 18

typical applications

Basic 3 Amp Regulator



*Required if LM123 is more than 4" from filter capacitor.
†Regulator is stable with no load capacitor into resistive loads.

LM340 series 3-terminal positive regulators

general description

The LM340 XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.0A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM340 XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO 220 and metal TO-3 packages

voltage range

LM340-05	5V	LM340-15	15V
LM340-06	6V	LM340-18	18V
LM340-08	8V	LM340-24	24V
LM340-12	12V		

absolute maximum ratings

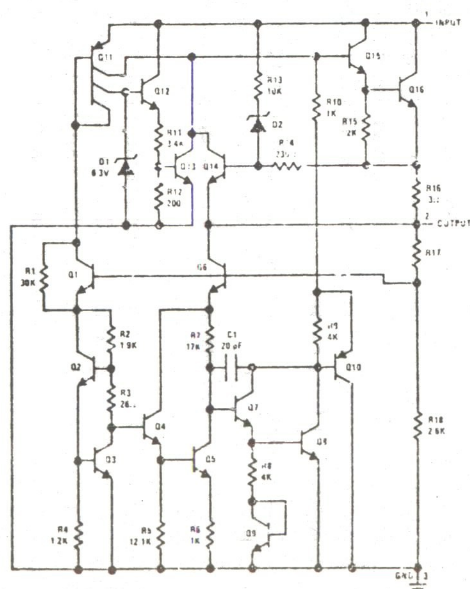
Input Voltage (V_O = 5V through 18V)	35V
(V_O = 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to 70°C
Maximum Junction Temperature	
TO-3 Package	150°C
TO-220 Package	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
TO-3 Package (Soldering, 10 sec)	300°C
TO-220 Package (Soldering, 10 sec)	230°C

electrical characteristics

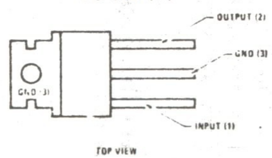
LM340-5 (V_{IN} = 10V, I_{OUT} = 500 mA, $0°C \le T_A \le 70°C$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	T_j = 25°C	4.8	5	5.2	V
Line Regulation	T_j = 25°C; $7V \le V_{IN} \le 25V$				
	I_{OUT} = 100 mA			50	mV
	I_{OUT} = 500 mA			100	mV
Load Regulation	T_j = 25°C, $5\ mA \le I_{OUT} \le 1.5A$			100	mV
Output Voltage	$7V \le V_{IN} \le 20V$, $5\ mA \le I_{OUT} \le 1.0A$, $P_D \le 15W$	4.75		5.25	V
Quiescent Current	T_j = 25°C		7	10	mA
Quiescent Current Change	$7V \le V_{IN} \le 25V$			1.3	mA
	$5\ mA \le I_{OUT} \le 1.5A$			5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Long Term Stability				20	mV/1000 hr
Ripple Rejection	f = 120 Hz		60		dB
Dropout Voltage	T_j = 25°C, I_{OUT} = 1.0A		2		V

schematic and connection diagrams



TO-220 (T)

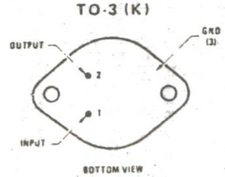


Order Numbers:

LM340T-5.0	LM340T-15
LM340T-6.0	LM340T-18
LM340T-8.0	LM340T-24
LM340T-12	

See Package 26

TO-3 (K)



Order Numbers:

LM340K-5.0	LM340K-15
LM340K-6.0	LM340K-18
LM340K-8.0	LM340K-24
LM340K-12	

See Package 16

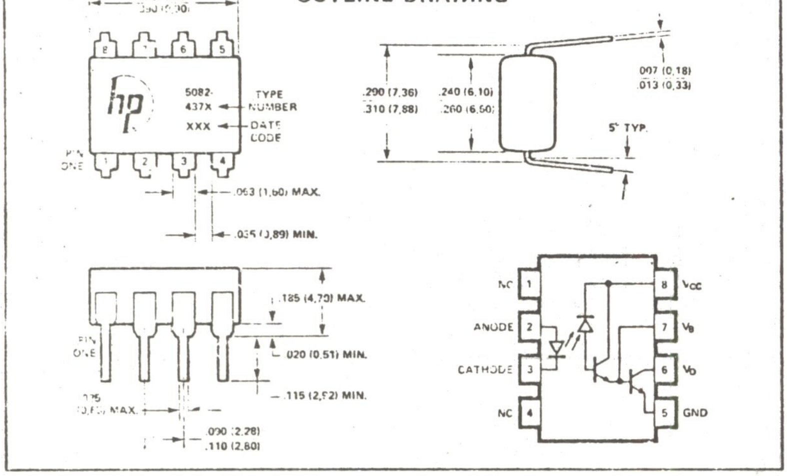
HEWLETT PACKARD COMPONENTS

LOW INPUT CURRENT, HIGH GAIN OPTICALLY COUPLED ISOLATORS

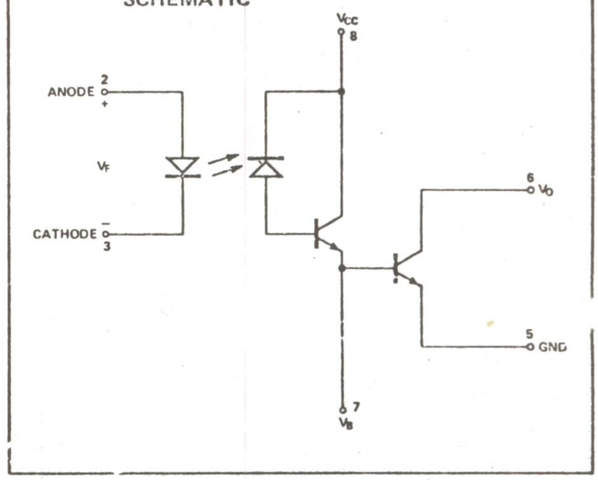
5082-4370
5082-4371

TECHNICAL DATA JANUARY 1975

OUTLINE DRAWING



SCHEMATIC



Features

- High Current Transfer Ratio — 800% Typical
- Low Input Current Requirement — 0.5 mA
- TTL Compatible Output — 0.1V V_{OL}
- 2500 Vdc Insulation Voltage
- High Common Mode Rejection — 500V/μs
- Performance Guaranteed Over Temperature 0°C to 70°C
- Base Access Allows Gain Bandwidth Adjustment
- High Output Current — 60mA
- DC to 1M bit/s Operation
- Recognized Under the Component Recognition Program of Underwriters Laboratories, Inc.

Description

The 5082-4370 series isolators use a Light Emitting Diode and an integrated high gain photon detector to provide 2500V dc electrical insulation, 500V/μs common mode transient immunity and extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 5082-4371 is suitable for use in CMOS, LTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5mA of LED current.

The 5082-4370 is suitable for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6mA [1 TTL unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. in, 1 U.L. out with a 2.2 kΩ pull-up resistor.

Applications

- Ground Isolate Most Logic Families — TTL/TTL, CMOS/TTL, CMOS/CMOS, LTTL/TTL, CMOS/LTTL
- Low Input Current Line Receiver — Long Line or Partyline
- EIA RS-232C Line Receiver with 2500V, 60Hz Common Mode Rejection
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator — Low Input Power Dissipation
- Low Power Systems — Ground Isolation

Absolute Maximum Ratings

Storage Temperature . . . . -55°C to +125°C
Operating Temperature . . . . 0°C to +70°C
Lead Solder Temperature . . . . 260°C for 10 Sec
(1/16" below seating plane)
Average Input Current — I_F . . . . 20mA [1]
Peak Input Current — I_F 40mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F 1.0A
($\leqslant$ 1μsec pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation . . . . 35mW [2]
Output Current — I_O (Pin 6) . . . . 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) 5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
5082-4370 . . . . -0.5 to 7V
5082-4371 . . . . -0.5 to 18V
Output Power Dissipation . . . . 100mW [4]

See notes, page 2.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device 5082-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	4371	400	800		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V		5,6
			500	900			I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
		4370	300	600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	4371		0.1	0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V		6
				0.1	0.4		I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V		
				0.2	0.4		I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V		
		4370		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}	4371		0.05	100	μA	I_F = 0mA, V_O = V_{CC} = 18V		6
		4370		0.1	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.2		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.8		mV/°C	I_F = 1.6mA		
Input Capacitance	C_O			40		pF	f = 1 MHz, V_F = 0		
Insulation Voltage (Input-Output)	V_{I-O}		2500			V dc	45% Relative Humidity, T_A = 25°C		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		7

*All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A = 25°C

Parameter	Sym.	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	4371		5	25	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				0.2	1		I_F = 12mA, R_L = 270Ω		
		4370		1	10	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}	4371		5	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	6,8
				1	7		I_F = 12mA, R_L = 270Ω		
		4370		4	35	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H			>500		V/μs	I_F = 0mA, R_L = 2.2kΩ, $\lvert V_{cm}\rvert$ = $10V_{p-p}$	10	9
Common Mode Transient Immunity at Logic Low Level Output	CM_L			<−500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ, $\lvert V_{cm}\rvert$ = $10V_{p-p}$	10	9

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).

APPENDIX C :

PRODUCTION OF PROMS

C1 PROM data

The output of the two PROMS shall be the same as address bits 0-6 if bit 7=0 and inverse of address bits 0-6 if bit 7=1.

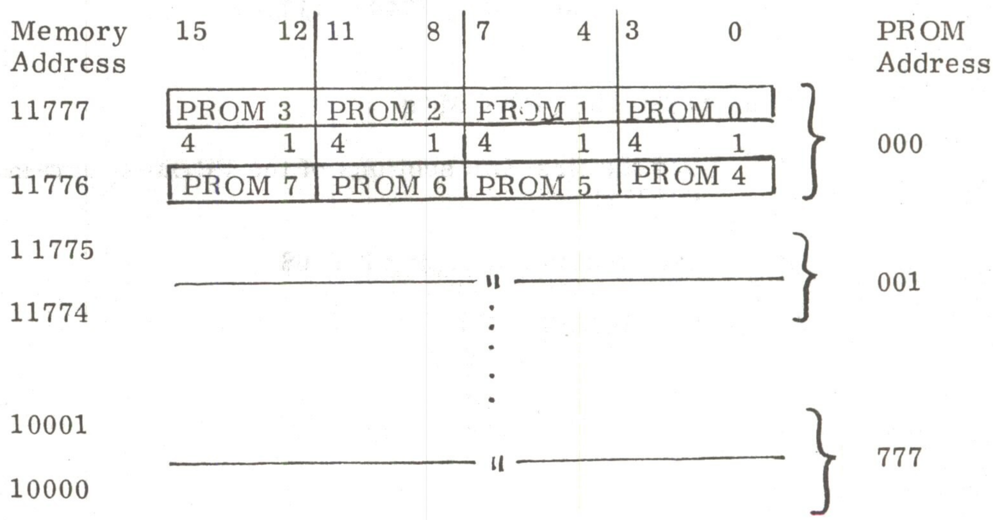
Hence the content shall be

ADDRESS	PROM-H	PROM-L
000	0000	0000
001	0000	0001
⋮		
376	1111	1110
377	1111	1111
400	1111	1111
⋮		
776	0000	0001
777	0000	0000

C2 Preparing the Burn-data

The program of the "PROM-Burner" takes data from the field 10 000 to 11777.

The data must be given in inverse polarity of the desired PROM output. It is possible to burn 8 PROM's simultanously. Data for the PROM's must be stored in the following format:



To prepare a datatape which is able to burn a set of two PROM's in any position on the PROM-Burner, follow the below procedure. PROM's in positions 0,2,4 and 6 will be PROM-L and positions 1,3,5,7 will produce PROM-H.

I Under SINTRAN recover MAC and assemble the following program:

```
ØØ774Ø  PROM,    SAA -1
ØØ7741           LDX (1ØØØØ
ØØ7742           LDT (11ØØØ
ØØ7743  L1,      COPY SA DD
ØØ7744           STD,  X
ØØ7745           ADD  (-4Ø1
ØØ7746           AAX 2
ØØ7747           SKP DX EQL ST
ØØ775Ø           JMP L1
ØØ7751           LDT (12ØØØ
ØØ7752  L2,      ADD (4Ø1
ØØ7753           COPY SA DD
ØØ7754           STD, X
ØØ7755           AAX 2
ØØ7756           SKP DX EQL ST
ØØ7757           JMP L2
ØØ776Ø           MCN Ø
ØØ7761           )FILL
ØØ7766           )LINE
```

II Type PROM!

III At @ type : OPEN F-P, W and @CONT
then type 10000<11777.

IV Punch data on papertape by typing)PUNCH.

NOTE! Assure that the MAC assembler program does not occupy addresses 7740 < 11777.

C3 Burning the PROM's

I Load the first two sections of the PROM-program and start MAC by
* 3777!

II Load datatape by typing 2,0,6$

III Type BURNT / 1↲
1↲
1↲
1↲

IV The cell BMASK must be defined according to the sockets in which PROM's are inserted. Examples : BMASK/3 for sockets 0-1, BMASK/17 for sockets 0-3, BMASK/377 for sockets 0-7.

V Push Master Clear on Burn-Box and set switch to Burn On.

VI Type START!

VII When program prints All packs OK, switch to Burn off and type TEST!

VIII Mark PROM's in positions 0,2,4,6 with L and positions 1,3,5,7 with H.

APPENDIX D :

UNISETTER

D1 Characteristics

- Data : 1-polarity
- Sprocket : 1-polarity
- Forward : 0-polarity
- Clear : Unused
- Speed : 100 bytes / sec.
- Logic level : + 5 volts

D2 Modifications

On logic board B (schematic sheet 3) the line receivers in positions P12, P13, P14 and L14 are removed.

Connect the following pins by wire-wrapping:

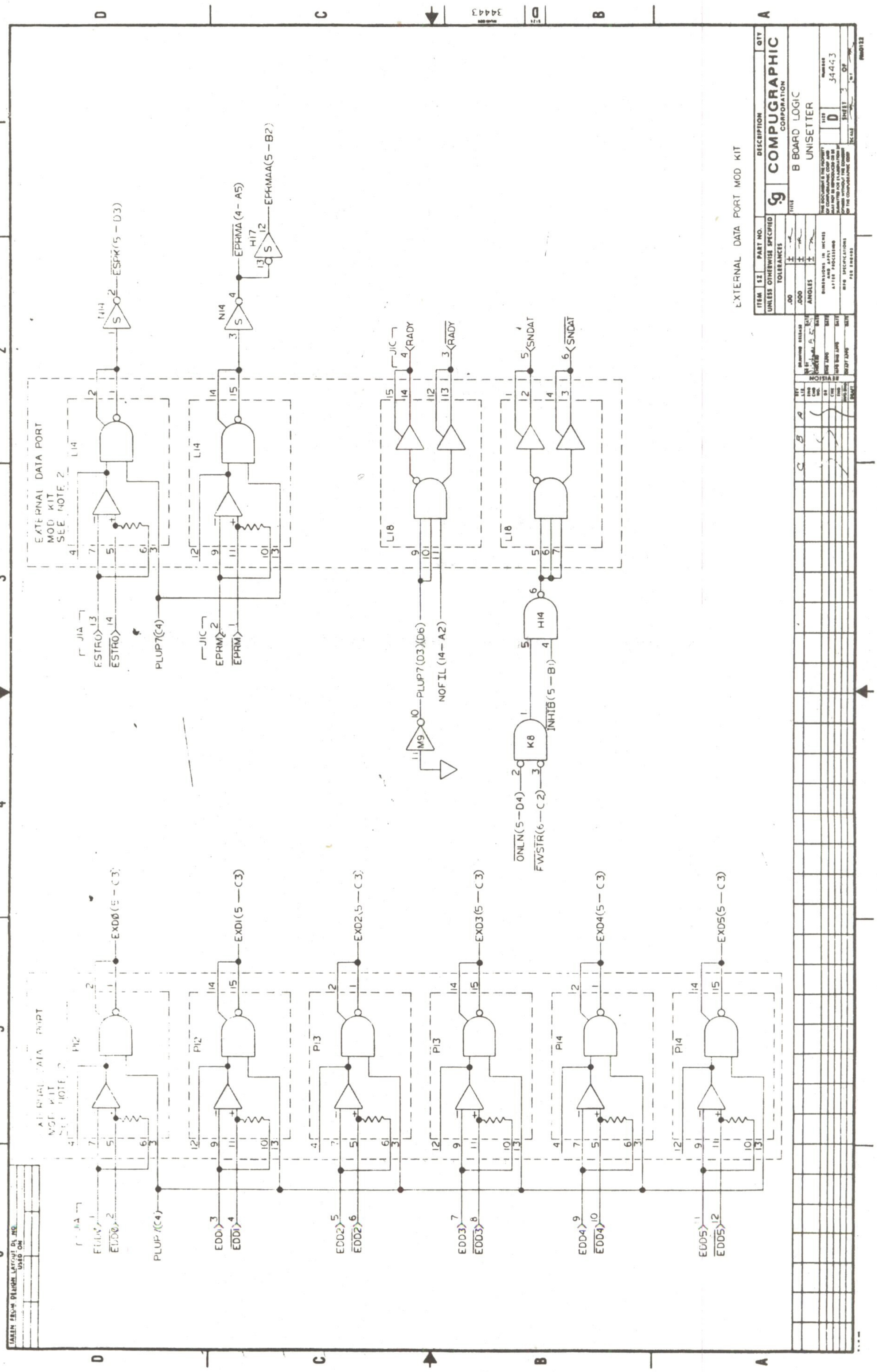
P12 : 7-8, 5-2, 9-8, 11-15

P13 : 7-8, 5-2, 9-8, 11-15

P14 : 7-8, 5-2, 9-8, 11-15

L14 : 7-8, 5-2, 8-15

Also remove the wire to chassis ground from the mains cable.



UNISETTER input circuits

1-4-25

A/S NORSK DATA-ELEKTRONIKK	Title: COMPUTER ADAPTER to PHOTOSETTER DEVICE CABLE	Drawing no. D3

NO.	SIGNAL	PLUG BERG (CPU POS.)	PLUG BURNDY	INTERNAL BURNDY PLUG STRAPS	DEVICE PLUG AMP 204745 - 1
1	DATA 1	BERG 95	A		A2
	DATA 2	" 94	C		A4
2	DATA 3	" 93	B		A6
	DATA 4	" 92	D		A8
3	DATA 5	" 91	E		A10
	DATA 6	" 90	H		A12
4	DATA 7	" 89	F		
	DATA 8	" 88	J		
5	SPROCKET	" 87	K		A14
	RETURN	" 86	M		A1,3,5,7
6	HANDSHAKE	" 85	L		9,11,13
		" 84	N		
7		" 83	P		
		" 82	S		
8	FORW. RUN	" 81	R		C6
		" 80	T	X	
9		" 79	U		
	EXREF	" 78	W	V	
10	V -	" 77	V	WW	
	V +	" 76	X	T	
11	PPOL	" 75	Y	AA	
	GND	" 74	AA	Y	
12	RPOL	" 73	Z		
	GND	" 72	BB		
13	HPOL	" 71	CC	EE	
	GND	" 70	EE	CC	
14		" 69	DD		
		" 68	FF		
15		" 67	HH		
		" 66	KK		
16		" 65	JJ		
		" 64	LL		
17		" 63	MM	PP	
		" 62	PP	MM	
18		" 61	NN	RR	
		" 60	RR	NN	
19		" 59	SS		
		" 58	UU		
20		" 57	TT	VV	
		" 56	VV	TT	

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	UNISETTER	Replaced by	Date
DATE			

APPENDIX E :

ACM 9000

E1 Characteristics

- Data : 0-polarity
- Sprocket : 0-polarity
- Forward :: 1-polarity
- Clear : Unused
- Speed : 100 bytes / sec.
- Logic level : + 12 volts

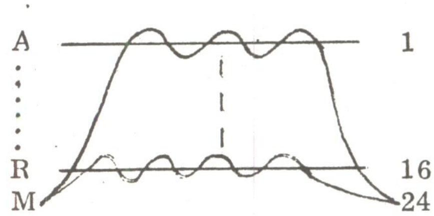
E2. Modifications,

Cable to the photosetter reader must be disconnected and the Adapter cable is connected to the free plug.

A/S NORSK DATA-ELEKTRONIKK	Title: COMPUTER ADAPTER to PHOTOSETTER DEVICE CABLE	Drawing no. E2

NO.	SIGNAL	PLUG BERG (CPU POS.)	PLUG BURNDY	INTERNAL BURNDY PLUG STRAPS	DEVICE PLUG AMP
1	DATA 1	BERG 95	A		1
	DATA 2	" 94	C		2
2	DATA 3	" 93	B		3
	DATA 4	" 92	D		4
3	DATA 5	" 91	E		5
	DATA 6	" 90	H		6
4	DATA 7	" 89	F		19
	DATA 8	" 88	J		20
5	SPROCKET	" 87	K		8
	RETURN	" 86	M		24
6	HANDSHAKE	" 85	L		
		" 84	N		
7		" 83	P		
		" 82	S		
8	FORW.RUN	" 81	R		16
		" 80	T	X	
9		" 79	U		
	EXREF	" 78	W	V	
10	V -	" 77	V	W	
	V +	" 76	X	T	
11	PPOL	" 75	Y	AA	
	GND	" 74	AA	Y	
12	RPOL	" 73	Z	BB	
	GND	" 72	BB	Z	
13	HPOL	" 71	CC	EE	
	GND	" 70	EE	CC	
14	DPOL	" 69	DD	FF	
	GND	" 68	FF	DD	
15	SPOL	" 67	HH	KK	
	GND	" 66	KK	HH	
16	PS0	" 65	JJ		
	GND	" 64	LL		
17	PS1	" 63	MM	PP	
	GND	" 62	PP	MM	
18	PS2	" 61	NN	RR	
	GND	" 60	RR	NN	
19	PS3	" 59	SS		
	GND	" 58	UU		
20	VR	" 57	TT		
	GR	" 56	VV		

Note ! A, C, B, D, E, H, F, J, K, R shall be twisted with ground which is connected to M in Adapter end and 24 in Photosetter end.



DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	ACM 9000	Replaced by	Date
DATE			

1122

NORD-10 4 ASYNC. CURRENT LOOP PROGRAMMING SPECIFICATIONS

+++
+

1 TERMINAL ADDRESS CODES

The codes below are relevant for the first terminal on the first card. The codes have to be consecutive for the four interfaces on one card (IOX- and IDENT-codes). The codes are set by switches on the card and all combinations may be used, f.inst. the codes for async.modems. Further information in section 11.

2 INPUT CHANNEL (INTERRUPT LEVEL 12)

2.1 Read Data Register

IOX 300

The number of data bits read into the A register is specified by bits 11 and 12 in the input channel control register. (See section 6.2). The received character is right justified. (From bit 0 and upwards).

2.2 Read Status Register

IOX 302

See section 6.1 for the specification of status bits.

2.3 Write Control Register

IOX 303

See section 6.2 for the specification of control bits.

3 OUTPUT CHANNEL (INTERRUPT LEVEL 10)

3.1 Write Data Register

IOX 305

The number of bits specified by bits 11 and 12 in the input channel control register is written to the output data register, starting with bit 0 and counting upwards.

3.2 Read Status Register

IOX 306

See section 7.1 for the specification of status bits.

3.3 Write Control Register

IOX 307

See section 6.2 for the specification of control bits.

4 DATARATE SELECTION

IOX 301

See section 9 for baud rate selection, using either external or internal oscillator.

5 IDENT CODE

The ident code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel responding to level 10. The selection of different ident codes are given by the section 10.

6 INPUT CHANNEL

6.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Not used
	2	Not used
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Framing error
	6	Parity error
	7	Overrun
	8–15	Not used

Notes: Additional explanation to status bits.

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occured while working in parity generating/ checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

6.2 Control Register

Bit		
Bit	0	Enable interrupt on device ready for transfer
	1	Not used
	2	Not used
	3	Test mode
	4–10	Not used
	11-12	Character length
	13	Number of stop bits
	14	Parity generation/checking
	15	Not used

Notes: There is no need for separate activation. The received data will always be clocked into the receiver data buffer.

Bit 3: Test mode will loop transmitted data back to received data, and if the other terminal is connected to the line, transmitted data will also be transferred to this terminal. If test mode is selected for one of the four interfaces all four will be set in test mode.

Bit 11-12: The content of these bits gives the following character lengths, both for the input channel and the output channel:

Bit 12	Bit 11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is added to the number given in this table.

Bit 13: This bit = 0 will select 1,5 stop bit for 5 bits character and 2 stop bit else. This bit = 1 will select 1 stop bit.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

7 OUTPUT CHANNEL

7.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Not used
	2	Not used
	3	Device ready for transfer
	4-15	Not used

Bit 3: This bit indicates that the output data buffer is ready to receive a new character.

7.2 Control Register

Bit	0	Enable interrupt on device ready for transfer
	1-15	Not used

Notes:

The device is activated when a character is loaded into the output character register (section 3.1). There is no need for separate activation.

8 CONTROL AND STATUS WORDS

8.1 Input

Bit	Status	Control
0	RFT en	Enable RFT
1		
2		
3	Dev. RFT	Test
4	ERR OR	
5	Framing	
6	Parity	
7	Overrun	
8		
9		
10		
11		Char. length
12		Char. length
13		Stop bits
14		Parity gen./check
15		

8.2 Output

Bit	Status	Control
0	RFT en	Enable RFT
1		
2		
3	Dev. RFT	
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		

9 DATA RATE SELECTION

There are two possibilities to control the data rate for input and output serial data.

The data rate can be selected by:

a) SWITCH SETTING on card. All four interfaces are operated at the data rate selected by the switches each time MASTER CLEAR button is pressed. The switch setting is common for input and output.

Switch settings for the different baud rates are given in table 9.1.

b) IOX INSTRUCTION. If data rate is selected by software for one of the interfaces the programmed data rate is selected for all four interfaces.

Input and output are independant, and are selected by the same IOX instruction (Group device number + 1). The content of the A register before the IOX instruction is executed determines the baud rate. The 4 least significant bits (0-3) are used for the input channel, and the next 4 bits (4-7) are used for the output channel. Table 9.1 gives the bit pattern and corresponding baud rate.

Table 9.1

		OUTPUT				INPUT				SWITCHES			
BAUD RATE	BIT	7	6	5	4	3	2	1	0	15F 4	3	2	1
0		0	0	0	0	0	0	0	0	ON	ON	ON	ON
0		0	0	0	1	0	0	0	1	ON	ON	ON	OFF
50		0	0	1	0	0	0	1	0	ON	ON	OFF	ON
75		0	0	1	1	0	0	1	1	ON	ON	OFF	OFF
110		1	1	1	1	1	1	1	1	OFF	OFF	OFF	OFF
134.5		0	1	0	0	0	1	0	0	ON	OFF	ON	ON
150		1	1	1	0	1	1	1	0	OFF	OFF	OFF	ON
200		0	1	0	1	0	1	0	1	ON	OFF	ON	OFF
300		1	1	0	1	1	1	0	1	OFF	OFF	ON	OFF
600		0	1	1	0	0	1	1	0	ON	OFF	OFF	ON
1200		1	0	1	1	1	0	1	1	OFF	ON	OFF	OFF
1800		1	0	1	0	1	0	1	0	OFF	ON	OFF	ON
2400		0	1	1	1	0	1	1	1	ON	OFF	OFF	OFF
2400		1	1	0	0	1	1	0	0	OFF	OFF	ON	ON
4800		1	0	0	1	1	0	0	1	OFF	ON	ON	OFF
9600		1	0	0	0	1	0	0	0	OFF	ON	ON	ON

10 IDENT CODES AND INTERRUPT MECHANISM

10.1 Ident Codes

The ident codes are binary coded by the switches (bits 2-7) in position 6E, with 0 corresponding to OFF and 1 corresponding to ON .

All ident codes from 0 to 377_8 can be selected. Switch selection in section 11.

10.2 Interrupt Mechanism

What is needed for a device to give an interrupt?

First of all the device must be ready for a transfer, i.e. status bit 3 must be on. For input this means that a whole character is received by the input buffer, and is ready to be read into the A register. For output it means that it is possible to place at least one more character in the otuput buffer. Secondly, interrupt on ready for transfer must be enabled. It means that a 1 is written into the control register bit 0 (which also is status register bit 0). The AND function of Ready for Transfer and Ready for Transfer Interrupt Enabled is gated to "wire-or" lines, separate for input and output. Input is connected to interrupt level 12 (terminal 35) and output is connected to interrupt level 10 (terminal 27). When an interrupt is detected (dependant on the status in CPU and the program), the CPU usually responds by executing an IDENT instruction for the interrupting level, which gives the ident code in A register. The ident code is identical for input and output channel.

11 DEVICE NUMBER AND IDENT CODE SELECTION

Device numbers and ident codes are selected by the switches in positions 10A and 6E. The four interfaces on one card has consecutive device device numbers and ident codes. The switches are binary coded and other combinations than those in table may be used. Switch number 10A6 is not used.

DEVICE NUMBERS							IDENT CODES						
SWITCH BIT NO.	10A6 NONE	10A5 BA9	10A4 BA8	10A3 BA7	10A2 BA6	10A1 BA5	SWITCH BIT CODE	6E6 7	6E5 6	6E4 5	6E3 4	6E2 3	6E1 2
200		OFF	OFF	ON	OFF	OFF	60	OFF	OFF	ON	ON	OFF	OFF
210		"	"	"	"	"	61	"	"	"	"	"	"
220		"	"	"	"	"	62	"	"	"	"	"	"
230		"	"	"	"	"	63	"	"	"	"	"	"
240		OFF	OFF	ON	OFF	ON	64	OFF	OFF	ON	ON	OFF	ON
250		"	"	"	"	"	65	"	"	"	"	"	"
260		"	"	"	"	"	66	"	"	"	"	"	"
270		"	"	"	"	"	67	"	"	"	"	"	"
300		OFF	OFF	ON	ON	OFF	120	OFF	ON	OFF	ON	OFF	OFF
310		"	"	"	"	"	121	"	"	"	"	"	"
320		"	"	"	"	"	122	"	"	"	"	"	"
330		"	"	"	"	"	123	"	"	"	"	"	"
340		OFF	OFF	ON	ON	ON	44	OFF	OFF	ON	OFF	OFF	ON
350		"	"	"	"	"	45	"	"	"	"	"	"
360		"	"	"	"	"	46	"	"	"	"	"	"
370		"	"	"	"	"	47	"	"	"	"	"	"
1100		ON	OFF	OFF	ON	OFF	130	OFF	ON	OFF	ON	ON	OFF
1110		"	"	"	"	"	131	"	"	"	"	"	"
1120		"	"	"	"	"	132	"	"	"	"	"	"
1130		"	"	"	"	"	133	"	"	"	"	"	"
1140		ON	OFF	OFF	ON	ON	134	OFF	ON	OFF	ON	ON	ON
1150		"	"	"	"	"	135	"	"	"	"	"	"
1160		"	"	"	"	"	136	"	"	"	"	"	"
1170		"	"	"	"	"	137	"	"	"	"	"	"
1200		ON	OFF	ON	OFF	OFF	70	OFF	OFF	ON	ON	ON	OFF
1210		"	"	"	"	"	71	"	"	"	"	"	"
1220		"	"	"	"	"	72	"	"	"	"	"	"
1230		"	"	"	"	"	73	"	"	"	"	"	"
1240		ON	OFF	ON	OFF	ON	74	OFF	OFF	ON	ON	ON	ON
1250		"	"	"	"	"	75	"	"	"	"	"	"
1260		"	"	"	"	"	76	"	"	"	"	"	"
1270		"	"	"	"	"	77	"	"	"	"	"	"
1300		ON	OFF	ON	ON	OFF	50	OFF	OFF	ON	OFF	ON	OFF
1310		"	"	"	"	"	51	"	"	"	"	"	"
1320		"	"	"	"	"	52	"	"	"	"	"	"
1330		"	"	"	"	"	53	"	"	"	"	"	"
1340		ON	OFF	ON	ON	ON	54	OFF	OFF	ON	OFF	ON	ON
1350		"	"	"	"	"	55	"	"	"	"	"	"
1360		"	"	"	"	"	56	"	"	"	"	"	"
1370		"	"	"	"	"	57	"	"	"	"	"	"

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NORD-10 DUAL ASYNC. V24 (MODEM) PROGRAMMING SPECIFICATIONS

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1 TERMINAL ADDRESS CODES

The codes below are relevant for the first terminal on the first card. The codes have to be consecutive for the two interfaces on one card (IOX- and IDENT-codes). The codes are set by switches on the card and all combinations may be used. Further information in section 11.

2 INPUT CHANNEL (INTERRUPT LEVEL 12)

2.1 Read Data Register

IOX 200

The number of data bits read into the A register is specified by bits 11 and 12 in the input channel control register. (See section 6.2). The received character is right justified. (From bit 0 and upwards).

2.2 Read Status Register

IOX 202

See section 6.1 for the specification of status bits.

2.3 Write Control Register

IOX 203

See section 6.2 for the specifications of control bits.

3 OUTPUT CHANNEL (INTERRUPT LEVEL 10)

3.1 Write Data Register

IOX 205

The number of bits specified by bits 11 and 12 in the input channel control register is written to the output data register, starting with bit 0 and counting upwards.

3.2 Read Status Register

IOX 206

See section 7.1 for the specification of status bits.

3.3 Write Control Register

IOX 207

See section 6.2 for the specification of control bits.

4 DATARATE SELECTION

IOX 201

See section 9 for baud rate selection, using either external or internal oscillator.

5 IDENT CODE

The ident code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel responding to level 10. The selection of different ident codes are given by the section 10.

6 INPUT CHANNEL

6.1 Status Register

Bit	0	Ready for transfer interrupt enabled
	1	Not used
	2	Not used
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Framing error
	6	Parity error
	7	Overrun
	8	
	9	Not used
	10	
	11	Carrier missing
	12	
	13	Not used
	14	
	15	

Notes: Additional explanation to status bits.

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occured while working in parity generating/ checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Bit 11: Carrier missing gives the status of receive line signal detector, or carrier on the line.

0 indicates Carrier present

1 indicates Carrier missing

6.2 Control Register

Bit	0	Enable interrupt on device ready for transfer
	1	Not used
	2	Not used
	3	Test mode
	4	Start timeout for breaking connection
	5	
	6	
	7	Not used
	8	
	9	
	10	
	11-12	Character lenght
	13	Number of stop bits
	14	Parity generation/checking
	15	Not used

Notes: There is no need for separate activation. The received data will always be clocked into the receiver data buffer.

Bit 3: Test mode will loop transmitted data back to received data, and if the other terminals is connected to the line, transmitted data will also be transferred to this terminal. If test mode is selected for one of the two interfaces both will be set in test mode.

Bit 4: If this bit is activated, the DATA TERMINAL READY signal will drop after appr. 20 sek. if no characters are received

Bit 11-12: The content of these bits gives the following character lenghts, both for the input channel and the output channel:

Bit 12	Bit 11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is <u>added</u> to the number given in this table.

Bit 13: This bit = 0 will select 1,5 stop bit for 5 bits character and 2 stop bit else. This bit = 1 will select 1 stop bit.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the receiver character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

7 OUTPUT CHANNEL

7.1 Status Register

Bit	
0	Ready for transfer interrupt enabled
1	Not used
2	Not used
3	Device ready for transfer
4-10	Not used
11	Carrier missing
12-15	Not used

Bit 3: This bit indicates that the output data buffer is ready to receive a new character.

Bit 11: As for input channel.

7.2 <u>Control Register</u>

Bit	
0	Enable interrupt on device ready for transfer
1-15	Not used

Notes:

The device is activated when a character is loaded into the output character register (section 3.1). There is no need for separate activation.

8 CONTROL AND STATUS WORDS

8.1 Input

Bit	Status	Control
0	RFT en	Enable RFT
1		
2		
3	Dev. RFT	Test
4	ERR OR	Start timeout
5	Framing	
6	Parity	
7	Overrun	
8		
9		
10		
11	Carrier missing	Char. lenght
12		Char. lenght
13		Stop bits
14		Parity gen./check
15		

8.2 Output

Bit	Status	Control
0	RFT en	Enable RFT
1		
2		
3	Dev. RFT	
4		
5		
6		
7		
8		
9		
10		
11	Carrier missing	
12		
13		
14		
15		

9 DATA RATE SELECTION

There are two possibilities to control the data rate for input and output serial data.

The data rate can be selected by:

a) SWITCH SETTING on card. Both interfaces are operated at the data rate selected by the switches each time MASTER CLEAR buttom is pressed. The switch setting is common for input and output.

Switch setting for the different baud rates are given in table 9.1.

b) IOX INSTRUCTION. If data rate is selected by software for one of the interfaces the programmed data rate is selected for both interfaces.

Input and output are independant, and are selected by the same IOX instruction (Group device number + 1). The content of the A register before the IOX instruction is executed determines the baud rate. The 4 least significant bits (0-3) are used for the input channel, and the next 4 bits (4-7) are used for the output channel. Table 9.1 gives the bit pattern and corresponding baud rate.

Table 9.1

		OUTPUT				INPUT					SWITCHES		
BAUD RATE	BIT	7	6	5	4	3	2	1	0	15F 4	3	2	1
0		0	0	0	0	0	0	0	0	ON	ON	ON	ON
0		0	0	0	1	0	0	0	1	ON	ON	ON	OFF
50		0	0	1	0	0	0	1	0	ON	ON	OFF	ON
75		0	0	1	1	0	0	1	1	ON	ON	OFF	OFF
110		1	1	1	1	1	1	1	1	OFF	OFF	OFF	OFF
134.5		0	1	0	0	0	1	0	0	ON	OFF	ON	ON
150		1	1	1	0	1	1	1	0	OFF	OFF	OFF	ON
200		0	1	0	1	0	1	0	1	ON	OFF	ON	OFF
300		1	1	0	1	1	1	0	1	OFF	OFF	ON	OFF
600		0	1	1	0	0	1	1	0	ON	OFF	OFF	ON
1200		1	0	1	1	1	0	1	1	OFF	ON	OFF	OFF
1800		1	0	1	0	1	0	1	0	OFF	ON	OFF	ON
2400		0	1	1	1	0	1	1	1	ON	OFF	OFF	OFF
2400		1	1	0	0	1	1	0	0	OFF	OFF	ON	ON
4800		1	0	0	1	1	0	0	1	OFF	ON	ON	OFF
9600		1	0	0	0	1	0	0	0	OFF	ON	ON	ON

10 IDENT CODES AND INTERRUPT MECHANISM

10.1 Ident Codes

The ident codes are binary coded by the switches (bits 1-7) in position 6E, with 0 corresponding to OFF and 1 corresponding to ON.

All ident codes from 0 to 377_8 can be selected. Switch selection in section 11.

10.2 Interrupt Mechanism

What is needed for a device to give an interrupt?

First of all the device must be ready for a transfer, i.e. status bit 3 must be on. For input this means that a whole character is received by the input buffer, and is ready to be read into the A register. For output it means that it is possible to place at least one more character in the output buffer. secondly, interrupt on ready for transfer must be enabled. It means that a 1 is written into the control register bit 0 (which also is status register bit 0). The AND function of Ready for Transfer and Ready for Transfer Interrupt Enabled is gated to "wire-or" lines, separate for input and output. Input is connected to interrupt level 12 (terminal 35) and output is connected to interrupt level 10 (terminal 27). When an interrupt is detected (dependant on the status in CPU and the program), the CPU usually responds by executing an IDENT instruction for the interrupting level, which gives the ident code in A register. The ident code is identical for input and channel.

11 DEVICE NUMBER AND IDENT CODE SELECTION

Device numbers and ident codes are selected by the switches in positions 10A and 6E. The two interfaces on one card has consecutiv device device numbers and ident codes. The switches are binary coded and other combinations than those in table may be used. Switch number 6E8 is not used.

DEVICE NUMBERS						
Switch Bit / No.	10A6 BA9	10A5 BA8	10A4 BA7	10A3 BA6	10A2 BA5	10A1 BA4
200	OFF	OFF	ON	OFF	OFF	OFF
210	OFF	OFF	ON	OFF	OFF	OFF
220	OFF	OFF	ON	OFF	OFF	ON
230	OFF	OFF	ON	OFF	OFF	ON
240	OFF	OFF	ON	OFF	ON	OFF
250	OFF	OFF	ON	OFF	ON	OFF
260	OFF	OFF	ON	OFF	ON	ON
270	OFF	OFF	ON	OFF	ON	ON
300	OFF	OFF	ON	ON	OFF	OFF
310	OFF	OFF	ON	ON	OFF	OFF
320	OFF	OFF	ON	ON	OFF	ON
330	OFF	OFF	ON	ON	OFF	ON
340	OFF	OFF	ON	ON	ON	OFF
350	OFF	OFF	ON	ON	ON	OFF
360	OFF	OFF	ON	ON	ON	ON
370	OFF	OFF	ON	ON	ON	ON
1100	ON	OFF	OFF	ON	OFF	OFF
1110	ON	OFF	OFF	ON	OFF	OFF
1120	ON	OFF	OFF	ON	OFF	ON
1130	ON	OFF	OFF	ON	OFF	ON
1140	ON	OFF	OFF	ON	ON	OFF
1150	ON	OFF	OFF	ON	ON	OFF
1160	ON	OFF	OFF	ON	ON	ON
1170	ON	OFF	OFF	ON	ON	ON

IDENT CODES							
Switch Bit / Code	6E7 7	6E6 6	6E5 5	6E4 4	6E3 3	6E2 2	6E1 1
60	OFF	OFF	ON	ON	OFF	OFF	OFF
61	OFF	OFF	ON	ON	OFF	OFF	OFF
62	OFF	OFF	ON	ON	OFF	OFF	ON
63	OFF	OFF	ON	ON	OFF	OFF	ON
64	OFF	OFF	ON	ON	OFF	ON	OFF
65	OFF	OFF	ON	ON	OFF	ON	OFF
66	OFF	OFF	ON	ON	OFF	ON	ON
67	OFF	OFF	ON	ON	OFF	ON	ON
120	OFF	ON	OFF	ON	OFF	OFF	OFF
121	OFF	ON	OFF	ON	OFF	OFF	OFF
122	OFF	ON	OFF	ON	OFF	OFF	ON
123	OFF	ON	OFF	ON	OFF	OFF	ON
44	OFF	OFF	ON	OFF	OFF	ON	OFF
45	OFF	OFF	ON	OFF	OFF	ON	OFF
46	OFF	OFF	ON	OFF	OFF	ON	ON
47	OFF	OFF	ON	OFF	OFF	ON	ON
130	OFF	ON	OFF	ON	ON	OFF	OFF
131	OFF	ON	OFF	ON	ON	OFF	OFF
132	OFF	ON	OFF	ON	ON	OFF	ON
133	OFF	ON	OFF	ON	ON	OFF	ON
134	OFF	ON	OFF	ON	ON	ON	OFF
135	OFF	ON	OFF	ON	ON	ON	OFF
136	OFF	ON	OFF	ON	ON	ON	ON
137	OFF	ON	OFF	ON	ON	ON	ON

DEVICE NUMBERS						
Switch / Bit / No.	10A6 BA9	10A5 BA8	10A4 BA7	10 A3 BA6	10A2 BA5	10A1 BA4
1200	ON	OFF	ON	OFF	OFF	OFF
1210	ON	OFF	ON	OFF	OFF	OFF
1220	ON	OFF	ON	OFF	OFF	ON
1230	ON	OFF	ON	OFF	OFF	ON
1240	ON	OFF	ON	OFF	ON	OFF
1250	ON	OFF	ON	OFF	ON	OFF
1260	ON	OFF	ON	OFF	ON	ON
1270	ON	OFF	ON	OFF	ON	ON
1300	ON	OFF	ON	ON	OFF	OFF
1310	ON	OFF	ON	ON	OFF	ON
1320	ON	OFF	ON	ON	OFF	ON
1330	ON	OFF	ON	ON	OFF	ON
1340	ON	OFF	ON	ON	ON	OFF
1350	ON	OFF	ON	ON	ON	OFF
1360	ON	OFF	ON	ON	ON	ON
1370	ON	OFF	ON	ON	ON	ON

IDENT CODES							
Switch / Bit / Code	6E7 7	6E6 6	6E5 5	6E4 4	6E3 3	6E2 2	6E1 1
70	OFF	OFF	ON	ON	ON	OFF	OFF
71	OFF	OFF	ON	ON	ON	OFF	OFF
72	OFF	OFF	ON	ON	ON	OFF	ON
73	OFF	OFF	ON	ON	ON	OFF	ON
74	OFF	OFF	ON	ON	ON	ON	OFF
75	OFF	OFF	ON	ON	ON	ON	OFF
76	OFF	OFF	ON	ON	ON	ON	ON
77	OFF	OFF	ON	ON	ON	ON	ON
50	OFF	OFF	ON	OFF	ON	OFF	OFF
51	OFF	OFF	ON	OFF	ON	OFF	OFF
52	OFF	OFF	ON	OFF	ON	OFF	ON
53	OFF	OFF	ON	OFF	ON	OFF	ON
54	OFF	OFF	ON	OFF	ON	ON	OFF
55	OFF	OFF	ON	OFF	ON	ON	OFF
56	OFF	OFF	ON	OFF	ON	ON	ON
57	OFF	OFF	ON	OFF	ON	ON	ON

NORD 10

DUAL TELEX CONTROLLER

PROGRAMMING SPECIFICATION

INPUT CHANNEL (Interrupt level 12):

1. Read Data Register, IOX DEVNO+0
2. Read Status Register, IOX DEVNO+2
3. Write Control Register, IOX DEVNO+3

OUTPUT CHANNEL (Interrupt level 10):

1. Write Data Register, IOX DEVNO+5
2. Read Status Register, IOX DEVNO+6
3. Write Control Register, IOX DEVNO+7.

The IOX- and IDENT-codes are set by switches on the card and are consecutive for the two interfaces on one card. The identcodes for the input and output channels are identical.

INPUT CHANNEL

Status Register.

Bit	0	Interrupt enabled
	1	Not used
	2	Not used
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Framing error
	6	Parity error
	7	Overrun
	8	Not used
	9	Not used
	10	Not used
	11	Line polarity
	12	Line impedance
	13	Missing connection
	14	Watchdog
	15	Not used

Bit 4: This is an inclusive OR of the bits 5, 6, 7, 13 and 14.

Bit 5: Framing error means that the stop bit is missing.

Bit 6: Parity error means that a parity error has occurred while working in parity generating/checking mode.

Bit 7: Overrun means that at least one character is overwritten while input is active.

Bit 11: If this bit is set the line is in an active state or disconnected from the Telex Exchange. If the bit is not set the line is connected to the Telex Exchange, but is in a nonactive state. This bit is controlled by the Telex Exchange and should be zero before starting a call.

Bit 12: This bit ="0" means that the telex-transmitter is connected to the line (low impendance). A "1" means disconnection. The bit is controlled by the Output Control Register bit 10 and 11, but is automatically set to a "0" when the Telex Exchange calling by changing polarity (bit 11 goes to a "1").

Bit 13: If this bit is set the line has been nonactive (missing line current) for more than one character (>150 ms).

Bit 14: If this bit is set, the Telex line has been disconnected from the telex transmitter and connected to a standby Telex device for manual operation. There is three ways for setting this bit:

1) Missing input control word for more than 6 sec. (Telex program not running for this line.)

2) Pushing the STANDBY TELEX button on the Telex Transmitter.

3) Any other fault in the system such as missing supply voltage.

This bit can only be reset by pushing the COMPUTER button on the Telex Transmitter.

Bits 13 or 14 are interrupt conditions to level 12.

<u>Control Register</u>.

Bit	0	Enable interrupt
	1–2	Not used
	3	Test mode
	4–10	Not used
	11–12	Character length
	13	Number of stop bits
	14	Parity generation/checking
	15	Not used

Notes: There is no need for separate activation. The received data will always be clocked into the receiver data buffer.

Bit 3: Test mode will loop transmitted data back to received data. If test mode is selected for one of the two interfaces both will be set in test mode.

Bit 11-12: The content of these bits gives the following character lengths, both for the input channel and the output channel:

Bit 12	Bit 11	
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

If bit 14 is a 1, a parity bit is added to the number given in this table.

Bit 13: This bit = 0 will select 1,5 stop bit for 5 bits character and 2 stop bit else.
This bit = 1 will select 1 stop bit.

Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

For Telex communication the number of bits is 5 with 1,5 stop bit and no parity checking/generation.

OUTPUT CHANNEL

Status Register.

Bit	0	Ready for transfer interrupt enabled
	1, 2	Not used
	3	Device ready for transfer
	4–10	Not used
	11	Line polarity
	12	Line impedance
	13	Missing connection
	14	Watchdog
	15	

Bit 3: This bit indicates that the output data register is ready to receive a new character.

Bit 11-14: As for the Input channel and should be checked before starting a call.

Control Register.

Bit	0	Enable interrupt on ready for transfer
	1–9	Not used
	10	Set line impendance low (call)
	11	Set line impendance high (break)
	12	Not used
	13, 14	1/2 and 1/4 speed
	15	Not used

Bit 10: This bit is used to call the Telex Exchange. The impendance (Status bit 12) remains low until reset by Control Register bit 11.

Bit 11: Break connection to the Telex Exchange.

Bit 13-14: 1/2 speed is used when connected to special lines and means that every second character only is sent on the telex line. It means that a dummy character has to be loaded into the output data register between the data characters.
1/4 speed means that every fourth character is sent and three dummy characters must be loaded between the data characters.
The content of these bits gives the following combinations:

Bit 14	Bit 13	Operation
0	0	Normal
0	1	1/2 speed
1	0	Not used
1	1	1/4 speed

BAUD RATE SELECTION

The baud rate for telex communication is 50 baud, but is selectable by switches on the card according to the following table. The data rate is common for input and output and for both interfaces.

BAUD RATE	SWITCHES 4	3	2	1
50	ON	ON	OFF	ON
75	ON	ON	OFF	OFF
100	ON	ON	ON	ON
100	ON	ON	ON	OFF
110	OFF	OFF	OFF	OFF
134,5	ON	OFF	ON	ON
150	OFF	OFF	OFF	ON
200	ON	OFF	ON	OFF
300	OFF	OFF	ON	OFF
600	ON	OFF	OFF	ON
1200	OFF	ON	OFF	OFF
1800	OFF	ON	OFF	ON
2400	ON	OFF	OFF	OFF
2400	OFF	OFF	ON	ON
4800	OFF	ON	ON	OFF
9600	OFF	ON	ON	ON

DEVICE NUMBER AND IDENT CODE SELECTION

Device numbers and ident codes are selected by the switches in positions 10A and 6E. The two interfaces on one card has consecutiv device numbers and ident codes. The switches are binary coded and other combinations than those in table may be used. Switch number 6E8 is not used.

DEVICE NUMBERS						
Switch / Bit / No.	10A6 BA9	10A5 BA8	10A4 BA7	10A3 BA6	10A2 BA5	10A1 BA4
200	OFF	OFF	ON	OFF	OFF	OFF
210	OFF	OFF	ON	OFF	OFF	OFF
220	OFF	OFF	ON	OFF	OFF	ON
230	OFF	OFF	ON	OFF	OFF	ON
240	OFF	OFF	ON	OFF	ON	OFF
250	OFF	OFF	ON	OFF	ON	OFF
260	OFF	OFF	ON	OFF	ON	ON
270	OFF	OFF	ON	OFF	ON	ON
300	OFF	OFF	ON	ON	OFF	OFF
310	OFF	OFF	ON	ON	OFF	OFF
320	OFF	OFF	ON	ON	OFF	ON
330	OFF	OFF	ON	ON	OFF	ON
340	OFF	OFF	ON	ON	ON	OFF
350	OFF	OFF	ON	ON	ON	OFF
360	OFF	OFF	ON	ON	ON	ON
370	OFF	OFF	ON	ON	ON	ON
1100	ON	OFF	OFF	ON	OFF	OFF
1110	ON	OFF	OFF	ON	OFF	OFF
1120	ON	OFF	OFF	ON	OFF	ON
1130	ON	OFF	OFF	ON	OFF	ON
1140	ON	OFF	OFF	ON	ON	OFF
1150	ON	OFF	OFF	ON	ON	OFF
1160	ON	OFF	OFF	ON	ON	ON
1170	ON	OFF	OFF	ON	ON	ON

IDENT CODES							
Switch / Bit / Code	6E7 7	6E6 6	6E5 5	6E4 4	6E3 3	6E2 2	6E1 1
60	OFF	OFF	ON	ON	OFF	OFF	OFF
61	OFF	OFF	ON	ON	OFF	OFF	OFF
62	OFF	OFF	ON	ON	OFF	OFF	ON
63	OFF	OFF	ON	ON	OFF	OFF	ON
64	OFF	OFF	ON	ON	OFF	ON	OFF
65	OFF	OFF	ON	ON	OFF	ON	OFF
66	OFF	OFF	ON	ON	OFF	ON	ON
67	OFF	OFF	ON	ON	OFF	ON	ON
120	OFF	ON	OFF	ON	OFF	OFF	OFF
121	OFF	ON	OFF	ON	OFF	OFF	OFF
122	OFF	ON	OFF	ON	OFF	OFF	ON
123	OFF	ON	OFF	ON	OFF	OFF	ON
44	OFF	OFF	ON	OFF	OFF	ON	OFF
45	OFF	OFF	ON	OFF	OFF	ON	OFF
46	OFF	OFF	ON	OFF	OFF	ON	ON
47	OFF	OFF	ON	OFF	OFF	ON	ON
130	OFF	ON	OFF	ON	ON	OFF	OFF
131	OFF	ON	OFF	ON	ON	OFF	OFF
132	OFF	ON	OFF	ON	ON	OFF	ON
133	OFF	ON	OFF	ON	ON	OFF	ON
134	OFF	ON	OFF	ON	ON	ON	OFF
135	OFF	ON	OFF	ON	ON	ON	OFF
136	OFF	ON	OFF	ON	ON	ON	ON
137	OFF	ON	OFF	ON	ON	ON	ON

DEVICE NUMBERS						
Switch / Bit / No.	10A6 BA9	10A5 BA8	10A4 BA7	10 A3 BA6	10A2 BA5	10A1 BA4
1200	ON	OFF	ON	OFF	OFF	OFF
1210	ON	OFF	ON	OFF	OFF	OFF
1220	ON	OFF	ON	OFF	OFF	ON
1230	ON	OFF	ON	OFF	OFF	ON
1240	ON	OFF	ON	OFF	ON	OFF
1250	ON	OFF	ON	OFF	ON	OFF
1260	ON	OFF	ON	OFF	ON	ON
1270	ON	OFF	ON	OFF	ON	ON
1300	ON	OFF	ON	ON	OFF	OFF
1310	ON	OFF	ON	ON	OFF	ON
1320	ON	OFF	ON	ON	OFF	ON
1330	ON	OFF	ON	ON	OFF	ON
1340	ON	OFF	ON	ON	ON	OFF
1350	ON	OFF	ON	ON	ON	OFF
1360	ON	OFF	ON	ON	ON	ON
1370	ON	OFF	ON	ON	ON	ON

IDENT CODES							
Switch / Bit / Code	6E7 7	6E6 6	6E5 5	6E4 4	6E3 3	6E2 2	6E1 1
70	OFF	OFF	ON	ON	ON	OFF	OFF
71	OFF	OFF	ON	ON	ON	OFF	OFF
72	OFF	OFF	ON	ON	ON	OFF	ON
73	OFF	OFF	ON	ON	ON	OFF	ON
74	OFF	OFF	ON	ON	ON	ON	OFF
75	OFF	OFF	ON	ON	ON	ON	OFF
76	OFF	OFF	ON	ON	ON	ON	ON
77	OFF	OFF	ON	ON	ON	ON	ON
50	OFF	OFF	ON	OFF	ON	OFF	OFF
51	OFF	OFF	ON	OFF	ON	OFF	OFF
52	OFF	OFF	ON	OFF	ON	OFF	ON
53	OFF	OFF	ON	OFF	ON	OFF	ON
54	OFF	OFF	ON	OFF	ON	ON	OFF
55	OFF	OFF	ON	OFF	ON	ON	OFF
56	OFF	OFF	ON	OFF	ON	ON	ON
57	OFF	OFF	ON	OFF	ON	ON	ON

Start transmitter.

Before starting to transmit the status bits 11-14 should be checked. The correct status when the line is idle should be:

```
Status bit  11 = 0
  "     "   12 = 1
  "     "   13 = 0
  "     "   14 = 0
```

Interrupt enable, 5 bits character, 1,5 stop bit and no parity check/gen. should then be set. The line is activated by setting output control word bit 10 (Line impedance) and the Telex Exchange should (within 5 sec.) answer by changing polarity, which gives interrupt to level 10. The correct status when the line is active should be:

```
Status bit  11 = 1
  "     "   12 = 0
  "     "   13 = 0
  "     "   14 = 0
```

The line is now ready for data exchange and starts with reception of the Telex Exchange Register number (interrupt level 12).

Stop Transmitter.

After transmission of data the line impendance is set high. The Telex Exchange should within 500 ms change polarity on the line (No interrupt) and the status signals will go into idle state. Wait at least 2 sec. before a new call can take place.

Start Receiver.

The receiver is automatically started with interrupt to level 12 when the first character is received and the status should be

```
Status bit  11 = 1
  "     "   12 = 0
  "     "   13 = 0
  "     "   14 = 0
```

Stop Receiver.

After reception of the last data the Telex Exchange will disconnect, which gives Missing connection interrupt to level 12. Status should then be:

```
Status bit  11 = 1
  "     "   12 = 0
  "     "   13 = 1
  "     "   14 = 0
```

Then the impedance should be set high and wait 2 sec. before a call can take place.

HDLC

PROGRAMMING SPECIFICATIONS

The HDLC interface for NORD-10 computers is designed around a Multi Protocol Communication Controller, MPCC, of the type X2652 from Signetics or the almost equivalent COM 5025 from SMC Micro systems.

Sixteen different I/O instructions are used to control the interface. Eight are used to read from or write into the MPCC, four are for status and control and four are for DMA Module Address and Command.

Possible interface standards are:

a) CCITT V-24, CCITT X-21 BIS, CCIT X-21 (X-27 signal levels), EIA RS-232-C and EIA RS-422.

b) CCITT V-35.

The interface is also equipped with an internal clock which makes it easy for two interfaces to communicate without external communication equipment (MODEMS).

The interface may be extended with a DMA module to reduce software load on interrupt and I/O handling. Four I/O instructions are used separate from the DMA module and four are used together with data module.

The 16 I/O instructions are:

Group No. + 0	Read Receiver Data Register	(RxDR)
Group No. + 1	Write Parameter Control Register	(PCR)
Group No. + 2	Read Receiver Status	(RxSR)
Group No. + 3	Write Synch/Address Register	(SAR)
Group No. + 4	Write Character Length	(CL)
Group No. + 5	Write Transmitter Data Register	(TxDR)
Group No. + 6	Read Transmitter Status Register	(TxSR)
Group No. + 7	Write Transmitter Control Register	(TxCW)
Group No. + 10	Read Receiver Transfer Status	
Group No. + 11	Write Receiver Transfer Control	
Group No. + 12	Read Transmitter Transfer Status	
Group No. + 13	Write Tranmitter Transfer Control	
Group No. + 14	Read DMA Address	
Group No. + 15	Write DMA Address	
Group No. + 16	Read DMA Command Register	
Group No. + 17	Write DMA Command	

Instructions 0-7 operate directly on the MPCC. For a detailed description of these registers (bit mapping, etc.) the reader is advised to study the data sheets from the manufacturers or the HDLC Interface Control Hardware Manual (ND-11.018).

Note that all I/O instructions operate only on bits 0-7 when the DMA module is not installed.

In this text registers 0-7 are named related to X2652 Signetics notations. For cross reference to COM 5025 and HDLC Hardware Manual equivalent register notations are given.

IOX Instruction Overview Table

IOX + GP 0, Read Receiver Data Register:

Receiver Data Register is the low byte of the Receiver Data/Status Register (RDSRL) as described in the data sheet. An assembled character (byte) is read from the interface into the A register in the CPU. (Character length is specified by IOX GP + 4 or indicated by RDSRH (IOX GP + 2.) The received character is right justified.

IOX GP + 1, Write Parameter Control Register (PCSARH):

This is the high byte (bits 8-15) of the Parameter Control Sync/Address Register (PCSARH) described in the data sheet. The register defines protocol, etc. Refer to the data sheet.

IOX GP + 2, Read Receiver Status Register:

This is the high byte of the Receive Data/Status Register (RDSRH) and contains receiver status information. Bit mapping is described in the data sheet.

IOX GP + 3, Write Sync/Address Register:

The Sync/Address Register holds the secondary station address in bit-oriented procedures or the SYNC character in byte-oriented procedures. It is the lower byte (Byte Control Procedure) of the Parameter Control Sync/Address Register (PCSARL). Refer to the data sheet.

IOX GP + 4, Write Character Length:

The high byte of the Parameter Control Register (PCRH) is used to specify character length for receiver (bits 0-2) and transmitter (bits 5-7). At this point there is a difference between X2652 and Signetics and COM 5025 from SMC Micro systems. See the data sheet. Equal operation when bits 3 and 4 are 0.

IOX GP + 5, Write Transmitter Data Register:

The low byte of the Transmit Data/Status Register (TDSRL) holds the character to be transmitted. The character length is specified by IOX GP + 4. Character must be right-justified.

IOX GP + 6, Read Transmitter Status Register:

The high byte of the Transmit Data/Status Register (TDSRH) contains transmitter command and status information. The functions of the different bits are described in the data sheets.

IOX GP + 7, Write Transmitter Control Register:

This is the same byte as may be read by IOX GP + 6.

IOX GP + 10, Read Receiver Transfer Status:

The low byte is the receiver transfer status from the data modules. The high byte is the transfer status from the DMA module, and is not used unless the DMA module is installed.

Bit mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OR				EMTY	LE	FE	BE	RI	DSR	SD	DMA RQ	SFR	RXA	RXSA	RXDA
DMA ONLY															

Bit 0: Data Available

Indicates that a character has been assembled and may be read from the Receiver Data Register (RDSRL). Interrupt on level 13 if enabled.

Bit 1: Status Available

Indicates that status information is available in the Receiver Status Register (RDSRH). Interrupt on level 13 if enabled.

Bit 2: Receiver Active

The receiver has seen the start of a frame, but not the end. This means that the receiver is active within a frame.

Bit 3: Sync/Flag Received

At least one SYNC character or FLAG has been receiver after the last reading of Receiver Transfer Status or Master Clear/ Device Clear.

Bit 4: 0 (DMA Module Request)

This bit is activated by the DMA module. If the DMA module is installed, this bit may be the reason for an interrupt on level 13 if enabled. It is, however, always read as 0 because it is cleared at the beginning of IOX GP + 10. If the DMA module caused an interrupt, the reason for this interrupt is given in the most significant byte of the Transfer Status.

Bit 5: Signal Detector (SD)

Status of the Signal Detector (CCITT circuit 109) from the Data Communication Equipment. A change in the status causes an interrupt on level 13 if enabled.

Bit 6: Data Set Ready/I (DSR)

Status of the Data Set Ready (CCITT circuit 107) signal (V-24, X-21 BIS) or the I signal (X-21) from the Data Communication Equipment. A change in the status causes an interrupt on level 13 if enabled.

Bit 7: Ring Indicator (RI)

Status of the Ring Indicator (CCITT circuit 125) from the Data Communication. A change in the status causes an interrupt on level 13 if enabled.

Bit 8: Block End Status bit from DMA module.

Bit 9: Frame End Status bit from DMA module.

Bit 10: List End Status bit from DMA module.

Bit 11: List Empty Status bit from DMA module.

Bit 15: Receiver Overrun Status bit.

Note: Bits 8-15 are cleared by reading the Receiver Transfer Status.

IOX GP + 11, Write Receiver Transfer Control:

The low byte is for interrupt and data enabling on the data module and also some Data Communication Equipment control signals. The high byte is for DMA module control signal.

Bit mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					LE Int. Ena.	PE Int. Ena.	BE Int. Ena.	Msc. Int. Ena.	DTR	Maint. (Dev. clear)	Int. Ena. DMA	Ena. DMA	RXE	Int. Ena Status	Int Ena. Data
DMA ONLY															

Bit 0: Data Available Interrupt Enable

A 1 in this bit together with Data Available (RXDA) will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 1: Status Available Interrupt Enable

A 1 in this bit together with Status Available (RXSA) will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 2: Enable Receiver (RXE)

Incoming serial data stream is enabled into the receiver. The bit is cleared by MASTER CLEAR.

Bit 3: Enable Receiver DMA

With a 1 in this bit, Data Available (RXDA) will cause a request to the DMA module. The bit is cleared by MASTER CLEAR and by a "List Empty" key during DMA operation.

Bit 4: DMA Module Interrupt Enable

A 1 in this bit together with a request from the DMA module will cause an interrupt on level 13. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 5: Device Clear/Select Maintenance

Writing a 1 into this bit first gives a DEVICE CLEAR, clearing interrupts and interrupt enabling flip-flops, control signals to the Data Communication Equipment, transmitter control signals, Data Communication Equipment status latches and the Multi Protocol Communication Controller. Then it turns the Multi Protocol Communication Controller into maintenance mode, looping transmitted data back to the received data. When the interface is in maintenance mode, the DEVICE CLEAR function is disabled. The bit is cleared by MASTER CLEAR.

Bit 6: Data Terminal Ready/C (DTR)

This bit controls a line to the Data Communication Equipment. It is the Data Terminal Ready (CCITT circuit 108) signal (V-24, X-21 BIS) or the C signal (X-21). The bit is cleared by MASTER CLEAR.

Bit 7: Modem Status Change Interrupt Enable

When set, this bit will cause an interrupt on level 13 when one or more of the Data Communication Equipment status signals connected to the receiver changed to a state different from the last reading (SD, DS/I, RI). The bit is cleared by servicing IDENT, by MASTER CLEAR and DEVICE CLEAR.

Bit 8: Block End Interrupt Enable

This bit will, together with Block End and DMA Module Interrupt Enable, cause an interrupt on level 13.

Bit 9: Frame End Interrupt Enable

This bit will, together with Frame End and DMA Module Interrupt Enable, cause an interrupt on level 13.

Bit 10: List End Interrupt Enable

This bit will, together with List End and DMA Module Interrupt Enable, cause an interrupt on level 13.

Bit 15: Always 1 after IOX + 11 if inspected after a DUMP command (M11).

Note that List Empty (Receiver Transfer Status, Bit 11) always gives a DMA Module Request (Bit 4).

IOX GP + 12, Read Transmitter Status:

The low byte is the transmitter transfer status from the data module. The high byte is the transfer status from the DMA module if installed.

Bit mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR				TR FIN	LE	FE	BE		RFS		DMA RQ		TXA	TXU	TXBE
DMA ONLY															

Bit 0:	Transmit Buffer Empty Indicates that the Transmit Buffer (TDSRL) may be loaded with a new character. Interrupt on level 12 if enabled.
Bit 1:	Transmitter Underrun Indicates that the Transmit Buffer has not been loaded with a new character in time. The transmitter will act as defined by the IOX GP + 1 instruction (PCSARH). The underrun condition may cause an interrupt on level 12 if enabled. Transmitter Underrun may be cleared by Master Clear, Device Clear or Transmit Start of Message (TSOM) command.
Bit 2:	Transmitter Active This bit is turned on by sending Start of Message. It will go off when Transmitter Enable (TXE) is turned off and the characters or sequences already in the transmitter are shifted out on the Transmit Data Line (TSO).
Bit 3:	Not used
Bit 4:	0 (DMA Module Request) This bit is activated by the DMA module, and thus it has no meaning unless the DMA module is installed. It is, however, always read as 0 because it is cleared at the beginning of IOX GP + 12. If the DMA module is installed, additional information is given in the high byte. DMA Module Request causes an interrupt on level 12 if enabled.
Bit 5:	Not used
Bit 6:	Ready for Sending (RFS) Status signal from the Data Communication Equipment (CCITT circuit 106). A change in the status causes an interrupt on level 12 if enabled.
Bit 7:	Not used
Bit 8:	Block End Status bit from DMA module.
Bit 9:	Frame End Status bit from DMA module.
Bit 10:	List End Status bit from DMA module.
Bit 11:	Transmission Finished status bit from the DMA module.
Bit 15:	Illegal Key or Illegal Format in Transmitter Buffer Descriptor This status bit indicates an error stop and the transmitter should be restarted.

IOX GP + 13, Write Transmitter Transfer Control:

The low byte is for interrupt and data enabling on the data module and also two signals concerning the connection to the Data Communication Equipment. The high byte if for the DMA module.

Bit mapping:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved for DMA module					LE Int. Ena.	FE Int. Ena.	BE Int. Ena.	MSC Int. Ena.	RQTS	HDX	Int. Ena. DMA	EN DMA	TXE	Int. Ena. Status	Int. Ena. Data
DMA ONLY															

Bit 0: Transmit Buffer Empty Interrupt Enable

A 1 in this bit together with Transmit Buffer Empty (TXBE) will cause an interrupt on level 12. This bit is cleared by a servicing IDENT, by MASTER CLEAR or DEVICE CLEAR.

Bit 1: Transmitter Underrun Interrupt Enabled

A 1 in this bit together with a Transmitter Underrun condition will cause an interrupt on level 12. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 2: Transmitter Enabled (TXE)

A 1 in this bit together with Ready for Sending (RFS) (CCITT circuit 106) enables the transmitter part of the Multi Protocol Communication Control (MPCC) to be 1 (MARK) and the Transmitter (TXA) to go off when closing flag or last character has been transmitted. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 3: Enable Transmitter DMA

With a 1 in this bit, Transmitter Buffer Empty (TXBE) will cause a request to the DMA module. This bit is cleared by MASTER CLEAR by Transmission Finished or by Illegal Key/Format (DMA operation).

Bit 4: DMA Module Interrupt Enable

A 1 in this bit together with a request from the DMA module will cause an interrupt on level 12. The bit is cleared by a servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 5: Half Duplex

A 1 in this bit will cause the interface to operate in a half duplex mode. The request to send (RQTS) (CCITT circuit 105) signal is not turned ON unless the Signal Detector (SD) (CCITT circuit 109) is off. A 0 in this bit will cause the interface to operate in a full duplex mode. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 6: Request to Send (RQTS)

This is a control signal to the Data Communication Equipment (CCITT circuit 105). In full duplex, 1 means ON and 0 means OFF. In half duplex, Signal Detector (SD) (CCITT circuit 109) must be OFF before the Request to Send line goes ON. Normal response from the Data Communication Equipment is to turn Ready for Sending (CCITT circuit 106) ON when Request to Send is ON. The bit is cleared by MASTER CLEAR and by DEVICE CLEAR.

Bit 7: Modem Status Change Interrupt Enable

When set, this bit will cause an interrupt on level 12 when Ready for Sending from the Data Communication Equipment changes to a state different from the last reading. The bit is cleared by servicing IDENT, by MASTER CLEAR and by DEVICE CLEAR.

Bit 8: Block End Interrupt Enable

This bit will, together with Block End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 9: Frame End Interrupt Enable

This bit will, together with Frame End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 10: List End Interrupt Enable

This bit will, together with List End and DMA Module Interrupt Enable, cause an interrupt on level 12.

Bit 15: Always 1 after IOX GP + 13 if inspected after a DUMP command (M15)

Note that Transmission Finished (Transmitter Transfer Status, bit 11) always gives a DMA Module Request (bit 4).

Note that bit 15 is 1 if inspected after a DUMP command.

IOX GP + 14, Read DMA Address:

The last value written to this register by IOX GP + 15 is read back. May be used for debugging or control.

IOX GP + 15, Write DMA Address:

The 16 least significant bits for the first location in a load/dump area or the first location in a list of buffer descriptors are written into a register (M3) in the DMA module.

IOX GP + 16, Read DMA Command Register:

Before a new command is written to the DMA module, this register should be inspected. If it is zero, the new command sequence can be started. If not, wait until it becomes zero. A MASTER CLEAR command sequence can, however, be started even if the command register is not zero.

IOX GP + 17, Write DMA Command:

The two most significant bits of the address for the first location in a load/dump area or the first location in a list of buffer descriptors are written into a register (M2) in the DMA module together with a value giving one of 8 commands. The data format for this instruction is described in the next section.

The HDLC DMA module is partly controlled by I/O instructions, and partly by control information in buffers in main memory. I/O instructions are used to set buffer addresses, to start operations (give commands), to enable interrupts and to read status.

Control information in the memory is used as additional information for the interface when an operation has been started (by a command).

HDLC IOX INSTRUCTIONS

	MPCC
	1141
1151	1141

IOX GROUP NO.+	FUNCTION	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	READ RECEIVER DATA REGISTER									Rx7	Rx6	Rx5	Rx4	Rx3	Rx2	Rx1	Rx0
1	WRITE PARAMETER CONTROL REG.									0	PROT SEL.	STRIPS GA	SEC A MODE	IDLE MODE	CRC SEL2	CRC SEL1	CRC SEL0
2	READ RECEIVER STATUS									RERR	RSCL2	RSCL1	RSCL0	ROV RUN	RABORT	REOM	RSOM
3	WRITE SYNC/ADDRESS REGISTER									SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
4	WRITE CHARACTER LENGTH									TxCL2	TxCL1	TxCL0	0	0	RxCL2	RxCL1	RxCL0
5	WRITE TRANSMITTER DATA REGISTER									TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
6	READ TRANSMITTER STATUS REG.									TUNDR	0	0	0	TGA	TABORT	TEOM	TSOM
7	WRITE TRANSMITTER CONTROL REG.									0	0	0	0	TGA	TABORT	TEOM	TSOM
10	READ RECEIVER TRANSFER STATUS	ROV RUN				LIST EMTY	LE	FE	BE	RI	DSR	SD	DMA RQ	SFR	RXA	RXSA	RXDA
11	WRITE RECEIVER TRANSFER CONTROL	*					INT EN	INT EN	INT EN	MSG INT E	DTR	MAINT	DMA INT E	ENA DMA	RXE	INIT EN	INIT EN
12	READ TRANSMITTER TRANSFER STATUS	ERR				TR FIN	LE	FE	BE		RFS		DMA RQ		TXA	TXU	TXBE
13	WRITE TRANSMITTER TRANSF. CONTR.	*					INT EN	INT EN	INT EN	MSC INT E	RQTS	HDX	DMA INT E	ENA DMA	TXE	INT EN	INT EN
14	READ DMA ADDRESS.	16 LEAST SIGNIFICANT BITS OF COMMAND ADDRESS															
15	WRITE DMA ADDRESS	16 LEAST SIGNIFICANT BITS OF COMMANDS ADDRESS															
16	READ DMA COMMAND REGISTER	0	0	0	0	0	Command Code			0	0	X	0	0	0	Bank Bits	
17	WRITE DMA COMMAND REG. + TRIGGER	0	0	0	0	0	Command Code			0	0	X	0	0	0	Bank Bits	

NOTES:

* THIS BIT IS 1 IF INSPECTED AFTER A DUMP COMMAND. DMA PQ IS ALWAYS READ AS 0 (CLEARED AT THE START OF THE IOX INSTRUCTION) IOX GP+10 or IOX GP+12.

X BIT 5 IN COMMAND SHOULD BE 0 EXCEPT FOR DEVICE CLEAR COMMAND

A.4.1 *Speed Selection (Switch Setting on 1181) Intercomputer Link*

	11F1	11F2	11F3	11F4	11F5	11F6
2,400 bps	OFF	OFF	OFF	ON	OFF	ON
4,8000 bps	OFF	OFF	ON	OFF	OFF	ON
9,600 bps	OFF	ON	OFF	OFF	OFF	ON
19,200 bps	ON	OFF	OFF	OFF	OFF	ON
38,400 bps	OFF	OFF	OFF	ON	ON	OFF
76,800 bps	OFF	OFF	ON	OFF	ON	OFF
153,600 bps	OFF	ON	OFF	OFF	ON	OFF
307,200 bps	ON	OFF	OFF	OFF	ON	OFF

HDLC DATA 1181

Switch	Position	Device No. (octal)	Ident Code (octal)	Comments
3C1	OFF ON		0 1	
3C2	OFF ON		0 2	
3C3	OFF ON		0 4	
3C4	OFF ON		0 10	
3C5	OFF ON		0 20	
3C6	OFF ON		0 40	
3C7	OFF ON		0 100	
3C8	OFF ON		0 200	
10A1	OFF ON			Test, CLK Disconnected Normal, CLK Connected
10A2	OFF ON			X-21 Interface V-24 Interface
10A3	OFF ON	0 20		
10A4	OFF ON	0 40		
10A5	OFF ON	0 100		
10A6	OFF ON	0 200		
10A7	OFF ON	0 400		
10A8	OFF ON	0 1000		

Standard Device Numbers:

1640-1657
1660-1667
1700-1720
1740-1757
1760-1777

2 MASS STORAGE DEVICES

NORD-10 DRUM PROGRAMMING SPECIFICATION

1 DRUM DEVICE REGISTER ADDRESSES

The codes below are relevant for drum unit 0. For several drums connected to one system the codes for each drum system are found by adding $10_8 \cdot N$ to those specified. N = drum number (0, 1, 2, 3).

1.1 Read Core Address

IOX 540

1.2 Load Core Address

IOX 541

1.3 Read Sector Counter

IOX 542

1.4 Load Block Address

IOX 543

1.5 Read Status Register

IOX 544

1.6 Load Control Register

IOX 545

1.7 Load Word Count Register

IOX 547

The minumum number of words to be transferred is one sector 100 words, the maximum number of words is one track, i.e. 32 sectors.

1.8 Read Block Address

This instruction is implemented for maintenance purposes only.

By first loading a control word with bit 3 (Tes Mode) the instruction

IOX 546

will return the previously loaded block address to the A-register.

1.9 Control Word

Bit		
Bit	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5	Address bit 16
	6	Address bit 17
	7-10	Not assigned
	11	Device operation
	12	Device operation

1.10 Device Operation Code

Bit	12	11	
	0	0	Read transfer
	0	1	Write transfer
	1	0	Read parity
	1	1	Compare

1.11 Status Word

Bit	0	Ready for transfer, interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors (status bits 5-11)
	5	Write protect violate
	6	Time out

7	Hardware error
8	Bit transfer error
9	Parity error
10	Compare error
11	DMA channel error
12	Transfer complete
13	Transfer on
14	No assignment
15	Bit 15 loaded by previous control word

1.12 Interrupt

The drum interrupt level is 11 and the ident number for the first drum is 2.

NORD-10 DISC PROGRAMMING SPECIFICATION HAWK/FALCON DISK

1 DISC DEVICE REGISTER ADDRESS

The codes below are relevant for disc system I. Each disc system may consist of 4 disc units. For disc system II add 10_8 to the specified codes.

1.1 Read Core Address

IOX 500

1.2 Load Core Address

IOX 501

1.3 Read Sector Counter

IOX 502

1.4 Load Block Address

IOX 503

1.5 Read Status Register

IOX 504

1.6 Load Control Word

IOX 505

1.7 Seek Instruction

IOX 506

1.8 Load Word Count Register

IOX 507

The minimum number of words to be transferred is one sector i.e. 200_8 words, the maximum number of words is one track i.e. 24 sectors.

1.9 Read Block Address

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (Test Mode) the instruction

IOX 506

will return the previously loaded block address to the A-register.

1.10 Control Word

Bit		
Bit	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5	Address bit 16
	6	Address bit 17
	7 - 8	Not assigned
	9	Unit select
	10	Unit select
	11	Device operation
	12	Device operation
	13 - 14	Not assigned
	15	Write Format

<u>Unit select Code</u>

Bit	10	9	
	0	0	Unit 0
	0	1	Unit 1
	1	0	Unit 2
	1	1	Unit 3

<u>Device Operation Code</u>

Bit	12	11	
	0	0	Read transfer
	0	1	Write transfer
	1	0	Read parity
	1	1	Compare

To format a disc the key for formatting has to be turned on, Write transfer, and Write Format have to be specified.

1.11 Status Word

Bit	0	Ready for transfer, interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors (status bits 5-11)
	5	Write protect violate
	6	Time out
	7	Hardware error
	8	Address mismatch
	9	Parity error
	10	Compare error
	11	DMA channel error
	12	Transfer complete
	13	Transfer on
	14	On cylinder
	15	Bit 15 loaded by previous control word

1.12 Interrupt

The disc interrupt level is 11 and the ident number for the first disc system is 1.

NORD-10 LARGE DISC PROGRAMMING SPECIFICATION SMD

1 DISC DEVICE REGISTER ADDRESS

The codes below are relevant for disc system I. Each disc system may consist of 8 disc units. For disc system II add 10_8 to the specified codes.

Read Core Address

IOX 1540

Load Core Address

IOX 1541

Read Seek Condition

IOX 1542

Load Block Address

IOX 1543

Read Status Register

IOX 1544

Load Control Word

IOX 1545

Load Word Count Register

IOX 1547

The maximum number of words to be transferred are 16 sectors, 8K words.

Read Block Address

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (Test mode) the instruction

IOX 1546

will return the previous loaded block address to the A-register.

2 DISC FORMAT

2.1 Disc Address

The 16 bit in the Block Address Register have the following meaning:

15 — 7	6 — 4	3 — 0
cylinders	surface	sectors

Bit

0-3	Sector number, 16 sectors per track
4-6	Surface number, 5 surfaces
7-15	Cylinder number, totally 404 cylinders

The most significant bit (bit 15) in the Control word is used to extend the cylinder address to 10 bits, thus enabling a cylinder address of maximum 808 cylinders. This is only relevant for 80 Mbyte discs.

3 CONTROL WORD

3.1 Control Word Content

Bit

0	Enable interrupt on device not active
1	Enable interrupt on errors
2	Activate device operation
3	Test mode/Select unit
4	Device clear (clear the activate flip-flop) and controller error bits.
5	Address bit 16
6	Address bit 17
7-9	Unit select (maximum 8 units)
10	Marginal recovery cycle
11-14	Device operation code
15	Extended cylinder address

3.2 Select Unit

When a Control Word is loaded the disc unit number (0-7) has to be set up in bits 7-9. If the transfer is changed from one unit to another, the new unit must be selected with a special program sequence. Bit 3 in the Control Word, select unit bit (test bit) is used.

Example, selects unit one:

```
UNIT,        200                      %  Unit one, one in bit 7-9
SELUNIT,     LDA UNIT                 %  Load unit number
             AAA 10                   %  Set select unit bit, bit 3
             IOX 1545                 %  Load Control Word
             SAA 20                   %  Device clear to
             IOX LCW                  %  clear possible error status
             IOX 1544                 %  Read status
             BSKP IF ZERO 150 DA      %  Test unit ready
             JMP ERROR                %  No unit ready
% continue to initiate transfer.
```

3.3 Marginal Recovery Cycle

The marginal recovery cycle (control word bit 10) may be used in connection with read operation codes M0, M2 and M3 as defined in section 3.3. This control bit is included to be an aid in recovering marginal data.
For consecutive read transfers with this bit set the controller will cycle through the following conditions:

1	marginal read	: Servo offset positive, data strobe early
2	"	: No servo offset, data strobe early
3	"	: Servo offset negative, data strobe early
4	"	: Servo offset positive, nominal data strobe
5	"	: Servo offset negative, nominal data strobe
6	"	: Servo offset positive, data strobe late
7	"	: No servo offset, data strobe late
8	"	: Servo offset negative, data strobe late
9 = 1	etc.	

3.4 Device Operation

All device operation codes will be activated when the code is given together with bit 3 (activate device). For all codes except M6, the correct unit number must also be selected.

Bit 14	13	12	11		
0	0	0	0	M0	Read transfer
0	0	0	1	M1	Write transfer
0	0	1	0	M2	Read parity transfer
0	0	1	1	M3	Compare transfer
0	1	0	0	M4	Initiate seek
0	1	0	1	M5	Write format
0	1	1	0	M6	Seek complete search
0	1	1	1	M7	Return to zero seek

M0 Read transfer

This operation causes the controller to transfer data from the disc to the computer memory. The number of blocks transferred depends upon the word count as defined by the Word Count Register.

M1 Write transfer

Transfer of data from the computer memory to the disc.

M2 Read parity transfer

The controller will check the parity on the address and data of the sectors specified. Data is transferred to the controller and the cyclic check word for both the address field and the data field of a sector is compared with the correct check word as generated by the controller. No data transfer to the computer memory is performed.

M3 Compare transfer

This function is included to positively check the data written on the disc. During compare transfer the controller compared the data read from the disc and data from the computer memory is compared bit by bit. Mismatch causes compare error to be set.

M4 Initiate seek

This function is included to enable a unit to position the heads prior to a data transfer. The heads will be positioned according to the content of the Block Address Register. As soon as this function is accepted by the disc, the operation will be completed.

M5 Write format

Together with a switch on a card in the interface set, this function will cause the controller to write the adress field within each sector.

M6 Seek complete search

This function will enable the controller to go in a waiting state until any unit has completed a seek. This function is independent of the unit select code in the control word.

M7 Return to zero seek

This will cause the selected disc to perform a seek to cylinder 0 and will also clear the seek error bit in the unit.

3.5 Extended Cylinder Address

Bit 15 in the control word is used as an extension to the cylinder address in the Block Address Register. This extended bit is used to allow addresses of up to 808 cylinders.

4 READ SEEK CONDITION (IOX 1542)

Bit 0-7 SEEK COMPLETE

Seek complete status for unit 0-7. True if the unit has moved the heads to the correct cylinder or a seek error has occurred, and the heads are under the sector number prior to the one specified by the block address loaded before the initiate seek command. The seek complete status will only be set if an initiate seek command for that unit has first been issued.

Thus, after an initiate seek command is given, the SEEK COMPLETE bit for that unit will appear once per revolution after the unit is positioned on the correct cylinder, or a seek error has occurred. The condition will last until a transfer command is given.

Bit 8-10 UNIT SELECT

The unit number as loaded by the last control word.

Bit 11 SEEK ERROR

Seek error for the selected unit. This signal indicates that the unit was unable to complete a move within 500 ms, or that the heads have moved to a position outside the recording field, or that an address greater than the maximum number of tracks has been selected.

This signal will only be cleared by performing a RETURN to ZERO command on that unit.

5 READ STATUS

Status word:

Bit	0	Controller not acitve interrupt enabled.
	1	Error interrupt enabled
	2	Controller active.
	3	Controller finished with a device operation.
	4	Inclusive or of errors (Bit 5-13).
	5	Illegal load i.e. load while status bit 2 is true, or load of block address while the unit is not on cylinder.
	6	Time out.

Bit	7	Hardware error (Disc fault + missing read clocks + missing servo clocks.)
	8	Address mismatch
	9	Parity error
	10	Compare error
	11	DMA channel error
	12	Abnormal completion
	13	Disc unit not ready
	14	On cylinder
	15	Extended cylinder address

6 INTERRUPT

The disc interrupt level is 11 and the ident number for disc system I is 17 and for disc system II 20.

NORD-10 SUPER DISK PROGRAMMING SPECIFICATIONS

1. DISK DEVICE REGISTER ADDRESS

The IOX instruction can address two banks of registers. Which bank is being addressed is controlled by bit 15 of the Control Word Register (CWR).

The codes below are relevant for Disk System I. Each disk system may consist of 8 disk units. For Disk System II, add 10_8 to the specified codes.

	CWR bit 15 = 0		CWR bit 15 = 1
IOX1540:	READ CORE ADDRESS	-	READ CORE ADDRESS
IOX1541:	LOAD CORE ADDRESS	-	LOAD CORE ADDRESS
IOX1542:	READ SEEK CONDITION		READ ECC COUNT
IOX1543:	LOAD BLOCK ADDR I		LOAD BLOCK ADDR II
IOX1544:	READ STATUS REGISTER		READ ECC PATTERN
IOX1545:	LOAD CONTROL WORD	-	LOAD CONTROL WORD
IOX1547:	LOAD WORD COUNT		LOAD ECC CONTROL

Each transfer is limited to one track (18 sectors) of data.

IOX1546: READ BLOCK ADDRESS I   READ BLOCK ADDRESS II

This instruction is implemented for mainttenance purposes only. By first loading, a control word with bit 3 (Test Mode), this instruction will return the previous loaded block address to the A-register.

2. DISK FORMAT

2.1. Disk address

There are two block address registers that both have to be loaded to completely specify a disk address. The formats are:

Block Address Register I:

15 14 ... 9 8	7 6 ... 3 2 1 0
SURFACE	SECTOR

Bits 0-7 : Sector number, 18 per track (0-17)
Bits 8-15 : Surface number
- for 38/75 Mbytes disk: 5 max. (0-4)
- for 288 Mbytes disk: 19 max. (0-18)

Block address register II:

15 14	2 1 0
CYLINDER	

Bits 0-15: Cylinder number
- for 38 Mbytes disk: 411 max.
- for 75/288 Mbytes disk: 823 max.

3. CONTROL WORD

3.1 Control Word Content

Bit	
0	Enable interrupt on device not active
1	Enable interrupt on errors
2	Activate device operation
3	Test mode
4	Device clear (clear the active flip-flop) and controller error bits
5	Address bit 16
6	Address bit 17
7-9	Unit select (maximum 8 units)
10	Marginal recovery cycle
11-14	Device operation code
15	Register multiplex bit

3.2 Select Unit

When a Control Word is loaded, the disk unit number (0-7) has to be set up in bits 7-9.

3.3 Marginal Recovery Cycle

The marginal recovery cycle (control word bit 10) may be used in connection with read operation codes M0, M2 and M3 as defined in section 3.4. This control bits is included to be an aid in recovering marginal data. For consecutive read transfers with this bit set the controller will cycle through the following conditions:

1 marginal read : Servo offset positive, data strobe early
2 marginal read : No servo offset, data strobe early
3 marginal read : Servo offset negative, data strobe early
4 marginal read : Servo offset positive, nominal data strobe
5 marginal read : Servo offset negative, nomianl data strobe
6 marginal read : Servo offset positive, data strobe late
7 marginal read : No servo offset, data strobe late
8 marginal read : Servo offset negative, data strobe late
9=1 etc.

3.4 Device Operation

All device operation codes will be activated when the code is given together with bit 3 (activate device). For all codes except M6, the correct unit number must also be selected.

Bit 14	13	12	11		
0	0	0	0	M0	Read transfer
0	0	0	1	M1	Write transfer
0	0	1	0	M2	Read parity transfer
0	0	1	1	M3	Compare transfer
0	1	0	0	M4	Initiate seek
0	1	0	1	M5	Write format
0	1	1	0	M6	Seek complete search
0	1	1	1	M7	Return to zero seek
1	0	0	0	M8	Run ECC operation

M0 Read Transfer

This operation causes the controller to transfer data from the disk to the computer memory. The number of blocks transferred depends upon the word count as defined by the word Count Register.

M1 Write Transfer

Transfer of data from the computer memory to the disk.

M2 Read Parity Transfer

The controller will check the parity on the address and data of the sectors specified. Data is transferred to the controller and the check word for both the address field and the data field of a sector is compared with the correct check word as generated by the controller. No data transfer to the computer memory is performed.

M3 Compare Transfer

This function is included to positively check the data written on the disk. During compare transfer the controller compares the data read from the disk and data from the computer memory is compared bit by bit. Mismatch causes compare error to be set.

M4 Initiate Seek

This function is included to enable a unit to position the heads prior to a data transfer. The heads will be positioned according to the contents of the Block Address Register. As soon as this function is accepted by the disk, the operation will be completed.

M5 Write Format

Together with a switch on a card in the interface set, this function will cause the controller to write the address field within each sector.

M6 Seek Complete Search

This function will enable the controller to go in a waiting state until any unit has completed a seek. This function is independent of the unit select code in the control word.

M7 Return to Zero Seek

This will cause the selected disk to perform a seek to cylinder 0 and will also clear the seek error bit in the unit.

M8 Run ECC Operation

This function will, when a data error has occured, initiate the hardware operation that determines if the error is correctable or uncorrectable. If the error is correctable, the error pattern and its displacement within the data field is computed.

4. READ SEEK CONDITION

Bits 0-7 SEEK COMPLETE

Seek complete status for units 0-7. True if the unit has moved the heads to the correct cylinder or a seek error has occured, and the heads are under the sector number prior to the one specified by the block address loaded before the initiate seek command. The seek complete status will only be set if an initiate seek command for that unit has first been issued.

Thus, after an initiate seek command is given, the SEEK COMPLETE bit for that unit will appear once per revolution after the unit is positioned on the correct cylinder, or a seek error has occured. The condition will last until a transfer command is given.

Bits 8-10 UNIT SELECT

The unit number as loaded by the last control word.

Bit 11 SEEK ERROR

Seek error for the selected unit. This signal indicates that the unit was unable to complete a move within 500 ms, or that the heads have moved to a position outside the recording field, or that an address greater than the maximum number of tracks has been selected.

This signal will only be cleared by performing a RETURN TO ZERO command on the unit.

Bit 12 (Not defined)

Bit 13 ECC CORRECTABLE

After the hardware ECC operation has been performed after a data error, this bit signals that the error is correctable and that the ECC Count and ECC Pattern Registers contain valid information for correction of the data. The bit is reset by RESET ECC (ECC Control register bit Ø) or Device Clear.

Bit 14 ECC PARITY ERROR

This bit signals that a hardware fault condition exists in the ECC polynomials. This condition will also set bit 7 of the status word register and hence trigger an error interrupt if this is enabled. The error is reset by the RESET ECC signal (ECC Control register bit Ø) or by DEVICE CLEAR SIGNAL (CWR bit 4). The error is forced set when ECC Control Register bit 1 is active. (FORCE PARITY ERROR).

Bit 15 ADDRESS FIELD

This bit indicates that the last field read from the disk was the address field within a sector. (Used for ECC processing after a data check only).

5. READ STATUS

Status word:

Bit 0	Controller not active interrupt enabled
Bit 1	Error interrupt enabled
Bit 2	Controller active
Bit 3	Controller finished with a device operation
Bit 4	Inclusive OR of errors (bits 5-13)
Bit 5	Illegal load, i.e., load while status bit 2 is true, or load of block address while the unit is not on cylinder
Bit 6	Timeout
Bit 7	Hardware error (disk fault + missing read clocks + missing servo clocks + ECC parity error)
Bit 8	Address mismatch
Bit 9	Data error
Bit 10	Compare error
Bit 11	DMA channel error
Bit 12	Abnormal completion
Bit 13	Disk unit not ready
Bit 14	On cylinder
Bit 15	Register multiplex bit (from CWR bit 15)

6. ECC COUNT REGISTER (ECR)

When a correctable data error has been detected, this register will contain the bit displacement from the beginning of the data field to the last bit in error of the error burst.

7. ECC PATTERN REGISTER (EPR)

Bits 0-10 Contains the RIGHT justified error pattern, such that the last bit in error always occupies bit position 0 of this register. This pattern (the contents of this register bits 0-10) should be exclusively ORed with the data in the CPU memory at the proper location.

Bits 11-14 Set to logical "one".

Bit 15 Register Multiplex bit (from CWR bit 15)

8. ECC CONTROL

Bit 0 Reset ECC
This bit will cause the ECC polynomials to reset to the zero initial state. This function is only used when a data error has occured, otherwise the polynomials automatically go to the zero state upon completion of a READ or WRITE. Device Clear function will also reset ECC.

Bit 1 Force parity error
Used for maintance purposes only. This bit will force ECC parity error to be set.

Bit 2 Long
Used for maintenance purposes only. When a sector is read or written, the data field of the sector is extended by 64 bits (The length of the ECC appendage plus "end of record" byte). The data and the extra bits are read into or written from the memory of the CPU. This function is used to diagnose the operation of the ECC circuits, and can be used with the following Device Operations: M0,M1,M2,M3.

This bit is 'echoed' in ECR bit 14.

PROGRAMMING SPECIFICATION OF HP MAG. TAPE CONTROLLER

Mag. Tape device no.: 520 - 527

	IOX
READ CORE ADDRESS	520
LOAD CORE ADDRESS	521
READ STATUS	524
LOAD CONTROL	525
READ BAR (TEST)	526
LOAD WORD COUNT	527
LOAD BAR (TEST)	523

Read Status:

Bit	0	Ready interrupt enabled (cleared by the interrupt)
	1	Error interrupt enabled (cleared by the interrupt)
	2	Device active
	3	Device ready for transfer
	4	Inclusive or of error bit (6, 9, 10, 11 and 12) or if a reverse command is tried when the unit is at loadpoint.
	5	Write enable ring present
	6	LRC error
	7	EOF detected
	8	Load point (this status is remained also after the first forward command after load point is detected)
	9	EOT detected
	10	Parity error
	11	DMA error
	12	Overflow in read
	13	Density select 1 = 800 bpi, 0 = 556 or 200 bpi
	14	Mag. Tape unit ready (selected, on line and not rewinding)
	15	Bit 15 loaded by previous control word

Load Control:

Bit	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5	Address bit 16
	6	Address bit 17
	7	Read odd number of character
	8	Even parity (only to be used while writing/reading ASC II information on 7 tracks)
	9	Unit select Up to 4 units
	10	Unit select
	11	Device operation code
	12	Device operation code
	13	Device operation code
	14	Device operation code
	15	

Device Operation Code:

Bit: 14	13	12	11		
0	0	0	0	Read one record	M0
0	0	0	1	Write one record	M1
0	0	1	0	Advance to EOF	M2
0	0	1	1	Reverse to EOF	M3
0	1	0	0	Write EOF	M4
0	1	0	1	Rewind	M5
0	1	1	0	Erase gap (4 inches)	M6
0	1	1	1	Backspace one record	M7

Interrupt

The MT interrupt level is 11 and the ident number for the first MT system is 3.

HP MAG TAPE NORD-10

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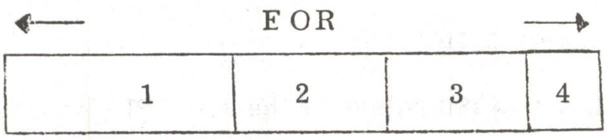
1 GAP GENERATION

1.1 EOR GAP



1- delay of 0,3" (6ms at 45 ips) after EOR gap command is issued until the signal reset command forward (RCF) is generated. This is to insure complete readback during read after write- this gap compensates for the physical distance between read and write head:

7 tracks = 0,3"
9 tracks = 0,15"

2 - stop distance = 0,19" Start/stop time = 8.33 ms at 45 ips.

3 - Start distance = 0,19"

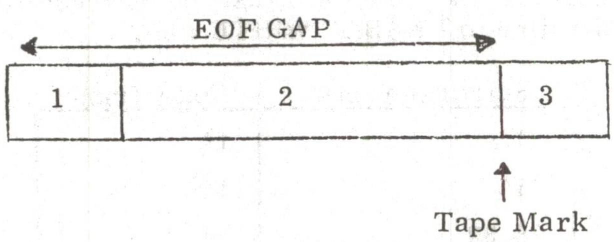
4 - delay after the tape is up to speed until it is actually written on. 9 tracks tape 0,6ms, 0,03", 7 tracks tape 1.6ms, 0,08" all at 45 ips.

Total length of EOR GAP is:

0,3 + 0,19 + 0,19 + 0.03 = 0,71" (9 tracks only)

0,3 + 0,19 + 0,19 + 0.08 = 0,76" (7 tracks or 7 and 9 tracks)

1.2 EOF GAP



1 - start distance = 0,19"

2 - delay before tape mark is written ~ 2800 pulses of the 800 BPI clock = 3,5"

3 - EOR GAP

1.3 Erase GAP

1	2	3

1 - start distance = 0,10"

2 - erase distance ~ 280 pulses of the 800 BPI clock = 3,5"

3 - stop distance = 0,19"

2 CLOCK ADJUSTMENTS

2.1 9 Tracks only

The oscillators on the 1063 card should be adjusted as follows:

The 800 BPI oscillator should be adjusted to have a period = T

$$T = \frac{1}{\text{Density x Tape Speed}}$$

Tape speed (ips)	T (us)	F (kHz)
25 option	50	20
37,5 option	33,3	30
45 standard	27,8	36

The 556 BPI oscillator is now used only to generate the delay from starting the tape until the tape is written on. This delay assures that the tape has reached full speed. The delay is measured by trigger on the CF : 55 and measureing the time to ENABLE WRITE : 54.

Tape speed ips	Start time (ms)	Delay (ms)
25 option	15	16
37,5 option	10	11
45 standard	8.33	9

2.2 9 & 7 tracks and 7 tracks only

If there is a system with a 7 tracks tape unit the 556 BPI oscillator has to be adjusted to give that density at the actual tape speed. This will automaticly gi ve a somewhat longer delay between start of tape until tape is written on.

The 800 BPI oscillator is adjusted according to previous section.

The 556 BPI oscillator should be adjusted to have a period T.

$$T = \frac{1}{\text{Density x Tape Speed}}$$

Tape speed (ips)	T (µs)	F (kHz)
25	72	13,9
37,5	48	20,85
45	40	25,02

PROGRAM SPECIFICATION FOR MAG TAPE FORMATER, TANDBERG

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1 MAG TAPE DEVICE NO.:

520 - 527

	IOX
Read Core Address	520
Load Core Address	521
Read Modus	522
Load Modus Word	523
Read Status	524
Load Control	525
In Test, Read previous loaded modus	526
Load Word Counter	527

1.1 Read Status

Bit	0-4	Standard
	4	Error inclusive or of bit 5, 6, 7, 8, 9, 11, 12
	5	Control or modus word. error. Trying to write protected tape, reversing tape at load point, tape unit not online etc. Action inhibit.
	6	Bad datablock. An error detected.
	7	End of file detected.
	8	The search character is detected.
	9	End of tape detected.
	10	Word counter not zero.
	11	DMA error.
	12	Overflow (in read) .
	13	Tape busy or formater busy.
	14	Formater busy.
	15	Interrupt when formater ready.

1.2 Read Modus Register

Bit	0	Tape online
	1	Write enable ring present
	2	Tape standing on load point
	3	CRC error / fatal error
	4	LRC error / soft error
	5-8	No. of VRC errors. If all is one, 15 or more.
	9-15	Not used, it may be one or zero.

1.3 Load Modus Word

Bit 0-8 Action code <u>or</u> bit 0-7 search word

<u>As action code:</u>

Bit	0	Density select (556 bpi)
	1	Density select (220 bpi)
	2	Reverse
	3	Write
	4	Space
	5	Filemark
	6	High speed
	7	Parity (only 7 track)
	8	Threshold

Bit 2-6 are combined to give a specific action.

	2	3	4	5	6
Write one block forward	0	1	0	0	0
Write filemark forward	0	1	0	1	0
Erase gap forward	0	1	1	0	0
Read one block forward	0	0	0	0	0
Read one block in reverse	1	0	0	0	0
Read one block in reverse (edit)	1	0	0	1	0
Space one block forward	0	0	1	0	0
Space one block in reverse	1	0	1	0	0
Search one file forward	0	0	1	1	0
Search one file in reverse	1	0	1	1	0
Search one file forward, high speed	0	0	1	1	1
Search one file in reverse, high speed	1	0	1	1	1
Search for searchword, forward	0	0	1	0	0
Search for searchword,in reverse	1	0	1	0	0
Search for searchword, forward high speed	0	0	1	0	1
Search for searchword, in reverse high speed	1	0	1	0	1

The action is initiated by loading the correct control word.

Bit	0-7	Search word
Bit	12 13 14	Unit no.
Bit	15	Odd no. of characters to be read

1.4 Load Control Word

Bit	0-6		Standard
	7-10		Not used
	12	11	
	0	0	Together with act the bit 0-8 in modus specify an action to be done
	0	1	Strobe search word into formater
	1	0	Rewind
	1	1	Rewind and unload
Bit	13-14		Should always be zero
	15		Give interrupt when the formater is ready (not waiting for the tape to be ready)

2 OPERATION

First modus is loaded, then Control Word is loaded with "act" and bit 11 and 12 zero.

<u>For search</u>:

First search word is placed in modus (with unit no.) and Control Word written.

Then an "position on block" action is executed.

Each time unit no. is changed a master clear should be given in advance.

N-10 FLOPPY DISK PROGRAMMING SPECIFICATION

1. DEVICE REGISTER ADDRESS

Codes given below are only relevant for disk system I.

Read Data Buffer

IOX 1560 (IOX RDAT)

Write Data Buffer

IOX 1561 (IOX WDAT)

Read Status Reg no. 1

IOX 1562 (IOX RSR1)

Write Control Word

IOX 1563 (IOX WCWD)

Read Status Reg no. 2

IOX 1564 (IOX RSR2)

Write Drive Address / Write Difference

IOX 1565 (IOX WDAD)

Read Test

IOX 1566 (IOX RTST)

Write Sector / Write Test Byte

IOX 1567 (IOX WSCT)

For disk System II add 10_8 to the codes specified above.

Each disk system can handle up to 3 drives.

Identcode for disk system I is 21_8

" " " " II " 22_8

Interrupt level is 11_{10}

2. INSTRUCTION FORMATS & DESCRIPTION

2.1 Read Data Buffer IOX RDAT

Reads one 16 bit word from the interface buffer.

Buffer address is automatically incremented after execution of the instruction.

2.2 Write Data Buffer IOX WDAT

Writes one 16 bit word to the interface buffer.

Buffer address is automatically incremented after execution of the instruction.

2.3 Read Status reg. No. 1 IOX RSR1

Bit 0. Not used

Bit 1. Interrupt enabled

Bit 2. Device busy

Bit 3. Device ready for transfer

Bit 4. Inclusive or of bits set in status reg. No. 2

NOTE: When bit 4 is set, an error has ocurred, and status reg No 2 must be read before proceeding.

Bit 5. Deleted Record.

This bit is set after read data command if the sector contained a Deleted Data Address Mark.

Bit 6. Read / Write Complete

A read or write operation is completed.

Bit 7. Seek Complete

The status bit is set after seek or recalibration command when the disk has finished moving the R/W head.

Bit 8. Time Out

Approx. 1,5 sek.

Bit 9, 10 & 11 are only used when formatting.

Bit 9	is active when buffer address bits 1 & 6 are active.
Bit 10	" " " " " " 1 & 7 " "
Bit 11	" " " " " " 1 & 8 " "

NOTE: Bits 4-7 are only significant after interrupt or when device busy is reset.

Bits 12-15 Not used.

2.4 Write Control Word IOX WCWD

Bit 0. Not used

Bit 1. Enable interrupt

Bit 2. Not used

Bit 3. Test Mode (for description see IOX RTST & IOX WSCT)

Bit 4. Device Clear (NB! Selected drive is deselected)

Bit 5. Clear interface buffer address

Bit 6. Enable timeout

Bit 7. Not used

The following bits are commands to the floppy disk drive, and these are the only control bits that generate device busy and give interrupt. (NB! with the exception of bit 15, Control Reset)

Bit 8. Format Track

Bit 9. Write Data

Bit 10. Write Deleted Data

Bit 11. Read ID

Bit 12. Read Data.

Bit 13. Seek

Bit 14. Recalibrate

Bit 15. Control Reset

2.5 Read Status Reg. No. 2 IOX RSR2

Bit 0-7 Not used

Bit 8. Drive not Ready

This bit is set if the addressed drive is not powered up, its door is open, the diskette is not properly installed, or drive address is invalid.

Bit 9. Write Protect

This bit is set if a write operation is attempted on a write protected diskette.

Bit 10. Not used

Bit 11. Sector Missing + No AM

This bit is set if the desired sector for a Read Data Write Data or Write Deleted Data cannot be located on the diskette.

In addition this bit may indicate a non-locatable data field address mark, or a non-locatable ID field address mark.

Bit 12. CRC Error

Bit 13. Not used

Bit 14. Data overrun

A data byte was lost in the communication between N-10 interface and the floppy disk system

Bit 15. Not used

2.6 Write Drive Address / Write Difference IOX WDAD

This is two instructions, depending on bit 0 in the A-reg.

a) Bit 0 = 1 Write Drive Address

This instruction selects Drive & Format

Bit 1-7 Not used

Bit 8-10 Drive Address (Unit. no.) 0,1 or 2

Bit 11. Deselect Drives

Bit 12-13 Not used

Bit 14-15 Format select

Bit 15	Bit 14	Format (All numbers decimal)	
0	x	IBM 3740 128 bytes/sector	26 sectors/track
1	0	IBM 3600 256 bytes/sector	15 sectors/track
1	1	IBM System 32-II 512 bytes/sector	8 sectors/track

Format Select	Format			Deselect	Drive addr. MSB	Drive addr.	Drive addr. LSB
15	14	13	12	11	10	9	8

b) Bit 0 = 0 Write Difference

This is the difference between current track and desired track. It is used as an argument for the seek command.

Bit 1- 7	Not used
Bit 8-14	Difference between current and desired track
Bit 15	Direction select
Bit 15 = 0	Access "out" to a lower track address
Bit 15 = 1	" "in" " "higher " "

IN/OUT	Diff MSB	Diff	Diff	Diff	Diff	Diff	Diff LSB
15	14	13	12	11	10	9	8

2.7 Read Test Data IOX RTST

This instruction is used for simulation of a data transfer between the floppy disk system and N-10 interface.

It does not transfer data from the N-10 interface to the A-reg, but puts one 8 bit byte into the interface buffer, each time the instruction is executed. The bytes are packed to 16 bit words in the buffer and may later be read by IOX RDAT instructions.

The byte may be chosen by using the IOX WSCT instruction. (see description of IOX WSCT.)

IOX RTST is used for test purposes only and does not generate interrupt and busy signals.

The instruction is only active when the interface is set in test mode by the following instructions:

```
SAA 10
IOX WCWD
```

To reset test mode, the following instructions must be used:

```
SAA 0
IOX WCWD     % Reset test mode bit
SAA 20
IOX WCWD     % Device clear
```

2.8 Write Sector / Write test byte IOX WSCT

When the interface is set in test mode, this instruction loads the test byte which is transferred by the IOX RTST command. If not in test mode, this instruction loads the sector no. to be used in a subsequent. Read / Write command.

a) Not in test .mode:

Bit 0-7 Not used

Bit 8-14 Sector to be used in a subsequent read/write command.

Sector range (octal) for different formats:

1-32	for	IBM 3740
1-17	for	IBM 3600
1-10	for	IBM Sys 32-II

NB! <u>0</u> must not be used.

Bit 15 Sector autoincrement

If this bit is true, the sector register is automatically incremented after each read/write command.

NOTE: This autoincrement is not valid past the last sector of a track.

Auto incr.	Sect MSB	Sect	Sect	Sect	Sect	Sect	Sect LSB
15	14	13	12	11	10	9	8

b) In test mode:

Bit 0-7 Not used

Bit 8-15 Test byte

3 PRINTERS + PLOTTERS. + 8 BIT PARALLEL 3-1-1

SPECIFICATION OF LINE PRINTER INTERFACE FOR CDC FOR NORD-10

Standard dev. no.:	0430 (0430 - 0433) oct.
No. of dev. no.:	4
Standard int. level:	10 des.
Standard ident no.:	3

Write Control Word IOX DEV NO + 3

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate device. (Print character now in buffer.)
Bit 3	Test
Bit 4	Device and interface clear
Bit 5 - 15	Not used

Read Status Word IOX DEV NO + 2

Bit 0	Interrupt enabled on ready
Bit 1	Interrupt enabled on error
Bit 2	Not used
Bit 3	Ready for transfer
Bit 4	Error, bit 5 or 6 set
Bit 5	Line printer not ready
Bit 6	Load immage request, used by a new type L.P.
Bit 7 - 10	Not used

Bit 11	Line ready. Mostly used for test of line printer
Bit 12	Illegal character in buffer
Bit 13 - 15	Not used

Write Data Word IOX DEV NO + 1

Write a data word in the buffer register. The word is transformed after the following table.

ASCII No.	ASCII 6543210	IL	C	LINEPR. 6543210	Meaning ASCII	Result (I hope)
0000-0007	0000xxx	1	1	0000000	Special character	Illegal, ignored
011	0001001	0	0	0100000	Hor. tab.	Space
012	0001010	0	1	0000001	Line feed	LF
014	0001100	0	1	0100000	Form. feed	FF
015	0001101	0	1	0000000	Carriage return	CR
10, 13, 16, 17	0001xxx	1	1	0000000	Special character	Ignored (illegal)
0020-0027	0010xxx	0	1	0110xxx	Special character	VFU channel
0030-0037	0011xxx	0	1	0010xxx	Special character	Line counter
0040-0077	01xxxxx	0	0	01xxxxx	Space - ?	Space - ?
0100-01377	10xxxxx	0	0	10xxxxx	@ -	@ - ←
0140-0177	11xxxxx	0	0	11xxxxx	Space	Reserved for 96 character sets

If CR is removed to speed up the line printer, CR will be an illegal character. An illegal character will be removed by the interface, because after an "act" the "act" will be ignored and the interface will remain ready for transfer. No special attention should be neccesary by software.

The "characters" 0140-0177 are used for line printer control.

0020 - 0027	VFU channels	
020	VFU channel 1	Top of FORM (FF)
021	VFU channel 2	Bottom for Form
022	VFU channel 3	

030 - 037	Line counter control	
030	Suppress space (CR)	0 Line feed
031	Single space (LF)	1 Line feed
032	Double space	2 Line feed

Standard for CDC line printer is 2 bits (4 channels) VFU and 2 bits (up to 3 line feeds) line counter.

Read Data Word IOX DEVN

Bit 3 is set in control word. The interface may be tested. You will read back the data transformed for the line printer. The control bit is read as bit 9. Bit 6, 7 and 8 are only read back. They are not transformed in any way.

Note

The interface is not NORD-1 compatible. The VFU channels are moved from 140 - 157 to 20 - 27 and line counter control is removed from 160 - 177 to 30 - 37.

140 - 177 are reserved for extention.

SPECIFICATION OF MATRIX PRINTER INTERFACE FOR

TALLY 1202/160 2

Standard dev. no.	:	0430 (0430-0433) oct.
No. of dev. no.	:	4
Standard int. level	:	10 des.
Standard ident no.	:	3

Write Control Word IOX DEV NO + 3

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate device. (Print character now in buffer)
Bit 3	Test
Bit 4	Device and interface clear
Bit 5 - 15	Not used

Read Status Word IOX DEV NO + 2

Bit 0	Interrupt enabled on ready
Bit 1	Interrupt enabled on error
Bit 2	Not used
Bit 3	Ready for transfer
Bit 4	Error, bit 5 or 6 set
Bit 5	Printer not ready

Read Status Word IOX DEV NO + 2 cont.

Bit 6	Printer not on-line
Bit 7	Not used
Bit 8	Not used
Bit 9	Inhibit, illegal character in buffer
Bit 10 - 15	Not used

Write Data Word IOX DEV NO + 1

Writes a character in the buffer register.

All character codes $0\text{-}37_8$ are illegal and ignored by the interface, exept following control codes:

Write Data Word IOX DEV NO + 1 cont.

11_8 : HT (Gives space in CDC controller)

12_8 : LF

14_8 : FF

15_8 : CR

Read Data Word IOX DEV NO

It is possible to read back the data written in the buffer register when running in test mode (bit 3 set in control word).

PROGRAMMING SPECIFICATION FOR THE VERSATEC MATRIX PLOTTER INTERFACED TO THE NORD-10 COMPUTER

1 The direct memory access (DMA) interface with NORD-10 computer conducts data transfer operations directly between memory and the plotter The controller, once initiated, has the capability of performing a transfer of one line or a specified number of words without any processor intervention. When using a word counter to specify the number of words, transfer of several lines may be initiated. After the controller device registers are initialized, all transfers take place under control of the controller. The processor may be notified by an interrupt when one line or the specified number of characters have been transferred to the Matrix unit.

The plotter may be used in three modes: plot mode, print mode or simultaneous print/plot.

2 IOX INSTRUCTIONS

Device number N. (Usually N=600.)

2.1 IOX N

Read Core Address

2.2 IOX N + 1

Load Core Address

2.3 IOX N + 3

Load Modus Register

2.4 IOX N + 4

Read Status Register

2.5 IOX N + 5

Load Control Register

2.6 IOX N + 7

Load Word Counter

3 CONTROL REGISTER

Bit	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5	Address bit 16
	6	Address bit 17
	7	Remote Reset
	8	Remote Form Feed
	9	Remote end of Transmission
	10	Remote Line terminate
	11 - 15	Unused

4 STATUS REGISTER

Bit	0	Ready for transfer, interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors (6 + 7)
	5	Not used
	6	No Paper
	7	Plotter not ONLINE
	13	Plotter ready
	8-12, 14-15	Unused, some bits may be set to one when the status register is read.

5 MODE REGISTER

Bit	0	0=PLOT 1=PRINT
	1	Simultaneous Plot/Print
	2	Disable data to plotter
	3	Termination modus

0: Transfer terminated when print cycle is started (buffer full or control character received in print mode).

1: Transf er terminated when the specified number of words are transferred i.e. the word counter is decremented to zero.

6 DATA FORMAT

Print and plot data is transferred in word mode (two bytes) between memory and the controller, and byte mode between the controller and Matrix. The controller has a sixteen bit (two byte) buffer for temporary storage of the data.

15 — 8	7 — 0	
First data byte	Second data byte	1 word
3 data byte	4 data byte	2 word

7 PRINTING

The print input accepts ASCII.

7 or 8 level code (data bit 8 is not used).

The character generator in the Matrix printer contains a read only memory (ROM) in which there are stored 64 or 96 characters. Up to 80 characters may be stored in the print buffer for 8 - 1/2" machines, or 132 characters for 11" machines.

When the buffer is full (1 line of characters) or a control character is received (Figure 7.2), the line is printed automatically.

If bit 4 in mode register is zero the transfer is now terminated, if bit 4 is one the transfer is continued untill the word counter is decremented to zero.

After a transfer one of the "Remote Control Signals" (Figure 7.1) may be used.

Signal	Operation
Clear	a) Clears Buffer when Matrix is in Data Entry
Remote Reset (RESET)	a) Clears Buffer and initializes all logic.
Remote Line Terminate (RLT)	a) Forces Write Cycle b) If in plot mode first RLT after full buffer is ignored.
Remote Form Feed (RFEED)	a) Forces Write Cycle b) With Fan-Fold Operation causes paper to advance to top of next page. c) With Roll operation causes paper to advance approximately 2.5 inches.
Remote End of Transmission (REOTR)	a) Forces Write Cycle b) With Fan Fold Operation causes paper to advance 8 inches, then to top of next page. c) With Roll Operation causes paper to advance approximately 8 inches.

Figure 7.1 Remote Control Signals

Control Signal Name	ASCII Code (Octal)	Operation
EOT (End of Transmission)	004	Causes print cycle and paper advance of 8 inches, then stop if in roll mode, or continue advance to top of next page if in fanfold mode. Do not use if in SPP mode.
FF (Form Feed)	014	Causes print cycle and paper advance of 2 - 1/2 inches if in roll mode, or advance to top of next page if in fal-fold mode. Do not use if in SPP mode.
LF (Line Feed)	012	Causes print cycle and paper advance of one line except when: a) Follows printing a full buffer b) Follows a Carriage Return.
CR (Carriage Return)	015	Causes print cycle and paper advance of one line, only if buffer has at least one character entered, but is not full (80 or 132).

Figure 7.2

8 PLOT OPERATIONS

Data consists of 8 bit, binary, unweighted bytes. A complete raster scan (a single plotted line) consists of 70 8-bit bytes, totaling 560 bits for 8 1/2" machined, or 128 8-bit bytes, totaling 1.024 bits on 11" machines.

Each dot corresponds to a single bit in the buffer. If a bit is "1" a black dot is plotted at the point corresponding to the bit position in the buffer.

When the last byte is stored in the plotter buffer a single scan is automatically generated and one row of data points is plotted. A space equal to the horizontal resolution is generated and the Matrix unit is then ready to receive another scan row of plot data.

When mode bit 4 is zero the transfer is terminated when one line is transferred from the buffer in core to the plotter buffer.

If mode bit 4 is set to one, the transfer is terminated when the word counter is decremented to zero.

After a transfer one of the "Remote Control Signals" may be used to empty the plotter buffer (if not full line).

9 SIMULTANEOUS PRINT/PLOT (SPP) OPERATIONS

Simultaneous Print/Plot (SPP) operation is provided to permit direct overlaying of character data generated by the internal Matrix character generator, with plotting data generated on a dot basis. This is an optional feature on Matrix printer/plotters.

Normal operation consists of first filling the print buffer (Mode 3). If the buffer is not filled, the line must be terminated by a CR code. MODE is changed to MODE 2 and unweighted binary plot data is now loaded into the plot buffer until the plot buffer is full (one line) and signle scan is generated. Note that the writing process is controlled by the plot buffer.

During the scanning process the print buffer is likewise scanned. The corresponding dot(s) of each character are OR'D with the plot buffer output thus overlaying the printed and plotted data.

A printed character for 8 1/2" Matrix units consists of 8 scans when using a 64 character set, and 10 scans when using a 96 character set. Likewise, a printed character for 11" Matrix unit consists of 10 scans when using a 64 character set or 12 scans when using a 96 character set. New data may be entered into the print buffer after the last scan of the previous line of characters is completed.

10 CORE ADDRESS

When a transfer is terminated the core address register points to the next memory address.

If the transfer is terminated by a control character (Mode 4=0) one word more than given to the plotter, is read from the memory.

SPECIFICATIONS FOR BUFFERED CALCOMP PLOTTER INTERFACE, 500 SERIE

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Plotter commands are not compatible with old (not buffered) 500 serie interface, but compatible with 900 serie interface.

Interface with 256 x 4 bits "first in first out" (FIFO) buffer.

Standard device:	440 (440 - 443) octal
Number of device number:	4
Standard interrupt level:	10 des.
Standard ident number:	11

Write Control Word

Bit	0	Enable interrupt on buffer empty
Bit	1	Not used
Bit	2	Activate device
Bit	3	Not used
Bit	4	Clear interface
Bit	5-15	Not used

Read Status

IOX DEV. NO. + 2

Bit	0	Interrupt enabled
Bit	1-2	Not used
Bit	3	Ready for transfer, buffer empty
Bit	4	Not used
Bit	6	Interface buffer ready to receive data (FIFO ready for input)
Bit	7	Data ready on output of buffer (output ready from FIFO)
Bit	8	Plotter busy (not ready)

Write Data Word

IOX DEV. NO. + 1

AC Bits (0-3) is written into the FIFO buffer register.
Status bit 6 has to be one.

Read Data Word (for test only)

IOX DEV. NO.

Output register is read into AC bit 0-3.

Signal name	CPU BUS Signal	GND	Burndy Signal	GND	Plotter Signal	GND
Carriage Right	95	94	A	C	8	15
Carriage Left	93	92	B	D	7	15
Drum Down	91	90	E	H	6	15
Drum Up	89	88	F	J	5	15
Pen down	87	86	K	M	12	15
Pen Up	85	84	L	N	11	15

Input Format Commands

Hex Code	Binary				Command
	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	+Y
1	0	0	0	1	+Y, +X
2	0	0	1	0	+X
3	0	0	1	1	-Y, +X
4	0	1	0	0	-Y
5	0	1	0	1	-Y, -X
6	0	1	1	0	-X
7	0	1	1	1	+Y, -X
8	1	0	0	0	Enter Special Function Mode
9	1	0	0	1	Pen Up
A	1	0	1	0	Pen Down
B	1	0	1	1	No Operation
C	1	1	0	0	Not Used
D	1	1	0	1	Not Used
E	1	1	1	0	Leave Special Function Mode
F	1	1	1	1	Not Used
8	1	0	0	0	Select PEN 1
9	1	0	0	1	
E	1	1	1	0	
8	1	0	0	0	Select PEN 2
9	1	0	0	1	
9	1	0	0	1	
E	1	1	1	0	
8	1	0	0	0	Select PEN 3
9	1	0	0	1	
9	1	0	0	1	
9	1	0	0	1	
E	1	1	1	0	

PROGRAMMING SPECIFICATION FOR THE CALCOMP PLOTTER, NORD-10

+++
+

Standard device:	440 (440 - 443) octal
Number of device number:	4
Standard interrupt level:	10 des.
Standard ident number:	11

Write Control Word

IOX DEV. NO. + 3

Bit	0	Enable interrupt
Bit	1	Not used
Bit	2	Activate device
Bit	3	Not used
Bit	4	Clear interface
Bit	5 - 15	Not used

Read Status

IOX DEV. NO. + 2

Bit	0	Interrupt enabled
Bit	1-2	Not used
Bit	3	Ready for transfer
Bit	4	Error bit. POWER off or manual
Bit	5-15	Not used

Write Data Word

IOX DEV. NO. + 1

AC Bits (0-3) is written into the interface buffer register.

Read Data Word (for test only)

IOX DEV. NO.

The buffer register is read into AC (0-3).

Input Format Commands

Hex Code	Binary				Command
	Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	0	+Y
1	0	0	0	1	+Y, +X
2	0	0	1	0	+X
3	0	0	1	1	-Y, +X
4	0	1	0	0	-Y
5	0	1	0	1	-Y, -X
6	0	1	1	0	-X
7	0	1	1	1	+Y, -X
8	1	0	0	0	Enter Special Function Mode
9	1	0	0	1	Pen Up
A	1	0	1	0	Pen Down
B	1	0	1	1	No Operation
C	1	1	0	0	Not Used
D	1	1	0	1	Not Used
E	1	1	1	0	Leave Special Function Mode
F	1	1	1	1	Not Used
8	1	0	0	0	Select PEN 1
9	1	0	0	1	
E	1	1	1	0	
8	1	0	0	0	Select PEN 2
9	1	0	0	1	
9	1	0	0	1	
E	1	1	1	0	
8	1	0	0	0	Select PEN 3
9	1	0	0	1	
9	1	0	0	1	
9	1	0	0	1	
E	1	1	1	0	

SPECIFICATIONS FOR

CALCOMP 565 INTERFACE

....oo0oo....

REGISTER NUMBERS:

Read Data	(DR)	- 440
Load Data	(DW)	- 441
Read Status	(RS)	- 442
Load Control Word	(CW)	- 443

Interrupt level: 10_{10}
Identification code: 11_8

FUNCTIONS:

Function	Data word Bits 3 2 1 0
Carriage Right	x x 1 1
Carriage Left	x x 1 0
Drum Down	1 0 x x
Drum Up	1 1 x x
Pen Down	0 1 0 1
Pen Up	0 1 0 0

NOTE: x means: don't care.

CONTROL WORD FORMAT:

Bit 0 - Enable interrupt on ready for xfere
Bit 1 - NA
Bit 2 - Activate
Bit 3 - NA
Bit 4 - Programmed MASTER CLEAR

STATUS REGISTER FORMAT:

Bit 0 - Interrupt Enabled
Bit 1 - NA
Bit 2 - NA
Bit 3 - Ready for xfere

CALCOMP 565 PLOTTER CABLE

Signal name	CPU BUS Signal	CPU BUS GND	Burndy Signal	Burndy GND	Plotter Signal	Plotter GND
Carriage Right	95	94	A	C	8	15
Carriage Left	93	92	B	D	7	15
Drum Down	91	90	E	H	6	15
Drum Up	89	88	F	J	5	15
Pen Down	87	86	K	M	12	15
Pen Up	85	84	L	N	11	15

NOTE: Cable is NOT N1 compatible.

PROGRAMMING EXAMPLES:

To perform a Pen Down:

```
START, SAA  5
       IOX <DW>               % Load 5
       SAA  4
       IOX <CW>               % Activate, i.e., Pen Down
       IOX <RS>.              % Read Status
       BSKP ONE 30 DA         % Bit 3 = 1?
       JMP  *-2               % Loop until bit 3 = 1
       CONTINUE               % Finished, i.e., Pen is down.
```

To write a line making a 45^{o} angle with the horizontal axis:

```
START, SAA  17                % Carriage Right and
                                Drum Up
       IOX <DW>               % Load Data write register
       SAA  4
       IOX <CW>               % Activate - one increment
                                on Carriage Right and
                                Drum Up
       IOX <RS>               % Read Status
       BSKP ONE 30 DA         % Increment finished?
       JMP  *-2               % Loop until finished
       CONTINUE               % Finished (Jump to START+2)
```

....oo0oo....

SPECIFICATION OF LINE PRINTER INTERFACE FOR CDC 9380 FOR NORD-10

Standard dev. no.	:	0430 (0430-0433) oct.
No. of dev. no.	:	4
Standard int. level	:	10 des.
Standard ident no.	:	3

Write Control Word IOX DEV NO + 3

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate device. (Print character now in buffer)
Bit 3	Test
Bit 4	Device and interface clear
Bit 5 - 15	Not used

Read Status Word IOX DEV NO + 2

Bit 0	Interrupt enabled on ready
Bit 1	Interrupt enabled on error
Bit 2	Not used
Bit 3	Ready for transfer
Bit 4	Error, bit 5 or 6 set
Bit 5	Line printer not ready

Read Status Word IOX DEV NO + 2 cont.

Bit 6	Out of paper
Bit 7	Compressed pitch
Bit 8	LP9 is on, to indicate to the controller that data on the lines is format information and is interpreted as control code
Bit 9	Inhibit, illegal character in buffer
Bit 10	Not used
Bit 11 Bit 12	Band detect

Bit 11	Bit 12	Type of band
0	0	128 characters
1	0	96 " "
0	1	64 " "
1	1	48 " "

Note! This interface is only handling 64, 96 character printers.

Bit 13 - 15	Not used

Write Data Word IOX DEV NO + 1

Writes a character in the buffer register.

All character codes $0\text{-}37_8$ are illegal and ignored by the interface, except following control codes:

Write Data Word IOX DEV NO + 1 cont.

11_8 : HT (Gives space in CDC controller)

12_8 : LF

14_8 : FF

15_8 : CR

20_8 - 33_8 VFU channels give LP9 and disable LP5

20_8 VFU channel 1 (FF)

21_8 VFU channel 2

⋮

33_8 VFU channel 12

Read Data Word IOX DEV NO

It is possible to read back the data written in the buffer register when running in test mode (bit 3 set in control word).

1 INTRODUCTION

Parallell Byte Cutput, ND-653, is a universal 8 bit interface. It has several selectable hardware options which allow direct connection of the following devices:

1. Versatec Matrix Printer/Plotter
2. Data Products Line Printer
3. Centronics Line Printers
4. Logabax Matrix Printer
5. CDC Matrix Printer
6. Qume Printers
7. Facit Tape Punch

The interface contains, Punch Interface, ND-352, as a subset. This subset is program and plug compatible with ND-352.

However, there is a minor difference in the definition of statusbit 2, ACTIVE.

In ND-352 ACTIVE is turned off when the peripheral becomes READY. ACTIVE is inverse of RFT.

In ND-653 ACTIVE is turned off when data are accepted by peripheral (READY disappears). Hence the interface may be neither ACTIVE nor RFT. It is idle waiting for the device.

See fig. 1.1

8 BIT PARALLEL

Output Interface

ND-653

November 1976

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4 INTERFACE SPECIFICATIONS

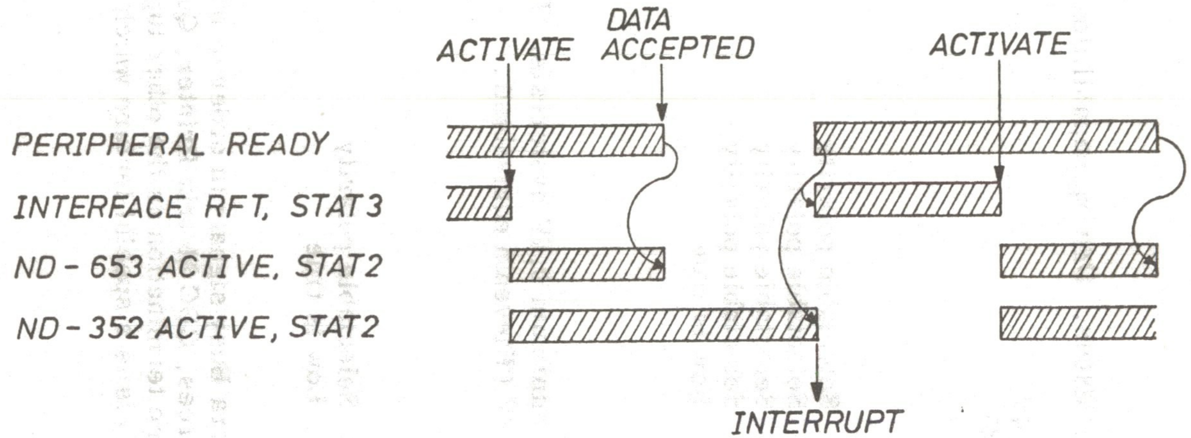


Fig. 1.1. Difference in ACTIVE in ND-653 and ND-352.
Note important difference between RFT and PERIPHERAL READY
(In Non-handshake mode ACTIVE is fixed = 10μs)

2 HARDWARE SPECIFICATIONS

2.1 Output Signals

Driving gates are DM8097 and DM8098. Driving capabilities are:

Source current:	5.2mA @ 2,4V
Sink current:	32mA @ 0,4V

2.1.1 The output signals are:

8 Data bits	Selectable polarity
1 Data strobe pulse	Selectable polarity
3 Function pulses	Selectable polarity
1 Initialize pulse, 80-150µs	Selectable polarity
2 Mode static levels	Low is true

2.2 Input Signals

Receive gates are SN7414 with minimum 0,4V hysteresis. The lines are terminated in 300Ω tied to +2,8V (Thevenin equivalent).

2.2.1 The input signals are:

1 Device Ready, level or pulse	Selectable polarity
1 Status level	Low is true

2.2.2 It is possible to apply three extra Busy signals in order to interface Devices with several Busy sources, CDC Matrix Printer, Qume Printer etc. Inputs are 74153 with same termination as the other inputs. Polarity is inverse of Device Ready. This is a special feature which is not concidered to be standard.

2.3 External Connection

15 output and 5 input signals are available to user on a 42 pins Burndy Plug. Data, Ready and Strobe signals are located on the same terminals as on Punch Interface Plug.

2.4 Data Channel Operation

The interface is prepared to be connected to a DMA controller which has word counter and the necessary logic to communicate with the channel.

2.5 Timing Specifications

2.5.1 Peripheral Requirements:

Time from INIT to RDY is removed	(Fig. 6 1.2)	t_1 : <80 µs
Deadtime after INIT	(Fig. 6.1.2 - 6.1.3)	t_2: 0 → ∞
Width of peripheral RDY	(Fig. 6.1.3 - 6.2.2)	t_3: >0.6 µs
Width of peripheral not RDY	(Fig. 6.2.1)	t_5 : >0.6 µs
Time from STRobe to not RDY	(Fig. 6.2.1)	t_4 : - T_1 → ∞

2.5.2 Interface Characteristics:

Time from peripheral RDY to STRobe	(Fig. 6.2.1 - 6.2.2),	T_1 : > 13 µs
Time from "Data Valid" to STRobe	(Fig. 6.2.1 - 6.2.2),	T_2 : > 3,5 µs
Width of STRobe in Handshake mode	(Fig. 6.2.1)	T3: 0,6 + t_4 + 1 µs
Width of STRobe in Non-Handshake mode	(Fig. 6.2.2),	T3: 8 → 12 µs

3 PROGRAMMING SPECIFICATIONS

3.1 Device Number

Device number, DN, is selectable by switches on card and may be set to any address divisible by 4. The interface uses the 4 numbers: DN, ... DN+3.

3.2 Interrupt Level

Interrupt level = 10_{10}. Interrupt occurs if status bit 0 and status bit 3 = 1.

3.3 Ident Code

Ident code may be set by switches to any number from 0 to 255.

3.4 Read Data Word = IOX DN

The data word which is sent to the device, may at any time be read back to A-register (not only in test mode as for Punch Interface).

Data is read in the same polarity as it is sent to the device. Hence the polarity is:

Same as previously loaded data if status bit 12 = 0.
Inverse of previously loaded data if status bit 12 = 1.

3.5 Write Data Word = IOX DN + 1

The 8 lower bits of A-register is loaded into the output buffer register.

3.6 Read Status Word = IOX DN + 2

Bit 0 Interrupt enabled

Set bit: Control word bit 0 = 1

Clear bit: Control word bit 0 = 0
Serviced IDENT PL10
Master clear

Bit 1 Not used

Bit 2 Active

The interface is considered active as long as the function pulses lasts (see control bits 8-9). The bit has not same meaning as for punch (where it is inverse of READY) and should only be used for test purposes. See Fig. 1.1.

Note that the polarity of bit 2 is inverted if status bits $(8+9)\cdot 11$ or $(8+9)\cdot 14$ is true.

Bit 3 Device Ready for transfer

Set bit: Ready level or Acknowledge pulse from device

Clear bit: Control word bit 2 = 1
Control word bit 4 = 1
Master clear

Bit 4 Not used

Bit 5 Status

This bit may be attached to selected features of the device.

Set bit: STS signal is low

Clear bit: STS signal is high

Bit 6-9 Mode and Function

Follow the same bits previously loaded by control word. Read for test purposes.

Bit 10 Non-handshake selected

Set bit: Control word bit 10 = 1
Select switch 1 = ON

Clear bit: Control word bit 10 = 0
Select switch 1 = OFF

Bit 11 -15 are set and cleared equivalent to this.

Bit 11 Strobe in 0-polarity selected

Bit 12 Data in 0-polarity selected

Bit 13 Ready in 0-polarity selected

Bit 14 Function 1-3 in 0-polarity selected

Bit 15 Initialize in 1-polarity selected

3.7 Write Control Word = IOX DN + 3

Bit 0 Enable Interrupt when Ready for transfer

Bit 1 Not used

Bit 2 Activate Function according to one of the 4 functions defined by control bit 8-9. Activate will always cause "Ready" to disappear for a while. Typical functions are Strobe Data, Advance to Top of Form, Print Buffer etc.

Note that Activate is a "Masked set"-bit, which means,
1 = Set bit
0 = Do nothing

Bit 3 Set Interface in Test Mode. Will cause Ready for Transfer to be set within 100 μs. See also Fig. 6.3.

Bit 4 Device Clear

This bit has the same effect as Master Clear and causes the following action:

A Clear Interrupt Enable

B Clear Data Register

C Clear Control bits 3, 6-15

D Clear Active

E Clear Ready for Transfer for minimum 100 μs

F Issue a 100 μs Initialize pulse to Device.

It is not necessary to output a dummy character in order to set the interface Ready for Transfer after initialize.

Bit 5 Not used

Bit 6 Mode A

Bit 7 Mode B

These two bits are stored and sent directly to device where they control selected features. They cause no action in the interface.

Example of use: Set in Plot mode, select Red Ribbon, Run Backwards etc.

Bit 8-9 Function

These two bits are decoded to 4 different functions. A function is defined as some action which remove the Ready signal from device. If a function is tried which the device does not respond to, the interface will lock up in an active state infinitely.

Setting of the function bits does not produce any function signals unless also the Activate-bit is set.

It is not legal to change function while interface is active.

Function = 00 is "Strobe Data", and is programmed by setting the Activate-bit only.

Bit 10-15 These bits allow programming of the interface's hardware features. They are normally set by the 6 select switches on card and define the intersection between computer and device.

This program facility is meant for test and maintenance only. Drivers from Norsk Data-Elektronikk will assume that the selection is done by switches.

When program controlled all switches must be put in off position. The meaning of the individual bits are:

Bit 10 = 1	Select Non-Handshake mode
Bit 11 = 1	Select Strobe in 0-polarity
Bit 12 = 1	Select Data in 0-polarity
Bit 13 = 1	Select Ready in 0-polarity
Bit 14 = 1	Select Function 1-3 in 0-polarity
Bit 15 = 1	Select Initialize in 1-polarity

4.1 Specification for Versatec Matrix Printer/Plotter

Bit	CONTROL		SWITCH	STATUS
0	Enable Interrupt			Interrupt Enabled
1	-			-
2	Activate Function			Function Active
3	Test Mode			Ready for Transfer
4	Clear (Initialize)			-
5	-			Status: ON LINE
6	Mode A: PLOT			Same as control
7	Mode B: SIM.PRINT/PLOT			Same as control
8-9	00: STROBE DATA			Same as control
	01: LINE TERMIN			Same as control
	10: END OF TRANS			Same as control
	11: FORM FEED			Same as control
10	Handshake	: YES	1: OFF	0
11	Strobe pol	: 1	2: OFF	0
12	Data pol	: 1	3: OFF	0
13	Ready pol	: 0	4: ON	1
14	Function 1-3 pol	: 0	5: ON	1
15	Initialize pol	: 0	6: OFF	0
	Extra Busy	: NO	7: OFF	

4.1.1 Description of Versatec Printer/Plotter

Three modes of operation are possible, Print, Plot and Simultanous Print/Plot. Although all Matrix units are not prepared for all modes, the general case is assumed.

The Matrix unit contains one buffer for printing one line of ASCII characters and another buffer for plotting one row of single points. Both buffers are filled from the interface data register at "Activate Function 00". Which of the buffers that shall receive the data is determinted by control bit 6 thus, 0 = print, 1 = plot. This is true whether the unit is in Simultanous Print/Plot mode or not.

To put the buffer contents down to paper a command must be given. Commands differ in the different modes and are stated below.

4.1.2 MODE A = 0, MODE B = 0 : PRINT ONLY

Data format is 7 bit ASCII without parity. (The 8th bit is ignored.) The character codes accepted are:

$40_8 - 137_8$ (64 character set)

or

$40_8 - 177_8$ (96 character set)

Several Models, each with several options are available. Below is described type 1110A with a buffer length of 132 characters and options, Simultanous Print/Plot and 96 Character Set.

Each line of text is built up by 12 rows of single dots (10 for 64 character set) and each character occupies 8 vertical columns. The 8th is always blank and the 7th is often blank. Hence the space between two characters is 1-2 dots wide.

In addition to filling the buffers two operations are possible, print content and/or advance paper. This is either performed automatically or due to ASCII control codes.*

Since the buffer is cleared after printing it is not possible to repeat the same line without refilling the buffer.

Printing is caused by:

	ADVANCE	CONDITIONS
FB (Full Buffer)	ONE LINE	
EOT (ASCII 004)	8 INCHES 8 INCHES, THEN GO TO TOP OF FORM	If roll paper is used If fan-fold paper is used
FF (ASCII 014)	2 1/2 INCHES TO TOP OF FORM	If roll paper is used If fan-fold paper is used
LF (ASCII 012)	ONE LINE	No operation after Printing caused by FB or CR
CR (ASCII 015)	ONE LINE	No operation after FB, LF, CR or DEVICE CLEAR

Advance to top of form is also caused automatically by "Full Page", when fan-fold paper is used. (Prevents printing on perforation folds.)

The conditions on LF and CR are very useful since they make the Matrix printer software compatible with traditional non-buffering printers.

The following commands all print contents of buffer and advance <u>one</u> line.

FB,
LF,
CR,
FB - LF - CR,
CR - LF,
LF - CR.

---

* Functions 1-3 are also legal, but not necessary in this mode, unless a 128 character set is used.

Observe the different conditions on LF and CR:

LF - LF = Print and advance <u>two</u> lines

whil e

CR - CR = Print and advance <u>one</u> line

4.1.3 MODE A = 1, MODE B = 0 : PLOT ONLY

Plot data are 8 bit bytes placed in succession in a 128 byte buffer. Each point in the row to be plotted corresponds to a bit position in the buffer. The MSB of byte 1 is the leftmost point and LSB of byte 128 is the rightmost.

1. BYTE								2. BYTE			128. BYTE	
7	6	5	4	3	2	1	0	7	6	-----	1	0

1 - 2 - 3 - 4 - 5 - 6 - 7 - 8 - 9 - 10   1023-1024

If a bit is "1" the corresponding point will have a black dot plotted.

In plot mode, operations are either automatic or caused by "Activate functions 1-3" of control word. They cause the buffered row to be plotted and advance paper as shown below:

	ADVANCE	CONDITION
FB (Full Buffer)	ONE ROW	
REOT (Function 2)	8 INCHES 8 INCHES , THEN GO TO TOP OF FORM	If roll paper is used If fan-fold paper is used
RFF (Function 3)	2 1/2 INCHES TO TOP OF FORM	If roll paper is used If fan-fold paper is used
RLT (Function 1)	ONE ROW	No operation after FB

One ROW is the minimum paper increment possible and hence equal to the vertical resolution (horisontal and vertical resolutions are equal).

4.1.4 MODE A = 0 or 1, MODE B = 1 : SIMULTANOUS PRINT/PLOT

This mode is provided to permit overlaying of ASCII text on dot plots. Another possibility is to generate user-defined symbols in a standard ASCII text string.

The normal operating sequence is:

a) Set mode to 10_2, and the data following will be set in the print buffer.

b) If the buffer is filled it will terminate automatically, else use CR. The text is not printed yet.

c) The Matrix unit should now be set to mode 11_2 (don't wait for "Ready for transfer").

d) Output the first row to be plotted to plot buffer, similiar to the "plot-only" mode.

e) The first row will be printed on paper when plot-buffer is full or RLT is programmed.

The dots put on paper will be an OR'ing of the plot data and the upper row in the character buffer.

f) The next line to be plotted is then put into plot-buffer. This line will be OR'ed together with the second row in the character buffer and printed.

The 10_{10} row in the character line is normally blank. The exeptions are the characters g, j, p, q and y which go down to the 12th row.

Until the last row is plotted the character buffer must not be reloaded. In SPP mode no automatic line space is generated. Hence each row constituting the vertical space between lines of text must be put out by program.
Note! The first two characters will fall outside (to the left) of the plot area. Hence the character buffer must start with two spaces to make the first real character coincide with the start of the plot-buffer content. (May differ on other models.)

Format information is found in section 6.2 Optional Accessories of Versatec Manual.

Also observe that the SPP mode is essentially a plot mode where mode 01_2 is identical to 11_2 if the print buffer is empty. In mode 10_2 only the commands CR and LF are legal.

4.2 Specification for Data Products Line Printer

		CONTROL		SWITCH	STATUS
Bit	0	Enable Interrupt			Interrupt Enabled
	1	-			-
	2	Activate Function			Function Active
	3	Test Mode			Ready for Transfer
	4	Clear (Initialize)			-
	5	-			Status: OFF LINE
	6	Mode A: -			Same as control
	7	Mode B: -			Same as control
	8-9	00: STROBE DATA			Same as control
		01: -			Same as control
		10: -			Same as control
		11: -			Same as control
	10	Handshake	: YES	1: OFF	0
	11	Strobe pol	: 1	2: OFF	0
	12	Data pol	: 1	3: OFF	0
	13	Ready pol	: 1	4: OFF	0
	14	Function 1-3 pol	: 1	5: OFF	0
	15	Initialize pol	: 0	6: OFF	0
		Extra Busy	: NO	7: OFF	

4.3 Specification for Centronics Line Printers

		CONTROL		SWITCH	STATUS
Bit	0	Enable Interrupt			Interrupt Enabled
	1	-			-
	2	Activate Function			Function Active
	3	Test Mode			Ready for Transfer
	4	Clear (Initialize)			-
	5	-			Status: FAULT
	6	Mode A: -			Same as control
	7	Mode B: -			Same as control
	8-9	00: STROBE DATA			Same as control
		01: -			Same as control
		10: -			Same as control
		11: -			Same as control
	10	Handshake	: NO	1: ON	1
	11	Strobe pol	: 0	2: ON	1
	12	Data pol	: 1	3: OFF	0
	13	Ready pol	: 0	4: ON	1
	14	Function 1-3 pol	: 1	5: OFF	0
	15	Initialize pol	: 0	6: OFF	0
		Extra Busy	: NO	7: OFF	

4.4 Specification for Logabax Matrix Printer

		CONTROL		SWITCH	STATUS
Bit	0	Enable Interrupt			Interrupt Enabled
	1	-			-
	2	Activate Function			Function Active
	3	Test Mode			Ready for Transfer
	4	Clear (Initialize)			-
	5	-			Status: -
	6	Mode A: -			Same as control
	7	Mode B: -			Same as control
	8-9	00: STROBE DATA			Same as control
		01: -			Same as control
		10: -			Same as control
		11: -			Same as control
	10	Handshake	: YES	1: OFF	0
	11	Strobe pol	: 0	2: ON	1
	12	Data pol	: 0	3: ON	1
	13	Ready pol	: 1	4: OFF	0
	14	Function 1-3 pol	: 1	5: OFF	0
	15	Initialize pol	: 0	6: OFF	0
		Extra Busy	: NO	7: OFF	

4.5 Specification for CDC Matrix Printer

		CONTROL			STATUS
Bit	0	Enable Interrupt			Interrupt Enabled
	1	-			-
	2	Activate Function			Function Active
	3	Test Mode			Ready for Transfer
	4	Clear (Initialize)			-
	5	-			Status: ON-LINE
	6	Mode A: -			Same as control
	7	Mode B: -			Same as control
	8-9	00: STROBE DATA			Same as control
		01: -			Same as control
		10: -			Same as control
		11: -			Same as control
				SWITCH	
	10	Handshake	: NO	1: ON	1
	11	Strobe pol	: 0	2: ON	1
	12	Data pol	: 0	3: ON	1
	13	Ready pol	: 1	4: OFF	0
	14	Function 1-3 pol	: 1	5: OFF	0
	15	Initialize pol	: 0	6: OFF	0
		Extra Busy	: YES	7: ON	

4.6 Specification for Qume Printers

		CONTROL			STATUS
Bit	0	Enable Interrupt			Interrupt Enabled
	1	-			-
	2	Activate Function			Function Active
	3	Test Mode			Ready for Transfer
	4	Clear (Initialize)			-
	5	-			Status: ERROR
	6	Mode A: LONG			Same as control
	7	Mode B: SIGN			Same as control
	8-9	00: STROBE DATA			Same as control
		01: MOVE CARRIAGE			Same as control
		10: FEED PAPER			Same as control
		11: FORM FEED			Same as control
				SWITCH	
	10	Handshake	: YES	1: OFF	0
	11	Strobe pol	: 0	2: ON	1
	12	Data pol	: 0	3: ON	1
	13	Ready pol	: 1	4: OFF	0
	14	Function 1-3 pol	: 0	5: ON	1
	15	Initialize pol	: 0	6: OFF	0
		Extra Busy	: YES	7: ON	

4.6.1 Description of Qume Printer

The printer is operated at a lower hardware level than normal. This implies that all carriage and paper movements must be programmed with magnitude and sign.

On the other hand this gives great freedom in positioning of the characters which makes it suitable as a slow plotter.

Functions:

00 Print the 7 bits ASCII character previously loaded in data register. The printwheel contains small as well as capital letters.

The following ASCII codes are ignored:

Commands	: $0\text{-}37_8$
Space	: 40_8
Rubout	: 177_8

01 Move carriage according to the 8 bit magnitude in data register. Move 1400 units extra if Long mode (control bit 6) is set.

The motion is right if Sign = 0 (control bit 7), left if Sign = 1.

Unit step,	1 =	0,42mm
Maximum step,	377_8 =	107,4mm
Long step (control bit 6),	1400_8 =	325,1mm
Paper width,	1434_8 =	337,0mm
Standard space,	6_8 =	2,5mm

For the standard character spacing of 10 characters/inch the space width will be 6 units. Hence there is room for 132_{10} characters per line.

The maximum movement at CARRIAGE RETURN is paper width 1434_8. To manage this, a number greater than 34 must be loaded in data register before execution of the control word 704 which means, "Activate-long-left-carriage-motion". See also table below.

10 Feed paper according to the 8 bit magnitude in data register. Move 1400_8 units extra if Long mode (control bit 6) is set.

Feed forward if Sign = 0 (control bit 7), backward if Sign = 1.

Unit feed,	1 =	0,53mm
Maximum feed,	377_8 =	134,4mm
Long feed,	1400_8 =	404,8mm
Standard linefeed,	10_8 =	4,2mm

For the standard line spacing of 6 lines/inch the paper feed is 10 units.

Summary:

Control bits 9 8 7 6		Function		Data
0 0 x x	■	Print character		41-176
0 1 0 0	■	Move carriage	Right	6 (space)
0 1 0 1		Move carriage Long	Right	
0 1 1 0		Move carriage	Left	
0 1 1 1	■	Move carriage Long	Left	34 (carr. return)
1 0 0 0	■	Feed paper	Forward	10 (line feed)
1 0 0 1		Feed paper Long	Forward	
1 0 1 0		Feed paper	Backward	
1 0 1 1		Feed paper Long	Backward	
1 1 x x	■	Form feed		

At normal character printing only the functions marked ■ are used.

The assosiated value which must be placed in data register is shown at right.

Remember that all characters must be followed by "Move carriage 6 units" i. e. space before the next is written.

4.6.2 Features which are not implemented

A. Programmable ribbon colour

B. Programmable ribbon advancement

C. Programmable Paper Bail lift

D. Paper empty detection

E. Split paper with independent motion

F. Databit -1 is unused (affects carri ge motion only)

4.6.3 Features which are modified

A. Controlbit 6, LONG = databit 8,9

B. Controlbit 7, SIGN = databit 10

4.7 Specification for Facit 4070 Punch

		CONTROL				STATUS
Bit	0	Enable Interrupt				Interrupt Enabled
	1	-				-
	2	Activate Function				Function Active
	3	Test Mode				Ready for Transfer
	4	Clear (Initialize)				-
	5	-				Status: -
	6	Mode A: -				Same as control
	7	Mode B: -				Same as control
	8-9	00: STROBE DATA				Same as control
		01: -				Same as control
		10: -				Same as control
		11: -				Same as control
				SWITCH		
	10	Handshake	: YES	1:	OFF	0
	11	Strobe pol	: 1	2:	OFF	0
	12	Data pol	: 1	3:	OFF	0
	13	Ready pol	: 1	4:	OFF	0
	14	Function 1-3 pol	: 1	5:	OFF	0
	15	Initialize pol	: 0	6:	OFF	0
		Extra Busy	: NO	7:	OFF	

5. BLOCK DIAGRAMS

5.1 I/O-Bus Communication

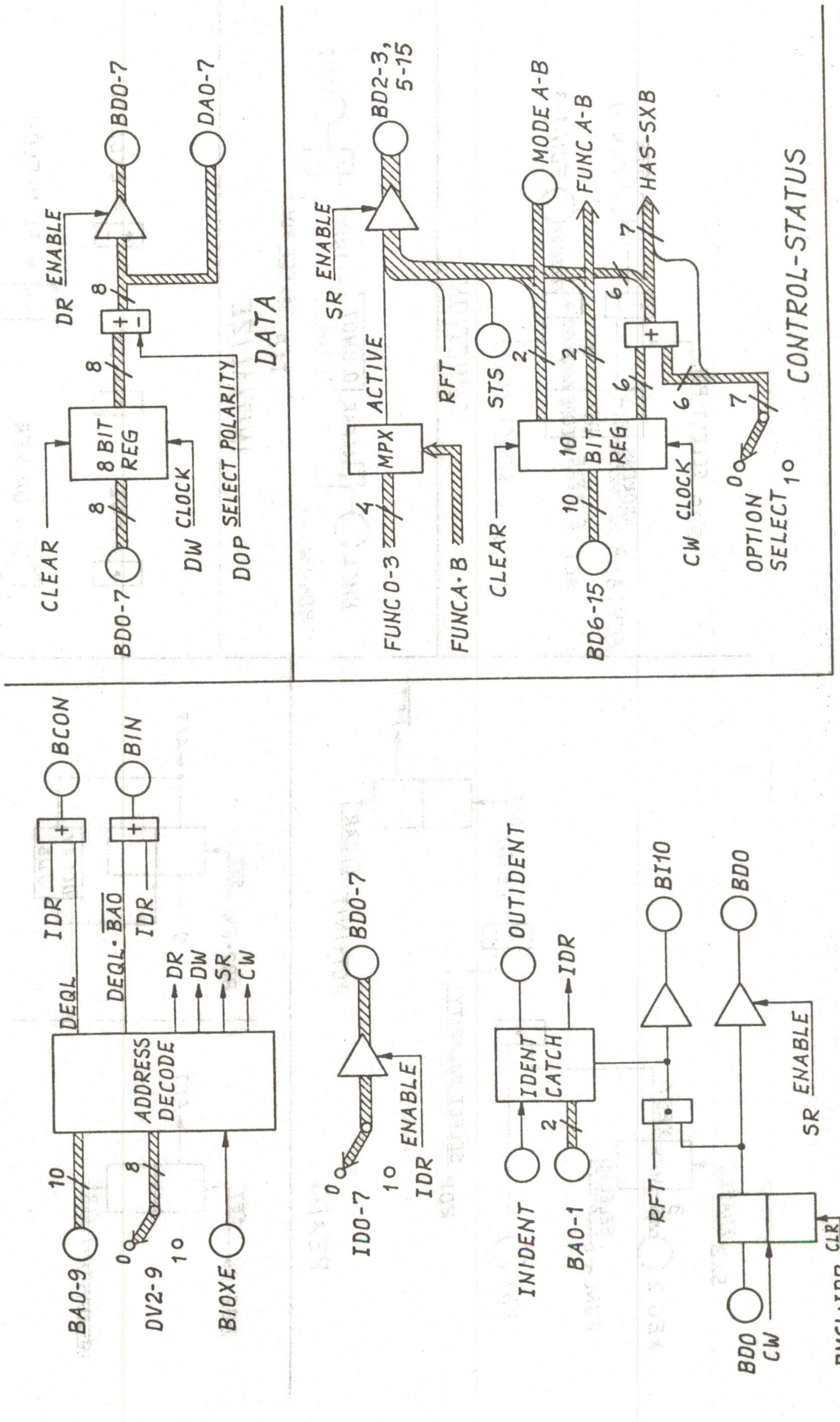


Fig.5.1 I/O-BUS COMMUNICATION

5.2 Device Communication

5-3a

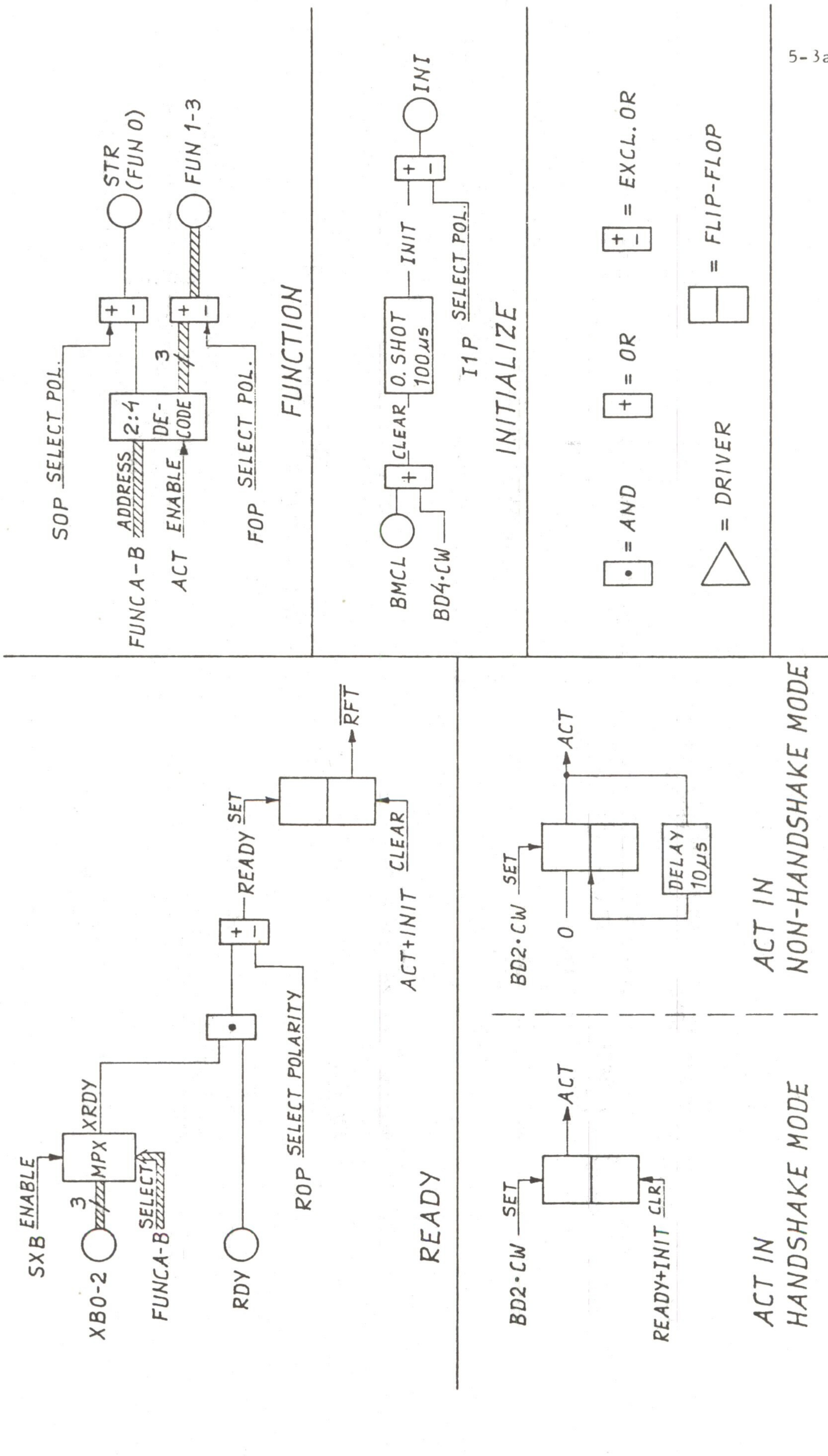
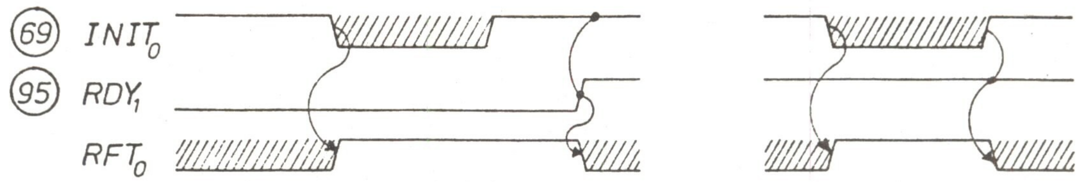


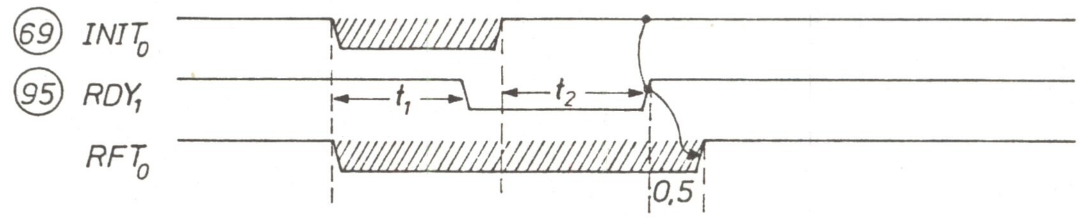
Fig.5.2 DEVICE COMMUNICATION

6. TIMING DIAGRAMS

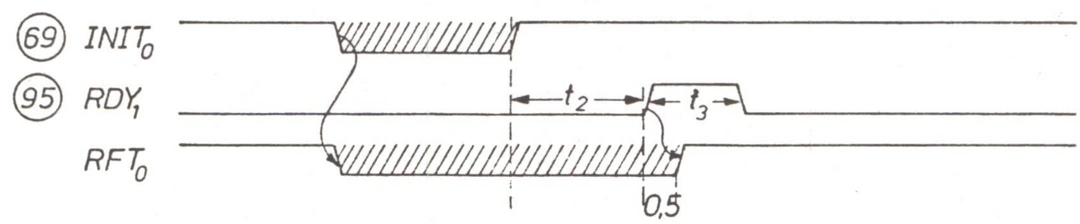
6.1 Initialization



6.1.1 Device Clear for devices which does not use the INIT signal. Shown for two states of RDY.



6.1.2 Device Clear for devices which use the INIT signal and responds with a READY-level.



6.1.3. Device Clear for devices which use the INIT signal and responds with a READY- pulse.

Fig. 6.1 Initialization

6.2 Device Timing

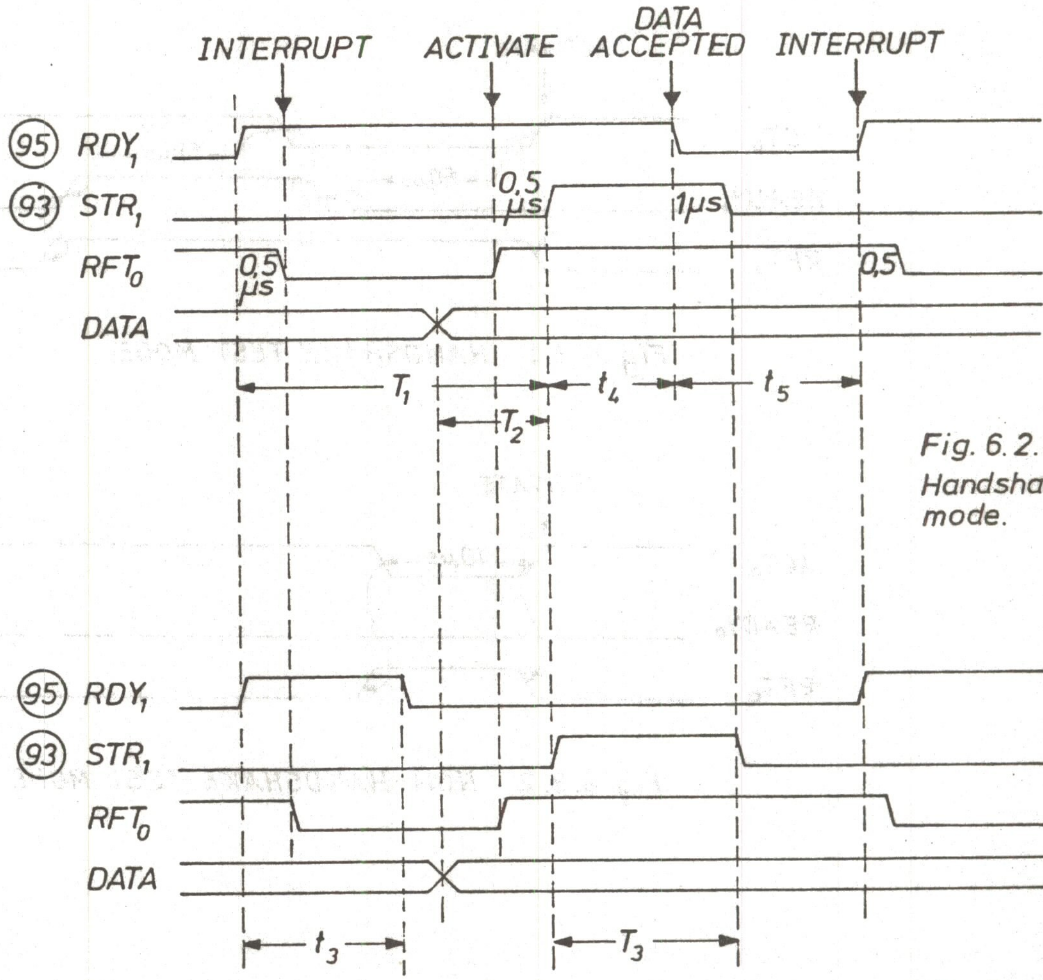


Fig. 6.2.1 Handshake mode.

Fig. 6.2.2 Non-handshake mode.

Fig. 6.2 Device timing

6.3 Test-mode Timing

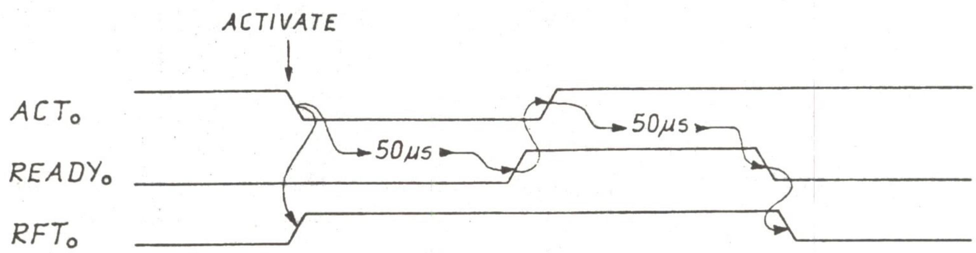


Fig. 6.3.1 HANDSHAKE TEST MODE

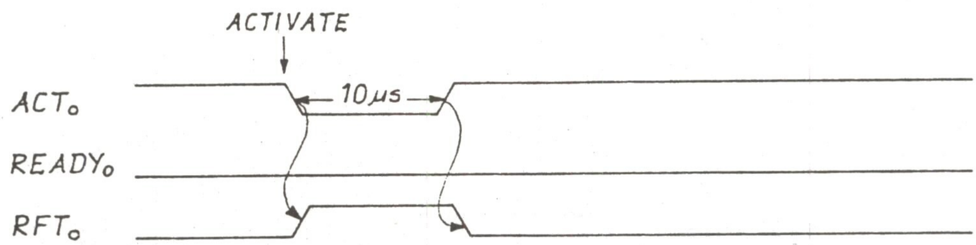


Fig. 6.3.2 NON-HANDSHAKE TEST MODE

Fig. 6.3 TEST MODE TIMING

7. SIGNAL DEFINITIONS

ABBREVIATION OF SECTION NAMES:
****

ACT	=	ACTIVATE
ADD	=	ADDRESS DECODING
COST	=	CONTROL-STATUS REGISTER
DATA	=	DATA REGISTER
DEV	=	DEVICE CONNECTION
DEVT	=	DEVICE TERMINALS
DMAT	=	DMA CONTROLLER TERMINALS
IDC	=	IDENT CONTROL
IDR	=	IDENT READ
INT	=	INTERRUPT CONTROL
IOB	=	IO-BUS TERMINALS
REDY	=	READY
TEST	=	TEST
XBUS	=	XBUSY

SIGNAL	POL	GENERATED	USED	DESCRIPTION
A 0	0	ADD	IDC	BUFFERED IOB ADDRESS
ACT	0	ACT		INTERFACE ACTIVE= STROBE ON.CLEARED BY ACTEND OR REMOVAL OF RDY
ACTEND	0	ACT	ACT	CLEAR ACT AFTER 10 MICROS. IN NON-HANDSHAKE MODE
ACTIVE	1	ACT	COST	INTERFACE ACTIVE. STATUS BIT 2. POLARITY DEPENDS ON S0P OR F0P
BA 0-9	0	IOB	ADD	IOB ADDRESS
BCON	0	IDC	IOB	IOB CONNECT
BD 0,2-3	0	IOB IDR DATA COST	DATA	IOB DATA
BD 1,4	0	IOB IDR DATA	DATA	IOB DATA
BD 2-7	0	IOB IDR DATA COST	DATA	IOB DATA
BD 8-9	0	IOB COST	DATA	IOB DATA
BD 10-15	0	IOB COST	COST	IOB DATA

SIGNAL	POL	GENERATED	USED	DESCRIPTION
BIN	0	IDC	IOB	IOB INPUT
BIOXE	0	IOB	ADD	IOB IOX-CYCLE ACTIVE
BI 10	0	INT	IOB	IOB INTERRUPT REQUEST ON LEVEL 10
BMCL	0	IOB	INI	IOB MASTER CLEAR
CLEAR	0	INI	INT DATA COST	MASTER CLEAR OR DEVICE CLEAR
CW	0	ADD	ADD INT	WRITE CONTROL WORD
CW	1	ADD	ACT COST INI	WRITE CONTROL WORD
D 0	1	DATA	INT	BUFFERED IOB DATA
D 1	1	DATA		BUFFERED IOB DATA
D 2	1	DATA	ACT	BUFFERED IOB DATA
D 3	1	DATA	COST	BUFFERED IOB DATA
D 4	1	DATA	INI	BUFFERED IOB DATA
D 5	1	DATA		BUFFERED IOB DATA
D 6-7	1	DATA	COST	BUFFERED IOB DATA
D 8-9	1	DATA	COST	BUFFERED IOB DATA
DA 0-7	1	DEV	DEVT	BUFFERED VERSION OF DAT 0-7
DAT 0-7	1	DATA	DEV	LATCHED DEVICE DATA
DEQL	1	ADD	IDC	ADDRESS BIT 2-9 MATCH DV 2-9, AND IOX IS ACTIVE
DMABUSY	0	INT	DMAT	INTERFACE NOT-READY SIGNAL TO DMA CONTROLLER
DMACT	0	DMAT	ADD	DMA DATA-STROBE SIGNAL FROM DMA CONTROLLER
DMACT	1	ADD	ACT	DMA DATA-STROBE SIGNAL FROM DMA CONTROLLER
DMAINIT	0	INI	DMAT	100 MICROSEC. INITIALIZE SIGNAL TO DMA CONTROLLER

SIGNAL	POL	GENERATED	USED	DESCRIPTION
DR	0	ADD	DATA	READ BACK DATAWORD TO A-REG. FOR TEST PURPOSES
DV 2-9	0	ADD	ADD	SWITCHES THAT DEFINES THE DEVICENUMBER
DW	0	ADD	DATA	WRITE IO-BUS DATA INTO DATAREG
DØP	0	COST	DATA	CAUSE DEVICE DATA, DA 0-7, IN 0-POLARITY WHEN LOW
FUN 1-3	1	DEV	DEVT	FUNCTION PULSES. CAUSE SOME ACTION THAT MAKE THE DEVICE BUSY
FUNC A-B	1	COST	ACT	TWO BITS THAT DECODED DETERMINE FUN(C) 0-3
FUNC 1-3	1	ACT	DEV	SAME AS FUN BEFORE BUFFERING
FØP	0	COST	ACT	CAUSE FUNCTION PULSES FUN 1-3 IN 0-POLARITY WHEN LOW
HAS	1	COST	ACT	SET INTERFACE IN HANDSHAKE-MODE WHEN HIGH
ID 0-7	1	IDR	IDR	SWITCHES THAT DETERMINES THE IDENT CODE
IDR	0	IDC	IDR INT	READ IDENT CODE, CLEAR INTERRUPT ENABLE
INGRANT	0	IOB	ADD	IOB DMA-CYCLE ACTIVE
INI	0	DEV	DEVT	BUFFERED VERSION OF INIP
INIDENT	0	IOB	IDC	IOB IDENT INSTRUCTION ACTIVE
INIP	0	INI	DEV	100 MICROSEC. INITIALIZE PULSE OF SELECTABLE POLARITY
INIT	0	INI	INT	100 MICROSEC. INITIALIZE PULSE. FORCE RFT = 0
INIT	1	INI	ACT	100 MICROSEC. INITIALIZE PULSE. FORCE ACT = 0
INT	1	IDC	IDC	NEXT INIDENT IS READY TO BE CATCHED
INTEN	0	INT	COST	ENABLE INTERRUPT ON RFT = 1
INT10	0	INT	ADD	INTERRUPT REQUEST ON LEVEL 10
I1P	0	COST	INI	CAUSE INI-PULSE IN 1-POLARITY WHEN LOW
MATCH	1	ADD	ADD	ADDRESSBITS 2-7 MATCH DV 2-7

SIGNAL	POL	GENERATED	USED	DESCRIPTION
MOD A-B	0	DEV	DEVT	BUFFERED VERSION OF MODE A-B
MODE A-B	1	COST	DEV	SET DEVICE IN A PREDETERMINED MODE. DOES NOT REMOVE READY
OUTGRANT	0	ADD	IOB	IOB GIVE AWAY DMA-CYCLE
OUTIDENT	0	IDC	IOB	IOB GIVE AWAY IDENT-CYCLE
RACT	0	ACT	INT TEST	SAME AS ACT, BUT MAY OCCUR EVEN IF PIN 19E13 IS LOW
RDY	0	DEV	REDY	DEVICE CAN ACCEPT DATA
RDY	1	DEVT	DEV	DEVICE CAN ACCEPT DATA
RFT	0	INT	COST	INTERFACE CAN ACCEPT (IS READY FOR) DATA FROM CPU
READY	0	REDY	INT ACT	DEVICE READY. TAKES ALSO EXTRA BUSY AND TESTMODE INTO ACCOUNT
RDIDENT	0	ADD	IDC	READY TO CATCH IDENT FOR THIS INTERFACE
R0P	0	COST	REDY	ACCEPT RDY-SIGNAL IN 0-POLARITY WHEN LOW
SR	0	ADD	COST	READ STATUS INTO A-REG
STR	1	DEV	DEVT	BUFFERED VERSION OF STROBE
STROBE	1	ACT	DEV	STROBE DATA INTO DEVICE. SAME AS FUNC 0
STS	0	DEVT	DEV	STATE OF SELECTED FEATURE OF DEVICE. DOES NOT CAUSE INTERRUPT
STS	1	DEV	COST	INVERTED STS
SXB	0	COST	ACT	ACCEPT EXTRA BUSY SIGNALS WHEN LOW
S0P	0	COST	ACT	CAUSE STR-SIGNAL IN 0-POLARITY WHEN LOW
TEST	1	COST	TEST	IGNORE DEVICE-RDY AND USE DELAYED ACT AS READY INSTEAD
XB 0-2	1	DEVT	XBUS ACT	EXTRA BUSY SIGNALS FROM DEVICE
XRDY	0	ACT	REDY	= EXTRA BUSY IN 1-POLARITYAFTER SELECTION ACCORDING TO FUNC A-B

8. TESTING

Normally two different types of tests are desired.

"Interface debugging" during production and repair and "Verification of interface and peripheral device" at QA-test and maintenance.

The interface cannot be guaranteed free of errors even if it works OK with a certain device since no device uses all features.

However, below a test program is described which together with some manual measurements is believed to check the interface completely.

It also contains routines to verify that the peripheral device works properly.

8.1 Test Parallel Byte Output, HAR 1942

The test program consists of 4 parts:

- operators communication
- interface debugging
- lineprinter test
- plotter test for Versatec 1110A

8.1.1 Operator communication

Terminal 1, consoll, and terminal 2 are interrupt controlled and the operator may at any time give commands on any of them.

The commands are printed by typing:

```
?
   COMMANDTABLE:
TP = TEST PLOTMODE ON VERSATEC
TV = TEST VERSATEC PRINTER
TD = TEST DATA PRODUCT
TCE= TEST CENTRONICS
TL = TEST LOGABAX
TCD= TEST CDC MATRIX PRINTER
TQ = TEST QUME
TF = TEST FACIT PUNCH
TI = TEST INTERFACE ONLY
X  = EXECUTE TEST
O  = READ OPTION SELECT SWITCHES
A  = PRINT/REDEFINE IOX ADDRESS (DEVICENO) TERMINATE WITH CR.
        DEFAULT IS 1774 (ALL SWITCHES ON)
B  = BREAK CURRENT TEST
```

```
P   = REDEFINE PATTERN TO BE PRINTED, TERMINATE WITH CR
        DEFAULTS ARE ASCII CHARACTERS 040 - 176,015,012.
S   = PRINT STATUS INFORMATION
C   = CONTINUE FROM ERRORLOOP
N   = GO TO NEXT SECTION
D   = PRINT DATA INFORMATION
I   = PRINT INTERRUPT INFORMATION
V   = PRINT/REDEFINE IDENT-VECTOR, TERMINATE WITH CR
        DEFAULT IS 0 (ALL SWITCHES ON)
```

The program issues only short messages, and further details must be requested by one of the above commands.

Always assure that the program uses the same device address that is defined by switch 7 D. To do this, type A and fill in the correct address if necessary:

```
A/001774 430
```

Type A again to verify the new value:

```
A/000430
```

8.1.2 Interface Debugging

To test the interface, type T I:

```
TEST INTERFACE ONLY
SET OPTION SELECT SWITCHES 1-7: OFF OFF OFF OFF OFF OFF OFF
```

Then check option-switch setting by typing O :

```
OPTION SELECT SWITCHES 1-6 ARE: OFF OFF OFF OFF OFF OFF
```

Define the Ident-Vector to match the actual switch setting by typing

```
V/000000 3
```

Type new code if necessary and check result

```
V/000003
```

Start test by typing X :

If the interface is OK, this message is printed:

```
X

SECTION 1-8 COMPLETE
ENTER SECTION 9: "SCOPE-LOOP"
```

Else a message like this is printed:

```
X
ERROR IN SECTION      1
```

and a loop with the failing data set is entered.

Error information must be requested by one of the commands S, D and I.

Only a few status bits are relevant in each section. The irrelevant bits are cleared according to "STATUS MASK" which is also printed at the command "S".

Each time the loop is repeated a "scope-trigger" pulse is present on pin E 9.

The table below shows which part of the interface is tested in the 9 sections:

SEC-	INT./	DATA	CONTROL														STATUS				
TION	IDENT	Ø-7	Ø	2	3	4	6	7	8	9	10	11	12	13	14	15	Ø	2	3	5	6-15
1																					X
2		X											X								
3		X											X								
4						X															
5									X	X		X			X			X			
6				X	X													X	X		
7																					
8	X		X														X				
9		X					X	X	X	X	X					X			X	X	

Further details are found in the listing.

8.1.3 Manual Test of Interface

Section 1-8 cannot check that the signals on device terminals are correct.

Hence in section 9 disconnect device and check with a scope that pulses appear on terminals 93-77 and 73-63 in descending order.

Type S and check that "Actual status" is 10. Grounding of terminals 95 and 75 should change the status to 40.

Close switch 7B7, SXB, which shall cause 19C3 to go high.

Ground terminal 61 - check on scope that 19C3 is low, except when terminals 63, 65 and 67 are high.

Ground terminal 60.19C3 shall be low while terminal 67 is high.

Ground terminal 59.19C3 shall be low while terminals 63 or 65 are high.

To recover from the "Scope loop" (or any other loop), type B.

8.1.4 Lineprinter Test

To verify that the peripheral device works properly, type one of the T-codes specified in the command table, for instance TL:

```
TEST LOGABAX MATRIX PRINTER
SET OPTION SELECT SWITCHES 1-7: OFF  ON  ON OFF OFF OFF OFF
```

Check that switches are correct by typing Q:

When typing X the lineprinter (or punch) shall print all ASCII codes from 40 - 176 followed by carriage return and linefeed. Parity is even.

A print on Versatec is shown below:

```
!"#$%&'()*+;-:/0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←-abcdefghijklmnopqrstuvwxyz{|}~
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←-abcdefghijklmnopqrstuvwxyz{|}~
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←-abcdefghijklmnopqrstuvwxyz{|}~
!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑←-abcdefghijklmnopqrstuvwxyz{|}~
```

The line will be repeated until B is typed:

```
B
PROGRAM IDLE
```

For debugging purposes etc., it is possible to define other textstrings. I.e. type P :

```
PRINT:
1234567890
```

The above string will be printed until another one is defined.

To recover the default string, press RESTART.

Two error messages may occur:

```
X

DEVICE NOT READY
```

and / or

```
STATUS ERROR
```

The program will try to print characters even if "STATUS ERROR" occurs.

To investigate the status error, type S. To terminate the test, type B.

8.1.5 Versatec Plot Test

To verify the Versatec 1110 A plotter, type TP :

```
TEST PLOTMODE ON VERSATEC
SET OPTION SELECT SWITCHES 1-7: OFF OFF OFF  ON  ON OFF OFF
```

Then type X :

The plotter shall first go to TOP OF FORM, then plot the ND-symbol consisting of grey and black dots.

Another TOP OF FORM preceedes a negative plot of the ND-symbol.

Finally, the signal END OF TRANSMISSION is programmed.

The plot test is executed once, then the program returns to idle state.

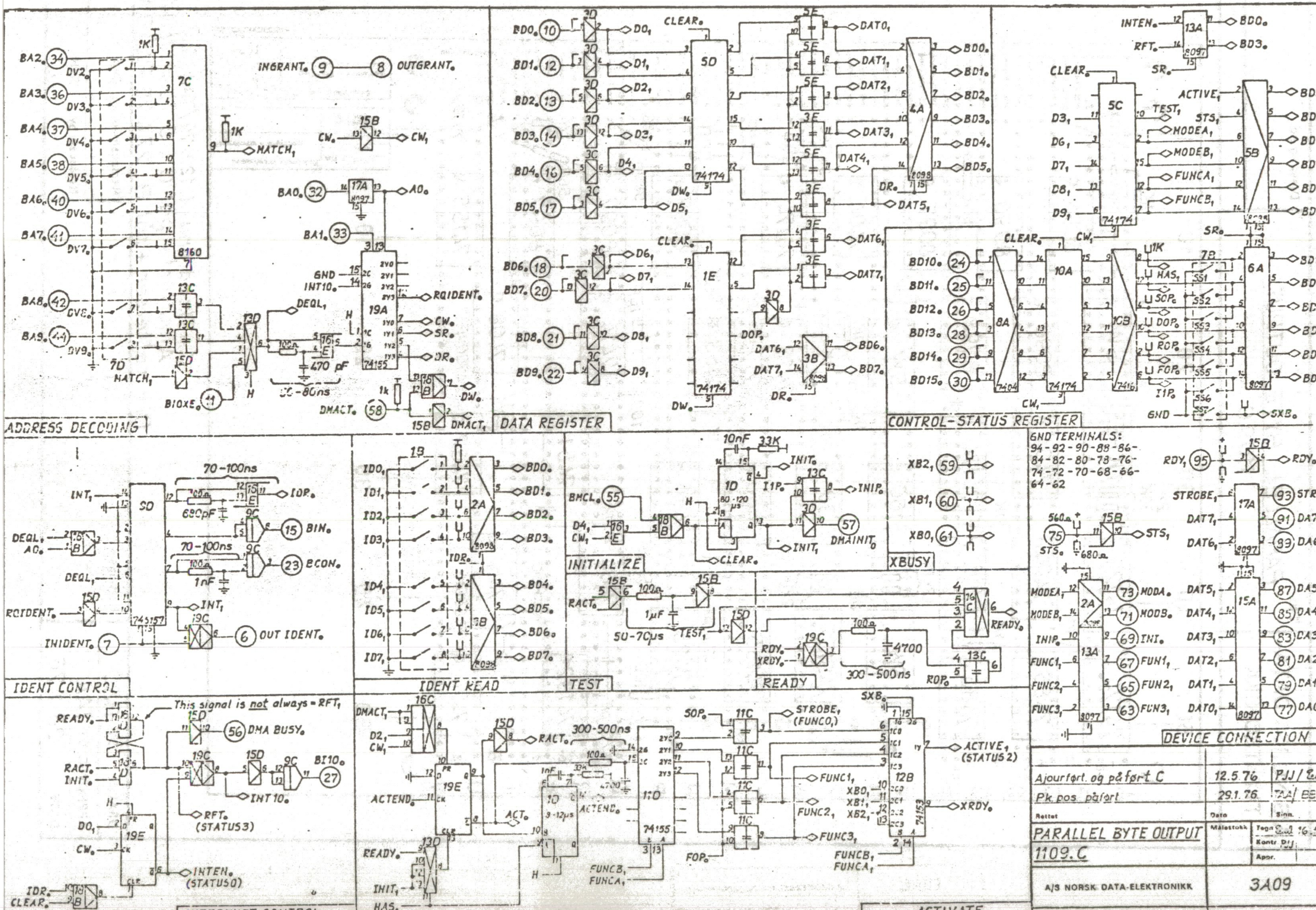
```
X

END OF PLOT
PROGRAM IDLE
```

One error message may occur:

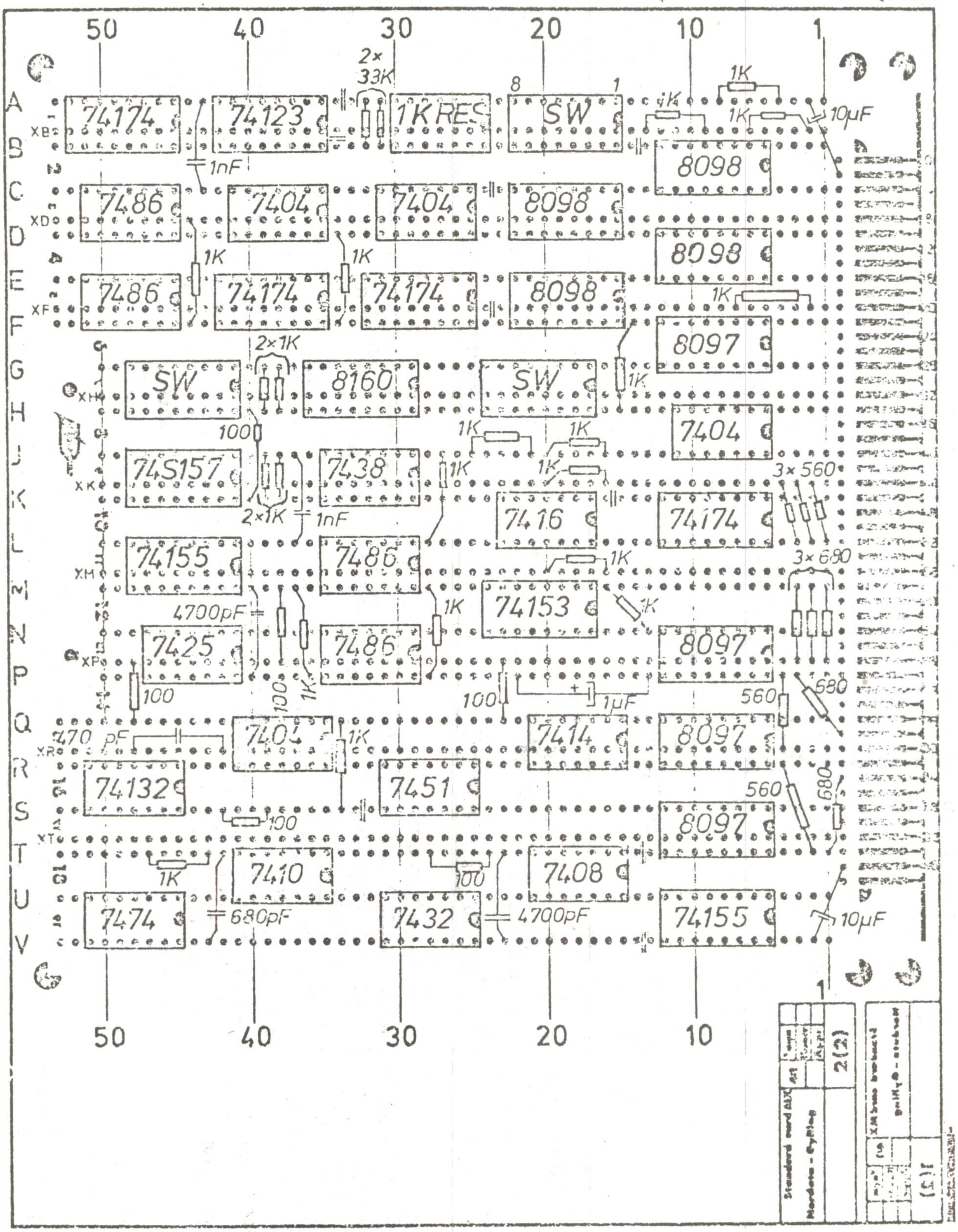
```
X

DEVICE NOT READY
```

The program tries about 4 seconds before the message is printed. Then it tries again until device is ready or B is typed.

9 LOGIC DIAGRAM


ADDRESS DECODING
DATA REGISTER
CONTROL-STATUS REGISTER
IDENT CONTROL
IDENT READ
INITIALIZE
TEST
READY
XBUSY
GND TERMINALS:
94-92-90-88-86-
84-82-80-78-76-
74-72-70-68-66-
64-62
This signal is not always = RFT₁
DEVICE CONNECTION
Ajourført og påført C
12.5.76
Pk.pos. påført
29.1.76
PARALLEL BYTE OUTPUT
1109.C
A/S NORSK DATA-ELEKTRONIKK
3A09
ACTIVATE

A/S NORSK DATA-ELEKTRONIKK	Title: PARALLEL BYTE OUTPUT 1109.C	Drawing no.



1μF kond. snudd. 12.5.76/TAA/Eml
Ajourført + påf. C. 4.5.76 PJJ/BW
Div. rettelser + påf. B. 27.4.76 PJJ/BW

DRAWN BY BBO	Remarks	Replacement for	Date
APPROVED BY TAA		Replaced by	Date
DATE 28.1.76.			

10 ARRANGEMENT DRAWING

11 DEVICE CABLE LISTS

A/S NORSK DATA-ELEKTRONIKK	Title: VERSATEC PRINT/PLOT with Parallel byte output 1109	Drawing no. 11.1

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	CANNON DCC-37 S	
1	RDY	1	BERG 95	A	11	
	GND		" 94	C	30	
2	STR	1	" 93	B	10	
	GND		" 92	D	29	
3	DA7	1	" 91	E	8	
	GND		" 90	H	27	
4	DA6	1	" 89	F	7	
	GND		" 88	J	26	
5	DA5	1	" 87	K	6	
	GND		" 86	M	25	
6	DA4	1	" 85	L	5	
	GND		" 84	N	24	
7	DA3	1	" 83	P	4	
	GND		" 82	S	23	
8	DA2	1	" 81	R	3	
	GND		" 80	T	22	
9	DA1	1	" 79	U	2	
	GND		" 78	W	21	
10	DA0	1	" 77	V	1	
	GND		" 76	X	20	
11	STS	0	" 75	Y	32	
	GND		" 74	AA	34	
12	MODA	0	" 73	Z	12	
	GND		" 72	BB	31	
13	MODB	0	" 71	CC	14	
	GND		" 70	EE	33	
14	INI	0	" 69	DD	9	
	GND		" 68	FF	28	
15	FUN1	1	" 67	HH	18	
	GND		" 66	KK	37	
16	FUN2	1	" 65	JJ	17	
	GND		" 64	LL	36	
17	FUN3	1	" 63	MM	16	
	GND		" 62	PP	35	
18	XB0		" 61	NN		
	XB1		" 60	RR		
19	XB2		" 59	SS		
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 28/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: DATA PRODUCT S LP with Parallel byte output 1109	Drawing no. 11.2

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	DEVICE-PLUG	
1	RDY	~~1~~	BERG 95	A	EE	
	GND		" 94	C	C	
2	STR	1	" 93	B	j	
	GND		" 92	D	m	
3	DA7		" 91	E		
	GND		" 90	H		
4	DA6	1	" 89	F	n	
	GND		" 88	J	k	
5	DA5	1	" 87	K	Z	
	GND		" 86	M	b	
6	DA4	1	" 85	L	V	
	GND		" 84	N	X	
7	DA3	1	" 83	P	R	
	GND		" 82	S	T	
8	DA2	1	" 81	R	L	
	GND		" 80	T	N	
9	DA1	1	" 79	U	F	
	GND		" 78	W	J	
10	DA0	1	" 77	V	B	
	GND		" 76	X	D	
11	STS	1	" 75	Y	y	
	GND		" 74	AA	AA	
12	MODA		" 73	Z		
	GND		" 72	BB		
13	MODB		" 71	CC		
	GND		" 70	EE		
14	INI		" 69	DD		
	GND		" 68	FF		
15	FUN1		" 67	HH		
	GND		" 66	KK		
16	FUN2		" 65	JJ		
	GND		" 64	LL		
17	FUN3		" 63	MM		
	GND		" 62	PP		
18	XB0		" 61	NN		
	XB1		" 60	RR		
19	XB2		" 59	SS		
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 28/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: CENTRONICS LP with Parallel byte output 1109	Drawing no. 11. 3

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	AMP	
1	RDY	0	BERG 95	A	10	
	GND		" 94	C	28	
2	STR	1	" 93	B	1	
	GND		" 92	D	19	
3	DA7	1	" 91	E	9	
	GND		" 90	H	27	
4	DA6	1	" 89	F	8	
	GND		" 88	J	26	
5	DA5	1	" 87	K	7	
	GND		" 86	M	25	
6	DA4	1	" 85	L	6	
	GND		" 84	N	24	
7	DA3	1	" 83	P	5	
	GND		" 82	S	23	
8	DA2	1	" 81	R	4	
	GND		" 80	T	22	
9	DA1	1	" 79	U	3	
	GND		" 78	W	21	
10	DA0	1	" 77	V	2	
	GND		" 76	X	20	
11	STS		" 75	Y	32	
	GND		" 74	AA	29	
12	MODA		" 73	Z		
	GND		" 72	BB		
13	MODB		" 71	CC		
	GND		" 70	EE		
14	INI		" 69	DD	31	
	GND		" 68	FF	30	
15	FUN1		" 67	HH		
	GND		" 66	KK		
16	FUN2		" 65	JJ		
	GND		" 64	LL		
17	FUN3		" 63	MM		
	GND		" 62	PP		
18	XB0		" 61	NN		
	XB1		" 60	RR		
19	XB2		" 59	SS		
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 28/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: LOGA BAX MP with Parallel byte output 1109	Drawing no. 11.4

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	DEVICE PLUG	
1	RDY	1	BERG 95	A	15 A	
	GND		" 94	C	1 B	
2	STR	0	" 93	B	6 A	
	GND		" 92	D	2 B	
3	DA7		" 91	E		
	GND		" 90	H		
4	DA6	0	" 89	F	9 A	
	GND		" 88	J	3 A	
5	DA5	0	" 87	K	8 A	
	GND		" 86	M	1 A	
6	DA4	0	" 85	L	7 A	
	GND		" 84	N	1 A	
7	DA3	0	" 83	P	11 A	
	GND		" 82	S	2 A	
8	DA2	0	" 81	R	12 A	
	GND		" 80	T	2 A	
9	DA1	0	" 79	U	13 A	
	GND		" 78	W	1 B	
10	DA0	0	" 77	V	10 A	
	GND		" 76	X	2 B	
11	STS		" 75	Y		
	GND		" 74	AA		
12	MODA		" 73	Z		
	GND		" 72	BB		
13	MODB		" 71	CC		
	GND		" 70	EE		
14	INI		" 69	DD		
	GND		" 68	FF		
15	FUN1		" 67	HH		
	GND		" 66	KK		
16	FUN2		" 65	JJ		
	GND		" 64	LL		
17	FUN3		" 63	MM		
	GND		" 62	PP		
18	XB0		" 61	NN		
	XB1		" 60	RR		
19	XB2		" 59	SS		
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 28/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: CDC MATRIX PRINTER with Parallel byte output 1109	Drawing no. 11.5

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)		PLUG BURNDY	AMP 206150-1	
1	RDY	1	BERG	95	A	19	
	GND		"	94	C	20	
2	STR	0	"	93	B	17	
	GND		"	92	D	18	
3	DA7	0	"	91	E	10	
	GND		"	90	H	16	
4	DA6	0	"	89	F	12	
	GND		"	88	J	11	
5	DA5	0	"	87	K	14	
	GND		"	86	M	13	
6	DA4	0	"	85	L	9	
	GND		"	84	N	15	
7	DA3	0	"	83	P	7	
	GND		"	82	S	8	
8	DA2	0	"	81	R	5	
	GND		"	80	T	6	
9	DA1	0	"	79	U	3	
	GND		"	78	W	4	
10	DA0	0	"	77	V	1	
	GND		"	76	X	2	
11	STS	0	"	75	Y	27	
	GND		"	74	AA	28	
12	MODA		"	73	Z		
	GND		"	72	BB		
13	MODB		"	71	CC		
	GND		"	70	EE		
14	INI	0	"	69	DD	21	
	GND		"	68	FF	22	
15	FUN1		"	67	HH		
	GND		"	66	KK		
16	FUN2		"	65	JJ		
	GND		"	64	LL		
17	FUN3		"	63	MM		
	GND		"	62	PP		
18	XB0	1	"	61	NN	23	
	XB1		"	60	RR		
19	XB2		"	59	SS		
			"	58	UU		
20			"	57	TT		
			"	56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 18/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: QUME with Parallel byte output 1109	Drawing no. 11.6

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	60 pin-0,1" Edge-Connector	
1	RDY		BERG 95	A		
	GND		" 94	C		
2	STR	0	" 93	B	18	
	GND		" 92	D	19	
3	DA7	0	" 91	E	10	
	GND		" 90	H	15	
4	DA6	0	" 89	F	9	
	GND		" 88	J	15	
5	DA5	0	" 87	K	8	
	GND		" 86	M	15	
6	DA4	0	" 85	L	7	
	GND		" 84	N	15	
7	DA3	0	" 83	P	6	
	GND		" 82	S	15	
8	DA2	0	" 81	R	5	
	GND		" 80	T	15	
9	DA1	0	" 79	U	4	
	GND		" 78	W	15	
10	DA0	0	" 77	V	3	
	GND		" 76	X	15	
11	STS	0	" 75	Y	37	
	GND		" 74	AA	38	
12	MODA	0	" 73	Z	11&12	
	GND		" 72	BB	15	
13	MODB	0	" 71	CC	13	
	GND		" 70	EE	15	
14	INI	0	" 69	DD	16	
	GND		" 68	FF	17	
15	FUN1	0	" 67	HH	20	
	GND		" 66	KK	21	
16	FUN2	0	" 65	JJ	22	
	GND		" 64	LL	23	
17	FUN3	0	" 63	MM	26	
	GND		" 62	PP	27	
18	XB0	1	" 61	NN	39	NOT TWISTED
	XB1	1	" 60	RR	41	
19	XB2	1	" 59	SS	43	
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY	BSE	Remarks	Replacement for	Date
APPROVED BY	PJJ	Databit -1 is not used	Replaced by	Date
DATE	28/5-76			

A/S NORSK DATA-ELEKTRONIKK	Title: FACIT PUNCH with Parallel byte output 1109	Drawing no. 11.7

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)	PLUG BURNDY	CANNON DB 25 P	
1	RDY	1	BERG 95	A	12	
	GND		" 94	C	25	
2	STR	1	" 93	B	9 & 11	
	GND		" 92	D	25	
3	DA7	1	" 91	E	8	
	GND		" 90	H	25	
4	DA6	1	" 89	F	7	
	GND		" 88	J	25	
5	DA5	1	" 87	K	6	
	GND		" 86	M	25	
6	DA4	1	" 85	L	5	
	GND		" 84	N	25	
7	DA3	1	" 83	P	4	
	GND		" 82	S	25	
8	DA2	1	" 81	R	3	
	GND		" 80	T	25	
9	DA1	1	" 79	U	2	
	GND		" 78	W	25	
10	DA0	1	" 77	V	1	
	GND		" 76	X	25	
11	STS		" 75	Y		
	GND		" 74	AA		
12	MODA		" 73	Z		
	GND		" 72	BB		
13	MODB		" 71	CC		
	GND		" 70	EE		
14	INI		" 69	DD		
	GND		" 68	FF		
15	FUN1		" 67	HH		
	GND		" 66	KK		
16	FUN2		" 65	JJ		
	GND		" 64	LL		
17	FUN3		" 63	MM		
	GND		" 62	PP		
18	XB0		" 61	NN		
	XB1		" 60	RR		
19	XB2		" 59	SS		
			" 58	UU		
20			" 57	TT		
			" 56	VV		

DRAWN BY BSE	Remarks	Replacement for	Date
APPROVED BY PJJ		Replaced by	Date
DATE 28/5-76			

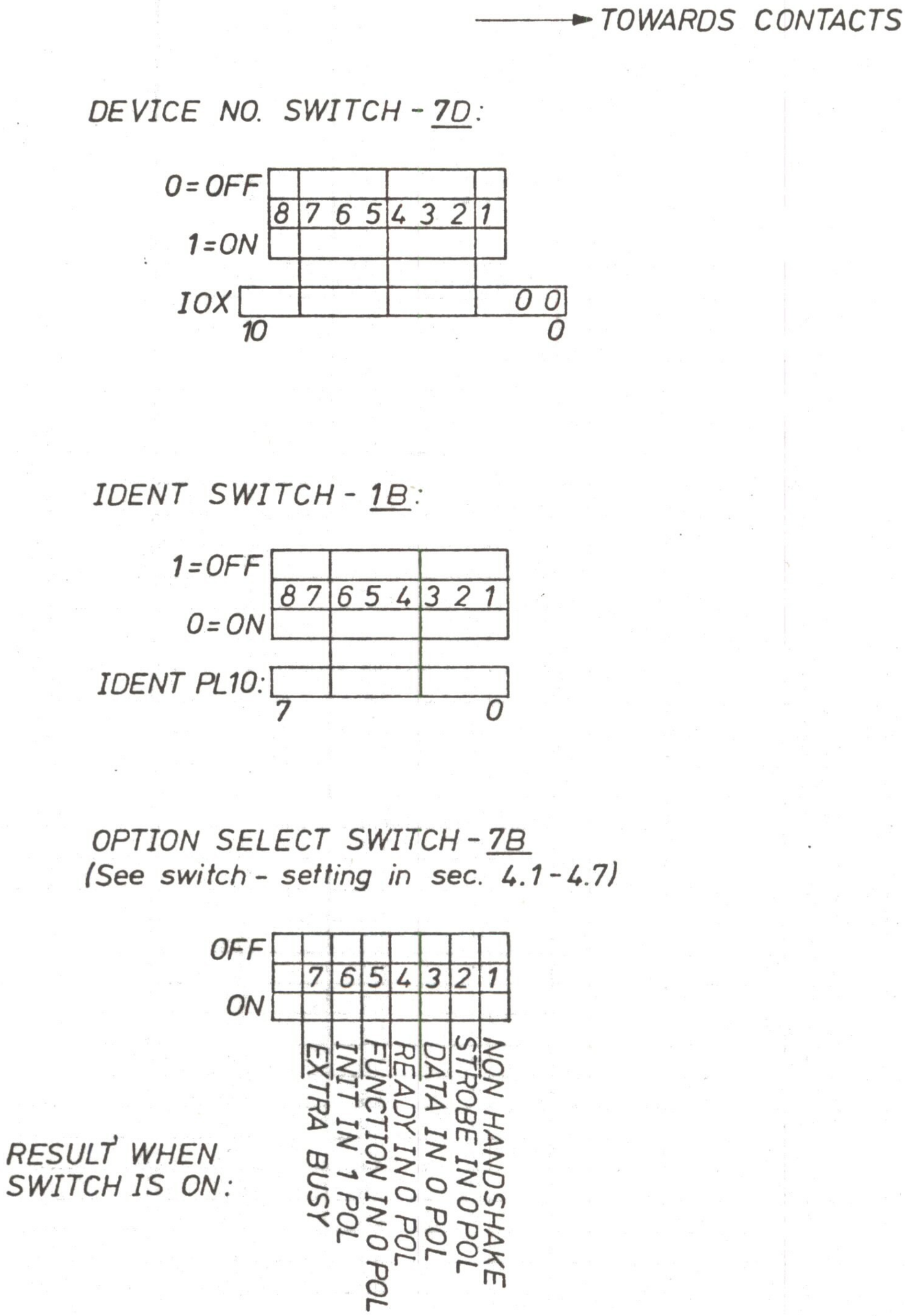


Fig. 12.1. SWITCH CODING.

4: Paper Tape/Card Equipment

SPECIFICATION OF TAPE READER INTERFACE

Standard dev. no. 0400 (0400 - 0403) oct.

No. of dev. no. 4

Standard int. level 12 des.

Standard ident no. 2

Control word IOX DEV. NO. + 3

Bit 0	Enable interrupt on ready for transfer.
Bit 2	Activate device. (Start reading next character on tape.)
Bit 3	Test
Bit 4	Device clear.
Bit 1 and	5-15 not used.

Status word IOX DEV. NC. + 2

Bit 0	Int. enabled on ready for transfer.
Bit 2	Reader active
Bit 3	Reader ready for transfer. (Character read.)
Bit 1 and	4-15 not used.

IOX DEV NO + 1	Not used.
IOX DEV NO	Read character. The same character may be read several times if wanted.

TEST

When bit 3 in the control word is set to 1, the interface may be tested without reader.

If bit 2 also is set to 1, the interface will give "ready for transfer" after a while.

If "ready for transfer" is constantly 1, the data register will increment for each time IOX DEV NO + 3 (Control word write) is used, and then it is possible to test the data path.

SPECIFICATION OF THE PUNCH INTERFACE

Standard dev. no.	0410 (0410 - 0413) oct.
No. of dev. no.	4
Standard int. level	10 des.
Standard ident no.	2

Write control word IOX DEV NO + 3

Bit 0	Enable interrupt
Bit 2	Activate device (Punch character now in buffer)
Bit 3	Test
Bit 4	Device clear
Bits 1 and 5-15	not used

Read status word IOX DEV NO +2

Bit 0	Interrupt enabled
Bit 2	Device active
Bit 3	Device ready

Write data word IOX DEV NO + 1

Write the 8 bits to be punched in a buffer register.

Read data IOX DEV NO

Only used under test.

It is not wise to write a character into the buffer if the punch is not ready.

Test

The interface may be tested without punch.

When bit 3 in the control word is one, the buffer register may be read back by IOX DEV NO. If the interface is activated, it will become "Ready for transfer" after a while.

SPECIFICATION OF CARD READER BUFFER (DOCUMATION) FOR NORD-10

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Standard device number 0420 (0420 - 0423) octal.

No. of dev. no.	4
Interrupt level	12 des.
Ident number	3

Write Control Word	IOX DEV + 3
Bit 0	Enable interrupt on ready for transfer.
Bit 1	Enable interrupt on error.
Bit 2	Activate): Feed one card. Clear end of card.
Bit 3	Test
Bit 4	Device clear. Clear interrupt flip-flop, overrun-flip-flop. Continue feed flip-flop and set end of card.
Bit 5-8	Not used.
Bit 9	Continous feed): Feed next card immediately.
Bit 10-15	Not used.

Read Status Word	IOX DEV + 2
Bit 0	Interrupt enabled on ready for transfer.
Bit 1	Interrupt enabled on error.
Bit 2	Card reader active. Signal from card reader.
Bit 3	Ready for transfer): A column may be read. This bit is turned off by "read data". IOX DEV.
Bit 4	Bit 5-9 set, error.
Bit 5	Hopper check error set from card reader.
Bit 6	Light or dark error from card reader.
Bit 7	Motion check error from card reader.

Bit 8	Overrun, one column was lost because it was not read before the next column was strobed into buffer. Cleared by master clear.
Bit 9	End of card.
Bit 10-15	Not used.
	Be aware that the card reader sends hopper check during reading the last card.

Write Data IOX DEV + 1

Only used for testing the interface without card reader.

Read Data IOX DEV

Read last column.

Test

The interface may be tested without card reader.

When bit 3 in the control word is set to one, the interface is in "test mode".

After IOX DEV + 3 with the A-register = 010, the interface will be in test mode.

An IOX DEV + 1 will then set ready-for-transfer (bit 3 in the status register), and increment the data register.

After the IOX DEV + 1, IOX DEV will read the data register into the A-register (lowest 12 bits), and IOX DEV + 2 will read the status register into the A-register with status bit 3 set (=1).

An "end of card" is simulated by IOX DEV + 1 and bit 5 set to one.

Programming example

Without interrupt.

```
CRDEV   =   420
   RD   =     0
   RS   =     2
   RC   =     3
```

```
%
%         CLEAR DEVICE
%
CRINI,    SAA 20; IOX + CRDEV + WC; EXIT
%
%         ROUTINE FOR READING A CARD
%         INTO A BUFFER, CRBUF
%
%         ACTIVATE DEVICE
%
CRREA,    SAX -120; SAA 4; IOX CRDEV CW
%
%         TESTING STATUS
%
CRT,      IOX CRDEV RS
          BSKP 40 DA EQL ZRO; JMP CRERT
          BSKP 30 DA EQL ONE; JMP CRT
%
%
%
%
%         READING DATA
CR1,      JXN CR2; JMP CRER2
CR2,      IOX CRDEV: STA I, X (CBUF + 120)
          AAX 1; JMP CRT
)FILL
%
%         ERROR BIT SET
%
CRERT,    BSKP 110 DA ZRO; JMP CREOC
%         ERROR STATUS IN A-REG.
          EXIT
%
%
CRER2,
%         ERROR TC MANY OR FEW
%         COLUMNS READ
          EXIT
CREOC,    JXZ * +2; JMP CRER2
          LDX (CBUF; EXIT AD1
```

)FILL
CBUF,   0
CPUF + 120 / 0

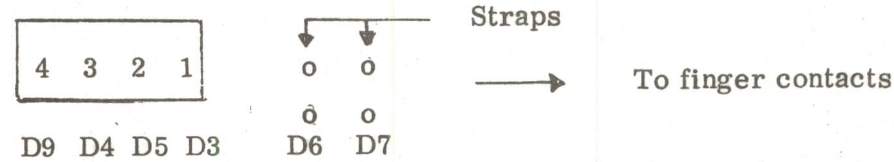
5: BUS CONTROL (1022, 1155 and 1158 with Switch setting)

BUS CONTROL CODING

On the NORD-10 1022 BUS CONTROL CARD there are three select functions to be set.

Select 1: Device number

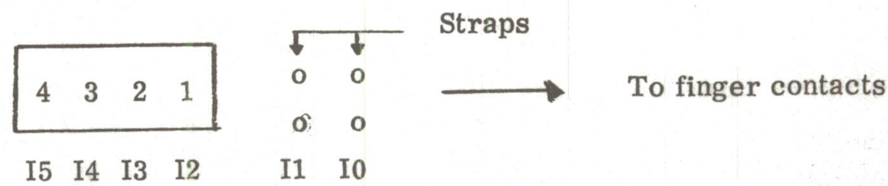
Position 10B:



IOX:	Device:	10B1	10B2	10B3	10B4	D6 strap	D7 strap
500-507	Disc 1	OFF	OFF	OFF	OFF	YES	NO
510-517	Disc 2	ON	OFF	OFF	OFF	YES	NO
520-527	M-T 1	OFF	OFF	ON	OFF	YES	NO
530-537	M-T 2	ON	OFF	ON	OFF	YES	NO
540-547	Drum 1	OFF	ON	OFF	OFF	YES	NO
550-557	Drum 2	ON	ON	OFF	OFF	YES	NO
560-567	Drum 3	OFF	ON	ON	OFF	YES	NO
570-577	Drum 4	ON	ON	ON	OFF	YES	NO
600-607	Versatec 1	OFF	OFF	OFF	OFF	BREAK	YES
610-617	Core-core	ON	OFF	OFF	OFF	BREAK	YES
1540-1547	Big Disc	OFF	ON	OFF	ON	YES	NO

Select 2: Ident number

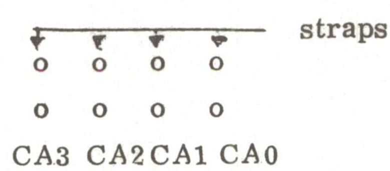
Position 18A:



IOX:	Device:	Ident no.	I0 strap	I1 strap	18A1	18A2	18A3	18A4
500-507	Disc 1	1	NO	YES	ON	ON	ON	ON
510-517	Disc 2	5	NO	YES	OFF	ON	ON	ON
520-527	MT-1	3	NO	NO	ON	ON	ON	ON
530-537	MT-2	7	NO	NO	OFF	ON	ON	ON
540-547	Drum 1	2	YES	NO	ON	ON	ON	ON
550-557	Drum 2	6	YES	NO	OFF	ON	ON	ON
560-567	Drum 3	12	YES	NO	ON	OFF	ON	ON
570-577	Drum 4	16	YES	NO	OFF	OFF	ON	ON
600-607	Versatec 1	4	YES	YES	OFF	ON	ON	ON
610-617	Core-core	11	NO	YES	ON	OFF	ON	ON
1540-1547	Big Disc	17	NO	NO	OFF	OFF	ON	ON

Select 3: Core address number

Position 8C:



The card beeing closest to the RACK CONTROLLER should have the lowest CAR number.

CAR 0	=	CA3, CA2, CA1 all straps
CAR 1	=	CA3, CA2 straps
CAR 2	=	CA3, CA1 straps and so on

CA0 is not used.

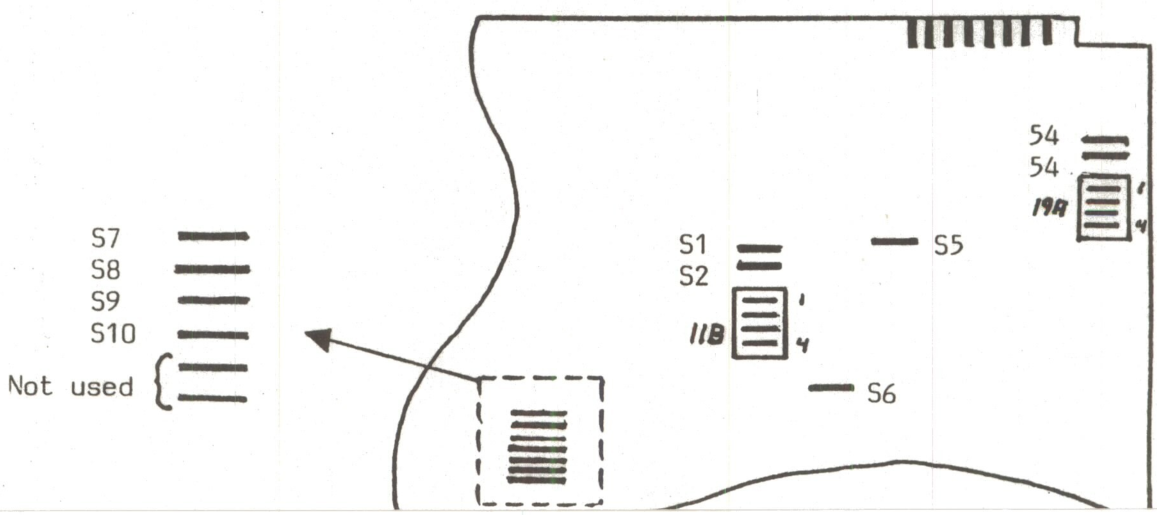
BUS CONTROL CODING FOR 1155 CARD

Device numbers are selected by four switches and two straps in position 11B. Ident codes are selected by four switches and two straps in position 19A, one strap in position 14B, and one strap in position 12C.
Core address registers are selected by four straps, S7-S10, in position 7C.

DEVICE NUMBER			IDENT CODE			CORE ADDRESS REGISTER	
Bus addr.bit	Switch	Strap	Ident code bit	Switch	Strap	Core addr.reg.bit	Strap
BA9	11B		I7		S6	CA0	S7
BA7		S1	I6		S5	CA1	S8
BA6		S2	I5	19A4		CA2	S9
BA5	11B1		I4	19A2		CA3	S10
BA4	11B3		I3	19A1			
BA3	11B4		I2	19A3			
			I1		S4		
			I0		S3		

Standard switch setting.

Device name	Device no.	Switch in pos. 11B				Strap		Ident code.	Switch in pos. 19A				Straps			
		1	2	3	4	S1	S2		1	2	3	4	S3	S4	S5	S6
DISC1	500	OFF	OFF	OFF	OFF	OFF	ON	1	ON	ON	ON	ON	OFF	ON	ON	ON
DISC2	510	OFF	OFF	OFF	ON	OFF	ON	5	ON	ON	OFF	ON	OFF	ON	ON	ON
M-T 1	520	OFF	OFF	ON	OFF	OFF	ON	3	ON	ON	ON	ON	OFF	OFF	ON	ON
M-T 2	530	OFF	OFF	ON	ON	OFF	ON	7	ON	ON	OFF	ON	OFF	OFF	ON	ON
DRUM1	540	ON	OFF	OFF	OFF	OFF	ON	2	ON	ON	ON	ON	ON	OFF	ON	ON
DRUM2	550	ON	OFF	OFF	ON	OFF	ON	6	ON	ON	OFF	ON	ON	OFF	ON	ON
DRUM3	560	ON	OFF	ON	OFF	OFF	ON	12	OFF	ON	ON	ON	ON	OFF	ON	ON
DRUM4	570	ON	OFF	ON	ON	OFF	ON	16	OFF	ON	OFF	ON	ON	OFF	ON	ON
Versatec1	600	OFF	OFF	OFF	OFF	ON	OFF	4	ON	ON	OFF	ON	ON	ON	ON	ON
Core-to-Core	610	OFF	OFF	OFF	ON	ON	OFF	11	OFF	ON	ON	ON	OFF	ON	ON	ON
Big Disc 1	1540	ON	ON	OFF	OFF	OFF	ON	17	OFF	ON	OFF	ON	OFF	OFF	ON	ON
Big Disc 2	1550	ON	ON	OFF	ON	OFF	ON	20	ON	OFF	ON	ON	ON	ON	ON	ON
Versatec2	1600	OFF	ON	OFF	OFF	ON	OFF	14	OFF	ON	OFF	ON	ON	ON	ON	ON



BUS CONTROL CODING FOR 1185 CARD

Device numbers are selected by six switches in position 11B.
Ident codes are selected by eight switches in position 19A.
Core address registers are selected by four switches in position 7C.

DEVICE NUMBER		IDENT CODE		CORE ADDRESS REGISTER	
Bus addr.bil	Switch	Ident code bit.	Switch	Core addr.reg.bit.	Switch sw 7C
BA9	11B4	17	19A8	CA0	7C1
BA7	11B6	16	19A7	CA1	7C2
BA6	11B5	15	19A6	CA2	7C3
BA5	11B3	14	19A5	CA3	7C4
BA4	11B2	13	19A4		
BA3	11B1	12	19A3		
		11	19A2		
		10	19A1		

STANDARD SWITCH SETTING

DEVICE NAME	DEVICE NO.	SWITCH IN POS. 11 B 6	5	4	3	2	1	IDENT CODE	SWITCH IN POS. 19 A 8	7	6	5	4	3	2	1
DISC 1	500	OFF	ON	OFF	OFF	OFF	OFF	1	ON	ON	ON	ON	ON	ON	ON	OFF
DISC 2	510	OFF	ON	OFF	OFF	OFF	ON	5	ON	ON	ON	ON	ON	OFF	ON	OFF
M-T 1	520	OFF	ON	OFF	OFF	ON	OFF	3	ON	ON	ON	ON	ON	ON	OFF	OFF
M-T 2	530	OFF	ON	OFF	OFF	ON	ON	7	ON	ON	ON	ON	ON	OFF	OFF	OFF
DRUM 1	540	OFF	ON	OFF	ON	OFF	OFF	2	ON	ON	ON	ON	ON	ON	OFF	ON
DRUM 2	550	OFF	ON	OFF	ON	OFF	ON	6	ON	ON	ON	ON	ON	OFF	OFF	ON
VERSATEC 1	600	ON	OFF	OFF	OFF	OFF	OFF	4	ON	ON	ON	ON	ON	OFF	ON	ON
CORE-TO-CORE	610	ON	OFF	OFF	OFF	OFF	ON	11	ON	ON	ON	ON	OFF	ON	ON	OFF
BIG DISC 1	1540	OFF	ON	ON	ON	OFF	OFF	17	ON	ON	ON	ON	OFF	OFF	OFF	OFF
BIG DISC 2	1550	OFF	ON	ON	ON	OFF	ON	20	ON	ON	ON	OFF	ON	ON	ON	ON
VERSATEC	1600	ON	OFF	ON	OFF	OFF	OFF	14	ON	ON	ON	ON	OFF	OFF	ON	ON

6: Real Time Clocks (1024, 1210, 1166)

CLOCK AND PARITY 1210 - ND 014

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CLOCK SPESIFICATIONS

Hardware

The clock contains a crystal oscillator with an accuracy of about 1 sec/24 h. The interrupting frequency is set by straps on the card. The possible choices are:

RATE	STRAP POSITION	PERIOD
800 Hz	5D1	1,25 ms
400 Hz	5D2	2,5 ms
200 Hz	5D3	5 ms
100 Hz	5D4	10 ms
50 Hz	5D5	20 ms
10 Hz	5D6	100 ms

50 Hz is standard

Software

The clock responds to the device numbers 10-13 (gives connect) as the Real time clock 1024 (ND-015) does, but 10 = Clock read and 11 = Clock write are dummy.

Device number and ident code are fixed wired and cannot be changed.

Interrupt level = 13_{10}

Interrupt occurs if status bit 0 and status bit 3 = 1.

Ident code = 1

Read data = IOX 10

A-reg. is cleared, else "no operation".

Write data = IOX 11

Dummy command, "no operation".

Read status word = IOX 12

Bit 0 Interrupt enabled

	Set bit:	Control word bit 0 = 1
	Clear bit:	Control word bit 0 = 0
		Serviced IDENT PL 13
		Master clear

Bit 3 Ready for transfer, RFT.

	Set bit:	At the end of preselected time period
	Clear bit:	Master clear
		Control word bit 13 = 1

The remaining 14 bits are not assigned.

Write control word = IOX 13

Bit 0 Enable interrupt
Write bit 0 of A-reg. to interrupt enable FF.

Bit 13 Clear RFT if bit 13 of A-reg. is 1, else don't (= Masked clear)

The remaining 14 bits are unused.

Hence CLOCK 1210 (ND-014) is a subset of REAL TIME CLOCK 1024 (ND-015).

PARITY SPECIFICATIONS

The memory "Parity Generate and Check" is analogous to the NORD-10 option. (Ref. N-10 Inst. man. 5.4.11.)

The differences are that IOX instructions are required to manage the operation instead of TRA instructions.

Error interrupts trigger level 13 instead of 14.

Hardware

Memory cards with 18 bits of data storage are necessary. The two extra bits are used to store parity information thus:

Bit 16	=	1	if bits 0-7 has EVEN parity
Bit 16	=	0	if bits 0-7 has ODD parity
Bit 17	=	1	if bits 8-15 has EVEN parity
Bit 17	=	0	if bits 8-15 has ODD parity

Hence the total parity of the 18 bits word is EVEN.

When an 18 bits dataword is read from memory,error is recognized if the left and/or right byte has even parity. This may cause an interrupt on level 13.

The card may be placed in any I/O slot of NORD-12/42 and the two generated parity-bits are available on standard device terminals for connection to memory.

It is possible to investigate if the parity error occured during DMA transfer, instruction FETCH or instruction EXECUTION. The FETCH signal must then be fetched at 1207 card in position 7, pin 44 and connected to pin 57 on parity card.

Software

Interrupt level = $13_{\cancel{10}}$

Interrupt occurs if status bit 0 and status bit 6 = 1 (bit 6 = bit 4 + bit 5).

Ident code = 4 (Fixed wired)

Read error address IOX 4 (= TRA PEA)

The Parity Error Address, PEA,-register holds the last used memory address. Under normal condition it updates the address on each memory request. When a parity error occurs the content is trapped until it is read(cfr. Mousetraps; the trapped mouse must be removed before another can be caught).

Read status word IOX 6 (≈ TRA PES)

The status word is similiar to NORD-10 PES register and contains the following bit:

Bit 0 : IE - Interrupt enabled
Write bit 0 : Load control word bit 0
Clear bit 0 : Serviced IDENT PL 13+Master Clear

Bit 1 : N ot used

Bit 2 : F - Error occured during instruction fetch

Bit 3 : DMA - Error occured during DMA

Bit 4 : RB - Parity error in right byte (bits 0-7)

Bit 5 : LB - Parity error in left byte (bits 8-15)

Bit 6 : BLC - Parity error has occured. Content of address and status register is locked while this bit is set

Write bits 2-6: Sampled from the appropriate lines by Memory Data Ready if BLC = 0. Blocked if BLC = 1.

Clear bits 2-6: Master Clear
IOX 4 (Read PEA)
Control word bit 2 = 1

Write control word IOX 7

Bit 0 : Enabl e interrupt. Write bit 0 of A-register to interrupt enable FF.

Bit 2 : Activate.
Clear interrupt condition and prepare for next error detection.

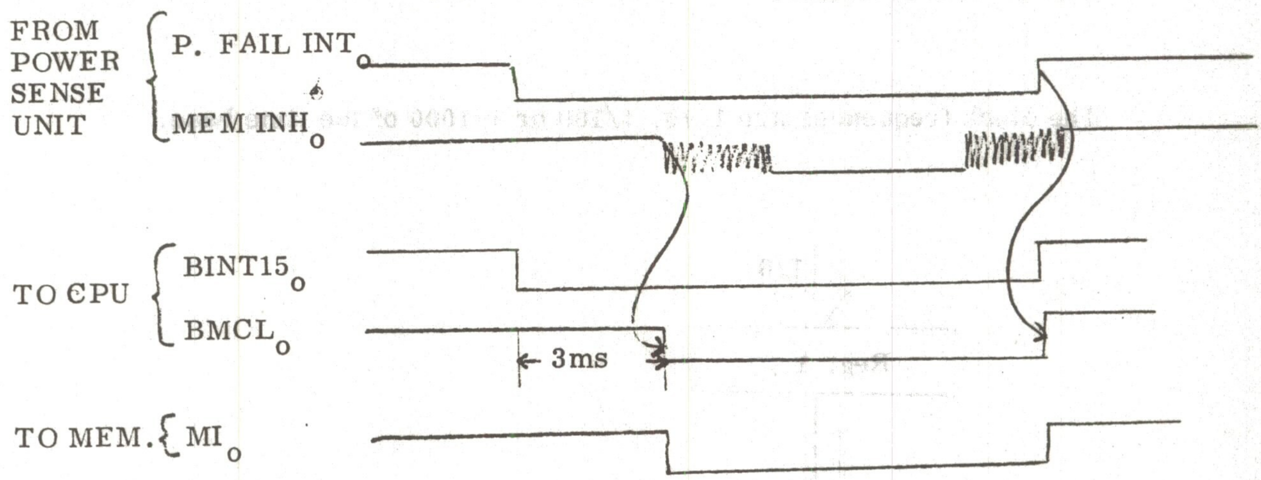
POWER FAIL SPECIFICATIONS

The card also contains the necessary circuitry to generate the control signals to shut down and restart the computer at power fail.

Hardware

On power fail an interrupt is generated on level 15.

3ms later Memory Inhibit and Master Clear is generated which lasts until power returns. 35mA of 5V stand by power from batteries is required.



SPECIFICATION OF THE REAL TIME CLOCK

Short description

The time base is an internal 10MHz crystal oscillator. An external time base may be used if wanted.

The clock frequences are 1/10, 1/100 or 1/1000 of the time base.

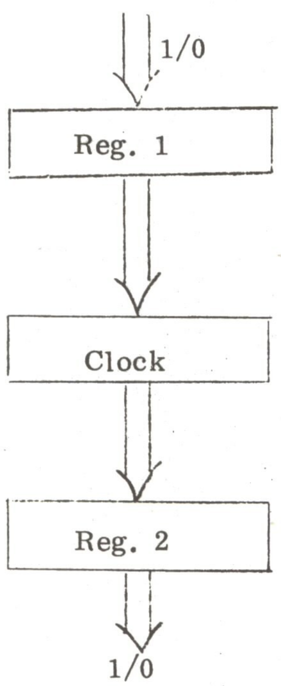


Figure 1

Reg. 1 is set by aIOX DEV NO + 1 (Write data) and gives no. of clock pulses between each interrupt.

Reg. 2 may be read at any time, and gives the value of the clock.

If reg. 1 is N then you read

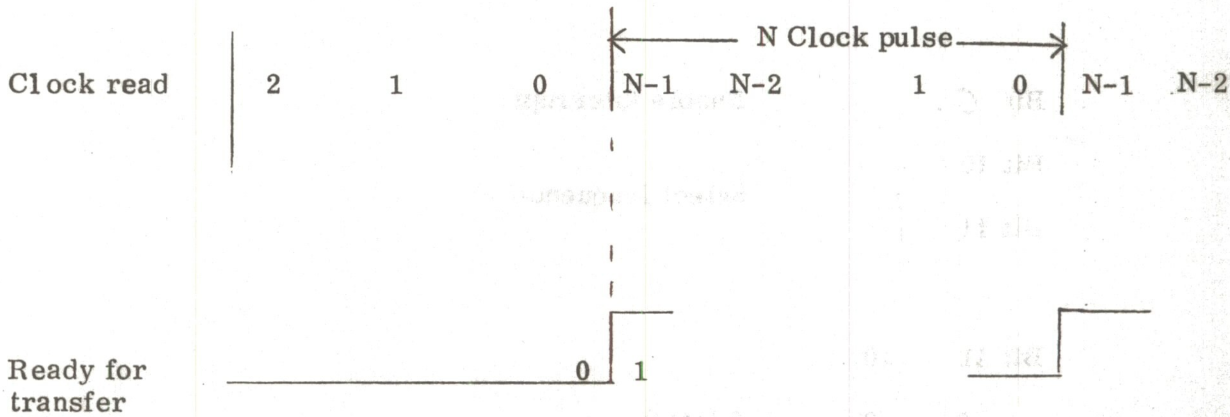


Figure 2

Each time the clock is zero, a pulse approx. 100n. sec. long is given from the device for external use.

An external signal "EXTERNAL HOLD" may give interrupt and lock reg. 2. This may be used to measure external signals.

Reading reg. 2, you get the time when the external signal arrived. However, the clock will continue to count, and you will not miss clock pulses.

When "Interrupt enable" is set to 1 and "Enable external hold" is set to 1, you have two sources for interrupt; either the clock "goes round" (have counted down to zero) or an external hold pulse have occured.

Data

Standard dev. no.	010 (010 - 013) oct.
No. of dev. no.	4
Standard int. level	13 des.
Standard ident no.	1

Write control word IOX DEV NO + 3

Bit 0	Enable interrupt
Bit 10, Bit 11	Select frequence

Bit 11	10	
0	0	0 (stop)
0	1	100 µsec (1/1000 of time base)
1	0	10 µsec (1/100 of time base)
1	1	1 µsec (1/10 of time base)

Bit 12	Enable external hold signal
Bit 13	If this bit is 1, "ready for transfer" is cleared.
Bit 14	If this bit is 1, the flip/flop "external hold signal occured" is cleared.
Bit 15	If this bit is 1, the clock starts counting. The clock is loaded with the content of the "reg. 1" after approx. 1 clock pulse.

Bits 1 to 9 are not used.

Read status word IOX DEV NO + 2

Bit 0 Interrupt enabled

Bit 2 External hold pulse has occured

Bit 3 Ready for transfer): the clock has sounted down to zero and starts again

Bits 1 and 4 to 15 are not used.

Write data IOX DEV NO + 1

Set the number of clock pulses between each interrupt. It is not necessary to set this register again after an interrupt.

Read data IOX DEV NO

Read the content of the clock. If an external hold pulse has occured, then you read the content of the clock at that time.

External signals

In to the interface

CLOCK IN used if external clock wanted.

EXTERNAL HOLD$_0$,if "Enable external hold" is set to 1, a negative pulse on this signal will set "External hold occured" to 1.

From the interface:

CLOCK OUT, the time base

PERIODE$_0$, an approx. 200 nsec negative pulse will come approx. 1 clock pulse before the device gives interrupt.

Hardware limitation

The interface uses standard tristate I.C. with a fan out of 10 and loads some data signals with 2 loads. The interface should not be used outside the CPU-rack without consideration.

PROGRAMABLE CLOCK 1166

4. PROGRAMMING SPECIFICATION

4.1. Device Number

Standard device number DN, is 10_8. Switch selectable from 0 to 70_8.

4.2. Interrupt Level = 13_{10}

Interrupt occurs if status bit 0=1 and statusbit 2 or 3 = 1.

4.3. Ident Code

Standard Ident Code is 1. Switch selectable from 1 to 17_8.

4.4. Read Clock/Time reg. = IOX DN

Returns the content of clock to A reg.

1) At the time of reading if statusbit 2=0.

2) Sampled at the time when the signal EXTERNAL HOLD arrived if statusbit 2=1.

4.5. Write Divisor Register = IOX DN+1

Load the division number N, of the clock. N is equivalent to the number of Time Units between each interrupt. Divisor and Time Unit is further described in 2.1.

4.6. Read Status Word = IOX DN+2

Bit 0 Interrupt enabled.

Set:	Control Word bit 0=1
Clear:	Control Word bit 0=0
	Serviced IDENT PL 13
	Master clear.

Bit 2 EXTERNAL HOLD signal has occured.

Set:	Control Word bit 12=1
	and EXTERNAL HOLD=1.
Clear:	Control Word bit 12=0
	Control Word bit 14=1
	Master clear.

Bit 3 Ready for transfer, RFT.

Set: At the $0 \rightarrow N-1$ transition of clock (see fig. 2.2.: Counting sequence).

Clear: Control Word bit 13=1
Master clear.

The remaining 13 bits are not assigned.

4.7. Load Control Word = IOX DN+3

Bit 0 Enable interrupt if bit=1.
Disable interrupt if bit=0.

Bit 10-11 Select time unit.
These bits define a number n, which is the number of time base periods in one time unit.

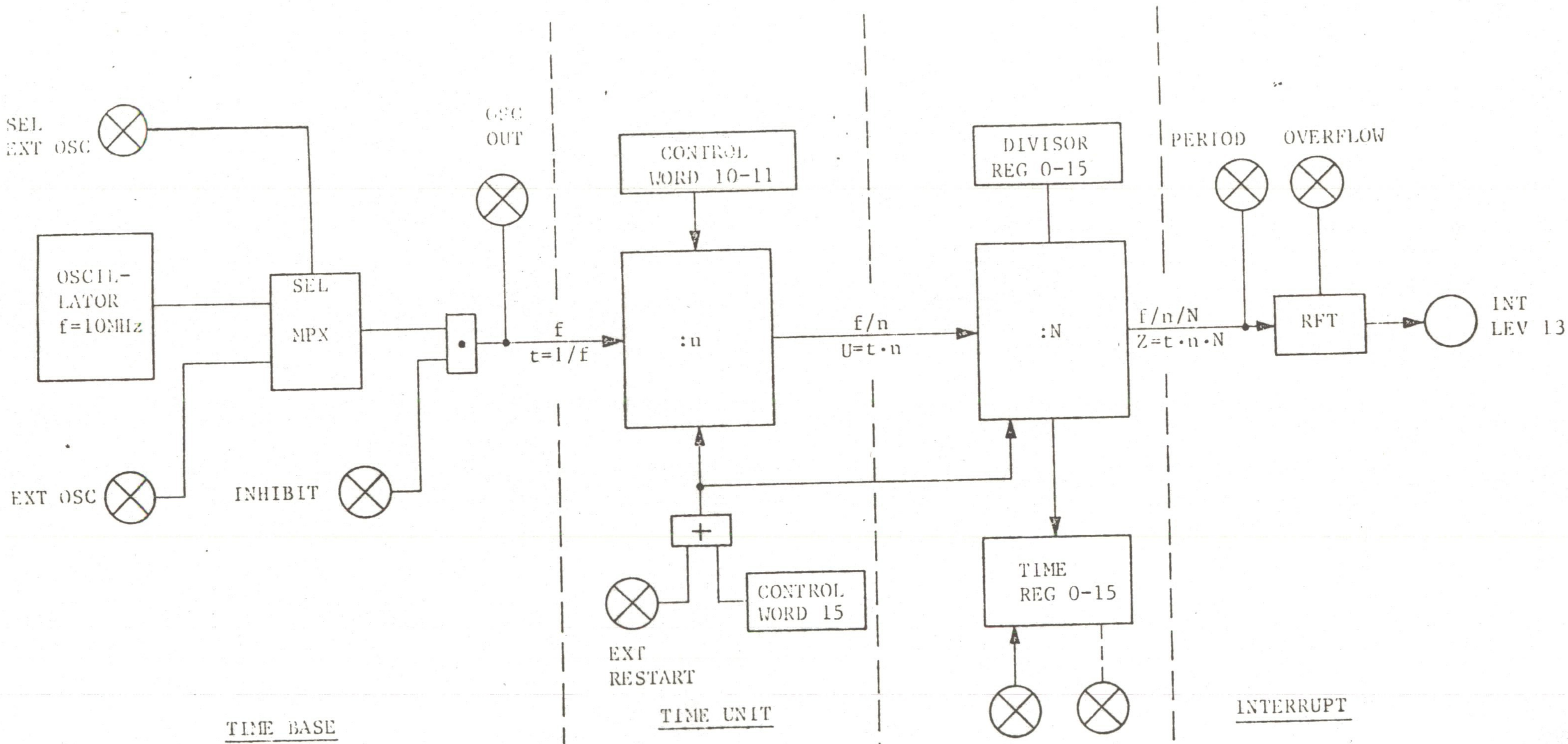
CONTROL BITS 11	10	SEL. EXT.	n	TIME UNIT U
0	0	0	∞	STOP
0	1	0	1000	100 µs
1	0	0	100	10 µs
1	1	0	10	1 µs
0	0	1	1	1 T
0	1	1	1000	1000 T
1	0	1	100	100 T
1	1	1	10	10 T

Bit 12 Enable external hold if bit=1.
Disable external hold if bit=0.

Bit 13 Clear RFT (statusbit 3) if bit=1.
Do nothing if bit=0.

Bit 14 Clear "External hold occur" (statusbit 2) if bit=1.
Do nothing if bit=0.

Bit 15 Restart the clock (preset to N-1) if bit=1.
Do nothing if bit=0.



CONTROL 11	10	SEL EXT	n
0	0	0	∞
0	1	0	1000
1	0	0	100
1	1	0	10
0	0	1	1
0	1	1	1000
1	0	1	100
1	1	1	10

7 MISCELLANEOUS

DIGITAL INPUT AND OUTPUT CODING

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1041 16 bit digital input

Switches for dev. no. are placed in 8B.
Switches for Ident no. are placed in 2C.

1042 16 bit digital output

Switches for dev. no. are placed in 10B.
Switches for Ident. no. are placed in 2C.

Dev. no.	Switch 8	7	6	5	4	3	2	1	Ident. no.
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0
4								ON	1
10							ON		2
20						ON			4
40					ON				10
100				ON					20
200			ON						40
400		ON							100
1000	ON								200
1774	ON	ON	ON	ON	ON	ON	ON	ON	377

SPECIFICATIONS

16 BIT INPUT 1041

16 BIT OUTPUT 1042

1 PROGRAMMING SPECIFICATION

16 bit digital input 1041

Standard device no.	
Standard interrupt level	12
No. of device no.	4
Standard ident no.	

IOX	DEVNO + 3	Load Control Word
IOX	DEVNO + 2	Read Status
IOX	DEVNO + 1	Not used
IOX	DEVNO + 0	Read Data

1.1 Load Control Word

IOX DEVNO + 3

Bit	0	Enable interrupt on ready for transfer
Bit	1	Enable interrupt on "error"
Bit	2	Active. Ready for next word
Bit	3	Not used
Bit	4	Device clear
Bit	7	One bit of information. This bit is sent to the other end, where it may do some useful things.

1.2 Read Status

IOX DEVNO + 2

Bit	0	Interrupt on ready for transfer enabled
Bit	1	Interrupt on error enabled
Bit	2	Not used
Bit	3	Ready for transfer. Data valid
Bit	4	Error. A sense line to the interface has been triggered. This bit is reset only by programmed clear or master clear.
Bit	5 - 15	Not used

1.3 Read Data Word

IOX DEVNO + 0

The 16 data lines are read directly into the A-register.

2 PROGRAMMING SPECIFICATION

16 bit digital output, 1042

Standard device no.	
Standard interrupt level	10
No of device no.	4
Standard Ident no.	

IOX	DEVNO + 3	Load Control Word
IOX	DEVNO + 2	Read Status Word
IOX	DEVNO + 1	Load Data Register
IOX	DEVNO + 0	Not used

2.1 Load Control Word

IOX DEV + 3

Bit	0	Enable interrupt on ready for transfer
Bit	1	Enable interrupt on "error"
Bit	2	Active. Buffer filled
Bit	3	Not used
Bit	4	Device clear
Bit	7	One bit of information. This bit is sent to the other end, where it may do some useful things.

2.2 Read Status Word

IOX DEV + 2

Bit	0	Interrupt on ready for transfer enabled
Bit	1	Interrupt on error enabled
Bit	2	Not used
Bit	3	Ready for transfer. Buffer ready for accepting next word.
Bit	4	Error. A sense line to the interface has been triggered. This bit is reset only by programmed clear or master clear.

2.3 Load Data Word

IOX DEV + 1

The output register is set by the content of the A-register.

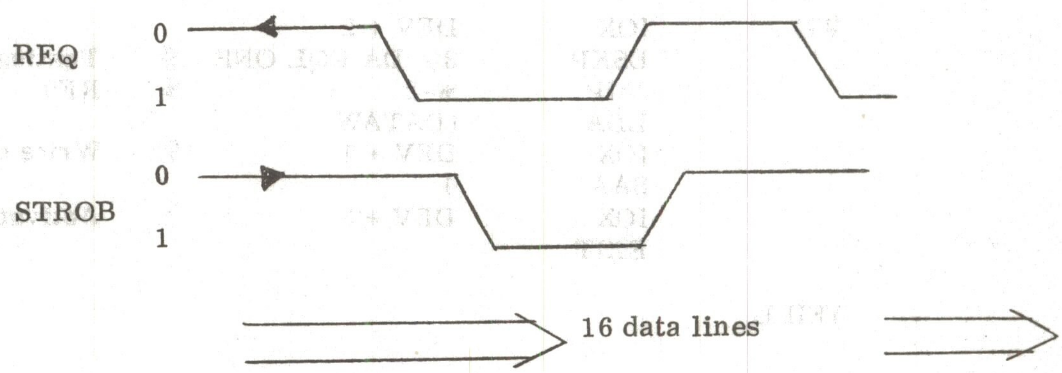
3 HARDWARE INFORMATION

3.1 Handshaking

The data transfer is controlled by two lines, one into and one out from the interfaces. These lines are controlled by the activating bit, bit 2 in the control word in the interfaces.

One line, REQ ("request" or "Ready for next data word"), is generated by the input part.

The other line, STROB ("strobe" or "Data on line valid"), is generated by the output part.



A "handshaking" technique is used. STROB must not be turned "on" before after REQ is "on" and off after REQ is turned off.

REQ must not be turned "on" before STROB is off and not turned off before STROB is on.

3.2 16 Bit Digital Input

After clear (Master Clear or programmed Clear) "REQ" is off and Ready for transfer ("RFT") is turned off.

Ready for transfer is turned on when STROB becomes one and off by activating. (Activating means requesting next data word.)

<u>Programming examples, without interrupt</u>

```
INIT    SAA     20
        IOX     DEV + 3          %    Clear
        SAA     4
        IOX     DEV + 3          %    Requesting first data word

RD      IOX     DEV + 2
        BSKP    30 DA  EQL  ONE
        JMP     * -2
        IOX     DEV
        STA     DATA
        SAA     4
        IOX     DEV + 3          %    Requesting next dataword
        EXIT
```

```
DATA        0
```

3.3 16 Bit Output Register

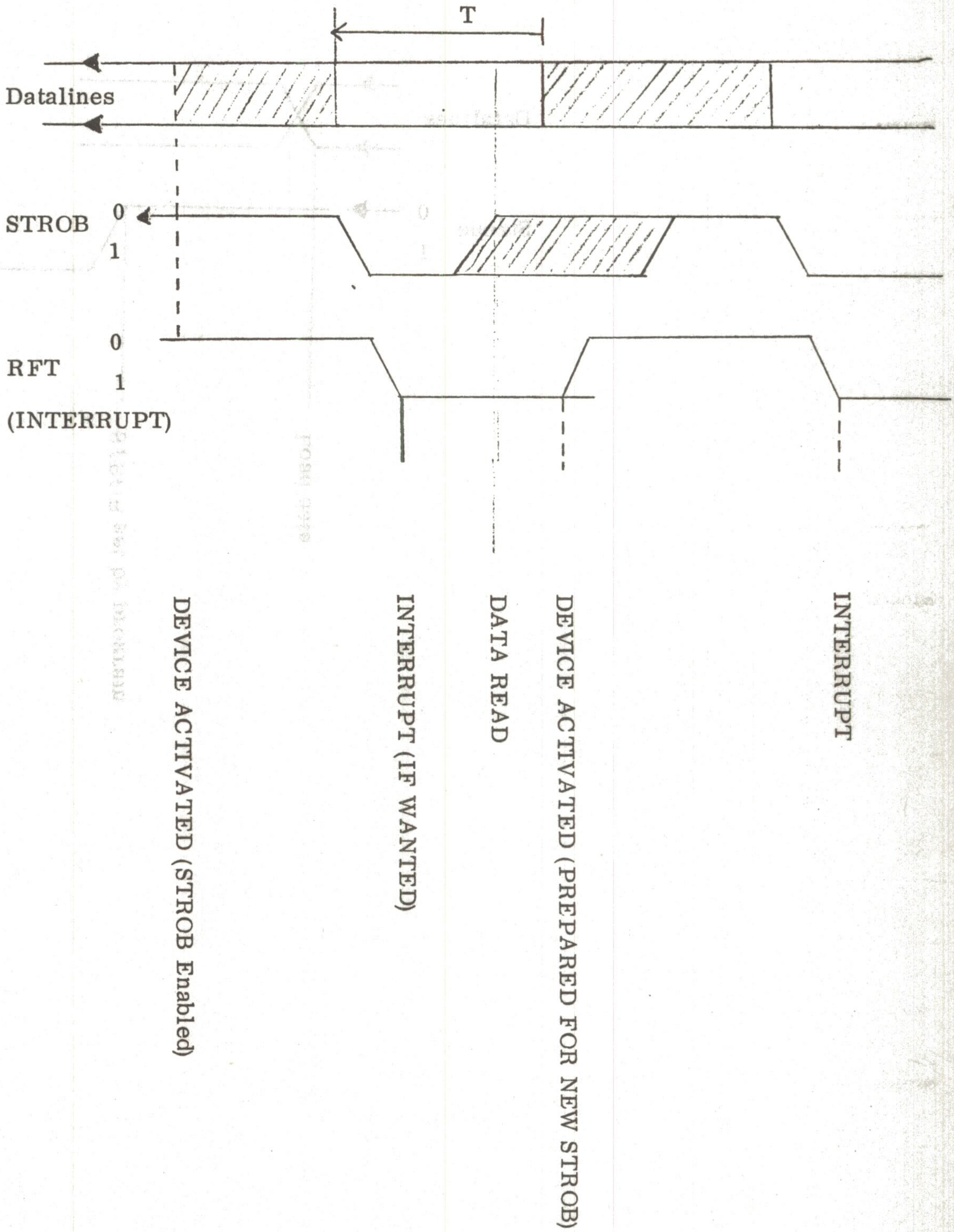
After clear (Master Clear or programmed Clear) "STROB" is off, and "Ready for transfer" is on.

Ready for transfer is turned off by activating the device, and on when STROB is turned off. (Activating means buffer contains valid data.)

Programming example, without interrupt

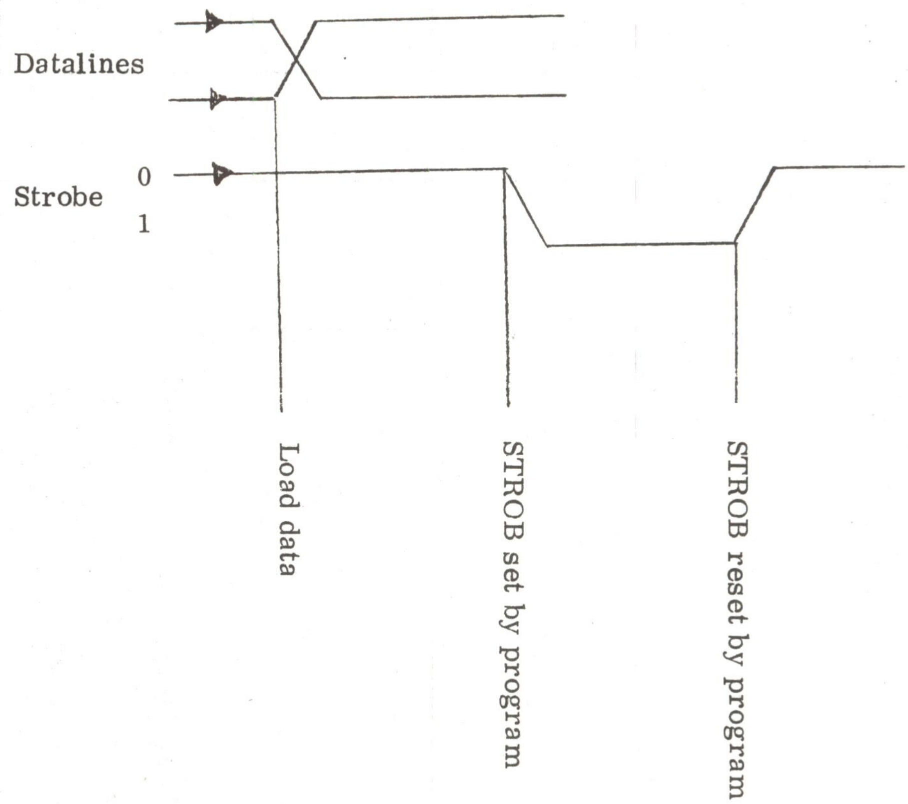
```
INIT    SAA     20
        IOX     DEV + 3          %   Programmed Master
        EXIT                     %   Clear

WD      IOX     DEV + 2
        BSKP    30 DA EQL ONE    %   Testing for
        JMP     *-2              %   RFT
        LDA     (DATAW
        IOX     DEV + 1          %   Write data to buffer
        SAA     4
        IOX     DEV + 3          %   Activating
        EXIT

)FILL
```

3.4 16 Bit Input, without Handshaking



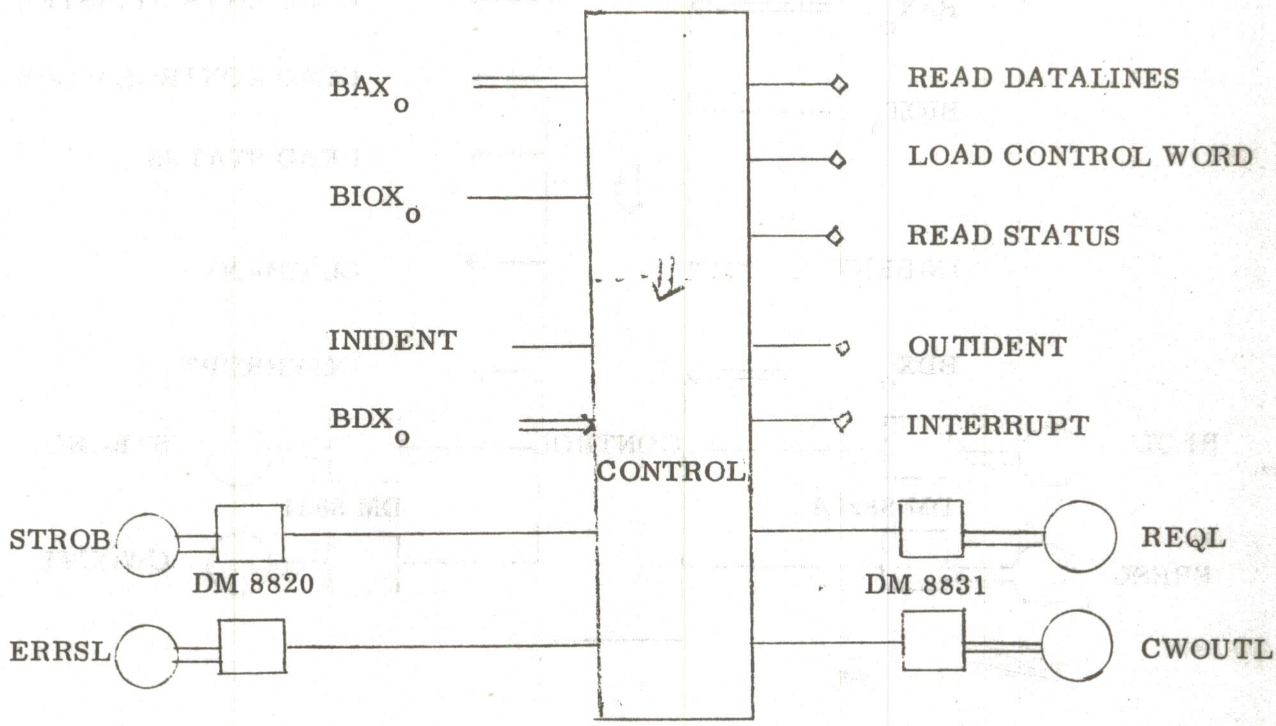
3.5 16 Bit Output, whithout Handshaking

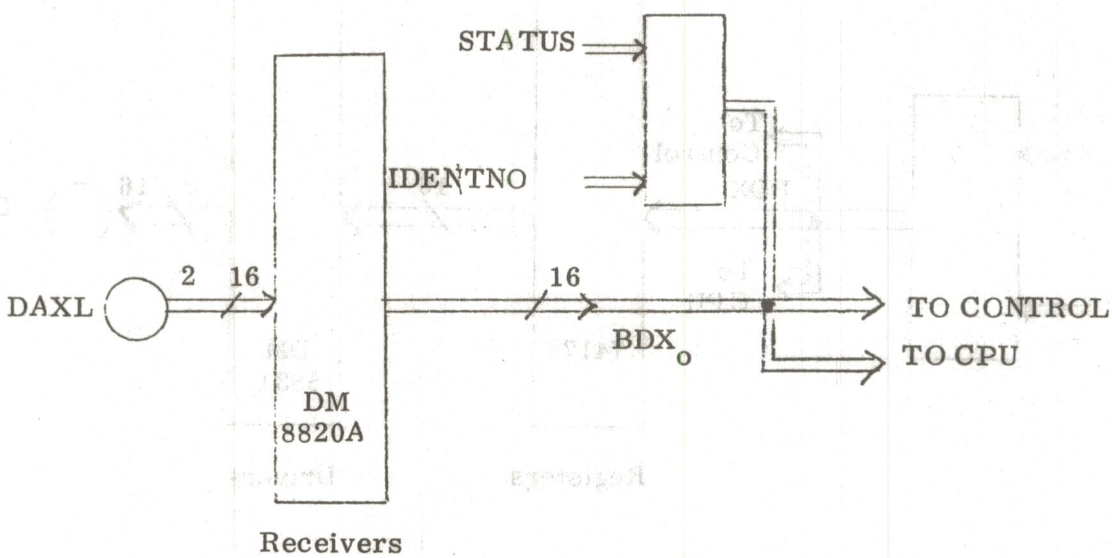
A strap on the card is required.



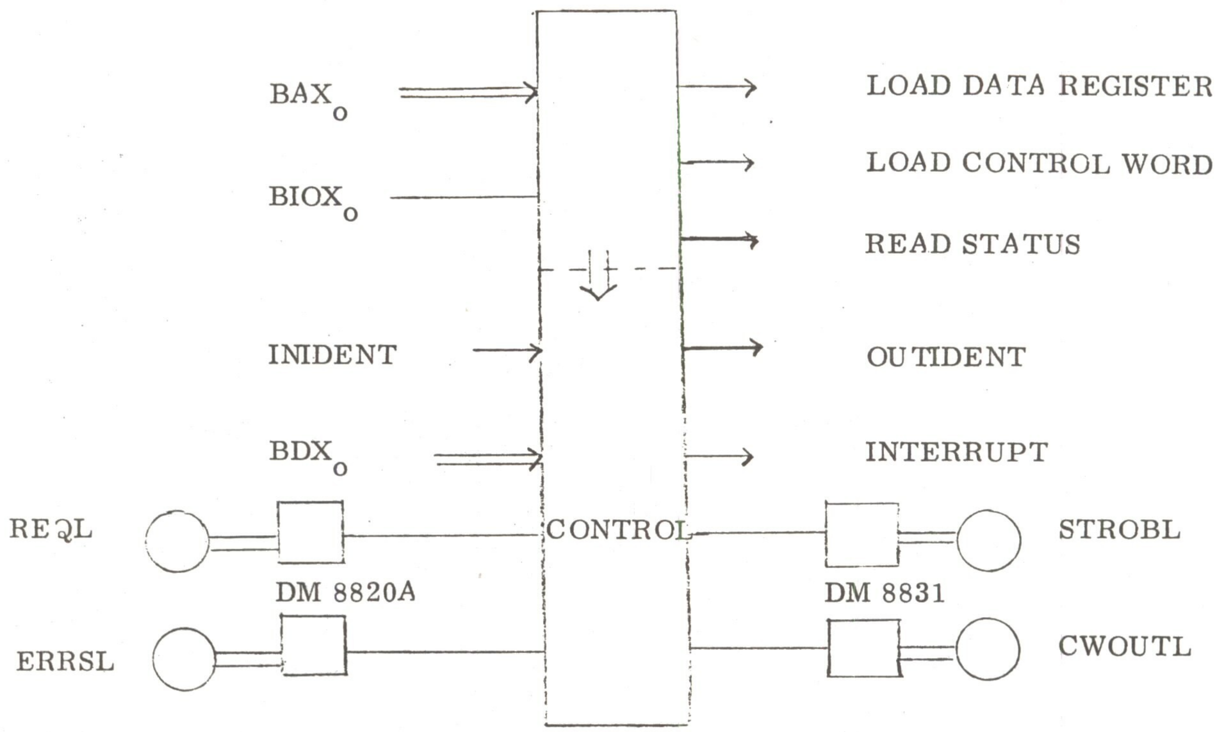
4 BLOCK DIAGRAM

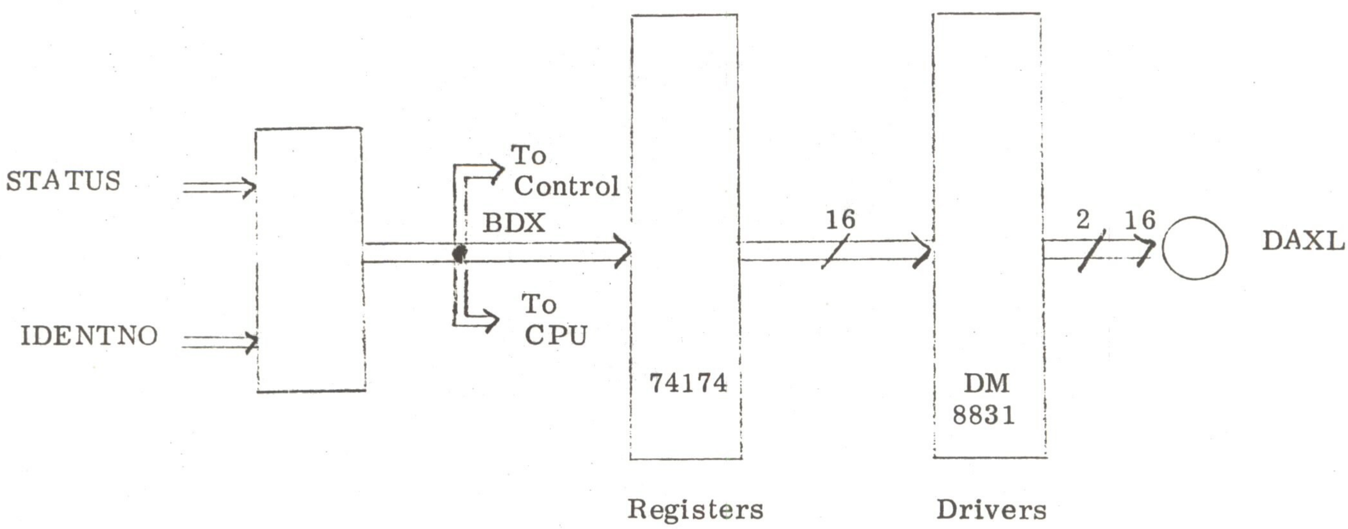
4.1 16 Bit Input





4.2 16 Bit Output





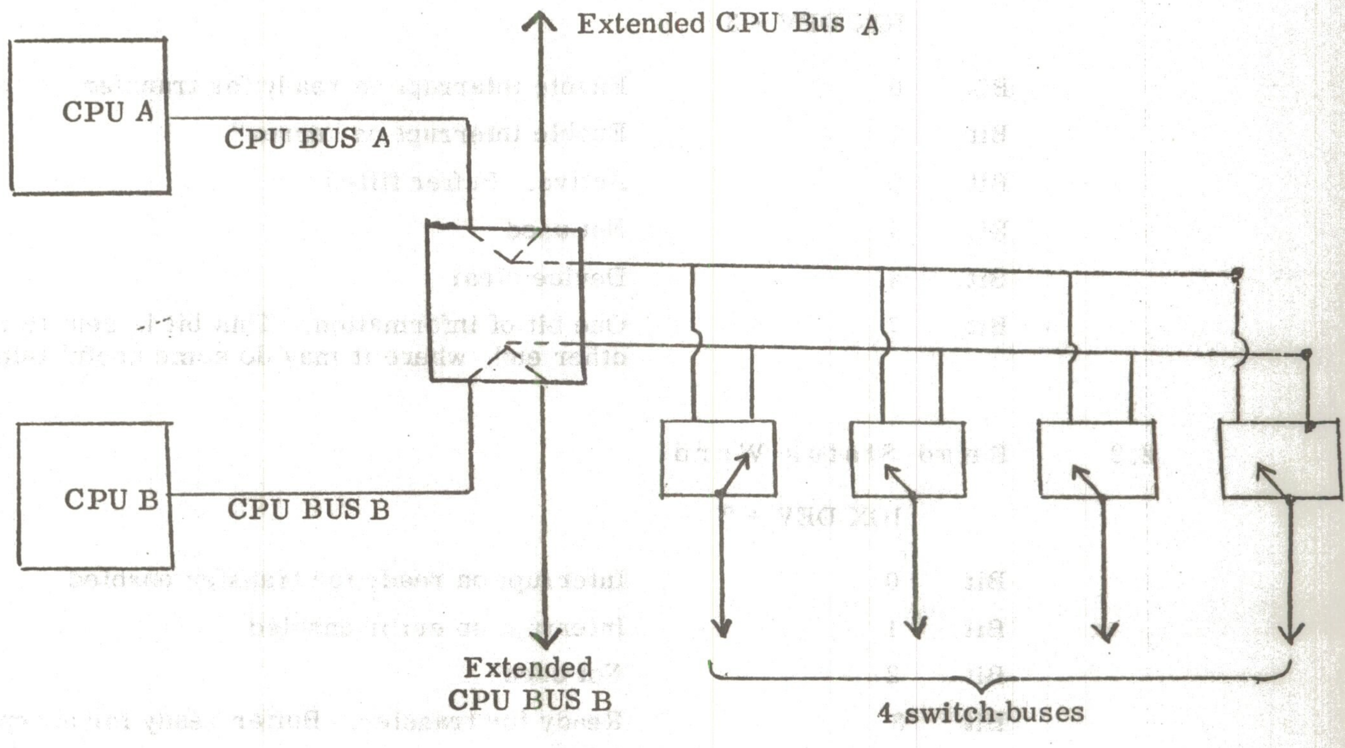
BUS-SWITCH

+‡+

It is often useful to transferè the control of peripheral devices from one CPU to another. A bus switch is designed for this purpose.

A bus switch is shown shematic in the following figure.

Bus-Switch



CPU BUS

Standard NORD-10 I/O bus from CPU or bus controller.

Extended CPU Bus

Standard NORD-10 I/O bus from the bus switch. This bus is a direct extention of a CPU bus and cannot be switched to the other CPU bus.

Switch-bus

Standard NORD-10 I/O bus from the bus-switch. It is possible to connect up to four switch-buses to one bus-switch. Each of the four buses may independently select one of the two CPU buses as source bus. The selection of source bus is controlled by an external signal, select signal. The select signal is usually given by a toggle-switch.

2 PROGRAMMING SPECIFICATION

16 bit digital output, 1042

Standard device no.	
Standard interrupt level	10
No of device no.	4
Standard Ident no.	

IOX	DEVNO + 3	Load Control Word
IOX	DEVNO + 2	Read Status Word
IOX	DEVNO + 1	Load Data Register
IOX	DEVNO + 0	Not used

2.1 Load Control Word

IOX DEV + 3

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on "error"
Bit 2	Active. Buffer filled
Bit 3	Not used
Bit 4	Device clear
Bit 7	One bit of information. This bit is sent to the other end, where it may do some useful things.

2.2 Read Status Word

IOX DEV + 2

Bit 0	Interrupt on ready for transfer enabled
Bit 1	Interrupt on error enabled
Bit 2	Not used
Bit 3	Ready for transfer. Buffer ready for accepting next word.
Bit 4	Error. A sense line to the interface has been triggered. This bit is reset only by programmed clear or master clear.

2.3 Load Data Word

IOX DEV + 1

The output register is set by the content of the A-register.

NORD-10 PAGED DMA CONTROLLER

1 BACKGROUND

While program adresses (virtual addresses) from the NORD-10 CPU may be mapped into physical addresses by a Paging System, the DMA channel uses physical addresses directly. Therefore, a DMA Controller which may break up one transfer into several pieces which go into separate pages in memory is needed. This function is obtained by replacing a single board, the Bus Control, in a DMA Controller which uses physical addresses.

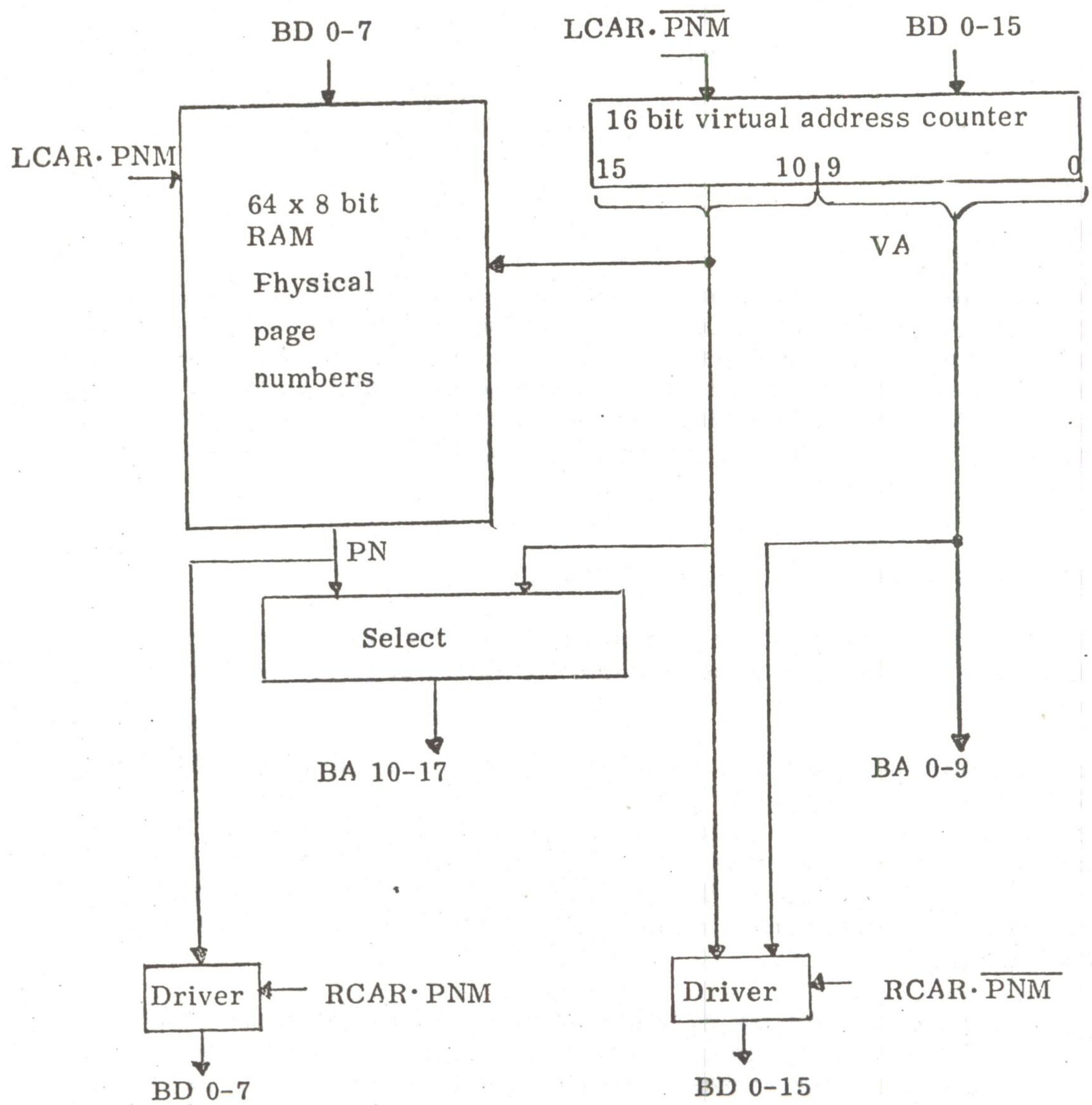
2 MEMORY ADDRESS REGISTER STRUCTURE

The least significant bits of the memory address register are held in a 10 bit counter, which gives displacement within a page of 1k words in memory.

The most significant 8 bits are contained in a device page table of 64 words by 8 bits, which holds physical page numbers PN. This page table is addressed by means of a 6 bit counter which is an extension of the 10 bit displacement counter. The full 16 bit counter thus holds the virtual address VA for the transfer. This technique causes no timing overhead for the DMA, since the virtual address is available well in advance of the DMA cycle.

NOTE 1: If the device page table has not been initialized after a Master Clear or programmed Clear (that is, page number mode has not been set, see section 3.1) the virtual address will be used as a 16 bit physical address directly, thus conforming to the requirements of the firmware mass storage loader.

NOTE 2: Physical page number 0 may not be specified, this page number is decoded as protect violation and will stop the transfer and set an error flag. This restriction is not serious, since part of the operating system resides permanently in page number 0.



3 PROGRAMMING SPECIFICATIONS

3.1 Load Control Word

The instruction

IOX <dev. no.> + 5

will have the same effect as previously described in individual device programming specifications, except for the use of Control Word bits 5 and 6. These bits previously contained physical address bits 16 and 17. In the Paged DMA Controller bit 5 is not used, while bit 6 of the Control Register is named PNM (page number mode) and controls loading and reading of the virtual address counter and the page table, see section 3.2 and 3.3. PNM is set to zero by Master Clear

3.2 Load Memory Address

The instruction

IOX <dev. no.> + 1

will cause either loading of the virtual address counter or loading of physical page number to the page table, depending on control word bit 6, PNM.

If PNM = 0, the virtual address counter will be loaded by the contents of accumulator bits 0-15.

If PNM = 1, one physical page number is entered into the page table. The page table address is taken from bits 10-15 of the virtual address counter, which subsequently is automatically augmented by 2000_8 (or 1024_{10}, i.e. the virtual page number is incremented by one).

3.3 Read Memory Address

The instruction

IOX <dev. no.>

will cause either reading of the virtual address counter or reading of physical page number from the page table, depending on control word bit 6, PNM.

If PNM = 0, the contents of the virtual address counter is read to the accumulator.

If PNM = 1, the physical page number pointed to by virtual address bits 10-15 is read to accumulator bits 0-7, without altering the content of the virtual address counter.

NOTE 3: If there was a page error (protect violation) during the transfer, this instruction will set accumulator bit 15 (if PNM = 1) in addition to setting Device Status Register bit 4 (Inclusive OR of errors).

4 PROGRAMMING SEQUENCE

The following sequence of operations is necessary to initialize the DMA memory addresses before a transfer:

a) Load Control Word with A register bit 6 = 0

b) Load Virtual Address Counter with virtual start address

c) Load Control Word with A register bit 6 = 1

d) Load the required number of Physical Page Numbers

e) Load Control Word with A register bit 6 = 0

f) Load Virtual Address Counter with virtual start address

Note that only the Virtual Address Counter needs initialization if the whole page table has been initialized and the corresponding pages are constantly resident in physical memory, thus reducing the described initialization sequence to step f). Also, since both Master Clear, programmed Clear of device, and step e) reset Control Word bit 6 (PNM), step a) is redundant.

PROGRAMMING SPECIFICATIONS OF BUS SWITCH CONTROL

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1 A control unit is designed to set the state of the Bus-Switch from a program. When this unit is used, the toggle switches on the Bus-Switch panel have to be set in the neutral position. Select signals from the panel override the select signals from the programmed control unit. The programming is identical from the two CPU's, CPU A and CPU B.

This unit is also a "watch dog" for the two CPU's. Both CPU's trig a circuit with an IOX instruction. Status of this circuit may be read from both CPU's. This status contains two bits, one for each CPU, which are set to 0 if the corresponding CPU has trigged the "watch dog" with too low frequence.

2 Two IOX instructions are used to program the Bus-Switch control unit.

2.1 Load Control Word

IOX DEVN + 3

Format of the control word:

Bit 0: Enable this CPU active. This bit is used to set a status bit (bit 0) which indicates that this CPU is active. Active means that the CPU trigging the "Watch-dog".

Bit 1: Disable active.

Bit 2: Activate, trig the watch dog. Activate has to be set at least once a second if status bit 1 should not be reset.

Bit 3: Not used.

Bit 4: Clear the bus switch control. Disable this CPU active. Set status bit 1 to 1.

Bit 5-10: Not used.

Bit 11: Connect switch BUS 1 to this CPU

Bit 12: Connect switch BUS 2 to this CPU

Bit 13: Connect switch BUS 3 to this CPU

Bit 14: Connect switch BUS 4 to this CPU

Bit 15: Not used.

2.2 Read Status Word

IOX DEVN + 2

Format of status word:

Bit 0: This CPU is active.

Bit 1: If 1 this CPU has trigged (activated) the watch dog with a legal frequence.

Bit 2: Same as bit 0, but for the other CPU.

Bit 3: Same as bit 1, but for the other CPU.

Bit 4-10: Not used.

Bit 11, 1: Switch BUS 1 connected to this CPU

Bit 12, 1: Switch BUS 2 connected to this CFU

Bit 13, 1: Switch BUS 3 connected to this CPU

Bit 14, 1: Switch BUS 4 connected to this CFU

Bit 15: Not used.

Note: The term "this CPU" means the CPU that executes the IOX instruction.

NORD-10 CAMAC CRATE CONTROLLER PROGRAMMING SPECIFICATION

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1 CAMAC ADDRESSES

The codes in chapters 2 to 8 are relevant for the crate with address 0. It is possible to have 16 crates on each NORD-10, with octal crate numbers from 0 to 17. The codes for any crate are found by adding $(C \cdot 100)_8$ to the codes given in chapters 2 to 8. The instruction format is

	IOX						Crate no. (4 bits)				Addr. (3 bits)			Function (3 bits)		
	1	1	1	0	1	1										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

The address field is used to address 7 registers or commands. They are:

0	Camac Z-cycle
1	Camac C-cycle
2	Data Register
3	NAF Register
4	Graded LAM status
5	Not used
6	Mask Register
7	Control and Status Register

The function bits are used to specify one of the following functions:

0	Read
1	Write
3	Clear all bits corresponding to 1 in A-register
5	Set all bits corresponding to 1 in A-register
7	Execute Dataway cycle

Not all functions are available on all addresses. The total address-function table is:

Address		Function: Read	Write	Masked clear	Masked set	Execute DTW-cycle
Z	0					7
C	1					7
Data	2	0	1			7
NAF	3	0	1			7
LAM	4	0				
Mask	6	0	1	3	5	
Cost	7	0	1	3	5	

2 CAMAC Z-CYCLE

IOX 2007

Generates a Camac Z-cycle. Clears NAF register, Data register and COST register except bits 0, 12 and 13 (I, C and Z) in the crate controller, and also clears the A-register in the computer. All LAM sources are cleared due to the Z-cycle, so Graded LAM register is 0. The Mask-register remain unchanged. Bits 0, 12 and 13 in COST register should be one after a Camac Z-cycle.

3 CAMAC C-CYCLE

IOX 2017

Generated a Camac C-cycle. Clears NAF register and Data register in the controller, and also clears the A-register in the computer. Bit 12 in COST register should be one after a Camac C-cycle.

4 DATA REGISTER

The Data register is a 16 bits register.

4.1 Read Data Register

IOX 2020

Reads the content of the Data register into A-register in computer.

4.2 Write Data Register

IOX 2021

Writes the content of the A-register into the Data register.

4.3 Execute Data

IOX 2027

This instruction is split into three parts, dependent on the content of the NAF register at the moment the instruction is executed.

a) If the NAF code function bits indicates a read function, a dataway cycle is executed and the value of the Camac bus read lines (16 bits) are read into Data register and also into A-register.

b) If the NAF code function bits indicates a write function, the content of the A-register is written into the Data register, and then enabled to the Camac bus write lines during the dataway cycle.

c) If the NAF code function bits indicates a control function, the content of the A-register is written into the Data register, but the Data register is not used or changed during the control function dataway cycle.

5 NAF REGISTER

The NAF register is a 16 bits register, and the bits are:

Bit		
	0	F (1)
	1	F (2)
	2	F (4)
	3	F (8)
	4	F (16)
	5	A (1)
	6	A (2)
	7	A (4)
	8	A (8)
	9	N (1)
	10	N (2)
	11	N (4)
	12	N (8)
	13	N (16)
	14	X error enable
	15	Q error enable

5.1 Read NAF Register

IOX 2030

Reads the B content of the NAF register into A-register.

5.2 Write NAF Register

IOX 2031

Writes the content of the A-register into the NAF register.

5.3 Execute NAF

IOX 2037

Writes the content of the A-register into the NAF register. Then a dataway cycle is executed, which may be either a read-, write- or control-cycle. If it is a read cycle, the value of the Camac bus read-lines are read into the Data register and A-register. If it is a write cycle, the content of the Data Register is enabled out on the Camac bus write-lines.

6 READ GRADED LAM STATUS

IOX 2040

Reads the value of the graded LAM into the A-register (16 bits).

7 MASK REGISTER

The Mask register is used, bit by bit, to enable the graded LAM to the interrupt handling logic. It is a 16 bits register.

7.1 Read Mask Register

IOX 2060

Reads the content of the Mask register into the A-register.

7.2 Write Mask Register

IOX 2061

Writes the content of the A-register into the Mask register.

7.3 Masked Clear Mask Register

IOX 2063

All bits in the A-register which are one will clear the corresponding bits in the Mask Register.

7.4 Masked Set Mask Register

IOX 2065

All bits in the A-register which are one will set the corresponding bits in the Mask register.

8 CONTROL AND STATUS REGISTER (COST REGISTER)

The COST register is a 16 bits register. All bits are readable. All bits but bit 9 are writeable, and can also be separately cleared or set by masked clear and masked set instruction. Bits 12, 13, 14 and 15 are dataway status bits, and therefore clocked at S1 in a programmed dataway cycle. The control and status bits are:

Bit			
	0	I (Inhibit-line)	C and S separate
	1	DMA enable	C and S same
	2	Continuous DMA enable	C and S same
	3	L-demand enable	C and S same
	4	Error enable	C and S same
	5	RT enable	C and S same
	6	Interrupt level 10 select	C and S same
	7	Interrupt level 11 select	C and S same
	8	Interrupt level 12 select	C and S same
	9	LAM demand	Status
	10	Error demand	Status
	11	RT demand	Status
	12	C status	Status
	13	Z status	Status
	14	X response	Status
	15	Q response	Status

Comments: Bit 0 is a control and status bit. The status bit is the OR function of the last written (set or cleared) value of the control bit and an external inhibit line. (Lemo socket on front).

Bit 1 is used to enable (1) or block (0) DMA request to memory.

Bit 2 defines block mode (1) or interleaved mode (0) of DMA.

Bit 3 is the interrupt enable flip-flop for Look-at-me-interrupts. The Graded LMA-lines are OR-ed together to a demand, and bit 3, if one, enables this demand to the level specified by bits 6, 7 and 8. (This bit is NOT cleared by IDENT. Instead the bit in the Mask register corresponding to the returned ident code is cleared.)

Bit 4 enables error interrupt to level 13. Error means expected Q and/or X response missing. This bit is cleared by IDENT when the interrupt is serviced.

Bit 5 enables external Real Time interrupt to level 13. (Lemo socket on front.) This bit is also cleared by IDENT when the interrupt is serviced.

Bit 6 selects interrupt level 10 for LAM demands.

Bit 7 selects interrupt level 11 for LAM demands.

Bit 8 selects interrupt level 12 for LAM demands.

Bit 9 is the OR function of masked Graded LAM.

Bit 10 is the OR function of expected and missing Q and X response.

Bit 11 is the latched external Real Time demand.

Bit 12 holds the status of the Camac bus C line during the last dataway cycle. (NB! also writeable).

Bit 13 holds the status of the Camac bus Z line during the last dataway cycle. (NB! also writeable.)

Bit 14 holds the X-response of the last dataway cycle. (NB! also writeable.)

Bit 15 holds the Q-response of the last dataway cycle. (NB! also writeable.)

8.1 Read COST Register

IOX 2070

Reads the content of the COST register into the A-register.

8.2 Write COST Register

IOX 2071

Writes the content of the A-register, except bit 9, into the COST register.

8.3 Masked Clear COST Register

IOX 2073

All bits in the A-register which are one, except eventually bit 9, will clear the corresponding bits in the COST register.

8.4 Masked Set COST Register

IOX 2075

All bits in the A-register which are one, except eventually bit 9, will set the corresponding bits in the COST register.

9 IDENT

The serviced IDENT will clear the Mask register bit corresponding to the Graded LAM bit that generated the interrupt on level 10, 11 or 12. The format of the ident vector read into the A-register is:

Bit		
0	(1)	Coded Graded LAM level. (One of sixteen.)
1	(2)	
2	(4)	
3	(8)	
4–7		Crate number (one of sixteen)
8		Always 1, indicating Camac

If more than one LAM source are requesting (on different levels) at the time the IDENT instruction is executed, the one with the highest number is serviced.

Serviced IDENT on level 13 gives one in bit 8, indicating Camac, the Crate number field is the same as for LAM interrupts, and bits 0, 1, 2 and 3 are zero.

Serviced IDENT on level 13 clears the enable flip-flop (COST 4 or/and 5) for the interrupting source. (COST 10 or/and 11.)

SPECIFICATIONS
FOR
DMA ADDRESS EXTENDER
(Board 1153)

INTRODUCTION

For large memory systems, it will be necessary to extend the address space for DMA channels above 256K (18 bits).

This is possible by installing a board (1153 - DMA ADDRESS EXTENDER ND167) in position 9 of the appropriate rack. The address space is hereby increased up to 16 Mwords (24 bits). However, only 2 Mwords (21 bits) are implemented in existing equipment (781031). The address extender will operate with any DMA controller using the MPX address facility in a Bus Memory Brancher.

To utilize this board, both hardware and software considerations are necessary.

Note: With the DMA ADDRESS EXTENDER in use, a DMA transfer may cross a 64K boundary.

PROGRAMMING SPECIFICATIONS

The extended address part (bit 16-23) must be loaded by program, but cannot be read. It is loaded by two consecutive IOX LCAR instructions. The first instruction loads the 8 most significant bits (16-23) to the DMA EXTENDER, while the second instruction loads the 16 least significant bits. This part of the address may be read as before.

Example:

```
LDA  MOST
IOX  LCAR
LDA  LEAST
IOX  LCAR
```

Note: With DMA ADDRESS EXTENDER installed, the most significant part must be loaded first!!

The two address bits 16 and 17, which are normally loaded by control word bit 5 and 6 are ignored when the DMA ADDRESS EXTENDER is operating. It is, however, possible to run old systems, even if this board is installed, by disabling the address extension. This is done by a switch located on the board. This switch selects bit 16 and 17 from controlword on to the memory address cable. A LED on the board will indicate that the address extension is disabled.

HARDWARE MODIFICATIONS

Ref. ECO 522-524.

1096

Connect 9D14-:5 $AC16_0$

Backwiring

Connect 7:49-9:57 $MPMRQ_0$

Connect 7:53-9:61 $MPMWR_0$

Connect 7:07-9:72 WE_0

Connect 1:05-9:70 $AC16_0$

Cable type: DAxxx (Ref. FLAT CABLE DEFINITIONS FOR NORD MEMORY SYSTEM)

A/S NORSK DATA-ELEKTRONIKK	Title: 1096 DMA ADDRESS	Drawing no.: B01

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V			50		BA14	0	
01		+5V			51		MPMWR	0	
02		GROUND			52		BA15	0	
03		GROUND			53		BA16	0	
04		WE	0		54		BA17	0	
05	G	AC16	0		55				
06		ELD	0		56	G	MRQ	1	
07					57	G	MRQ	0	
08		BGRANT	0		58	G	MWR	1	
09					59	G	MWR	0	
10	T	LD0	0		60	G	MA16	1	
11					61	G	MA16	0	
12	T	LD1	0		62	G	MA17	1	
13	T	LD2	0		63	G	MA17	0	
14	T	LD3	0		64	G	MA0	1	
15					65	G	MA0	0	
16	T	LD4	0		66	G	MA1	1	
17	T	LD5	0		67	G	MA1	0	
18	T	LD6	0		68	G	MA2	1	
19					69	G	MA2	0	
20	T	LD7	0		70	G	MA3	1	
21	T	LD8	0		71	G	MA3	0	MEMORY
22	T	LD9	0		72	G	MA4	1	ADDRESS
23					73	G	MA4	0	CABLE
24	T	LD10	0		74	G	MA5	1	
25	T	LD11	0		75	G	MA5	0	
26	T	LD12	0		76	G	MA6	1	
27					77	G	MA6	0	
28	T	LD13	0		78	G	MA7	1	
29	T	LD14	0		79	G	MA7	0	
30	T	LD15	0		80	G	MA8	1	
31					81	G	MA8	0	
32		BA0	0		82	G	MA9	1	
33		BA1	0		83	G	MA9	0	
34		BA2	0		84	G	MA10	1	
35					85	G	MA10	0	
36		BA3	0		86	G	MA11	1	
37		BA4	0		87	G	MA11	0	
38		BA5	0		88	G	MA12	1	
39		SMPX	0		89	G	MA12	0	
40		BA6	0		90	G	MA13	1	
41		BA7	0		91	G	MA13	0	
42		BA8	0		92	G	MA14	1	
43	G	MPX	0		93	G	MA14	0	
44		BA9	0		94	G	MA15	1	
45		BA10	0		95	G	MA15	0	
46		BA11	0		96		GROUND		
47		MPMRQ	0		97		GROUND		
48		BA12	0		98		+5V		
49		BA13	0		99		+5V		

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	G = OUTPUT	Replaced by	Date
DATE	T = THREE-STATE		

A/S NORSK DATA-ELEKTRONIKK	Title: 1093 BRANCH TRANSCEIVER (BRANCH ADDRESS)	Drawing no. B02

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	
00		+5V			
01		+5V			
02		GROUND			
03		GROUND			
04					
05					
06					
07		R1	0		
08					
09		R0	0		
10	T	LD0	0		
11		SLD	0		
12	T	LD1	0		
13	T	LD2	0		
14	T	LD3	0		
15	G	APR	0		
16	T	LD4	0		
17	T	LD5	0		
18	T	LD6	0		
19		EMA	0		
20	T	LD7	0		
21	T	LD8	0		
22	T	LD9	0		
23		EBA	0		
24	T	LD10	0		
25	T	LD11	0		
26	T	LD12	0		
27					
28	T	LD13	0		
29	T	LD14	0		
30	T	LD15	0		
31					
32	T	BA0	0		
33	T	BA1	0		
34	T	BA2	0		
35					
36	T	BA3	0		
37	T	BA4	0		
38	T	BA5	0		
39					
40	T	BA6	0		
41	T	BA7	0		
42	T	BA8	0		
43					
44	T	BA9	0		
45	T	BA10	0		
46		BA11	0		
47					
48		BA12	0		
49		BA13	0		
50		BA14	0		
51					
52		BA15	0		
53		BA16	0		
54		BA17	0		
55		GND1			
56					
57					
58					
59					
60	T	MBA16	1	MAIN I/O BUS CABLE IN (terminals 60–95)	
61	T	MBA16	0		
62	T	MBA17	1		
63	T	MBA17	0		
64	T	MBA0	1		
65	T	MBA0	0		
66	T	MBA1	1		
67	T	MBA1	0		
68	T	MBA2	1		
69	T	MBA2	0		
70	T	MBA3	1		
71	T	MBA3	0		
72	T	MBA4	1		
73	T	MBA4	0		
74	T	MBA5	1		
75	T	MBA5	0		
76	T	MBA6	1		
77	T	MBA6	0		
78	T	MBA7	1		
79	T	MBA7	0		
80	T	MBA8	1		
81	T	MBA8	0		
82	T	MBA9	1		
83	T	MBA9	0		
84	T	MBA10	1		
85	T	MBA10	0		
86	T	MBA11	1		
87	T	MBA11	0		
88	T	MBA12	1		
89	T	MBA12	0		
90	T	MBA13	1		
91	T	MBA13	0		
92	T	MBA14	1		
93	T	MBA14	0		
94	T	MBA15	1		
95	T	MBA15	0		
96		GROUND			
97		GROUND			
98		+5V			
99		+5V			

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	G = OUTPUT T = THREE-STATE	Replaced by	Date
DATE			

A/S NORSK DATA-ELEKTRONIKK

Title: TERMINATION PLUG OR EXTENDED ADDRESS PLUG

Drawing no. B03

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V			50	N	MPMWR	0	
01		+5V			51	N	MPMWR	0	
02		GROUND			52				
03		GROUND			53				
04					54	N	GND1		
05					55	N	GND1		
06					56				
07					57				
08					58				
09					59				
10					60		MBA16	1	
11					61		MBA16	0	
12					62		MBA17	1	
13					63		MBA17	0	
14	N	LD3	0		64		MBA0	1	
15	N	LD3	0		65		MBA0	0	
16					66		MBA1	1	
17					67		MBA1	0	
18					68		MBA2	1	
19					69		MBA2	0	
20					70		MBA3	1	
21					71		MBA3	0	
22					72		MBA4	1	MAIN I/O
23					73		MBA4	0	BUS
24					74		MBA5	1	EXTENSION
25	N	LD9	0		75		MBA5	0	PLUG
26					76		MBA6	1	OR
27					77		MBA6	0	TERMINATION
28					78		MBA7	1	PLUG
29					79		MBA7	0	
30	N	LD11	0		80		MBA8	1	
31					81		MBA8	0	
32					82		MBA9	1	
33	N	R1	0		83		MBA9	0	
34					84		MBA10	1	
35					85		MBA10	0	
36					86		MBA11	1	
37	N	LD14	0		87		MBA11	0	
38	N	SMPX	0		88		MBA12	1	
39	N	SMPX	0		89		MBA12	0	
40	N	R1	0		90		MBA13	1	
41	N	LD15	0		91		MBA13	0	
42	N	MPX	0		92		MBA14	1	
43	N	MPX	0		93		MBA14	0	
44					94		MBA15	1	
45					95		MBA15	0	
46	N	MPMRQ	0		96		GROUND		
47	N	MPMRQ	0		97		GROUND		
48					98		+5V		
49					99		+5V		

DRAWN BY	Remarks	Replacement for / Date
APPROVED BY	N = NOT USED	Replaced by / Date
DATE		

A/S NORSK DATA-ELEKTRONIKK	Title: TERMINATION PLUG OR EXTENDED DATA PLUG	Drawing no. B04

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS		TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	
00		+5V				50	N	MPMWR	0		
01		+5V				51	N	MPMWR	0		
02		GROUND				52					
03		GROUND				53					
04						54	N	GND1			
05						55	N	GND1			
06						56					
07						57					
08						58					
09						59					
10						60					
11						61					
12						62					
13						63					
14						64		MBD0	1		
15						65		MBD0	0		
16						66		MBD1	1		
17						67		MBD1	0		
18						68		MBD2	1		
19	N	LD4	0			69		MBD2	0		
20						70		MBD3	1		
21	N	LD5	0			71		MBD3	0		
22						72		MBD4	1		
23						73		MBD4	0	MAIN	
24						74		MBD5	1	I/O BUS	
25						75		MBD5	0	EXTENSION	
26						76		MBD6	1	PLUG	
27	N	LD6	0			77		MBD6	0	OR	
28						78		MBD7	1	TERMINATION	
29	N	LD7	0			79		MBD7	0	PLUG	
30						80		MBD8	1		
31						81		MBD8	0		
32						82		MBD9	1		
33						83		MBD9	0		
34	N	LD6	0			84		MBD10	1		
35						85		MBD10	0		
36	N	LD7	0			86		MBD11	1		
37						87		MBD11	0		
38	N	SMPX	0			88		MBD12	1		
39	N	SMPX	0			89		MBD12	0		
40	N	LD9	0			90		MBD13	1		
41						91		MBD13	0		
42	N	MPX	0			92		MBD14	1		
43	N	MPX	0			93		MBD14	0		
44						94		MBD15	1		
45						95		MBD15	0		
46	N	MPMRQ	0			96		GROUND			
47	N	MPMRQ	0			97		GROUND			
48	N	LD14	0			98		+5V			
49						99		+5V			

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	N = NOT USED	Replaced by	Date
DATE			

A/S NORSK DATA-ELEKTRONIKK	Title: 1093 BRANCH TRANSCEIVER (BRANCH DATA)	Drawing no. B05

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V			50	T	LD14	0	
01		+5V			51	N	MPMWR	0	
02		GROUND			52	T	LD15	0	
03		GROUND			53				
04					54				
05					55		GND1		
06					56				
07					57				
08					58				
09					59				
10	T	BD0	0		60				
11		SBD	0		61				
12	T	BD1	0		62				
13	T	BD2	0		63				
14	T	BD3	0		64	T	MBD0	1	
15	G	DPR	0		65	T	MBD0	0	
16	T	BD4	0		66	T	MBD1	1	
17	T	BD5	0		67	T	MBD1	0	
18	T	BD6	0		68	T	MBD2	1	
19		EMD	0		69	T	MBD2	0	
20	T	BD7	0		70	T	MBD3	1	
21	T	BD8	0		71	T	MBD3	0	
22	T	BD9	0		72	T	MBD4	1	
23		DLDA	0		73	T	MBD4	0	
24	T	BD10	0		74	T	MBD5	1	
25	T	BD11	0		75	T	MBD5	0	MAIN
26	T	BD12	0		76	T	MBD6	1	I/O BUS
27		EBD	0		77	T	MBD6	0	CABLE
28	T	BD13	0		78	T	MBD7	1	IN
29	T	BD14	0		79	T	MBD7	0	
30	T	BD15	0		80	T	MBD8	1	
31					81	T	MBD8	0	
32	T	LD0	0		82	T	MBD9	1	
33	T	LD1	0		83	T	MBD9	0	
34	T	LD2	0		84	T	MBD10	1	
35		DLDB	0		85	T	MBD10	0	
36	T	LD3	0		86	T	MBD11	1	
37	T	LD4	0		87	T	MBD11	0	
38	T	LD5	0		88	T	MBD12	1	
39	N	SMPX	0		89	T	MBD12	0	
40	T	LD6	0		90	T	MBD13	1	
41	T	LD7	0		91	T	MBD13	0	
42	T	LD8	0		92	T	MBD14	1	
43	N	MPX	0		93	T	MBD14	0	
44	T	LD9	0		94	T	MBD15	1	
45	T	LD10	0		95	T	MBD15	0	
46	T	LD11	0		96		GROUND		
47	N	MPMRQ	0		97		GROUND		
48	T	LD12	0		98		+5V		
49	T	LD13	0		99		+5V		

DRAWN BY BS/bbo.	Remarks	Replacement for	Date
APPROVED BY	G = OUTPUT T = THREE-STATE N = NOT USED	Replaced by	Date
DATE 23.9.75.			

A/S NORSK DATA-ELEKTRONIKK	Title: TERMINATION PLUG OR EXTENDED CONTROL PLUG	Drawing no. B06

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS		TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	
00		+5V				50	N	RO	0		
01		+5V				51	N	RO	0		
02		GROUND				52	N	MPMWR	0		
03		GROUND				53	N	MPMWR	0		
04						54					
05						55					
06						56					
07						57					
08						58		MINPUT	1		
09						59		MINPUT	0		
10						60		MCONNECT	1		
11						61		MCONNECT	0		
12	N	DPR	0			62		MREQ	1		
13	N	DRP	0			63		MREQ	0		
14						64		MINT 15	1		
15						65		MINT 15	0		
16	N	EMD	0			66		MINT 13	1		
17	N	EMD	0			67		MINT 13	0		
18						68		MINT 12	1		
19						69		MINT 12	0		
20	N	DLDA	0			70		MINT 11	1	MAIN	
21	N	DLDA	0			71		MINT 11	0	I/O BUS	
22						72		MINT 10	1	EXTENSION	
23						73		MINT 10	0	PLUG	
24						74		MOUTIDENT	1	OR	
25						75		MOUTIDENT	0	TERMINATION	
26						76		MIOXE	1	PLUG	
27						77		MIOXE	0		
28						78		MOUTGRANT	1		
29						79		MOUTGRANT	0		
30						80		MMCL	1		
31						81		MMCL	0		
32						82		MDRY	1		
33						83		MDRY	0		
34						84					
35						85					
36	N	DLDB	0			86					
37						87					
38						88					
39						89					
40	N	SMPX	0			90					
41						91					
42						92					
43						93					
44	N	MPX	0			94					
45						95					
46						96		GROUND			
47						97		GROUND			
48	N	MPMRQ	0			98		+5V			
49	N	MPMRQ	0			99		+5V			

DRAWN BY BS/bbo.	Remarks	Replacement for:	Date
APPROVED BY	N = NOT USED	Replaced by	Date
DATE 23.9.75.			

A/S NORSK DATA-ELEKTRONIKK	Title: 1101 BRANCH CONTROL	Drawing no. B07

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V			50	G	EIOXE	0	
01		+5V			51	W	BDRY	0	
02		GROUND			52		BA15	0	
03		GROUND			53	G	MPMWR	0	
04	G	BFQ1			54	G	BMCL	0	
05	G	BFQ2			55	G	GND1		
06	G	BIDENT	0		56				
07	G	WE	0		57				
08	G	ELD	0		58	W	MINPUT	1	
09	G	BGRANT	0		59	W	MINPUT	0	
10	G	GND2			60	W	MCONNECT	1	
11	G	BIOXE	0		61	W	MCONNECT	0	
12	G	SBD	0		62	W	MREQ	1	
13		DPR	0		63	W	MREQ	0	
14		BR	0		64	W	MINT 15	1	
15		BINPUT	0		65	W	MINT 15	0	
16	G	SLD	0		66	W	MINT 13	1	
17	G	EMD	0		67	W	MINT 13	0	
18	G	EM	0		68	W	MINT 12	1	
19		MPX ADR	0		69	W	MINT 12	0	
20		APR	0		70	W	MINT 11	1	
21	G	DLDA	0		71	W	MINT 11	0	
22	T	BD8	0		72	W	MINT 10	1	
23		BCONNECT	0		73	W	MINT 10	0	
24					74		MINIDENT	1	
25	G	EMA	0		75		MINIDENT	0	
26	G	EDD	0		76		MIOXE	1	
27		BINT 10	0		77		MIOXE	0	
28					78		MINGRANT	1	
29	G	EBD	0		79		MINGRANT	0	
30	G	GND3			80		MMCL	1	
31		BINT 11	0		81		MMCL	0	
32	G	EBA	0		82		MDRY	1	
33		BA0	0		83		MDRY	0	
34		BA1	0		84	G	MOUTIDENT	1	
35		BINT 12	0		85	G	MOUTIDENT	0	
36		R0	0		86	G	MOUTGRANT	1	
37	G	DLDB	0		87	G	MOUTGRANT	0	
38		R1	0		88				
39		BINT 13	0		89				
40					90				
41	G	SMPX	0		91				
42					92				
43		BINT 15	0		93				
44		BA10	0		94				
45		MPX	0		95				
46					96		GROUND		
47		BREQ	0		97		GROUND		
48					98		+5V		
49	G	MPMRQ	0		99		+5V		

DRAWN BY BS/bbo.
APPROVED BY
DATE 23.9.75.

Remarks
G = OUTPUT
W = WIRED-OR

Replacement for | Date
Replaced by | Date

A/S NORSK DATA-ELEKTRONIKK	Title: 1093 BRANCH TRANSCEIVER (DMA DATA)	Drawing no. B08

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS	TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V			50				
01		+5V			51	W	BDRY	0	
02		GROUND			52				
03		GROUND			53				
04	G	PYE0	0		54				
05	G	PYE1	0		55		BMCL	0	
06					56		MDRY	1	
07					57		MDRY	0	
08					58				
09					59				
10	T	BD0	0		60	T	MD16	1	
11		GND2			61	T	MD16	0	
12	T	BD1	0		62	T	MD17	1	
13	T	BD2	0		63	T	MD17	0	
14	T	BD3	0		64	T	MD0	1	
15	G	BR	0		65	T	MD0	0	
16	T	BD4	0		66	T	MD1	1	
17	T	BD5	0		67	T	MD1	0	
18	T	BD6	0		68	T	MD2	1	
19		EM	0		69	T	MD2	0	
20	T	BD7	0		70	T	MD3	1	
21	T	BD8	0		71	T	MD3	0	
22	T	BD9	0		72	T	MD4	1	MEMORY
23					73	T	MD4	0	DATA
24	T	BD10	0		74	T	MD5	1	PLUG
25	T	BD11	0		75	T	MD5	0	
26	T	BD12	0		76	T	MD6	1	
27		EDD	0		77	T	MD6	0	
28	T	BD13	0		78	T	MD7	1	
29	T	BD14	0		79	T	MD7	0	
30	T	BD15	0		80	T	MD8	1	
31		GND3			81	T	MD8	0	
32					82	T	MD9	1	
33					83	T	MD9	0	
34					84	T	MD10	1	
35					85	T	MD10	0	
36					86	T	MD11	1	
37					87	T	MD11	0	
38					88	T	MD12	1	
39					89	T	MD12	0	
40					90	T	MD13	1	
41					91	T	MD13	0	
42					92	T	MD14	1	
43					93	T	MD14	0	
44					94	T	MD15	1	
45					95	T	MD15	0	
46					96		GROUND		
47					97		GROUND		
48					98		+5V		
49					99		+5V		

DRAWN BY: BS/bbo	Remarks:	Replacement for: — Date:
APPROVED BY:	G = OUTPUT	Replaced by: — Date:
DATE: 23.9.75.	W = WIRED-OR T = THREE-STATE	

A/S NORSK DATA-ELEKTRONIKK	Title: I/O BUS POSITIONS POS 9 DMA ADDRESS EXTENDER	Drawing no. B09 or B24

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
00		+5V		
01		+5V		
02		GROUND		
03		GROUND		
04		BFQ1		
05		BFQ2		
06	G	OUTIDENT	0	
07		INIDENT	0	
08	G	OUTGRANT	0	
09		INGRANT	0	
10	T	BD0	0	
11		BIOXE	0	
12	T	BD1	0	
13	T	BD2	0	
14	T	BD3	0	
15	W	BINPUT	0	
16	T	BD4	0	
17	T	BD5	0	
18	T	BD6	0	
19	W	BMPX	0	
20	T	BD7	0	
21	T	BD8	0	
22	T	BD9	0	
23	W	BCONNECT	0	
24	T	BD10	0	
25	T	BD11	0	
26	T	BD12	0	
27	W	BINT10	0	
28	T	BD13	0	
29	T	BD14	0	
30	T	BD15	0	
31	W	BINT11	0	
32	T	BA0	0	
33	T	BA1	0	
34	T	BA2	0	
35	W	BINT12	0	
36	T	BA3	0	
37	T	BA4	0	
38	T	BA5	0	
39	W	BINT13	0	
40	T	BA6	0	
41	T	BA7	0	
42	T	BA8	0	
43	W	BINT15	0	
44	T	BA9	0	
45	T	BA10	0	
46	T	BA11	0	
47	W	BREQ	0	
48	T	BA12	0	
49	T	BA13	0	

TERMINAL	G=OUTPUT	SIGNAL	POLARITY	CONNECTED TO TERMINALS
50	T	BA14	0	
51		BDRY	0	
52	T	BA15	0	
53	T	BA16	0	
54	T	BA17	0	
55		BMCL	0	
56				
57		MPMRQ	0	
58				
59				
60				
61		MPMWR	0	
62				
63				
64				
65				
66				
67				
68				
69				
70		AC16	0	
71				
72		WE	0	
73				
74				
75				
76				
77				
78				
79				
80				
81				
82	T	MA20	1	
83	T	MA20	0	
84	T	MA19	1	
85	T	MA19	0	
86	T	MA18	1	
87	T	MA18	0	
88	T	MREQ	1	PART
89	T	MREQ	0	OF
90	T	MWRIT	1	MEMORY
91	T	MWRIT	0	CABLE
92	T	MA16	1	
93	T	MA16	0	
94	T	MA17	1	
95	T	MA17	0	
96		GROUND		
97		GROUND		
98		+5V		
99		+5V		

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY		Replaced by	Date
DATE			

DMA ADDRESS EXTENDER

Programming Specification

For large memory systems, it may be neccessary to provide the Bus Memory Brancher with a DMA Address Extender for addresses more than 18 bits long. This Extender will operate with any DMA controller that uses the MPX Address facility in a Bus Receiver/Bus Memory Brancher. Maximum address length will then be 24 bits.

The extended address part (bits 16-23) may be loaded by program, but not read. It is loaded by two consecutive IOX LCAR instructions. The first instruction loads the 8-bit most significant part (address bits 16-23) to the DMA Address Extender, and the second instruction loads the 16-bit least significant part of the memory address.

Example:

```
LDA MOST
IOX LCAR
LDA LEAST
IOX LCAR.
```

Note: With the DMA Address Extender installed, the most significant address bits must be loaded as described above.

The two address bits no. 16 and 17 which are normally loaded by control word bits 5 and 6 are ignored when the DMA Address Extender is installed.

Note: With the DMA Address Extender, a DMA transfer may cross a 64K word boundary.

The least significant 16 bits of the memory address register may be read as usual, and the DMA programming specifications are not otherwise affected.

BS/kkr/18/04/78

N O R D C O M - 7 4 G R I D P A T T E R N

USER SPECIFICATION

....oo0oo....

The four different grid patterns, 48 x 32, 24 x 16, 12 x 8 and 6 x 4 squares, are fix-wired as respectively BG0, BG1, BG2 and BG3 (Background pictures). The desired grid patterns are to be specified and selected for the actual monitor by setting the correcsponding SM according to chapter 3.6.4 in the Hardware Manual or according to chapter 7 in "SEMIGRAPHIC NORDCOM Programming specifications for SINTRAN III".

There is no programming to be done to the generator.

EXAMPLES OF PROGRAMMING

To select 24 x 16 squares on SM1 RED colour and helf intencity:

1. ACM-level:

ADDRESS: 142003_8 (SADR)
DATA: 011_8 (WDAT)

2. NORDCOM Test Monitor:

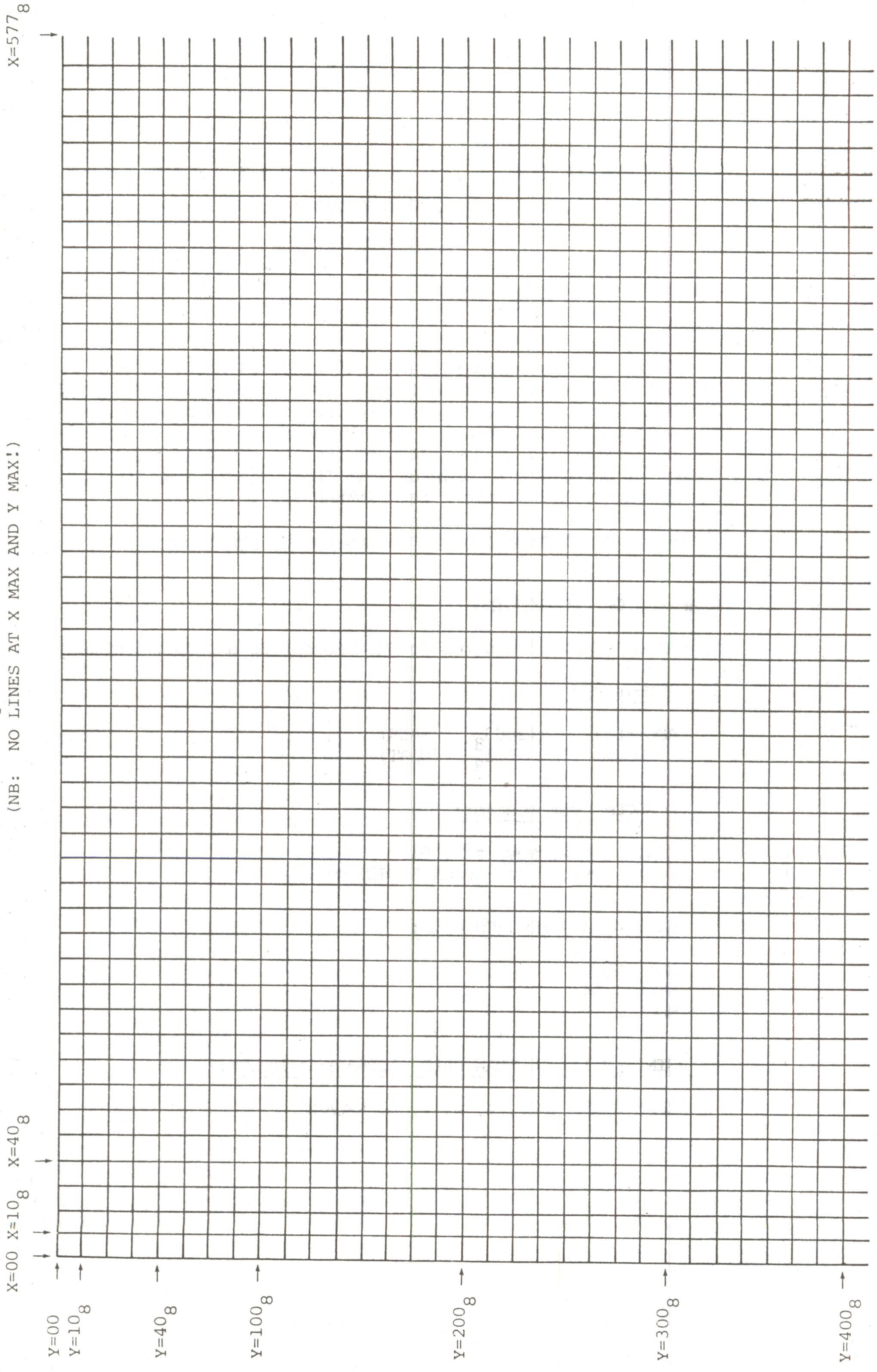
4, 1, xxx, yyy, zzz, 011
(xxx, yyy and zzz is MAIN-PICT or FG)

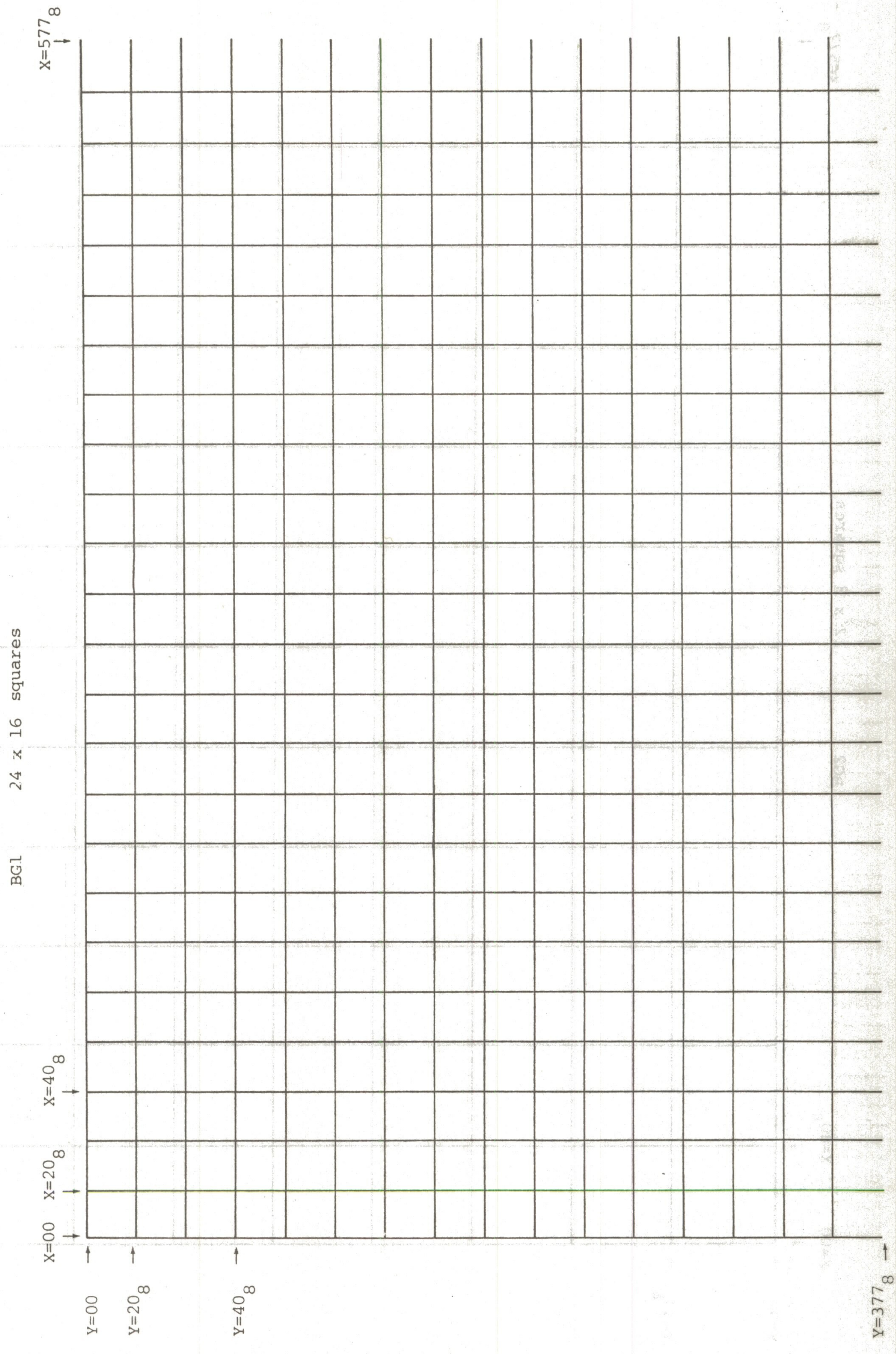
3. SINTRAN III MONITOR CALL:

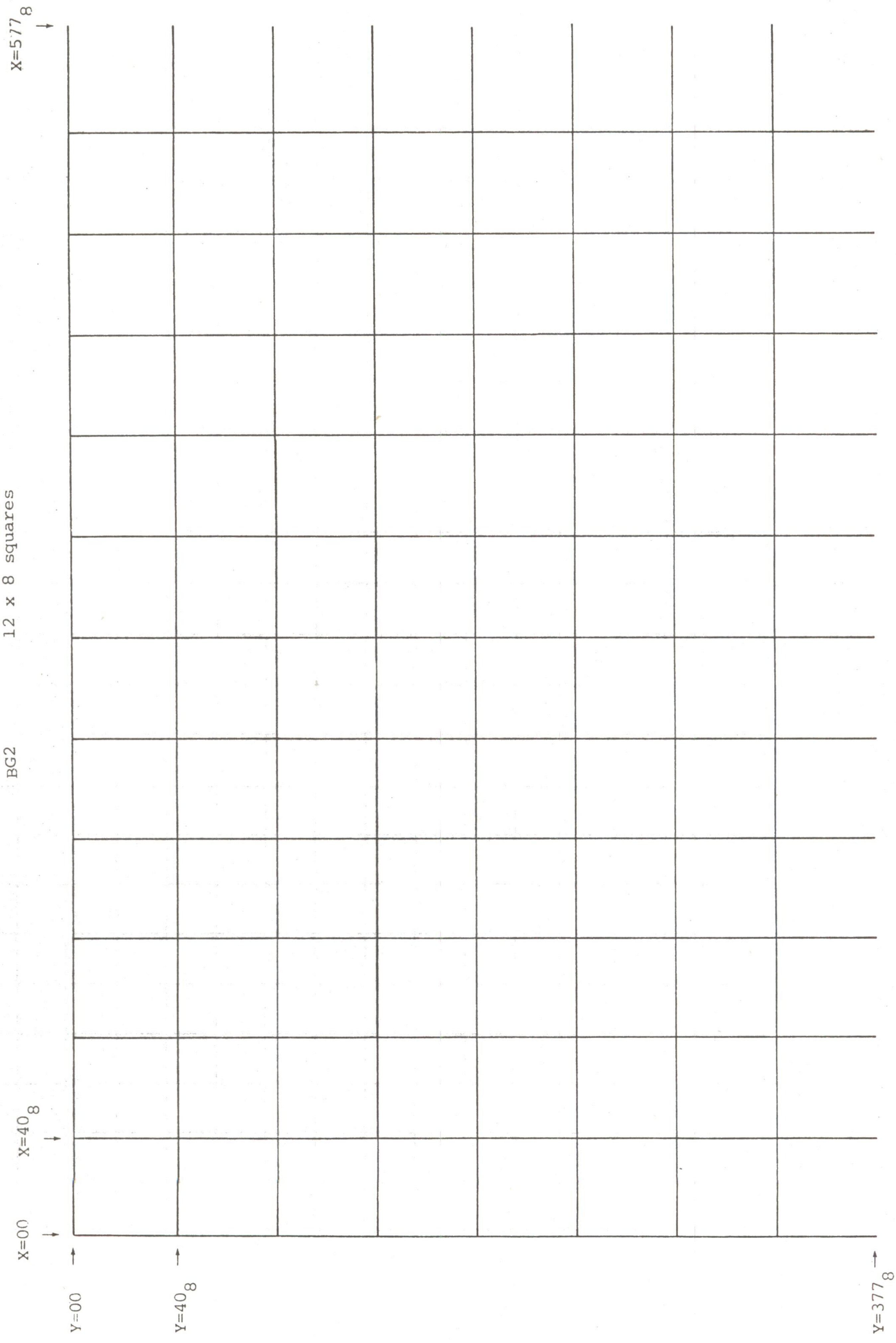
```
LDT  SMNO
LDA  (1641
MON  2
```

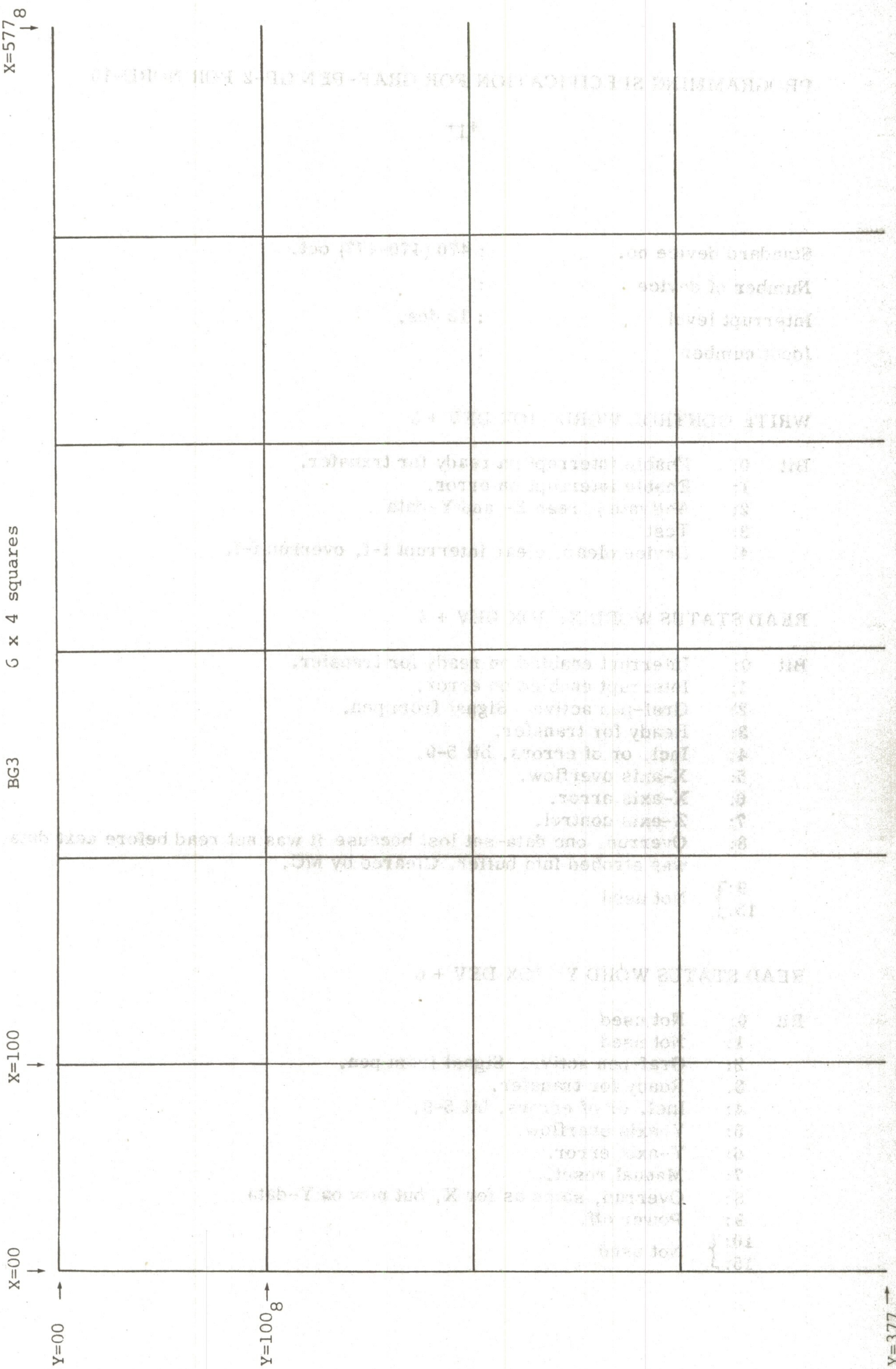
4. SINTRAN III FORTRAN CALL (LIBRARY ROUTINE):

```
CALL BGSEL (DEV, 1, 4, 1, 0, RFLAG)
```


X=577$_8$
48 x 32 squares
(NB: NO LINES AT X MAX AND Y MAX!)
BGØ
X=40$_8$
X=10$_8$
X=00
Y=00
Y=10$_8$
Y=40$_8$
Y=100$_8$
Y=200$_8$
Y=300$_8$
Y=400$_8$


$X=577_8$
BG1
24 x 16 squares
$X=40_8$
$X=20_8$
X=00
Y=00
$Y=20_8$
$Y=40_8$
$Y=377_8$


BG2
12 x 8 squares
X=577₈
X=40₈
X=00
Y=00
Y=40₈
Y=377₈


$X=577_8$
6 x 4 squares
BG3
X=100
X=00
Y=00
$Y=100_8$
$Y=377_8$

PROGRAMMING SPECIFICATION FOR GRAF-PEN GP-2 FOR NORD-10

+++

Standard device no.	: 470 (470-477) oct.
Number of device	:
Interrupt level	: 12 des.
Ident number	:

WRITE CONTROL WORD: IOX DEV + 3

Bit 0: Enable interrupt on ready for transfer.
1: Enable interrupt on error.
2: Activate): read X- and Y-data
3: Test
4: Device clear, clear interrupt f-f, overrun f-f.

READ STATUS WORD X: IOX DEV + 2

Bit 0: Interrupt enabled on ready for transfer.
1: Interrupt enabled on error.
2: Graf-pen active. Signal from pen.
3: Ready for transfer.
4: Incl. or of errors, bit 5-9.
5: X-axis overflow.
6: X-axis error.
7: Z-axis control.
8: Overrun, one data-set lost because it was not read before next data-set was strobed into buffer. Cleared by MC.
9:-15: Not used

READ STATUS WORD Y: IOX DEV + 6

Bit 0: Not used
1: Not used
2: Graf-pen active. Signal from pen.
3: Ready for transfer.
4: Incl. or of errors, bit 5-9.
5: Y-axis overflow.
6: Y-axis error.
7: Manual reset.
8: Overrun, same as for X, but now on Y-data.
9: Power off.
10:-15: Not used

WRITE DATA X: IOX DEV + 1

Only used for testing the interface without Graf-pen.

WRITE DATA Y: IOX DEV + 5

Only used for testing the interface without Graf-pen.

READ DATA X: IOX DEV + 0

Read 12 data bits from Graf-pen on X-lines.

READ DATA Y: IOX DEV + 4

Read 12 data bits from Graf-pen on Y-lines.

WRITE MODUS WORD: IOX DEV + 7

Bit	0:	Not used
	1:	Not used
	2:	Not used
	3:	Test
	4:	
	5:	Ext. reset, same as Manual Reset.
	6:	Ext. trigger, start sample in remote mode.
	7:	Rate osc. inhibit, will block the sample osc. in the modes free run and pen mode.
	8: - 15:	Not used

TEST

The interface may be tested without the Graf-pen connected. When bit 3 in the Control Word is set to one, the 12 X-bits will be tested, and the X-part of the interface will be in "test-mode". When bit 3 in the Modus Word is set to one, the 12 Y-bits will be tested, and the Y-part of the interface will be in "test-mode".

An IOX DEV + 1 will simulate one X-data-set (12 bits) read by the interface, set ready for transfer and increment the X-data-register.

An IOX DEV + 5 will simulate one Y-data-set (12 bits) read by the interface, set ready for transfer and increment the Y-data-register.

ACM I/O INTERFACE FOR NORD-10, PROGRAMMING SPECIFICATION

Standard dev. no.	40 - 43 (oct.)	ACM 1
	44 - 47 (oct.)	ACM 2
No. of dev. no.	4	
Standard interface level	10	
Standard ident no.	15, 25	

IOX	40	Read dataword
IOX	41	Load write word
IOX	42	Read status
IOX	43	Write control word

Control word

Bit	0	Interrupt enable
Bit	2	Activate
Bit	3	Test modus
Bit	4	Device clear
Bit	9 = 0	Reset MLOAD (other end free running)
	9 = 1	Set MLOAD (lock other end)
Bit	11	Used together with bit 2
Bit	12	

12	11	
0	0	Read data
0	1	Load data
1	0	Not used
1	1	Load address

Status word

Bit	0	Interrupt enabled
Bit	3	Device ready for transfer

Programming example

```
DRDTA,      000004          %   Read data
DSADT,      014004          %   Set address
DWDTA,      004004          %   Write data (4014 test mode)
DLOCK,      001000          %   Device lock
DUNLK,      000000          %   Device unlock

RMCL,       SAA     20
            IOW     WC + 40
            EXIT            %   Clear device

RLOCK,      LDA I (DLOCK
            IOX WC + 40
            EXIT            %   Lock

RUNLK,      IOX RS + 40
            BSKP 30 DA EOL ONE
            JMP * -2
            LDA I (DUNLK
            IOX WC + 40
            EXIT

)FILL

RSADT,      IOX WD + 40     %   Address placed in
            LDA I (DSADT    %   A-register
            IOX WC + 40
            IOX RS + 40
            BSKP 30 DA EQL ONE
            JMP * -2
            EXIT            %   Load address
```

```
RRDTA,      LDA I (DRDTA
            IOX WC + 40
            IOX RS + 40
            BSKP 30 DA EQL ONE
            JMP * -2
            IOX RD + 40
            EXIT              %    Data read in A-register.

RWDTA,      IOX WD + 40       %    Data in A-register
            LDA I (DWDTA
            IOX WC + 40
            IOX RS + 40
            BSKP 30 DA EQL ONE
            JMP * -2
            EXIT
```

POWER FAIL / AUTOMATIC RESTART

+++
+

1 POWER FAIL

A complete unit verifying the presence of an 50Hz AC voltage, normally the 230V mains voltage. Fast sense of power fail, delayed indication of power recovery. POWER FAIL (L) output is from an open-collector transistor. This signal is also clamped to ground via a relay (normally-closed).

1.1 Power Fail Unit Characteristics

The sequence for a power fail and automatic restart is shown in the timing diagram.

In the unit, the AC-voltage is full-wave rectified and applied to a RC combination with moderate time-constant, approximately 8 ms. Each 10 ms the capacitor is charged to the peak voltage, and then allowed to discharge towards the sense level at approximately half the peak value. At normal mains voltage the capacitor is recharged before the sense level is reached, and no POWER FAIL signal is generated.

If the capacitor is not properly recharged, because of too low or completely missing mains voltage, the sense level is passed and the FAIL signal is immediately set. With POWER FAIL active, the relay contacts are closed and connected to 0 volt. A hysterises of approximately 3% is obtained by shifting the sense level slightly up when POWER FAIL $\rightarrow$ 1.

When power again is restored, the capacitor is recharged above the sense level, and after a time-delay of approximately 0.7 sec. the output transistor and relay are activated and POWER FAIL $\rightarrow$ 0.

The unit consists of a circuit board, transformer and suppressor capacitor mounted in a steal box, with a connecting terminal block on the side of the box.

1.2 Specifications (Standard Adjustment)

Safe input range	: 0-300V rms, 50Hz
Trip level for OK POWER FAIL	: Adjusted to V_t=180V rms, $\pm$ 2%
Trip level for POWER FAIL OK	: Approx. 3% above V_t

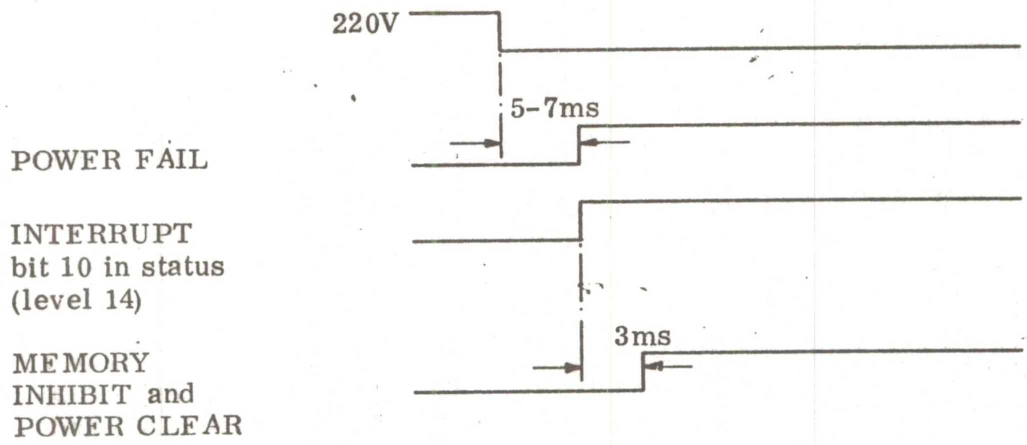
Response time for sense of POWER FAIL	: Typically 5-7 ms from a fast cutout of 230V input, depending on the breaking point in the AC cycle.
Response time for recovery to POWER FAIL = FALSE	: 0.7 sec. ± 20%
POWER	: Selfsupplied from input voltage.

2 AUTOMATIC RESTART

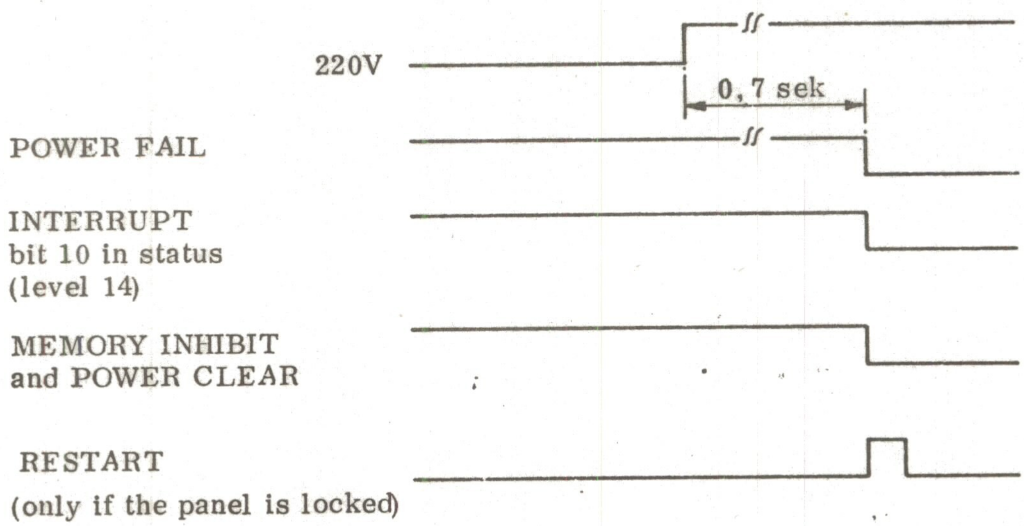
If the operator panel is locked, an automatic restart sequence is generated when the POWER FAIL signal disappears.

After a completed power up sequence the POWER CLEAR signal disappears and a RESTART signal is generated when this signal is detected by the micro-program, the CPU will start in memory location 20_8.

POWER FAIL SEQUENCE:



AUTOMATIC RESTART SEQUENCE:



Timing diagram

SPECIFICATIONS FOR PROCESS CONSOLE

The Process Console is a free standing unit. The unit is provided with communication interface for full duplex, TTY compatible connection, and for connection for asynchronous modem, RS-232.

Standard features:

- Alphanumeric display, 32 characters long
- Keyboard with up to 8 x 16 keys in a rectangular matrix. The number and arrangement of the keys are left to be decided by the customer. Specifications for the keyboard layout should be available in ND's production department 3 months prior to delivery.
- Each key may háve text and individually programmable light
- A lockable key switch will add the octal value 200 to any key number (force bit seven to one) to facilitate a selectable key lock function.
- Accoustic signal (600 Hz) with programmable duration
- Test mode. Echo on all received characters
- Transmission speeds: 110 or 1200 bauds

The Process Console is programmed through a set of instructions. These instructions are ordinary characters which are decoded inside the Process Console. Available instructions:

SCMND	Set Command	Octal code 100
SADR	Set Address	Octal code 140

Command bits in SCMND instruction:

Bit 0	Blank display
Bit 1	Clear display buffer
Bit 2	Sound on
Bit 3	Test mode on

Note : Command bits are active until they are reset by the program. Characters to display should be given in 6-bit ASCII code.

The SADR instruction transfers the column address (the 4 most significant bits of the 7 bit key address) to the console as bits 0 to 3 of the instruction. This instruction must always be followed by an 8-bit bit pattern for the corresponding 8 lamps in one column.

It is recommended to use one key for a lamp test function. The code of this key should be detected, and for a length of time determined by the program (1-5 sec.) all lamps should be lighted without disturbing the content of the lamp map in core.

For the ASEA double keyboard the keys with octal value 120, 121, 130 and 131 have an automatic repeat function (↑, ↓, →, ←).

P-NR :

KUNDE :

ANTALL :

177	T:167 F:	T:157 F:	T:147 F:	T:137 F:	T:127 F:	T:117 F:	T:107 F:	T:077 F:	T:067 F:	T:057 F:	T:047 F:	T:037 F:	T:027 F:	T:017 F:	T:007 F:
176	T:166 F:	T:156 F:	T:146 F:	T:136 F:	T:126 F:	T:116 F:	T:106 F:	T:076 F:	T:066 F:	T:056 F:	T:046 F:	T:036 F:	T:026 F:	T:016 F:	T:006 F:
175	T:165 F:	T:155 F:	T:145 F:	T:135 F:	T:125 F:	T:115 F:	T:105 F:	T:075 F:	T:065 F:	T:055 F:	T:045 F:	T:035 F:	T:025 F:	T:015 F:	T:005 F:
:174	T:164 F:	T:154 F:	T:144 F:	T:134 F:	T:124 F:	T:114 F:	T:104 F:	T:074 F:	T:064 F:	T:054 F:	T:044 F:	T:034 F:	T:024 F:	T:014 F:	T:004 F:
:173	T:163 F:	T:153 F:	T:143 F:	T:133 F:	T:123 F:	T:113 F:	T:103 F:	T:073 F:	T:063 F:	T:053 F:	T:043 F:	T:033 F:	T:023 F:	T:013 F:	T:003 F:
:172	T:162 F:	T:152 F:	T:142 F:	T:132 F:	T:122 F:	T:112 F:	T:102 F:	T:072 F:	T062 F:	T:052 F:	T042 F:	T:032 F:	T022 F:	T:012 F:	T002 F:
:171	T:161 F:	T:151 F:	T:141 F:	T:131 F:	T:121 F:	T:111 F:	T:101 F:	T:071 F:	T061 F:	T:051 F:	T041 F:	T:031 F:	T021 F:	T:011 F:	T001 F:
:170	T:160 F:	T:150 F:	T:140 F:	T:130 F:	T:120 F:	T:110 F:	T:100 F:	T:070 F:	T060 F:	T:050 F:	T040 F:	T:030 F:	T020 F:	T:010 F:	T:000 F:

HASTIGHET: 110 BD ☐
1200 BD ☐

N.B.: Med 1200 BD er maksimum avstand fra CPU 300 m.

Lys i tast avmerkes med L.

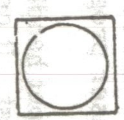
FILTER : (type 9)
1. HVIT
2. GRØNN
3. RØD
4. GUL

TASTER : (type 8)
2. GRØNN
3. RØD
4. GUL
5. BLÅ
6. LYS GRÅ
7. MØRK GRÅ
8. ANTRASITT

TASTER :

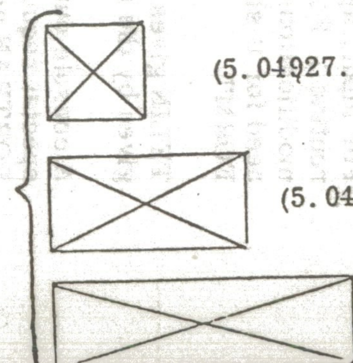
RAFI Kat. no.

Type no. 8 :



(5.46657.100)

Type no. 9:



(5.04927.117)

(5.04927.127)

(5.04927.137)

05/03/75/SFS/ab

The process console in a SINTRAN III system

For input, apply the driver TELIN. (TRGET should be used as its IOTRANS-routine.) For output, the normal teletype output driver may be used without modifications. Since TELIN may be a library routine in SINTRAN III, the need for it should be mentioned in the comment field of the "SINTRAN III ORDER FORM".

TELIN gives break for every character, and no echo is given. (This must be given by the user programme, which interprets the input.)

A console output handler KONSO has been made, and may be delivered on special request. It consists of a NPL subprogramme which may be called from FORTRAN and runs on application level. Characters may be written or read from the display, lamps or sound are put on/off, etc...... A complete version occupies approximately 600_8 locations.

(Specifications on the next pages.)

PROGRAMMING EXAMPLES. THE SINTRAN III MONITOR CALL OUTBT (MON 2) PERFORMS BYTE OUTPUT. SKIP-RETURN IF SUCCESSFUL.

```
        SCMND    =    1ØØ
        BLDIS    =     1
        CLDIS    =     2
        SOUND    =     4
        SADR     =    14Ø


%       CLEAR DISPLAY.  SET DISPLAY  POSITION Ø.
        LDT     ( CONS              % T : = LOGICAL CONSOLE DVN
        SAA     SCMND + BLDIS + CLDIS
        MON     2
        JMP     ERROR
        SAA     SCMND
        MON     2                   % OUTBT   SKIP IF SUCCESSFUL
        JMP     ERROR
                .
                .
                .

%       WRITE CHARACTER ONTO CURRENT DISPLAY POSITION
        LDT     (CONS
        SAA     SCMND
        MON     2
        JMP     ERROR
        LDA     CHAR                % A : = CHARACTER
        AND     (77                 % TRUNCATE
        MON     2
        JMP     ERROR
                .
                .
                .

%       PUT ON LAMP NO. 2 IN COLUMN NO. 7
%       (IN THIS EXAMPLE ALL OTHER LAMPS IN
%       COLUMN ARE SWITCHED OFF)
```

```
        LDT    (CONS
        SAA    SADR + 7                % SADR + COLUMN
        MON    2
        JMP    ERROR
        SAA    4                       % BIT-MASK FOR LAMP NO. 2
        MON    2
        JMP    ERROR
        SAA    SCMND
        MON    2
        JMP    ERROR
           .
           .
           .

%       SWITCH OFF LAMP 3 AND 5 IN COLUMN
%       NO. 1.  SWITCH ON ALL THE OTHER LAMPS IN THAT COLUMN

        LDT    (CONS
        SAA    SADR + 1
        MON    2
        JMP    ERROR
        LDA    (327
        MON    2
        JMP    ERROR
        SAA    SCMND
        MON    2
        JMP    ERROR

%       SWITCH ON SOUND :

        LDT    (CONS
        SAA    SCMND + SOUND
        MON    2
        JMP    ERROR

%       SWITCH OFF SOUND
        LDT    (CONS
        SAA    SCMND
        MON    2
        JMP    ERROR
```

If the console is handled by a stand-alone programme, the MON 2 - instruction may be replaced by a JPL I (OUTB instruction, where OUTB may look like this:

```
OUTB,       COPY  SA  DD
            LDX   (1ØØØØØ          % TIME-COUNTER
            IOX   DEV + 2          % READ STATUS
            BSKP  ZRO  4Ø  DA      % SKIP IF NO ERRORS
            EXIT
            BSKP  ONE  3Ø  DA
            JNC   * - 4
            JXZ   * - 3            % JUMP IF TIME-OUT
            COPY  SD  DA
            IOX   DEV + 1          % WRITE DATA
            SAA   4
            IOX   DEV + 3          % ACTIVATE DEVICE
            EXIT  AD1
)FILL
```

Output to the console

A general integer function KONSO is used for output to the console.

KONSO has 3 parameters:

I = KONSO (K, L, M)

K is console number (between 0 and BORDM, BORDM is a symbol defined in KONSO).

L is a function code (between 0 and FUMAX, FUMAX is a symbol defined in KONSO).

M depends on the function code L (M may be lamp number, character, display position, dummy).

I is the returned function value, where negative values indicate error:

I = - 1:K (console number) out of range
I = - 2:L (function code) out of range
I = - 3: Lamp number out of range
I = - 4: Display position out of range
I = - 5: Output character out of range

I = - 7: Any error from SINTRAN I/O (outbt error)

The implemented functions are:

L = 0, M = dummy

Update all lamps from the lamp table. Each lamp has a bit in the lamp table. If the bit is zero, the lamp is set to off. Initially, all lamps are off.

L = 1, M = lamp number $(0 - 127_{10})$

Read the status of the lamp specified in M. If the lamp is off, the function value I = 0. If the lamp is on, I = 1. (This information is found in the lamp table.)

L = 2, M = lamp number $(0 - 127_{10})$

Set the lamp specified in M to ON. The lamp table is updated (corresponding bit is set to "1").

L = 3, M = lamp number $(0 - 127_{10})$

Set the lamp specified in M to OFF. The lamp table is updated (corresponding bit is set to "0").

L = 4, M - display position $(0 - 31_{10})$

Set current display position to value specified in M.

If the current display position is decremented, the display is cleared and then the contents of the display table from the start to the new current position is copied to the display.

If the current position is incremented, the contents of the display table from the start to the new current position is copied to the display.

If the current position is incremented, the contents of the display table from the old to the new current position is copied to the display.

L = 5, M = character $(40_8 - 137_8)$, $32_{10} - 95_{10})$

Write the specified character to the current position of the display. The display table is updated, and the current position is incremented by one.

If the original current position was skip marked, the character will be written to the first not skip marked position. Space will be written to all skip marked positions. Space will be written to all skip marked positions. (Any other special character may be used instead of space.)

L = 6, M = display position (0 - 31)

Read the character in position M in the display table. The character will be returned as the function value I. If the specified position is skip marked, bit 8 of the returned character is "1".

Other functions may be implemented in KONSO.

These may be:

Reserve and release

Transparent output (not affecting the tables)

These functions may be performed by the Standard SINTRAN calls; however, the SINTRAN logical device numbers must be used instead of the logical console number used in KONSO. Therefore, it is convenient to define a function in KONSO to find the SINTRAN logical device number for a specified console.

L = 7, M = dummy

The SINTRAN logical devicenumber of the console specified in parameter K is returned as function value I.

$L = 10_8$, M = state

Sound on or off. ("On" if M unequal ∅.)

$L = 11_8$, M = display position ($\emptyset - 31_{10}$)

Clear console from given position. Set given position.

32K RAM - Preliminary Specification

1. Introduction

The recently introduced 16K x 1 bit MOS memory integrated circuit is used in a range of new memory modules.

A PC-board, 1132, is designed which will suite the types Texas TMS 4070-2 and Mostek MK 4116P-3.

However, it is prepared to suite types with other timing requirements as well as types with output latch. (I.e. Intel 2116, MK 4027 (4K x 1 bit), etc.)

Presently 6 types of memory modules are defined:

1132-0:	32K x 21 bits with MK 4116P-3 (200 ns access)
1132-1:	32K x 18 bits with MK 4116P-3 (200 ns access)
1132-2:	32K x 21 bits with TMS 4070-2 (250 ns access)
1132-3:	32K x 18 bits with TMS 4070-2 (250 ns access)
1132-4:	8K x 21 bits with MK 4027P-3 (200 ns access)
1132-5:	8K x 18 bits with MK 4027P-3 (200 ns access)

1132-0 is the basis configuration, and the other types are obtained by change of components, IC arrangement and/or straps

2. Data

A module has either 16 data bits + 2 parity bits (standard on NORD-10S), or 16 bits + 5 error-correction bits. In the latter case a signal, B21BIT, informs the controller that 21 bits are present. Hence it is possible to mix the two module types.

— 2 straps are required for 18 bit modules

3. Addresses

A module is divided into two blocks which are partly independent. They have separate address and clock drivers and common control logic. It is possible to access one block while the other is recovering from the previous access (Precharge period).

Normally one block, X, contains even addresses and the other, Y, odd addresses. I.e., address bit 0 is used to decide block.

It is possible to exchange address bit 0 and 14 such that block X holds the lower 16K and block Y the higher 16K. Hence it is possible to make 16K modules by removing the IC-circuits for one bank. However, no provision is made to inhibit response when the missing block is accessed.

— 2 straps are required to exchange address bit 0 and bit 14

On 32K modulas address bits 15, 16 and 17 are used to select modules by means of the code terminals S0-S2 which are hard-wired in each memory slot.

To allow use of an 8K module with 4K x 1bit chips, provision is made to use address bits 13-17 for module selection as shown in the table:

Code Terminal	8K Module	32K Module
S0	BA13	BA15
S1	BA14	BA16
S2	BA15	BA17
S3	BA16	Unused
S4	BA17	Unused

Table 2.1: Correspondance between selection code and address bits.

— 3 straps and rearrangement of one IC is required for 8K modules.

3. Type of Memory Chips

Apart from access times memory chips may differ in two respects.

a) 128 versus 64 refresh cycles for complete refresh.

b) Latched versus direct output of data.

Point a) is trivial since the brand (Intel) with 64 refresh cycles also may be operated with 128 refresh cycles.

— Change one IC, 74S00 to 74S20 to allow latched output chips.

4. Memory Chip Timing

Three different times characterize a memory chip:

T1: RAS to CAS
T2: CAS minimum on-time
T3: RAS minimum off-time, Precharge period

Even if the access times are equal, different manufactures may specify different times. Hence all are independant variables which must be accounted for.

During T1 address input to the chips are switched from Row address to Column address. Thus T1 is the sum of Row address hold time, T1R, and Column address setup time, T1S.

T1S is fixed ≈ 40 ns.

— T1R is set by a delay line with a strap from one of the taps (10ns increments)

T1 + T2 determines access time at read and T2 is determined by the frequency of an oscillator.

— The frequency is adjusted by a resistor (or a trimpot)

T1 + T2 + T3 determines cycle time, which is the minimum time between two accesses to the same block. (Minimum time between accesses to opposite blocks is determined by T1 + T2).

— T3 is set by a resistor.

5. EXTERNAL TIMING.

5.1 Read access.

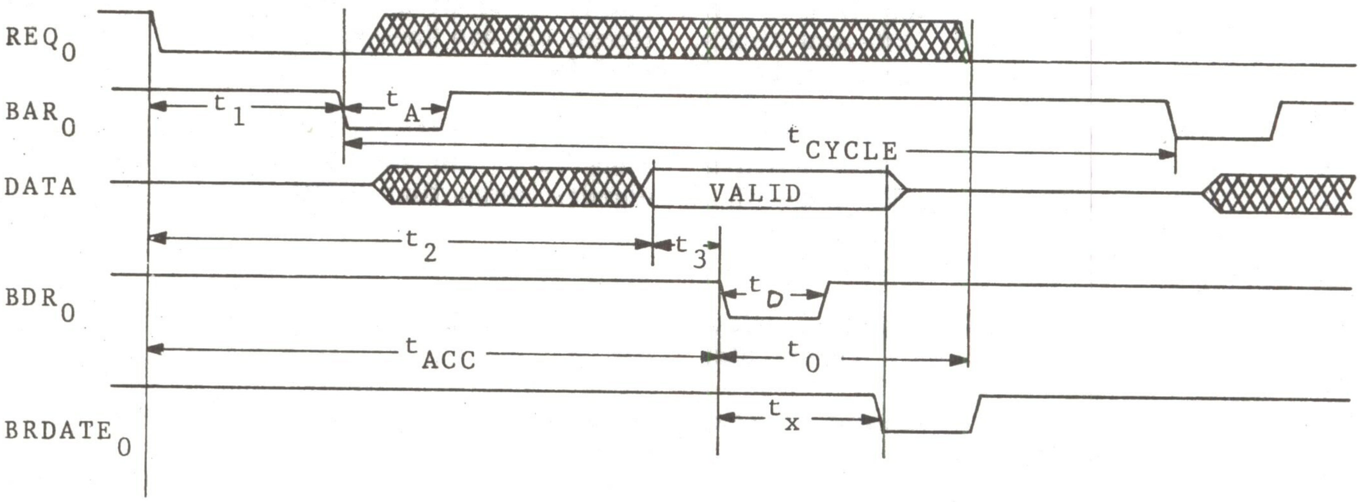


Fig. 5.1 : Timing for READ-cycle.

	MOSTEK 200ns Min	Typ	Max	TEXAS 250ns Min	Typ	Max	Comment
t_1		110	155		130	180	
t_2		245	305		295	360	
t_3	0	35		0	35		
t_{ACC}	265	280	330	315	330	390	
t_{CYCLE}	380	400	455	430	455	515	Same block and t_x, $t_0 \leqslant$ 90ns
t_0			90			90	Same block and $t_x \leqslant$ 90ns
t_0			t_x			t_x	Opposite block or $t_x >$ 90ns
t_A		80			105		
t_D		60			70		

Table 5.1 Times in ns at READ for memory-chips with 200 and 250ns accesstime. $t_{0\ Max}$ must be observed to attain minimum cycle-time. In other respect it has no limitations.

5.2 Write access.

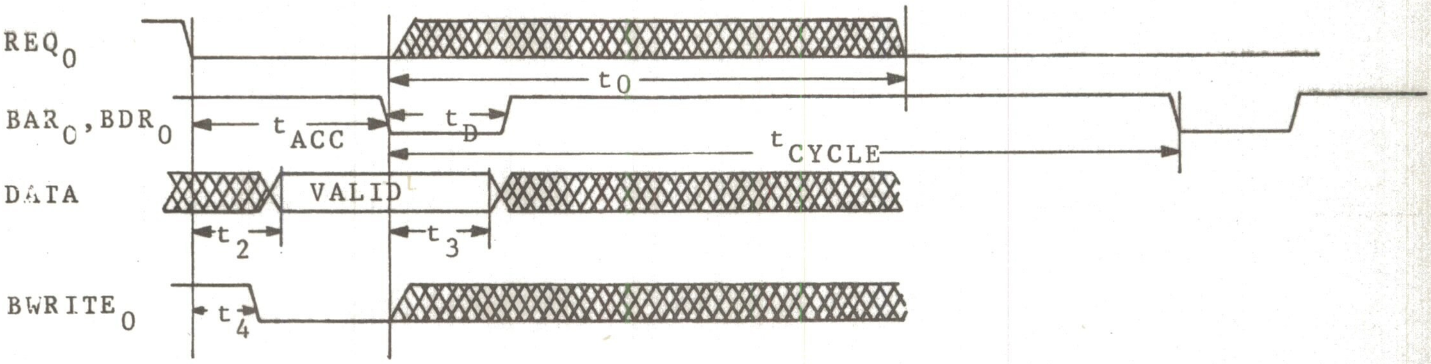


Fig. 5.2 : Timing for WRITE-cycle.

	MOSTEK 200ns			TEXAS 250ns			
	Min	Typ	Max	Min	Typ	Max	Comment
t_{ACC}		110	155		130	180	
t_2			70			90	
t_3	45			60			
t_4			30			50	
t_{CYCLE}	235	245	295	285	295	355	Opposite block
t_0			95			125	Opposite block
t_{CYCLE}	380	400	455	430	455	515	Same block
t_0			240			260	Same block
t_D		80			105		

Table 5.2 Times in ns at WRITE for memory-chips with 200 and 250ns accesstime. Condition on t_0 is the same as for READ.

REMOTE LOAD MODULE

Device spcification.

I Description.

A Remote Load Module (RLM) is designed to load a remote NORD computer. The computer to load and the computer to be loaded have to communicate via a HDLC line. A load request, remote load trigger frame (RLT frame) is sent to the remote computer (the computer to be loaded). When a computer receives a RLT frame, this is detected by the RLM and the following load sequence is started.

1) The RLM generate Master Clear to the computer.

2) The RLM generates LOAD to the computer.

3) The standard load program (microprogram) reads (binary load) a program from the RLM (stored in PROM) into the memory. This program is started when the character ! is read (standard binary load). The ALD register has to be set to the device number of the RLM.

4) Loading is now under program control, and the computer loads itself from the HDLC line. The comunication between the two computers follows a definf load procedure.

Remote load frame:

Flag	Address	CRC		Flag
01111110	10101010	00001010	10101111	01111110
←byte 1→	←byte 2→	←byte 3→	←byte 4→	←byte 5→

II Programming

1) READ DATA

IOX DEV

Data is read from the PROM on the RLM. A 8 bit dataword is read into the A-register.

This IOX instruction increments the PROM address counter with one.

2/....

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2) STEP TO NEXT STATE

IOX DEV +1

This IOX instruction is used to test the RLM card. The module has a state counter, 0-5. When the module detects a correct byte (8 bits) in the RLT frame, the state is incrementet by one. In state 5 a correct RLT frame is found, 5 bytes in sequence.

The detection of one byte can be simulated with this IOX instruction. After five executions of this instruction the module is in state 5 and a Remote Load sequence is started.

Test-bit must be set (Load control word bit 3).

3) READ STATUS

IOX DEV +2

Status from the RLM is loaded into the A-register.

Status word:

Bit 0	: Interrupt enabled
Bit 1	: Device number bit 4.
Bit 2	: Device busy (always ready)
Bit 3	: Device ready (always ready)
Bit 4	: Devicenumber bit 2
Bit 5-7	: State counter (0-5), inverted
Bit 8-12	: PROM address counter bits 0-4, inverted
Bit 12-15	: PROM address counter bit 7-9, inverted

4) LOAD CONTROLWORD

IOX DEV +3

The controlword in A-register is set to the RLM.

Control word:

Bit 0	: Enable interrupt on level 13. Interrupt in state 5.
Bit 1-2	: Not used.
Bit 3	: Set testmodus, inhibits clock from HDLC.
Bit 4	: Programmed clear. Address counter cleared. State counter cleared.
Bit 5-15	: Not used.

5) DEVICE NUMBER:

Standard devicenumber 1610.
Additional units 1614-1634.
IDENT number 3, level 13.

When Remote Load Trigger is detected (state 5) dev no. 1600 is used.

3/....

III INSTALLATION

1) Clock, terminal 76, remote load connected to terminal 76 on HDLC card.

2) Data, terminal 77, in remote load connected to terminal 77 on HDLC card.

3) Load, terminal 93, on remote load connected to SWLOAD (terminal (terminal 84 on 1121 card).

4) Master Clear, terminal 95 on remote load connected to TW13, terminal 90 on 1121.

5) More than one remote load module in one computer.

If a computer should be loaded from several other computers, one remote load module is needed for each HDLC interface. The different R2M must then be interconnected.

$OUTR_0$ (term 90) from the module with highest priority is connected to INR_0 (term. 91) on the next module and $OUTR_0$ from this to the third module etc.

STANDARD NORD-10/S DEVICE NUMBERS AND IDENT CODES

Logical Device No. Octal(Decimal)	Device No.	Interrupt Level	Ident Code (octal)	Device	SINTRAN III
	4- 7	13	4	Memory Parity N-12	
	10- 13	13	1	Real Time Clock 1	
	14- 17	13	2	Real Time Clock 2	
	30- 33	12	16	NORD-50/1	
	34- 37	10	16	ACM 5	
	40- 43	10	15	ACM 1	
	44- 47	10	25	ACM 2	
	50- 53	10	40	ACM 3	
	54- 57	10	41	ACM 4	
	60- 77			NORD-50/1 Regs.	
6	100-107	10-12	4	Synchr. Modem 1	
16 (14)	110-117	10-12	14	Synchr. Modem 2	
30 (24)	120-127	10-12	20	Synchr. Modem 3	
31 (25)	130-137	10-12	24	Synchr. Modem 4	
26 (22)	140-147	10-12	30	Synchr. Modem 5	
27 (23)	150-157	10-12	34	Synchr. Modem 6	
7	200-207	10-12	60	Asynchr. Modem 1	Terminal 17
17 (15)	210-217	10-12	61	Asynchr. Modem 2	Terminal 18
52 (42)	220-227	10-12	62	Asynchr. Modem 3	Terminal 19
53 (43)	230-237	10-12	63	Asynchr. Modem 4	Terminal 20
54 (44)	240-247	10-12	64	Asynchr. Modem 5	Terminal 21
55 (45)	250-257	10-12	65	Asynchr. Modem 6	Terminal 22
56 (46)	260-267	10-12	66	Asynchr. Modem 7	Terminal 23
57 (47)	270-277	10-12	67	Asynchr. Modem 8	Terminal 24
1	300-307	10-12	1(120*)	Teletype 1	Terminal 1
11 (9)	310-317	10-12	5(121*)	Teletype 2	Terminal 2
42 (34)	320-327	10-12	6(122*)	Teletype 3	Terminal 3
43 (35)	330-337	10-12	7(123*)	Teletype 4	Terminal 4
44 (36)	340-347	10-12	44	Teletype 5	Terminal 5
45 (37)	350-357	10-12	45	Teletype 6	Terminal 6
46 (38)	360-367	10-12	46	Teletype 7	Terminal 7
47 (39)	370-377	10-12	47	Teletype 8	Terminal 8
2	400-403	12	2	Paper Tape Reader 1	
12 (10)	404-407	12	22	Paper Tape Reader 2	
3	410-413	10	2	Paper Tape Punch 1	
13 (11)	414-417	10	22	Paper Tape Punch 2	
4	420-423	12	3	Card Reader 1	
14 (12)	424-427	12	23	Card Reader 2	
5	430-433	10	3	Line Printer 1	
15 (13)	434-437	10	23	Line Printer 2	
10 (7)	440-443	10	11	Calcomp Plotter 1	
50 (40)	444-447	10	12	Card Punch 1	
51 (40)	454-457	10	13	Card Punch 2	

*4 CURRENT-LOOP. MODULE 1122

Logical Device No. Octal(Decimal)	*Device No.*	*Interrupt Level*	*Ident Code (octal)*	*Device*	*SINTRAN III*
	500- 507	11	1	Disk System 1	
	510- 517	11	5	Disk System 2	
	520- 527	11	3	Magtape Controller 1	
	530- 537	11	7	Magtape Controller 2	
	540- 547	11	2	Drum 1	
	550- 557	11	6	Drum 2	
1006 (518)	560- 577	12-13	156	HDLC HASP 1	
22 (18)	600- 607	11	4	Versatec 1	
	610- 617	11	11	Core-to-Core 1	
1007 (519)	620- 637	12-13	157	HDLC HASP 2	
1040 (544)	640- 647	10-12	124		Terminal 33
1041 (545)	650- 657	10-12	125		Terminal 34
1042 (546)	660- 667	10-12	126		Terminal 35
1043 (547)	670- 677	10-12	127		Terminal 36
	700- 707	12	11	CATSY 1	
	710- 717	12	21	CATSY 2	
	720- 727			A/D Converter	
	730- 737	10	10	D/A Converter	
	750- 753	13	5	BIG MPM LOG module	
	770- 773	12	17	Dig. Reg. 1 Input	
	774- 777	10	17	Dig. Reg. 1 Output	
	1000-1003	12	26	Dig. Reg. 2 Input	
	1004-1007	10	26	Dig. Reg. 2 Output	
	1010-1013	12	27	Dig. Reg. 3 Input	
	1014-1017	10	27	Dig. Reg. 3 Output	
	1020-1023	12	43	Dig. Reg. 4 Input	
	1024-1027	10	43	Dig. Reg. 4 Output	
	1030-1033	12	116	NORD-50/2	
	1034			Watch Dog	
	1035			Process Output 1	
	1036			Process Output 2	
	1037			Process Output 3	
	1040-1043	12	15	Process Input 1	
	1044-1047	12	25	Process Input 2	
	1050-1053	12	40	Process Input 3	
	1060-1077			NORD-50/2 Reg.	
1044 (548)	1100-1107	10-12	130		Terminal 37
1	1110-1117	10-12	131		Terminal 38
1	1120-1127	10-12	132		Terminal 39
1	1130-1137	10-12	133		Terminal 40
1	1140-1147	10-12	134		Terminal 41
1	1150-1157	10-12	135		Terminal 42
1	1160-1167	10-12	136		Terminal 43

Logical Device No. Octal(Decimal)	Device No.	Interrupt Level	Ident Code (octal)	Device	SINTRAN III
1053 (555)	1170-1177	10-12	137		Terminal 44
70 (56)	1200-1207	10-12	70	Asynchr. Modem 9	Terminal 25
1	1210-1217	10-12	71	Asynchr. Modem 10	Terminal 26
1	1220-1227	10-12	72	Asynchr. Modem 11	Terminal 27
1	1230-1237	10-12	73	Asynchr. Modem 12	Terminal 28
1	1240-1247	10-12	74	Async 13/Photo 1	Terminal 29
1	1250-1257	10-12	75	Async 14/Photo 2	Terminal 30
1	1260-1267	10-12	76	Async 15/Photo 3	Terminal 31
77 (63)	1270-1277	10-12	77	Async 16/Photo 4	Terminal 32
60 (48)	1300-1307	10-12	50	Teletype 9	Terminal 9
1	1310-1317	10-12	51	Teletype 10	Terminal 10
1	1320-1327	10-12	52	Teletype 11	Terminal 11
1	1330-1337	10-12	53	Teletype 12	Terminal 12
1	1340-1347	10-12	54	Teletype 13	Terminal 13
65 (53)	1350-1357	10-12	55	Teletype 14	Terminal 14
66 (54)	1360-1367	10-12	56	Teletype 15	Terminal 15
67 (55)	1370-1377	10-12	57	Teletype 16	Terminal 16
1054 (556)	1400-1407	10-12	140		Terminal 45
1	1410-1417	10-12	141		Terminal 46
1	1420-1427	10-12	142		Terminal 47
1	1430-1437	10-12	143		Terminal 48
1	1500-1507	10-12	144		Terminal 49
1	1510-1517	10-12	145		Terminal 50
1	1520-1527	10-12	146		Terminal 51
1063 (563)	1530-1537	10-12	147		Terminal 52
	1540-1547	11	17	Big Disk System 1	
	1550-1557	11	20	Big Disk System 2	
	1560-1567	11	21	Floppy Disk 1	
	1570-1577	11	22	Floppy Disk 2	
23 (19)	1600-1607	11	14	Versatec 2	
	1640-1657	12-13	150	HDLC NORD NET-1	
	1660-1677	12-13	151	HDLC NORD NET-2	
	1700-1717	12-13	152	HDLC NORD NET-3	
	1720-1737	12-13	153	HDLC NORD NET-4	
	1740-1757	12-13	154	HDLC NORD NET-5	
	1760-1777	12-13	155	HDLC NORD NET-6	