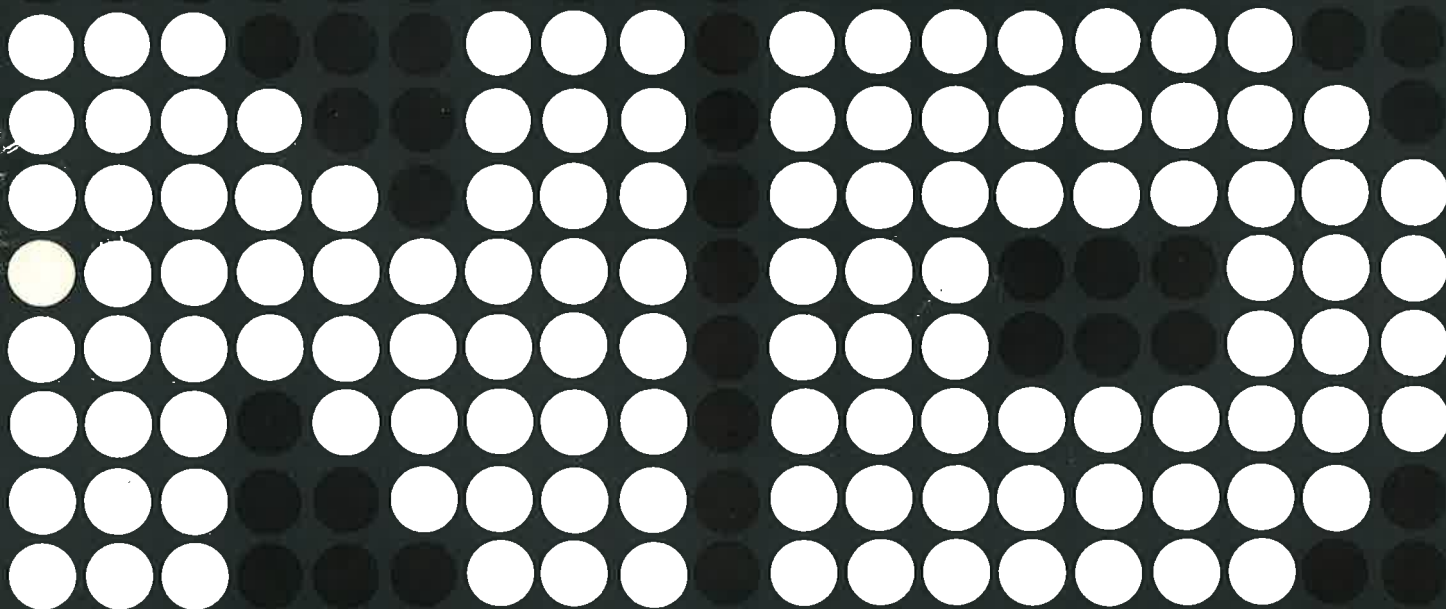


**NORD 10/S**  
**INPUT/OUTPUT SYSTEM**

**NORSK DATA A.S**





**NORD 10/S**  
**INPUT/OUTPUT SYSTEM**





## TABLE OF CONTENTS

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<i>Section:</i>		<i>Page:</i>
1	NORD-10/S INPUT/OUTPUT SYSTEM	1-1
1.1	Introduction	1-1
1.2	Nord-10/S I/O Bus-Architecture	1-4
1.2.1	Bus Transceiver	1-6
1.2.2	Bus Receiver/Brancher	1-6
1.3	I/O Card Crate Physical Layout	1-7
1.3.1	I/O Card Crate Expansion	1-8
2	PROGRAMMED INPUT/OUTPUT (PIO)	2-1
2.1	The Interface and the IOX Instruction	2-6
2.2	IOX Instruction Execution CPU	2-10
2.3	Programming a PIO Interface	2-15
2.3.1	Format of Status and Control Word	2-18
3	PROGRAMMED INPUT/OUTPUT LOCAL I/O BUS SIGNALS	3-1
4	I/O INTERRUPT-SYSTEM	4-1
4.1	General Description	4-1
4.2	I/O Interrupt	4-3
4.3	Interrupt Identification	4-4
4.4	Ident-Instruction	4-5
4.5	Ident-Instruction Execution Sequence	4-6
4.6	Interrupt Identification Signals	4-11
4.7	Input/Output Interrupt Programming	4-13
5	BUS-RECEIVER/BANCHER	5-1
5.1	General	5-1
5.2	Bus-Receiver Memory-Brancher Modules	5-4
5.3	Programmed Input/Output	5-5
5.4	DMA via CPU on MAIN I/O BUS	5-7
5.5	DMA Transfer Direct to/from Multiport	5-9
5.6	Disconnecting the Local I/O Bus	5-12
6	DIRECT MEMORY ACCESS (DMA)	6-1
6.1	General	6-1
6.2	IOX Format	6-4
6.3	Interface Organization	6-5
6.4	Core Address Register	6-6
6.5	Block Address Register	6-9
6.6	DMA/Transfer on MAIN I/O BUS	6-10
6.7	DMA-Transfer Improvements	6-15
6.8	DMA-Transfer Direct to/from Multiport	6-15

**2. DIRECT MEMORY ACCESS INTERFACE (DMA)**

The Direct Memory-Access interface normally consists of 4 to 12 cards located in the I/O rack. The DMA interface transfers blocks of data:

- Directly to/from the multiport memory via one separate port.
- To/from the local memory in the CPU-rack.
- To/from the multiport memory via the CPU port.

The two last transfers are based on CPU cycle stealing, while the first transfer takes place simultaneously with the CPU if the CPU and the DMA are accessing different banks. Typical DMA devices are DISKS, DRUMS, PLOTTERS and MAG-TAPES.

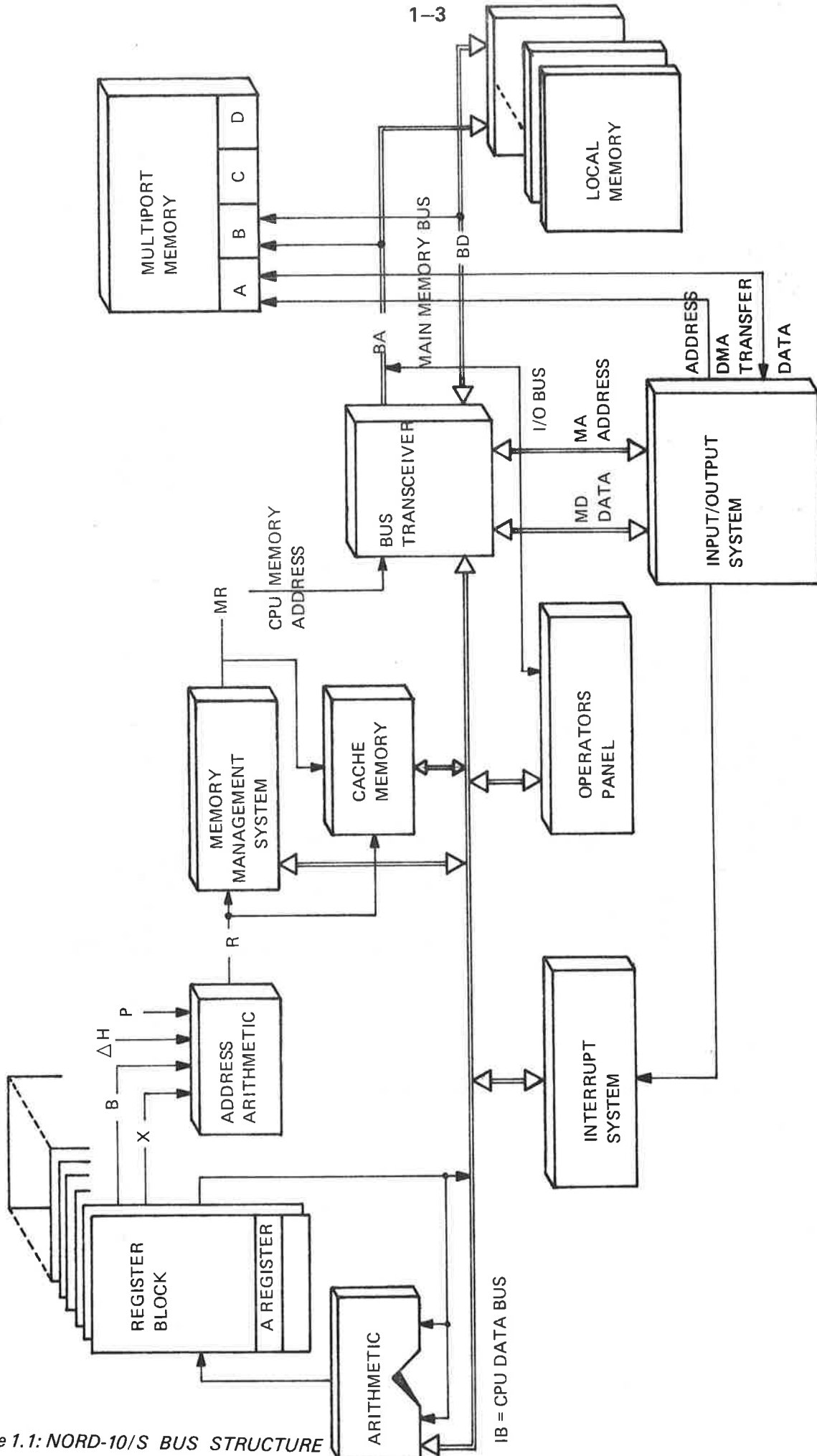


Figure 1.1: NORD-10/S BUS STRUCTURE

### 1.2.1 *BUS TRANSCEIVER:*

The BUS TRANSCEIVER which occupies 3 slots between the CPU and the local memory in the A-rack has the following main functions when communicating with a PIO interface (A) and a DMA interface (B):

A:

Establishes the communication between the addressed device interface register and the A-register.

The data lines MD will either be equal to the A-register if an output operation or equal to the addressed device-interface register if an input operation. Data is transferred to/from the A-register via the CPU data-bus IB.

The address given in the 11 lower bits in the Instruction-Register (IR) is routed out on the address lines MA.

B:

The BUS-TRANSCEIVER administrates the usage of the memory address bus BA and the memory data bus BD. These busses are connected either to the local memory in the A-rack or to one port in the multiport memory, or both.

Two sources are supplying data and address to the BUS TRANSCEIVER modules:

- CPU with the physical memory address as output of the paging system and data (if MEMORY-WRITE) on the CPU-data-bus or Information-bus IB.
- DMA with the memory-address on the MA-lines from a memory address register (CAR) and data from the interface on the MD lines.

During a DMA transfer the CPU is allowed to use the IB bus. This implies that CPU can fetch instructions and data from the CACHE memory independent of the DMA transfer. If a CPU and a DMA memory request should appear simultaneously, the BD and BA lines will be allocated to the DMA-transfer. The DMA requests have higher priority than the CPU request.

### 1.2.2 *BUS RECEIVER/BRANCHER. (8 left-most positions in the I/O rack)*

The modules installed here are called BUS-RECEIVER when establishing the communication between the Local I/O bus in the rack and the Main I/O bus.

The modules are called BUS-BRANCHER when communicating with one port in the multiport-memory during a DMA transfer.



### 1.3 I/O CARD CRATE- Physical Layout.

The 8 left-most positions in an I/O card crate are assigned for modules converting the Main I/O bus to a local tristate-bus. Three empty positions are set off for Main-bus expansion to the next I/O rack via plugs in the backwiring.

The right-most positions in the I/O rack are set-off for DMA interfaces.

Typical DMA interfaces and interface modules are listed below:

<i>Interface:</i>	<i>No. of Modules:</i>	<i>Remarks:</i>
DRUM Vermont)	8	1 DRUM
CARTRIDGE-DISK	8	Daisy-chain up to 4 DISK-DRIVES
PERTEC MAG-TAPE	4	Communicate with up to 2 Formatters.4 MAG-TAPE Units pr. formatter.
BIG-DISK(33 or 66 M-Bytes)	12	Communicate with up to 6 DISK-DRIVES. One module per drive.

In addition to the modules listed, the DMA interface is represented in the local I/O bus with one module (the BUS-CONTROL 1022 or 1155). (1155 module is used in the BIG-DISK interface with ERROR-CORRECTION).

The positions between the DMA interface and the BUS-RECEIVER/BRANCHER are assigned for a local I/O bus where PIO interfaces can be placed in any order.

### 1.3.1 *I/O CARD-CRATE Expansion (Refer to Figure 1.4)*

Only two I/O card crates (Band C) are installed in the CPU cabinet, for more I/O card crates the following is possible:

For ND:

The Main I/O bus is fed to three plugs in the plug panel via the empty expansion position in the C-rack.

For the Customer:

The local I/O bus is buffered and differentiated on three modules in the local I/O BUS, and fed to three plugs in the plug-panel.

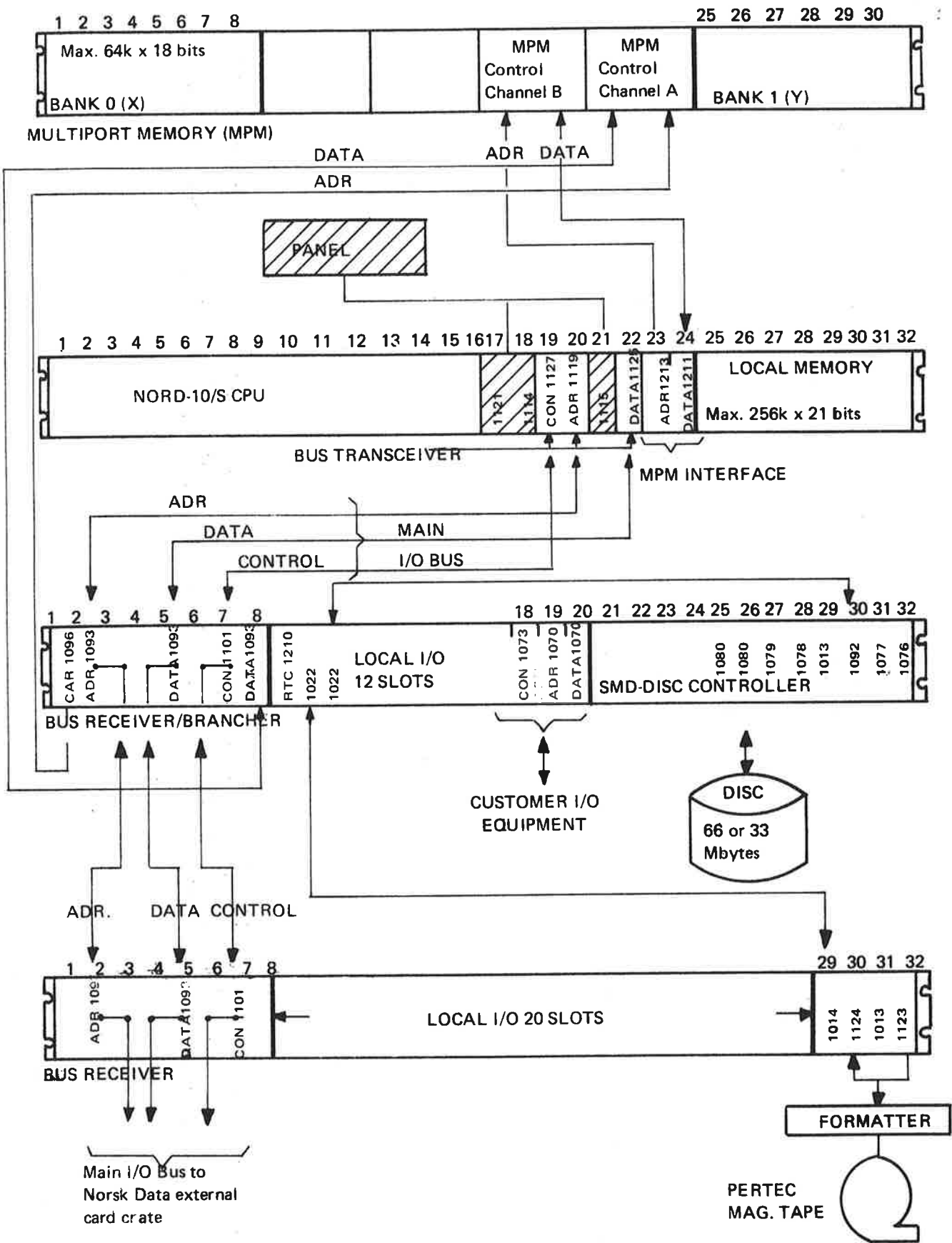


Figure 1.4: NORD-10/S EXAMPLE OF I/O CONFIGURATION



## 2. PROGRAMMED INPUT/OUTPUT (PIO)

This chapter will deal with the programmed input/output interface and further usage and implementation of the IOX instruction.

On each interface module there are at least three registers:

- 1- Data Register
- 1- Control Word Register
- 1- Status-Register

These registers are sufficient for a one way data flow interface. For a two-way data flow interface, communicating both ways as a teletype or modem, twice the amount of registers is necessary, 3 registers for output and 3 registers for input.

### *Data Register:*

There are two kinds of data registers; a register operating as a latch (in use on interfaces for parallel-data transfer, eg., tape-reader, tape punch, card reader, line printer).

or

Serial input/parallel output register or parallel input/serial output register, in use on interfaces for serial-data transfer, eg., teletype, display, modem.

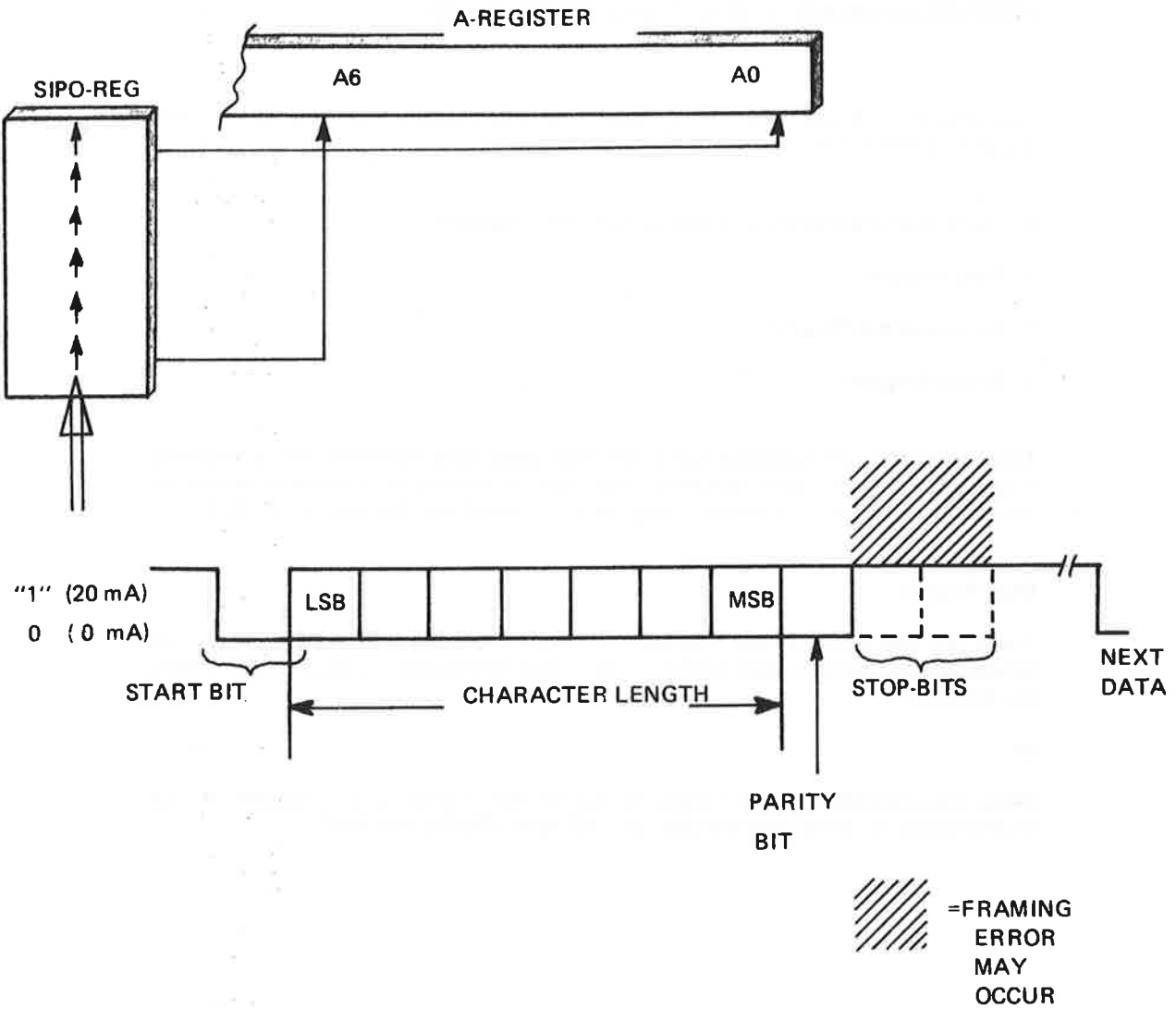


Figure 2.1: ASCII SERIAL FORMAT

*Control Word Register:*

- Activate device  
Feed card, advance paper-tape to next sprocket, print character if Bit 2 is set.
- Set mode of operation  
Test mode if Bit 3 is set
- Enables for interrupt: Bit 0 and 1
- Set character length, number of stop bits and parity on teletype and modem interfaces: Bit 11 to 14

*Status Register:*

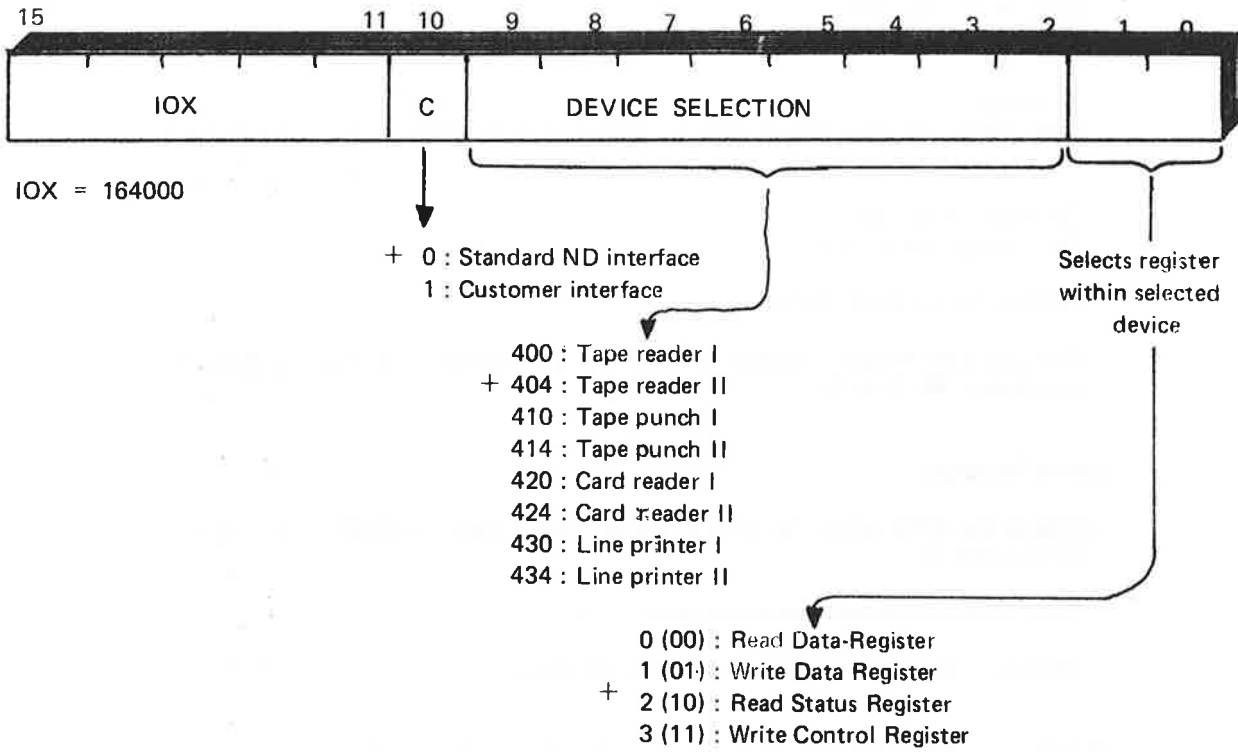
- Inform the CPU when the data is ready if input and data buffer are empty of output: Bit 3
- The quality of the data-transfer is given in Bit 4
- The interrupt enabled can be examined in Bit 0 and 1

The Standard ND format of the Control-Word and Status Register is given in chapter 2.4.

*PIO Interface Register Addressing:*

Each interface register is identified with its address. The address is given in the 11 lower bits of the Instruction-Register executing an IOX-instruction. A maximum of  $2^{11}$  i.e.  $3777_8$  or  $2048_{10}$  registers may be specified. Half of these addresses are used for standard ND interfaces while the second half are assigned for customer designed interfaces. 0-1777 = ND and 2000-3777 = Customer.

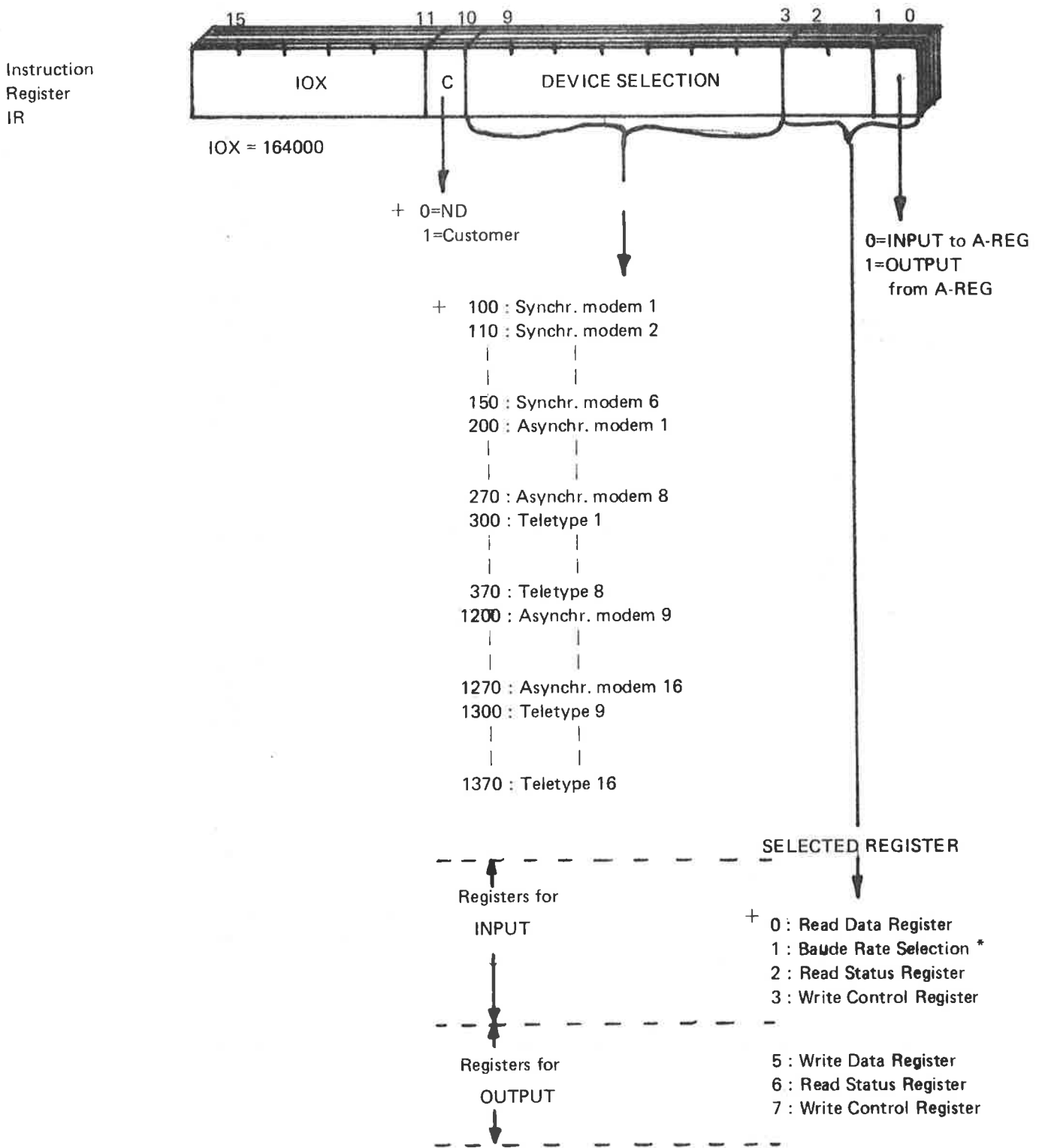
Different device-interfaces will require a different number of registers. One-way devices will usually require at least three different IOX-instructions (addresses), while two-ways and more complex interfaces as the DMA interfaces may need up to 8 registers addressed by 8 IOX instructions. The device addresses for a one way interface are in increments of four. Four device addresses per interface where the fourth register is normally a data register used for test purposes. Writeable for test pattern if input device and readable for test pattern if output device.



EX: Read Card Reader Status Register = 164422

**Figure 2.1.1: IR-REGISTER DURING AN IOX INSTRUCTION TRANSFERRING DATA TO/FROM A ONE-WAY DEVICE REGISTER**





\* Datarate selection possible on:

- 4 ASYNC CURRENT LOOP INTERFACE 1122
- 2 ASYNC MODEM INTERFACE 1147
- TERMINAL BUFFER 1095

Figure 2.1.2: TWO WAY DEVICE REGISTERS

## 2.1 THE INTERFACE AND THE IOX-INSTRUCTION

While executing, an IOX instruction the 11 lower bits of the IR-register are enabled to the address-bus (main and local). On each interface module the DEVICE SELECTION address bits, bits 2-9, if one-way and bits 3-9 if two-ways interface are compared against the address of the module. (Refer to figure 2.2).

These address bits on the module can either be given by straps or by switches. When the input to the comparator are equal (in pairs) the device address is recognized and a DEVICE EQUAL signal is generated. This signal activates the decoder, decoding the 2 or 3 least significant address-bits (BAO-2) selecting the proper register within the interface.

OUTPUT operation: (BAO = 1)

During an output operation (Ex.: IOX LOAD CONTROL WORD-REGISTER or IOX WRITE DATA REGISTER) the data on the data bus BD equal to the A-register is clocked into the proper register. The CONNECT signal can now be returned to CPU.

INPUT operation: (BAO = 0)

The register control signals from the decoder active during an INPUT-operation will:

- Select/enable the proper register out on the BD data-bus
- Be OR'ed together generating the INPUT-signal

When the input data is enabled out on the BD-bus, the CONNECT signal can be returned to the CPU.

The INPUT signal will enable the I/O Data-Bus on to the CPU data bus IB in the BUS TRANSCIEVER. The returned CONNECT signal will generate a clock signal to the H-register clocking the IB-bus. The H-register is then transferred to the A-register via the arithmetic.

As shown in figure 2.3, it may be possible to perform both an output and an input transfer on the same IOX instruction. This is done by delaying the CONNECT and INPUT signal until the BD-bus is strobed by the device. Standard ND produced interfaces are not using this feature, therefore, after an IOX input operation, the A-register will be a copy of the selected register.

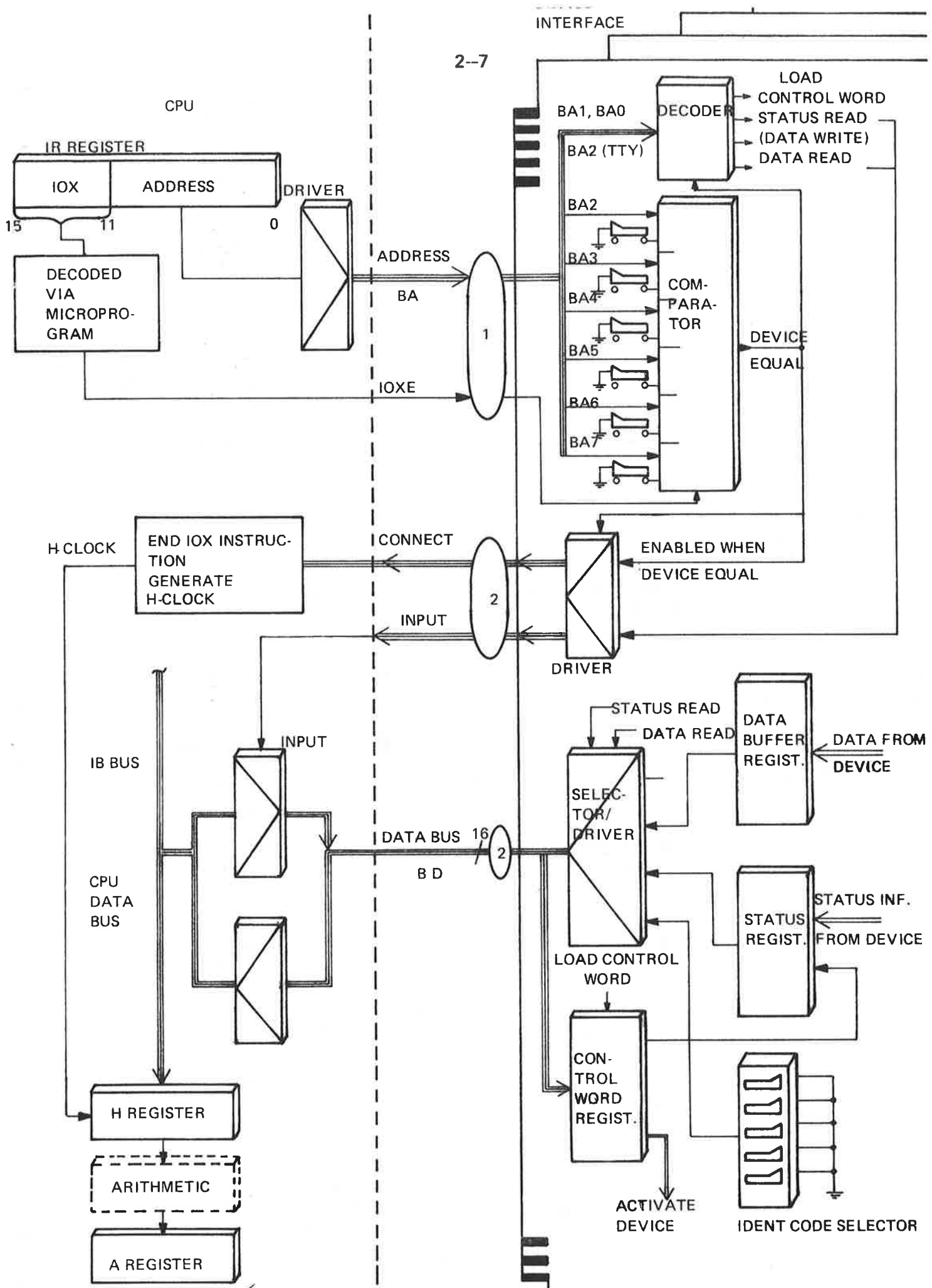
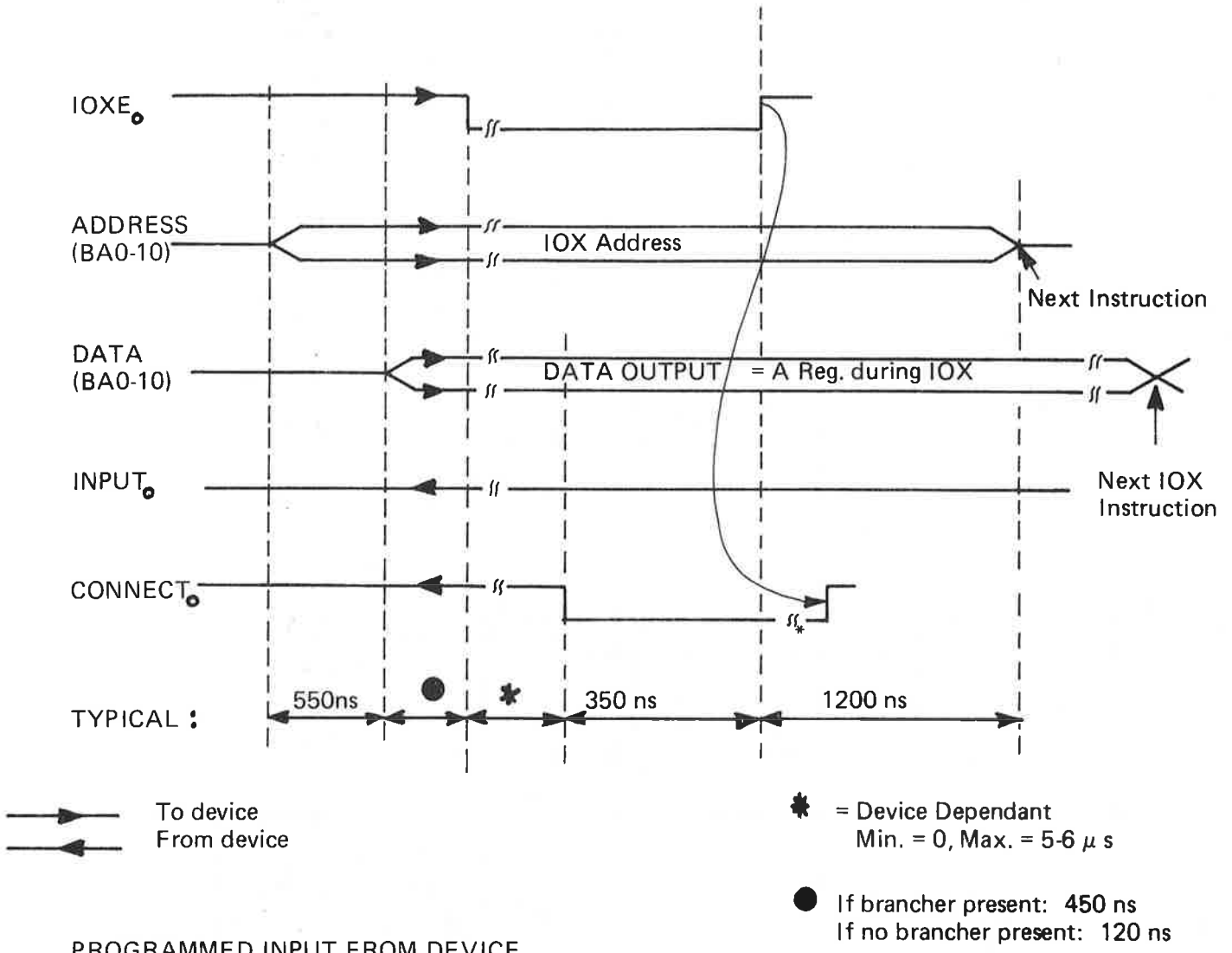


Figure 2.2: NORD-10/S COMMUNICATION WITH PIO INPUT INTERFACE



PROGRAMMED INPUT FROM DEVICE

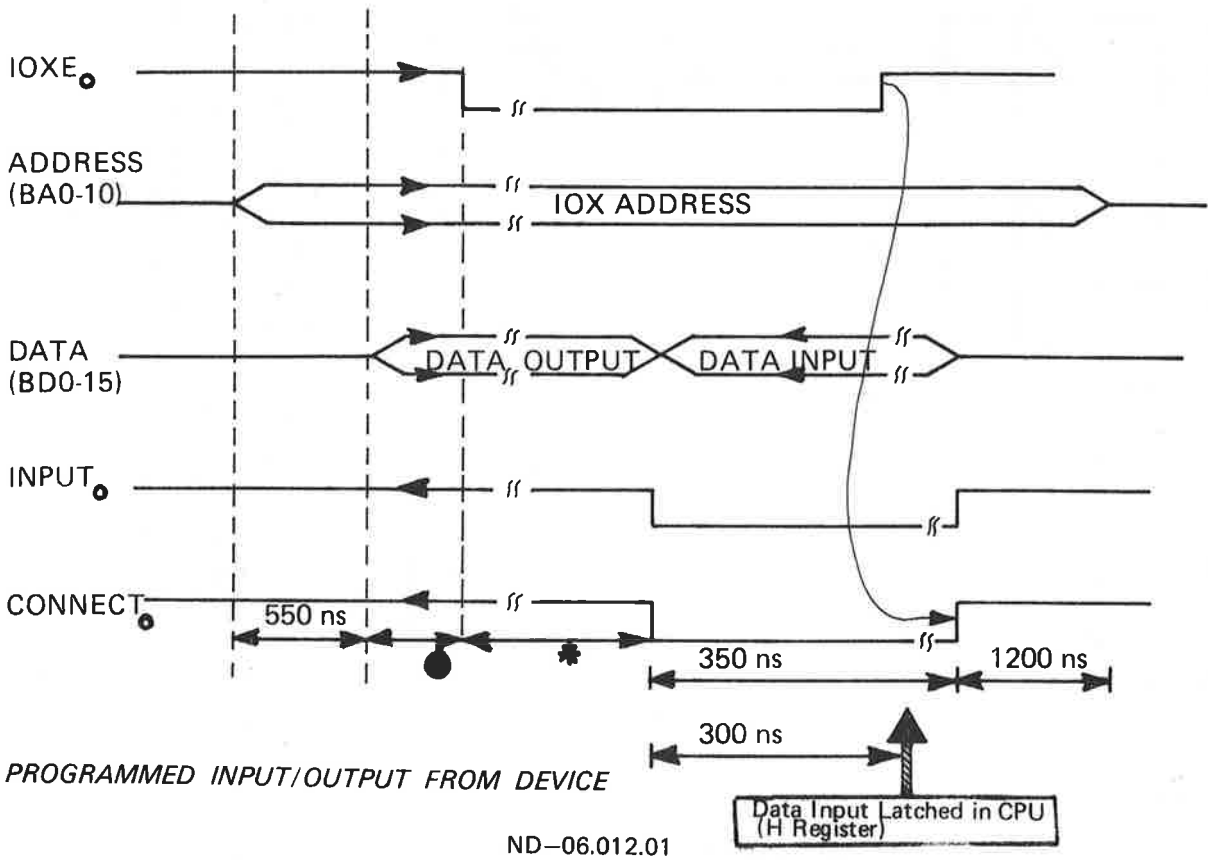


Figure 2.3: PROGRAMMED INPUT/OUTPUT FROM DEVICE

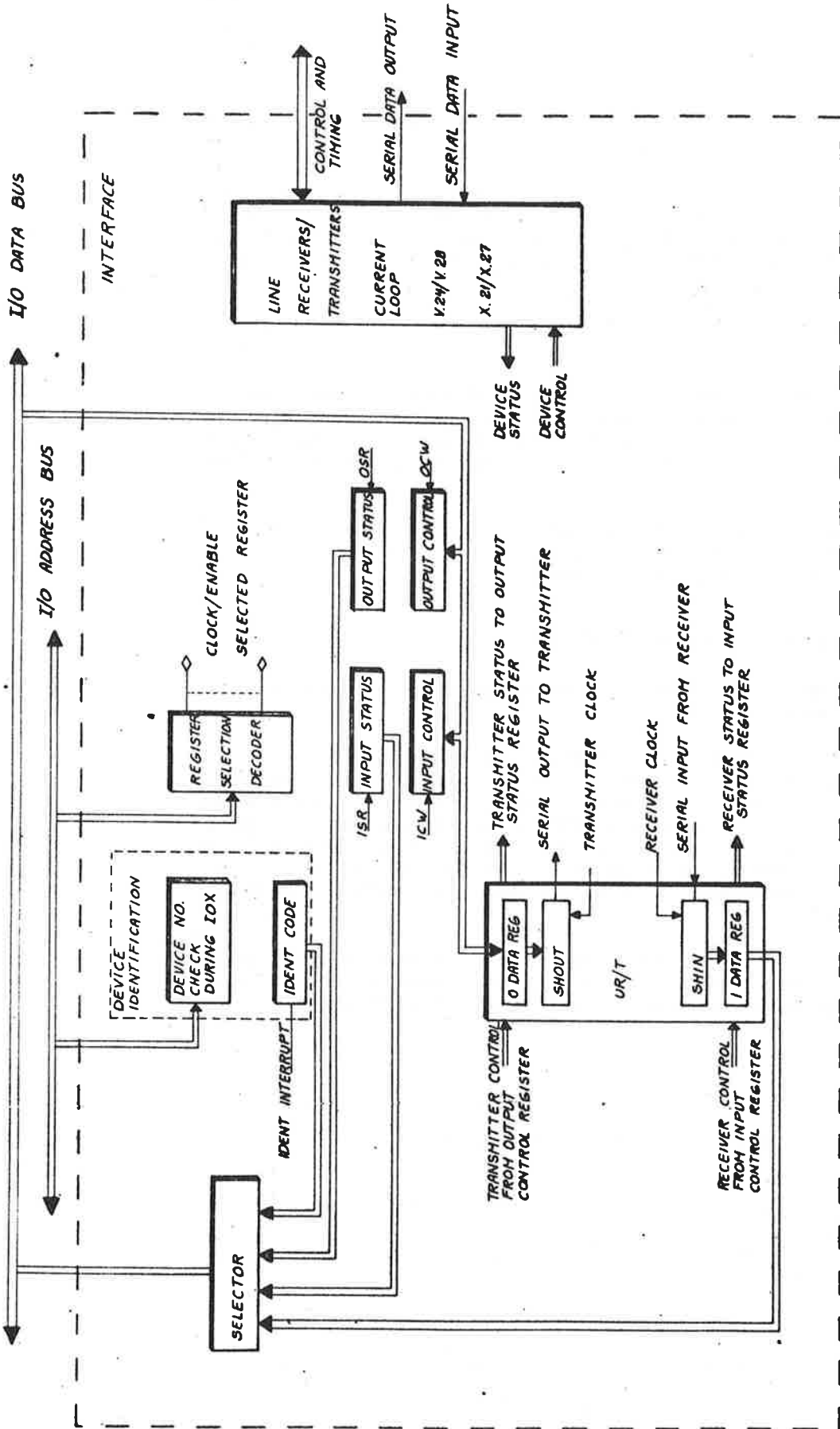


Figure 2.4: SERIAL TO PARALLEL/PARALLEL TO SERIAL INTERFACE PRINCIPLES

UR/T - UNIVERSAL RECEIVER/TRANSMITTER 40 PINS LSI CHIP

- ASYNCHRONOUS INTERFACES: UART - UNIVERSAL ASYNCH. REC. TRANSM.

- SYNCHRONOUS INTERFACES: USRT - UNIVERSAL SYNCH. REC. TRANSM.

- HDLC INTERFACE: MPCC - MULTI PROTOCOL COMM. CONTROLLER

Revised	Date	Edn.
SERIAL TO PARALLEL PARALLEL TO SERIAL INTERFACE PRINCIPLES		Year 00/01 P 5.5 '96
A/B WORK DATA-ELECTRONIK		Rev. EDC
		Appr.

## 2.2 IOX INSTRUCTION EXECUTION CPU

### General:

The microprogrammed NORD-10 CPU executes an IOX-instruction by fetching, clocking and decoding three micro-instructions located in the 32 bits wide Read Only Memory (ROM). In the following some remarks will be given to figure 2.5 IOX TIMING. Refer also to figure 2.6 for the CPU data and address flow.

### Remark 1:

The IOX instruction is clocked into the Instruction-Register by a positive edge of the CIKL-signal, derived from the memory data ready signal MDRY. The device-address (IRO-10) is now available on the address-bus. The IREN signal is always active except during DMA. Refer to TRANSCEIVER ADDRESS module 1119.

After 200-220ns including entry-point generation, and ROM-access time, the content of ROM address 172 is clocked into the 32 bits Micro-Instruction Register (MIR) given by the following mnemonics:

172/IOX, LOGM ADIR A,A BIO D, IO (or in words):

Select the A-register through the A-operated-selector and enable it out on the IB bus. The destination is the I/O bus.

The signal TRIO is decoded from the MIR-bits and since the IOX instruction is a privileged instruction, only allowed to be executed from memory pages belonging to ring 2 or 3, the signal is checked against the Paging-Control Register bits on the Interrupt Control 1058 module. This checking takes 100ns. On the TRANSCEIVER CONTROL module 1127 the signal TRIO and TRR (decoded from MIR when A-reg-output operation) are ANDed together generating the TRRIO signal that in turn set the IOCYC flip-flop (Input/Output cycle in progress).

The RIB signal enables the IB-bus out on the D-bus (TRANSCEIVER DATA module 1125). The IOCYC flip-flop set generates a memory data-ready-signal (MDRY). This in turn clocks the second microinstruction into MIR, entering.

### Remark 2:

ROM address 173:  
LOGM A,IO BIO % I/O-BUS→H-REGISTER

The TRRIO signal disappears and the D-bus is clocked into the Q latch (QO-Q15). The IB→D bus signal (RIB) and MDRY is removed. The A-register is now available on the Main I/O Bus MO-15. The TRAI0 signal decoded from the bits now in MIR generates the:

- IOXE signal; the Master Data and Address-Enabling signal
- RM signal; Enabling the M-bus out on the D-bus
- EIB signal; Enabling the D-bus out on the IB-bus

The CONNECT signal will be returned from the device interface recognizing the address together with the INPUT signal. The returned CONNECT-signal is delayed (DCON), ensuring stable data on the M-bus.

EM signal generation:

At DCON time the EM signal is generated depending on the state of the returned INPUT-signal.

INPUT TRUE (EM not TRUE):

- The Q latch is disabled from the M-bus. Data to IB is taken from the MAIN I/O data-bus.

INPUT NOT TRUE (EM TRUE):

- The Q latch is enabled onto the M-bus and fed back to the IB bus.

The DCON signal generates a memory-data ready signal (MDRY) and the IB-bus is clocked into the H-register. If no CONNECT signal is returned from the addressed interface within 5-6  $\mu$ s, a TIMEOUT signal is generated.

The TIMEOUT signal does:

- 1. Generate a MDRY signal for hang-up prevention.
- 2. Generate a internal-interrupt to level 14 (IOERR) if Interrupt-system is turned on.

The MDRY signal in turn clocks the third microinstruction into MIR entering.

*Remark 3:*

MIR now contains:

```
LOGM  CFC  ADIR  A,H  D,A  %  H-REG→A-REG  NEXT-INSTRUCTION
FETCH.
```

The TRAI0; IOXE; EIB and the RM signals disappear and as a response to removed IOXE, the CONNECT and INPUT signal will be dropped by the device-interface.

A removed CONNECT signal will reset the IOCYC flip-flop, indicating the I/O BUS is ready for new activity (DMA transfer or a new IOX).

During the activities mentioned, the H-register is selected as A-operand direct through the most significant arithmetic and enabled onto the most significant SUM-bus. In parallel with the H-register through the arithmetic, the next instruction is fetched from main memory. The next instruction is clocked into IR and the SUM-bus is clocked into the A-register, ending the story of the IOX instruction with this GENERAL REMARK:

- If an OUTPUT-operation, the content of the A-register is written back to itself.
- If an INPUT-operation, the data enabled out on the I/O data-bus is written into the A-register.

IOX TIMING

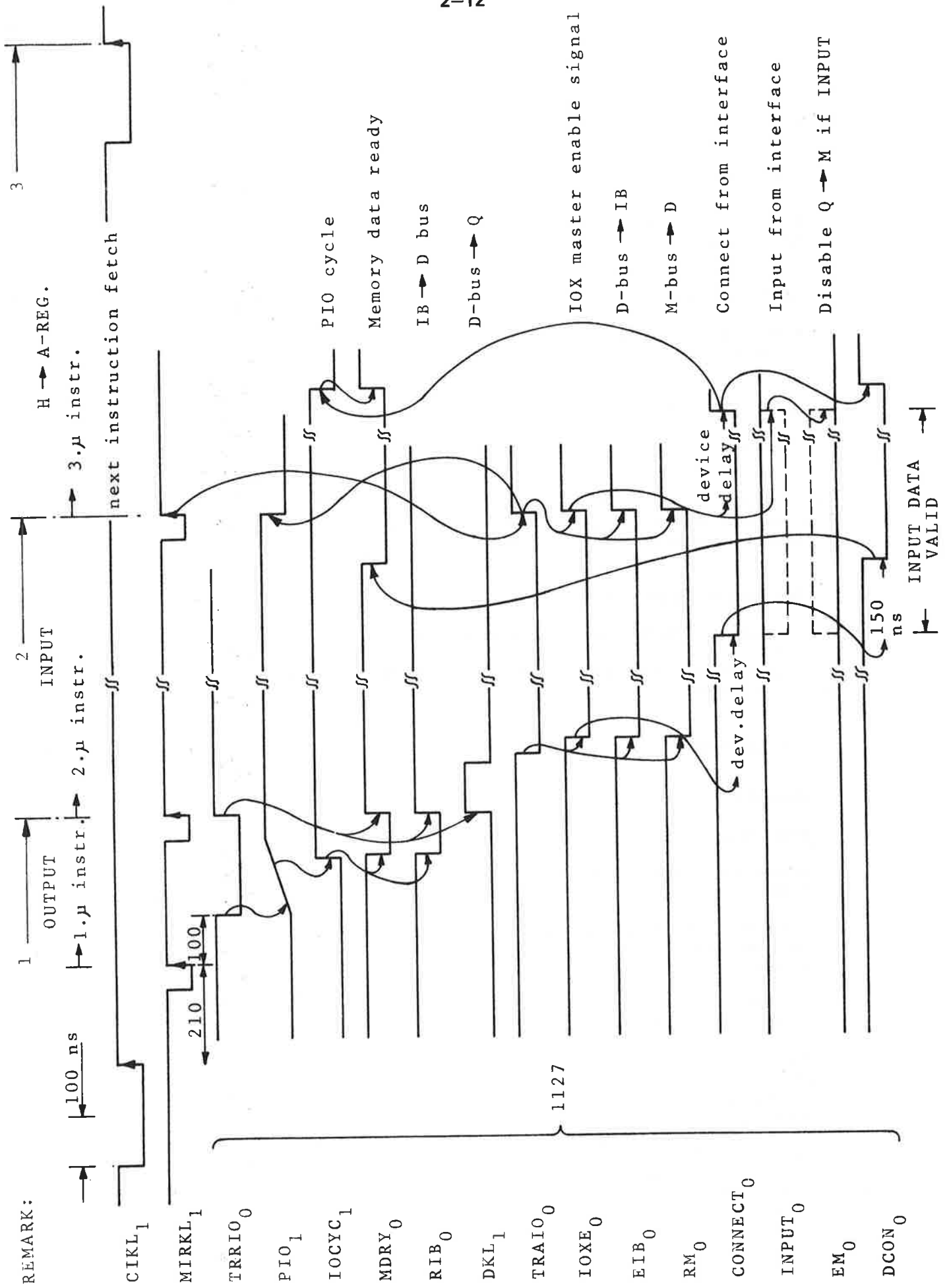


Figure 2.5: IOX TIMING



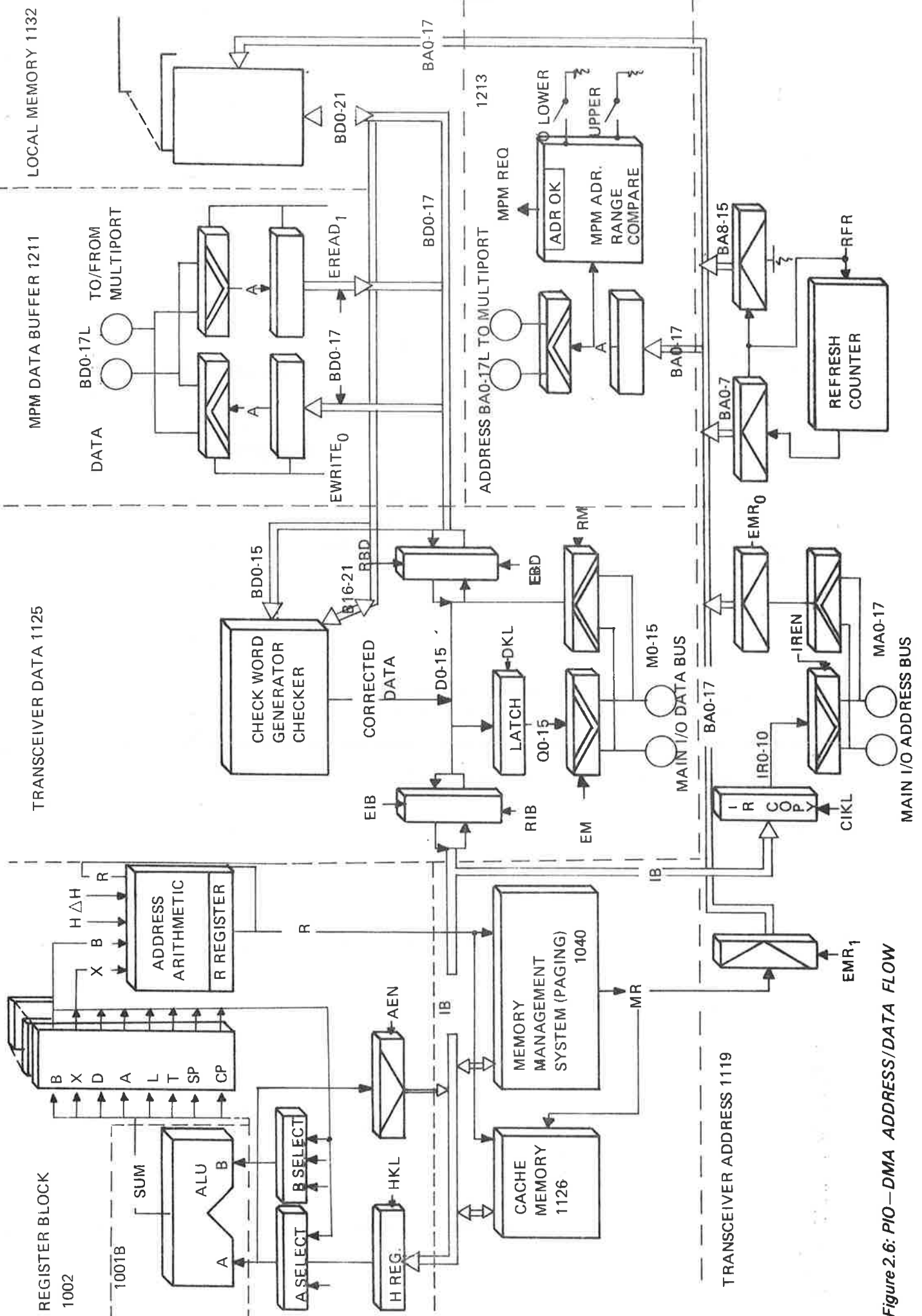
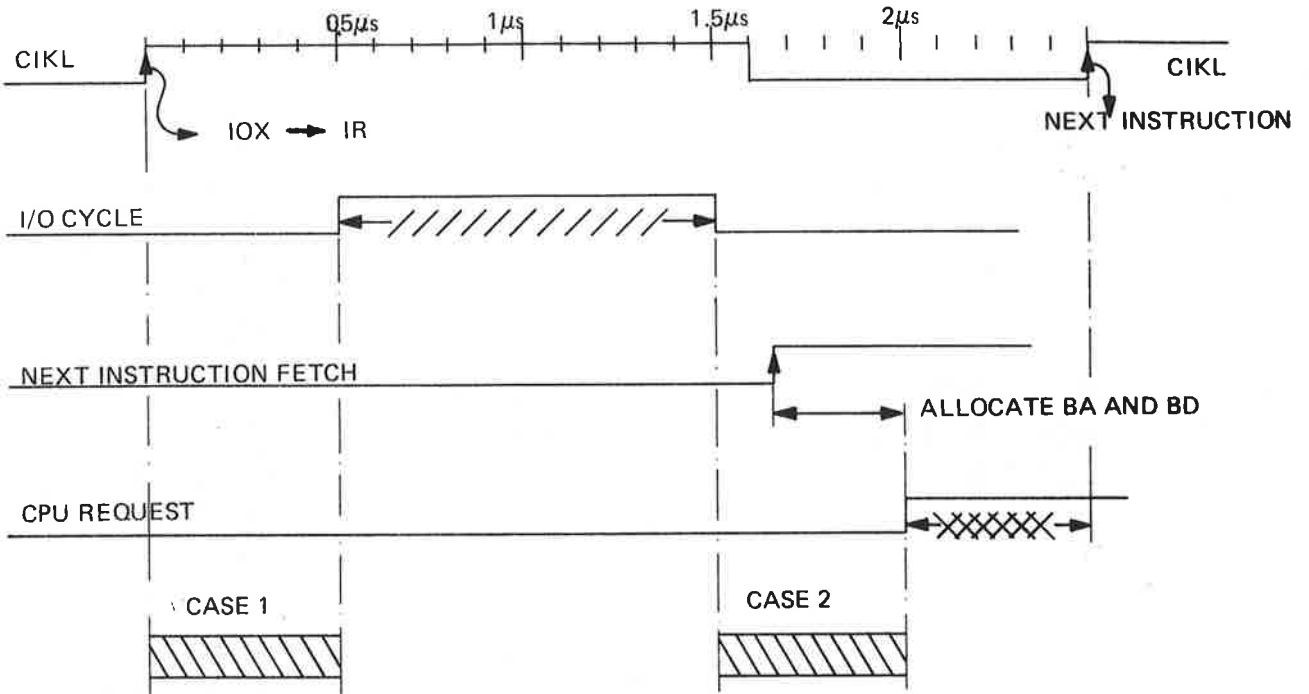


Figure 2.6: PIO—DMA ADDRESS/DATA FLOW

IOX EXECUTION AND BUS USAGE



////// The Main and Local I/O bus is used by the IOX instruction. The CPU data bus IB is also allocated for the IOX instruction.

Duration: from 1-5  $\mu$ s, dependent on device response.

XXXXXX The memory address bus BA and data bus BD together with the IB bus is allocated the CPU.

Duration: this time depends on the memory response time.

Typical:

0.5  $\mu$ s for local memory

1.0  $\mu$ s for multiport memory

//////// In this period the I/O Bus may be allocated a DMA-transfer to the local memory or multiport memory via the CPU port.

CASE 1: The IOCYCLE is started when the DMA-transfer has finished.

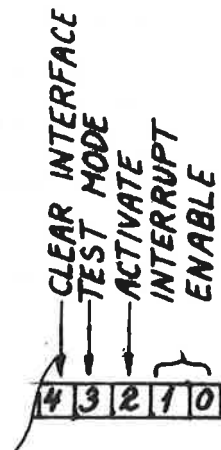
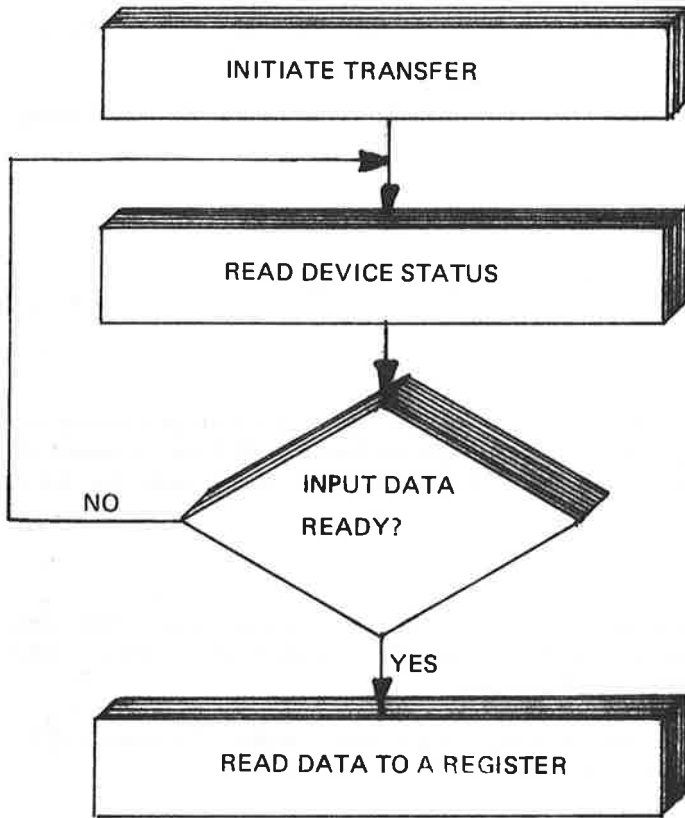
CASE 2: The CPU Request must wait until the DMA-transfer has finished.

Figure 2.7: IOX EXECUTION AND BUS USAGE

### 2.3 PROGRAMMING A PIO INTERFACE

#### INPUT

The flow diagram below shows the communication between the CPU and the interface for reading one word or byte of data.



The transfer is initiated by setting the CONTROL-WORD REGISTER informing of:

- Mode of operation
- Interrupt enabling
- Device activation

CW

```
LDA CW
IOX LCW
```

The presence of input-data is checked by reading the STATUS-register. Bit 3 in the interface status register is set to a one when parallel data is clocked or serial data is assembled in the DATA-register.

```
LOOP, IOX RSTAT
      BSKP ONE 30 DA
      JMP LOOP
```

The program will loop until bit 3 in the STATUS-REGISTER is set. The data can now be transferred to the A-register.

The advantage of interrupt-programming is clearly stated by this looping waiting for the DATA-READY.

#### WITHOUT INTERRUPT:

The CPU will do nothing but monitor bit 3 in the status register.

#### WITH INTERRUPT:

With the interrupt system in the CPU turned on, and the interface enabled for interrupt, the interface will tell the CPU when the DATA is READY by means of an interrupt signal. This enables the CPU to do other tasks while the data-transfer takes place.

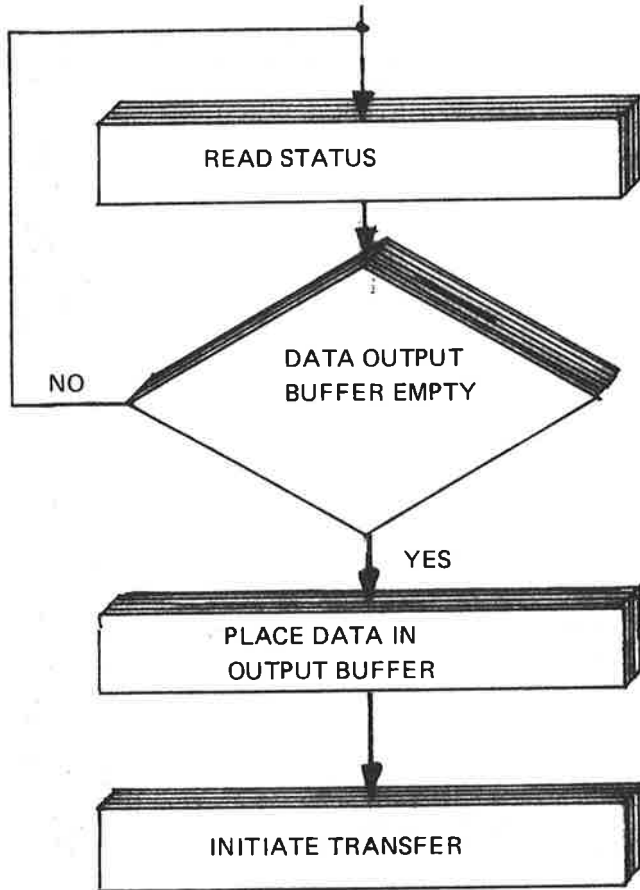
#### Example:

With the interrupt system turned on the CPU can execute about 1500-2200 instructions between two DATA-READY (sprocket) pulses when reading data from a TAPE-READER (330 character/sec).

At DATA-READY time the data is transferred to the A-register by means of an IOX read-data register instruction.

The data must then be stored away before the next transfer is initialized.

OUTPUT:



The interface STATUS-REGISTER is read, and bit 3 is checked for a 1. If a 1, this implies that the previous data transfer was finished and new data can be placed in the output data buffer. If NOT, loop.

```

    IOX RSTAT
    BSK ONE 30 DA
    JMP *-2
    BIT 3=1
    IOX WDATA
    IOX LCW
  
```

Transfer A-register to output-buffer:

Transfer A-register to control-word register:

With bit 2 set to a one:

This will initiate the move of data from the buffer-register in the interface to the physical device.

### 2.3.1 *FORMAT OF STATUS AND CONTROL WORD*

The format of status and control word may be assigned by the designer of each device controller. The following standard is used by ND for its own device control cards (when applicable) and is recommended for customer use.

#### *STATUS WORD*

Bit 0	Ready for transfer, interrupt enabled
Bit 1	Error interrupt enabled
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors
Bit 5	Error indicator
Bit 6	Error indicator
Bit 7	Error indicator
Bit 8	Error indicator
Bit 9	Selected unit
Bit 10	Selected unit
Bit 11	Operational mode of device
Bit 12	Operational mode of device
Bit 13	Operational mode of device
Bit 14	Operational mode of device
Bit 15	Operational mode of device

#### *CONTROL WORD*

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Enable interrupt on errors
Bit 2	Activate device
Bit 3	Test mode
Bit 4	Device clear
Bit 5	Address bit 16
Bit 6	Address bit 17
Bit 7	Not assigned
Bit 8	Not assigned
Bit 9	Unit
Bit 10	Unit
Bit 11	Device operation
Bit 12	Device operation
Bit 13	Device operation
Bit 14	Device operation
Bit 15	Device operation

### 3 PROGRAMMED INPUT/OUTPUT LOCAL I/O BUS SIGNALS

The following signals on the local I/O Bus are relevant for programmed input/output:

	<i>Name:</i>
DATA	BD xx
ADDRESS	BA xx
IOXE	BIOXE
CONNECT	BCONNECT
INPUT	BINPUT
MASTER CLEAR	BMC
16 DATA Source: Device or CPU	16 tristate lines carrying the data information from the CPU or from the device depending upon the control signal INPUT.
11 ADDRESS Source: CPU	Bit 0-9: Gives the value of the 10 least significant bits of the CPU instruction register, i.e., the device register address during an IOX-instruction.  Bit 10: Instruction register bit 10. IR10=0 ND standard interfaces IR10=1 Customer produced interfaces.
1 IOXE Source: CPU	IOX instruction master enable and timing signals. On the BRANCH CONTROL module this signal is input to circuits generating either a local IOXE (BIOXE) or an external IOXE (EIOXE) signal. Whether to generate BIOXE or EIOXE is given by IR bit 10 and a strap on the BRANCH CONTROL module.
1 BIOXE Source: BRANCHER	If strap closed: Local IOXE signal for IR10=0): Address < 2000 If strap open: Local IOXE signal for IR10=1): Address > 2000
1 EIOXE* Source: BRANCHER	External IOXE signal supplied to the customer via the bus driver/receiver modules. *This signal is not in the local I/O bus.

## 1 CONNECT

Source:

Device

A device answer on the IOXE signal has been received and that the device has:

- Decoded the ADDRESS bits 0-9 and recognized one of its device register addresses.
- If INPUT: The input DATA is enabled out on the BD data-bus
- If OUTPUT: The DATA on the BD-bus equal the A-register is taken care of by the device

CONNECT has to be returned within a specified time (max.5-6 $\mu$ s) otherwise the CPU will generate an internal interrupt on level 14 (IOX error).

## 1 INPUT

Source:

Device

Defines the direction of the data lines. INPUT true; data transferred from device to CPU A-register. INPUT false; data transferred from CPU A-register to device.

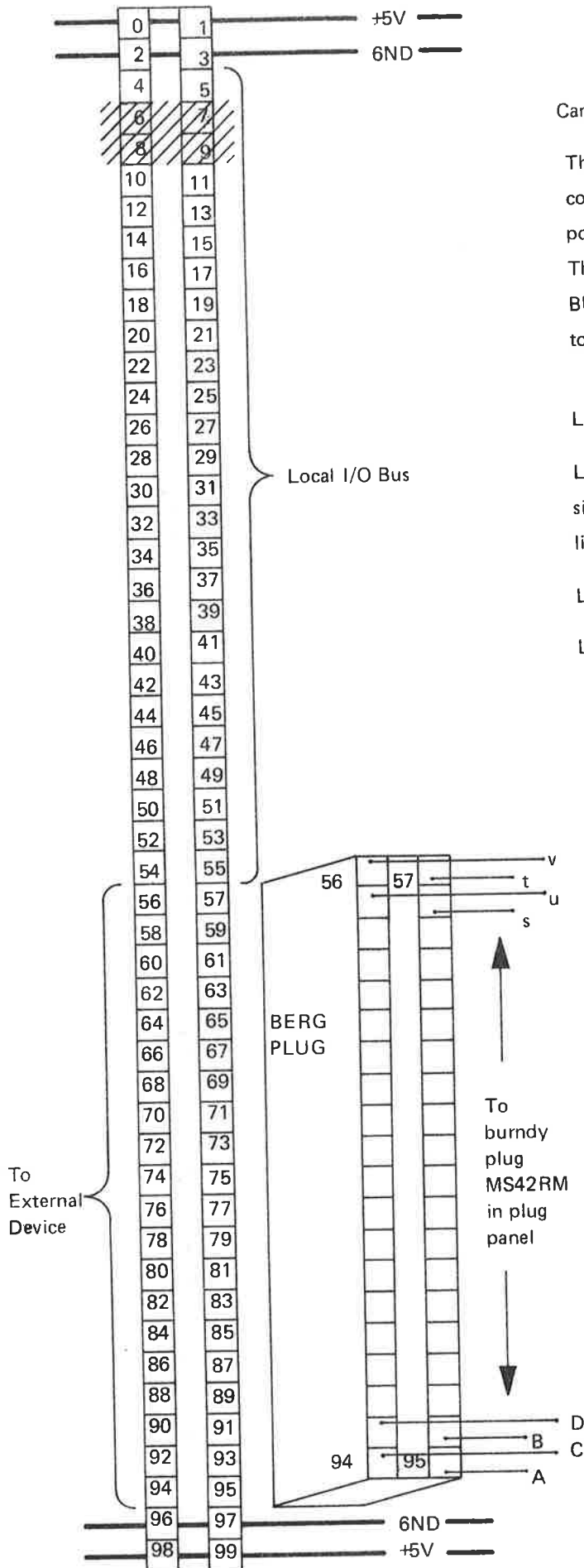
## 1 MASTER CLEAR

Source:

CPU

Used to clear the logic in the device controllers.





Card Module:

The interface module is fit into a 100 terminal connector where 4 of the terminals are used for power (+5V) and 4 terminals for ground (GND). The terminals 4-55 are assigned for the local I/O BUS, while terminal 56-95 are used for connection to the external device via the plug-panel.

Local I/O Bus Signal Levels:

Local I/O Bus signals are TRI-STATE TTL for all signals except interrupt lines and DMA request line, which are open collector TTL.

Logical "1" signal  $0 \leq S \leq 0,4V$

Logical "0" signal  $2,4 \leq S \leq 5V$


 These terminals do not have a 1-1 connection to the next I/O position (used for IDENT and GRANT)

Figure 3.1: I/O SLOT/PLUG LAYOUT



## 4 I/O INTERRUPT-SYSTEM

In this chapter some general remarks regarding the NORD-10/S interrupt system will be given together with information about the IDENT instruction.

### 4.1 NORD-10/S INTERRUPT SYSTEM GENERAL DESCRIPTION

The interrupt system consists of 16 program levels in hardware, each program level with its own complete set of general registers and status indicator. The program levels are numbered from 0 to 15 with increasing priority; program level 15 has the highest priority, program level 0 has the lowest.

The program levels are controlled from the two 16-bit registers:

- PIE-Priority Interrupt Enable Register
- PID-Priority Interrupt Detect Register

Each program level is controlled by the corresponding bits in these registers. The PIE register is program controlled, set from the A-register, and the PID register is controlled by both program and external asynchronous interrupt. At any time, the highest program level, which has its corresponding bits set in both PIE and PID, is running. This level is called PL, current program level. Refer also to figure 4.1.

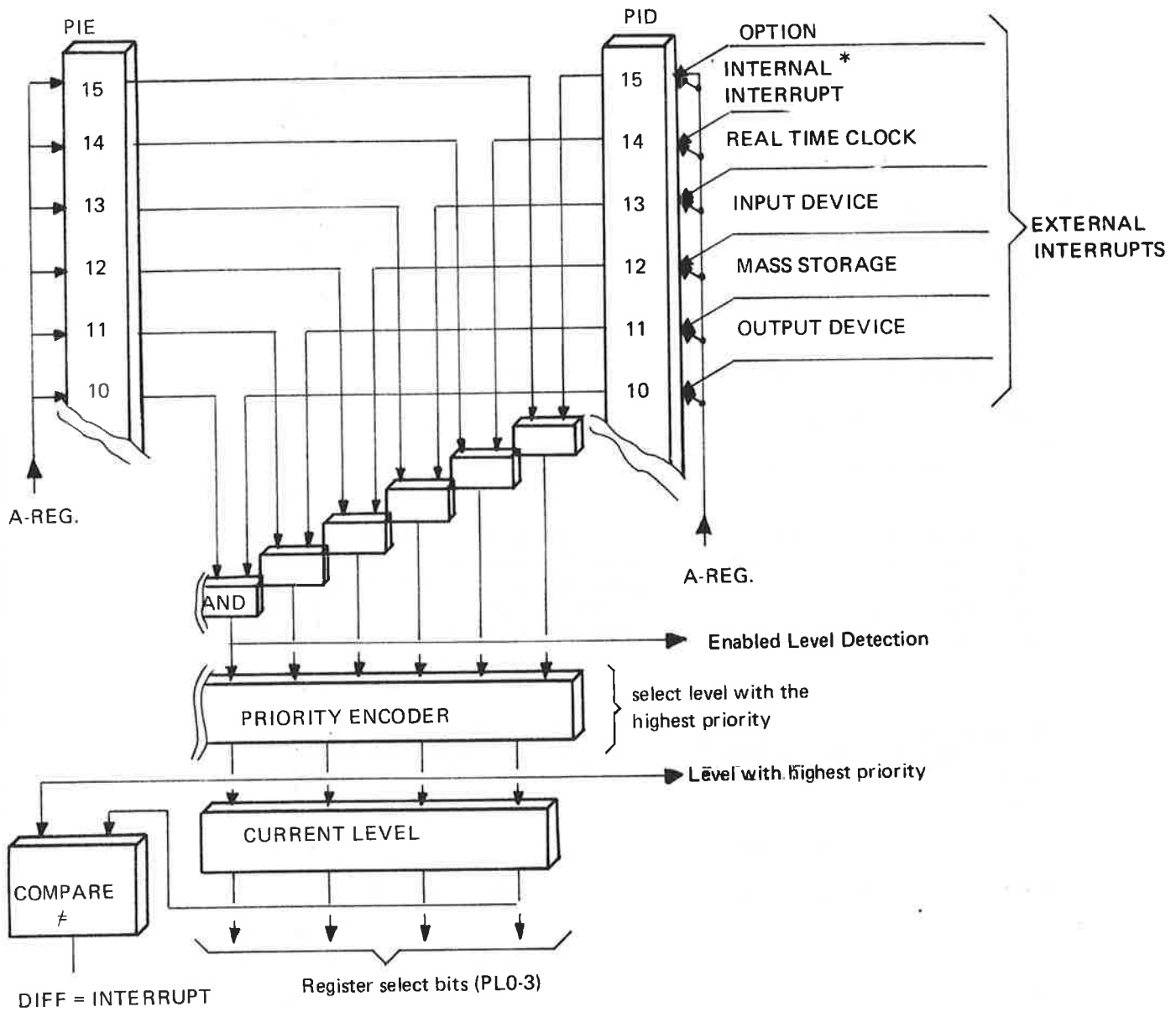
A change from a lower to a higher program level occurs when a bit in the PID register with higher priority than the running one is set. (The corresponding PIE bit must also be a one). This setting of the PID-register can take place in two ways:

1. Set by program; Programmed Interrupt
2. Set by the I/O system (PID bit 15, 13, 12, 11 and 10); I/O interrupt

A change from a higher program level to a lower takes place when the program on the higher program level gives up its priority. This done by executing a WAIT instruction on the current level.

At CHANGE-LEVEL time, this takes place in hardware:

- 1)The current program-level address is saved in the saved program counter, SP register.  $CP \rightarrow SP_{current\ level}$ .
- 2)The current-level indicator is set with the new level (4 bits code PL0-3). Selecting the register block for the new level.
- 3)The SP for the new level is transferred to Current Program Counter CP.  $SP_{new\ level} \rightarrow CP$ .



\* Internal interrupt LEVEL 14 NO CONNECT error, IOX-timeout is one source.

Figure 4.1: NORD-10/S INTERRUPT SYSTEM

## 4.2 I/O INTERRUPT

External interrupts may set PID bits 15,13,12,11 and 10. Program level 15 is not used by standard NORD equipment or software but is available for users who need immediate access to the CPU.

LEVEL:

13: Real Time Clock interrupt (Interrupt every 20ms.)

12: Input devices

11: Mass-storage or DMA devices

10: Output devices

An interrupt on level 12-10 may occur for two reasons:

1. Data Ready interrupt
- or
2. Error interrupt

A Data Ready interrupt indicates that for an input device, the data is ready to be transferred to the A-register. For an output device, the output-buffer is empty and new data may be transferred from the A-register to the buffer.

A Data Ready interrupt from a DMA-device indicates that the data-transfer is completed.

An Error Interrupt will occur if the data transfer was unsuccessful.

### 4.3 *INTERRUPT IDENTIFICATION*

For program levels 10,11,12 and 13 it is required to identify the I/O interrupt when it occurs, since several sources may be connected to the same level. This identification process is available through the instruction:

IDENT <program level>

The IDENT instruction is used to identify and service the actual interface that generated the interrupt. Actually there are four IDENT instructions, one to identify and service I/O interrupts on each of the four levels 10,11,12 and 13.

The four instructions are:

IDENT PL10 Identify Input/Output interrupt on level 10 Code:143604

IDENT PL11 Identify Input/Output interrupt on level 11 Code:143611

IDENT PL12 Identify Input/Output interrupt on level 12 Code:143622

IDENT PL13 Identify Input/Output interrupt on level 13 Code:143643

The result of the IDENT instruction is a unique identification code returned from the interrupting interface to the A-register. The 9 bits code is given in A-reg bits 0-8, with bits 9-15 all zeros.

If the IDENT instruction is executed, but there is no device to serve, the A-register is unchanged. An IOX error interrupt to level 14 (TIMEOUT) will occur if enabled.

If several devices on the same program level have simultaneous interrupts, the priority is determined by which Input/Output slot the device is plugged into. The interrupt line to the corresponding PID bit will remain active until all devices have been serviced. When an interface responds to an IDENT, the INTERRUPT-ENABLE flip-flop is turned off, and the interrupt-signal is dropped. The INTERRUPT-ENABLE flip-flop must then be set by software before the next interrupt can be handled.

For program level 15, however there is no IDENT instruction, since there should be only one source for this interrupt.

## APPENDIXES





## DETAILED CONTENTS

<i>SECTION:</i>		<i>PAGE:</i>
A	SIGNAL DISTRIBUTION WITHIN ONE CARD RACK	A-1
B	STANDARD NORD-10 DEVICE NUMBERS AND IDENT CODES	B-1
C	TEST LOOPS	C-1
D	PROGRAM SPECIFICATION	D-1
E	ASC II BINARY FORMAT	E-1
F	CARD MODULES	F-1
G	DRAWINGS	G-1
H	NORD 10 I/O SYSTEM HISTORIC OVERVIEW	H-1



## APPENDIX A

## SIGNAL DISTRIBUTION WITHIN ONE CARD RACK

	<i>Terminal No.</i>
DATA BIT 0	10
DATA BIT 1	12
DATA BIT 2	13
DATA BIT 3	14
DATA BIT 4	16
DATA BIT 5	17
DATA BIT 6	18
DATA BIT 7	20
DATA BIT 8	21
DATA BIT 9	22
DATA BIT 10	24
DATA BIT 11	25
DATA BIT 12	26
DATA BIT 13	28
DATA BIT 14	29
DATA BIT 15	30
ADDRESS BIT 0	32
ADDRESS BIT 1	33
ADDRESS BIT 2	34
ADDRESS BIT 3	36
ADDRESS BIT 4	37
ADDRESS BIT 5	38
ADDRESS BIT 6	40
ADDRESS BIT 7	41
ADDRESS BIT 8	42
ADDRESS BIT 9	44
ADDRESS BIT 10	45
ADDRESS BIT 11	46
ADDRESS BIT 12	48
ADDRESS BIT 13	49
ADDRESS BIT 14	50
ADDRESS BIT 15	52
ADDRESS BIT 16	53
ADDRESS BIT 17	54
OUTIDENT	6
INIDENT	7
OUTGRANT	8
INGRANT	9
IOXE	11
INPUT	15

	<i>Terminal No.</i>
MPX ADDRESS	19
CONNECT	23
INTERRUPT LEVEL 10	27
INTERRUPT LEVEL 11	31
INTERRUPT LEVEL 12	35
INTERRUPT LEVEL 13	39
INTERRUPT LEVEL 15	43
DMA REQUEST	47
DMA DATA READY	51
MASTER CLEAR	55
DEVICE INTER-CONNECTION	56-95
+ 5V	0,1,98,99
GROUND	2,3,96,97
BFO1 19,2 khz	4
BFO2 307,2 khz	5

## APPENDIX B

STANDARD NORD-10 DEVICE NUMBERS AND  
IDENT CODES

<i>Device No.</i>	<i>Interrupt Level</i>	<i>Ident Code (octal)</i>	<i>Device</i>	<i>SINTRAN III</i>
4- 7	13	4	Memory Parity N-12	
10- 13	13	1	Real Time Clock 1	
14- 17	13	2	Real Time Clock 2	
30- 33	12	16	NORD-50/1	
34- 37	10	16	ACM 5	
40- 43	10	15	ACM 1	
44- 47	10	25	ACM 2	
50- 53	10	40	ACM 3	
54- 57	10	41	ACM 4	
60- 77			NORD-50/1 Regs.	
100-107	10-12	4	Synchr. Modem 1	
110-117	10-12	14	Synchr. Modem 2	
120-127	10-12	20	Synchr. Modem 3	
130-137	10-12	24	Synchr. Modem 4	
140-147	10-12	30	Synchr. Modem 5	
150-157	10-12	34	Synchr. Modem 6	
200-207	10-12	60	Asynchr. Modem 1	Terminal 17
210-217	10-12	61	Asynchr. Modem 2	Terminal 18
220-227	10-12	62	Asynchr. Modem 3	Terminal 19
230-237	10-12	63	Asynchr. Modem 4	Terminal 20
240-247	10-12	64	Asynchr. Modem 5	Terminal 21
250-257	10-12	65	Asynchr. Modem 6	Terminal 22
260-267	10-12	66	Asynchr. Modem 7	Terminal 23
270-277	10-12	67	Asynchr. Modem 8	Terminal 24
300-307	10-12	1(120*)	Teletype 1	Terminal 1
310-317	10-12	5(121*)	Teletype 2	Terminal 2
320-327	10-12	6(122*)	Teletype 3	Terminal 3
330-337	10-12	7(123*)	Teletype 4	Terminal 4
340-347	10-12	44	Teletype 5	Terminal 5
350-357	10-12	45	Teletype 6	Terminal 6
360-367	10-12	46	Teletype 7	Terminal 7
370-377	10-12	47	Teletype 8	Terminal 8
400-403	12	2	Paper Tape Reader 1	
404-407	12	22	Paper Tape Reader 2	
410-413	10	2	Paper Tape Punch 1	
414-417	10	22	Paper Tape Punch 2	
420-423	12	3	Card Reader 1	
424-427	12	23	Card Reader 2	
430-433	10	3	Line Printer 1	
434-437	10	23	Line Printer 2	
440-443	10	11	Calcomp Plotter 1	
444-447	10	12	Card Punch 1	
454-457	10	13	Card Punch 2	

\* 4 CURRENT-LOOP MODULE 1122

<i>Device No.</i>	<i>Interrupt Level</i>	<i>Ident Code (octal)</i>	<i>Device</i>	<i>SINTRAN III</i>
500- 507	11	1	Disk System 1	
510- 517	11	5	Disk System 2	
520- 527	11	3	Magtape Controller 1	
530- 537	11	7	Magtape Controller 2	
540- 547	11	2	Drum 1	
550- 557	11	6	Drum 2	
560- 567	11	12	Drum 3	
570- 577	11	16	Drum 4	
600- 607	11	4	Versatec 1	
610- 617	11	11	Core-to-Core 1	
620- 637	11	10	CDC I/O Link	
640- 647	10-12	124		Terminal 33
650- 657	10-12	125		Terminal 34
660- 667	10-12	126		Terminal 35
670- 677	10-12	127		Terminal 36
700- 707	12	11	CATSY 1	
710- 717	12	21	CATSY 2	
720- 727			A/D Converter	
730- 737	10	10	D/A Converter	
750- 753	13	5	BIG MPM LOG module	
770- 773	12	17	Dig. Reg. 1 Input	
774- 777	10	17	Dig. Reg. 1 Output	
1000-1003	12	26	Dig. Reg. 2 Input	
1004-1007	10	26	Dig. Reg. 2 Output	
1010-1013	12	27	Dig. Reg. 3 Input	
1014-1017	10	27	Dig. Reg. 3 Output	
1020-1023	12	43	Dig. Reg. 4 Input	
1024-1027	10	43	Dig. Reg. 4 Output	
1030-1033	12	116	NORD-50/2	
1034			Watch Dog	
1035			Process Output 1	
1036			Process Output 2	
1037			Process Output 3	
1040-1043	12	15	Process Input 1	
1044-1047	12	25	Process Input 2	
1050-1053	12	40	Process Input 3	
1060-1077			NORD-50/2 Reg.	
1100-1107	10-12	130		Terminal 37
1110-1117	10-12	131		Terminal 38
1120-1127	10-12	132		Terminal 39
1130-1137	10-12	133		Terminal 40
1140-1147	10-12	134		Terminal 41
1150-1157	10-12	135		Terminal 42
1160-1167	10-12	136		Terminal 43
1170-1177	10-12	137		Terminal 44
1200-1207	10-12	70	Asynchr. Modem 9	Terminal 25
1210-1217	10-12	71	Asynchr. Modem 10	Terminal 26
1220-1227	10-12	72	Asynchr. Modem 11	Terminal 27
1230-1237	10-12	73	Asynchr. Modem 12	Terminal 28
1240-1247	10-12	74	Async 13/Photo 1	Terminal 29
1250-1257	10-12	75	Async 14/Photo 2	Terminal 30
1260-1267	10-12	76	Async 15/Photo 3	Terminal 31
1270-1277	10-12	77	Async 16/Photo 4	Terminal 32
1300-1307	10-12	50	Teletype 9	Terminal 9
1310-1317	10-12	51	Teletype 10	Terminal 10
1320-1327	10-12	52	Teletype 11	Terminal 11
1330-1337	10-12	53	Teletype 12	Terminal 12
1340-1347	10-12	54	Teletype 13	Terminal 13
1350-1357	10-12	55	Teletype 14	Terminal 14

<i>Device No.</i>	<i>Interrupt Level</i>	<i>Ident Code (octal)</i>	<i>Device</i>	<i>SINTRAN III</i>
1360-1367	10-12	56	Teletype 15	Terminal 15
1370-1377	10-12	57	Teletype 16	Terminal 16
1400-1407	10-12	140		Terminal 45
1410-1417	10-12	141		Terminal 46
1420-1427	10-12	142		Terminal 47
1430-1437	10-12	143		Terminal 48
1500-1507	10-12	144		Terminal 49
1510-1517	10-12	145		Terminal 50
1520-1527	10-12	146		Terminal 51
1530-1537	10-12	147		Terminal 52
1540-1547	11	17	Big Disk System 1	
1550-1557	11	20	Big Disk System 2	
1560-1567	11	21	Floppy Disk 1	
1570-1577	11	22	Floppy Disk 2	
1600-1607	11	14	Versatec 2	
1640-1647	10-12	150		Terminal 53
1650-1657	10-12	151		Terminal 54
1660-1667	10-12	152		Terminal 55
1670-1677	10-12	153		Terminal 56
1700-1707	10-12	154		Terminal 57
1710-1717	10-12	155		Terminal 58
1720-1727	10-12	156		Terminal 59
1730-1737	10-12	157		Terminal 60
1740-1747	10-12	160		Terminal 61
1750-1757	10-12	161		Terminal 62
1760-1767	10-12	162		Terminal 63
1770-1777	10-12	163		Terminal 64





## APPENDIX C

## TEST LOOPS

## 1. Core Address Register (CAR)

	<i>DRUM:</i>	<i>HAWK DISK:</i>	<i>BIG DISK:</i>
20/ TRA OPR	150002	150002	150002
IOX CAR	164541	164501	165541
SAA O	170400	170400	170400
IOX RCAR	164540	164500	165540
COPY SA DX	146157	146157	146157
JMP* -5	124373	124373	124373

X register shall follow the OPR switches

## 2. Block Address Test

20/ SAA 10	170410	170410	170410
IOX CONT	164545	164505	165545
TRA OPR	150002	150002	150002
IOX BAR	164543	164503	165543
SAA O	170400	170400	170400
IOX RBAR	164546	164506	165546
COPY SA DX	146157	146157	146157
JMP* -7	124371	124371	124371

X register shall follow the OPR switches

## 3. Check Ident Code

20/ SAA 1	170401	170401	170401
IOX LCONT	164545	164505	165545
SAA 0	170400	170400	170400
IDENT PL11	143611	143611	143611
COPY SA DX	146157	146157	146157
JMP* -5	124373	124373	124373

IDENT CODE in X register

## C.1 TEST LOOP FOR CDC HAWK DISK INTERFACE

10/400	% CAR (core address register)
12/200	% WC (word count)
14/ 0	% BAR (block address register). 125252 in Test Mode
16/ 4	% CW (control word)
START, 20/044370	% LOAD CAR
164501	% IOX CAR
044370	% LOAD WC
164507	% IOX WC
044370	% LOAD BAR
164503	% IOX BAR
044370	% LOAD CW
164505	% IOX CW
164504	% IOX Read Status
175025	% BSKIP Active
124376	% JMP* -2
175045	% BSKP protect violate
151013	% WAIT if PROTECT SWITCH is ON
146157	% Status to X
124362	% JMP START

200 octal words will be read from disk to main memory starting in address 400.

Status register → X register. NB! Parity error in Test Mode.

CAR, BAR, WC and CW can be changed as desired.

When this "loop" is run in test mode, the test word 125252 and 52525 will be read to consecutive words in memory.

<i>CW</i>	<i>Real</i>	<i>Test</i>
Read Transfer	4	14
Write transfer	4004	4014
Read parity	10004	10014
Compare test	14004	14014

NB! In test mode, BAR = 125252

C.2 BIG DISK TEST LOOP

20/	044024	START,	LDA CA	% LOAD CORE ADDRESS
	165541		IOX 1541	
	044023		LDA BLA	% LOAD BLOCK ADDRESS
	165543		IOX 1543	
	044022		LDA WC	% LOAD WORD COUNT
	165547		IOX 1547	
	044021		LDA CW	% LOAD CONTROL WORD
	165545		IOX 1545	% READ STATUS
30/	165544		IOX 1544	
	171700		SAX -100	
	132400		JNC *0	% DELAY-INCREMENT X AND JUMP IF NEGATIVE
	175235		BSKP ONE 30 DA	
	124374		JMP *-4	(Delay due to delay in FIFO)
	146151		COPY SA DD	
	165540		IOX 1540	% READ CORE ADDRESS
	064005		SUB CA	
40/	064006		SUB WC	
	131002		JAZ *2	
	151000		WAIT	% STOP IF ERROR IN CAR
	124355		JMP START	
44/	010000	C A,	10000	
	052525	BLA,	52525	% TEST MODE
	001000	WC,	1000	
	000014	CW,	14	

CONTROL WORD (CW) FORMAT:

	<i>Disk Connected (unit 0):</i>	<i>Test</i>
Read	4	14
Write	4004	4014
Read parity	10004	10014
Compare	14004	14014
Initiate seek	26004	
Write format	24004	
Seek complete search	30004	
Return to zero seek	34004	



## APPENDIX D

## PROGRAMMING SPECIFICATION FOR I/O DEVICES

D.1 *NORD-10/S TERMINAL BUFFER (MODULE 1095)  
PROGRAMMING SPECIFICATION (AS CURRENT-LOOP  
INTERFACE)*

*Terminal Buffer Addresses:*

The codes below are relevant for the first terminal. The codes for the first sixteen terminals are found by adding  $10_{\text{g}} \cdot N$  terminal number  $(0, 1, 2, \dots, 17)_{\text{g}}$ . For the next sixteen terminals the codes are found by adding  $(1000 + 10(N-20))_{\text{g}}$ .  $N =$  terminal number  $(20, 11, 12, \dots, 37)_{\text{g}}$ . For further information in section 11.

*Input Channel (Interrupt Level 12):*

Read Data Register

IOX 300

The number of data bits read into the A register is specified by bits 11 and 12 in the input control register. The received character is right justified.

Write Baude-rate Selection

IOX 301

Read Status Register

IOX 302

Write Control Register

IOX 303

*Output Channel (Interrupt Level 10):*

## Write Data Register

IOX 305

The number of bits specified by bits 11 and 12 in the *input* channel control register is written to the output data register, starting with bit 0 and counting upwards.

## Read Status Register

IOX 306

## Write Control Register

IOX 307

*IDENT Code:*

The IDENT code for the input channel and the output channel will be the same, with the input channel responding to level 12 and the output channel to level 10. The selection of different ident codes is switch-controlled.

## INPUT CHANNEL:

*Input Status Register Format:*

Bit 0	Ready for transfer interrupt enabled
Bit 1	Not used
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors
Bit 5	Framing error
Bit 6	Parity error
Bit 7	Overrun
Bit 8-10	Not used
Bit 11	Carrier missing
Bit 12	Request to Send missing*
Bit 13	Ready for Sending missing*
Bit 14	Not used
Bit 15	Half duplex*

\* Not used when connected to current loop (Used when connected to asynchronous modem).

## Notes:

- Bit 5: Framing error means that the stop bit is missing.
- Bit 6: Parity error means that a parity error has occurred while working in parity generation/checking mode.
- Bit 7: Overrun means that at least one character is overwritten while input is active.

*Input Control Word Register Format:*

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Not used
Bit 2	Active device
Bit 3	Test mode
Bit 4	Device clear
Bits 5-6	Not used
Bit 7	Carriage return delay enable
Bits 8-10	Not used
Bits 11-12	Character length
Bit 13	Number of stop bits
Bit 14	Parity generation/ checking
Bit 15	Half duplex*

\* When connected to asynchronous modem

## Notes:

- Bit 2:** After a Master Clear or a Device Clear (bit 4), the device has to be activated by writing a 1 into bit 2 of the control register. If not, received data will not be clocked into the receiver data buffer. The control bit will be 1 until 0 is written into it, or it is cleared by Master Clear or Device Clear.
- Bit 3:** Test mode will loop transmitted data back to received data, and if the other terminal is connected to the line, transmitted data will also be transferred to this terminal.
- Bit 4** Gives a clear pulse to the buffer card. After a Device Clear, the buffer card must be initialized.
- Bit 7:** Carriage return delay enable. If set to 1, this bit will cause a delay of 200-250 milliseconds each time an ASCII carriage return (octal value 15) is transmitted to the terminal. (Useful for Silent 700 terminal with data rate 300 bits/second). Characters with octal values 14, 16 and 17 (form feed, shift out and shift in) will also cause the same delay. (The parity bit is not checked).
- Bit 11-  
Bit 12:** The content of these bits give the following character lengths, both for the input channel and the output channel:

Bit:			
12	11		
0	0	8	bits
0	1	7	bits
1	0	6	bits
1	1	5	bits

If bit 14 is a 1, a parity bit is *added* to the number given in this table.

- Bit 13: The number of stop bits will be two if the control bit is 0, and one if the control bit is 1.
- Bit 14: If this control bit is 0, no parity bit will be added to the character on the output channel, and the received character will not be checked for parity. A 1 in this control bit will add an even parity bit to the character on the output channel, and give an error indication if the received character has an odd parity.

#### OUTPUT CHANNEL:

##### *Output Status Register Format:*

Bit 0	Ready for transfer interrupt enabled
Bit 1	Not used
Bit 2	Device active
Bit 3	Device ready for transfer
Bits 4-10	Not used
Bit 11	Carrier missing*
Bit 12	Request to Send missing*
Bit 13	Ready for Sending missing*
Bit 14	Not used
Bit 15	Half duplex*

\* When connected to asynchronous modem

##### Notes:

- Bit 2: This status bit will be a 1 as long as the device is busy transmitting characters.
- Bit 3: This bit indicates that the output data buffer is ready to receive a new character. This will be a 1 if bit 2 is 0, but may as well be a 1 when bit 2 is 1 due to the double buffer.

##### *Output-Control Word Register Format:*

Bit 0	Enable interrupt on device ready for transfer
Bit 1-15	Not used

##### Notes:

The device is activated when a character is loaded into the output data-register (IOX 305). There is not need for separate activation.



## DATA RATE SELECTION

There are several possibilities to control the data rate for input and output serial data.

The data rate can be selected by:

- a) EXTERNAL OSCILLATOR (16 x the bit rate), common for both input and output. The external oscillator is connected to card terminal 81 with a TTL or CCITT - V.24 (EIA RS - 232C) signal level.

In this case a high signal has to be connected to terminal 80 (select external oscillator). Switches as for 9600 baud.

- b) SWITCH SETTING on card. Independent speed for input and output. The switch in position 9 B 6 must be in the ON position, and the switch setting is sensed each time Master Clear is pressed. The selectable baud rates are: 9600, 4800, 2400, 1200, 600, 300, 200, 150, 110, 100, 75 and 50. In this case, no high signal must be connected to terminal 81. A high signal to terminal 80 will stop both input and output as long as the signal is high (BUSY).

Switch settings for the different baud rates are given in Table 1.

- c) IOX INSTRUCTION. The baud rate selection by software corresponds much to the switch setting referred to under b.

Input and output are independent, and are selected by the same IOX instruction (Group device number + 1). The content of the A register before the IOX instruction is executed determines the baud rate. The 4 least significant bits (0-3) are used for the input channel, and the next 4 (bits 4-7) are used for the output channel. Table 1 gives the bit pattern and corresponding baud rate.

The BUSY signal (terminal 80) will, as mentioned under b), stop the feeding of input and output data.

If the switch in position 9 B 6 is ON, pressing of the Master Clear button will select the baud rate given by the switches (15E1-15E8). If the switch in position 9 B 6 is OFF, the baud rate setting is only due to the IOX instruction, and is not changed by pressing Master Clear.

Note: A programmed device clear has no influence on the baud rate setting, but must always be given after the baud rate has been changed.

## INPUT CHANNEL (TO THE COMPUTER):

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REGISTER								Octal	
	15E4	15E3	15E2	15E1	Bit 7				Bit 0					
9600	ON	ON	ON	ON	X	X	X	X	0	0	0	0		0
4800	ON	ON	ON	OFF	X	X	X	X	0	0	0	1		1
2400	ON	ON	ON	OFF	X	X	X	X	0	0	1	0		2
1200	ON	ON	OFF	OFF	X	X	X	X	0	0	1	1		3
600	OFF	ON	ON	ON	X	X	X	X	1	0	0	0		10
300	OFF	ON	ON	OFF	X	X	X	X	1	0	0	1		11
200	OFF	OFF	ON	OFF	X	X	X	X	1	1	0	1		15
150	OFF	ON	OFF	ON	X	X	X	X	1	0	1	0		12
110	OFF	OFF	ON	ON	X	X	X	X	1	1	0	0		14
100	OFF	OFF	OFF	ON	X	X	X	X	1	1	1	0		16
75	OFF	ON	OFF	OFF	X	X	X	X	1	0	1	1		13
50	OFF	OFF	OFF	OFF	X	X	X	X	1	1	1	1		17

## OUTPUT CHANNEL (FROM THE COMPUTER):

	SWITCH SETTING				IOX (GP + 1) CONTENT IN A REGISTER								Octal	
	15E8	15E7	15E6	15E5	Bit 7				Bit 0					
9600	ON	ON	ON	ON	0	0	0	0	X	X	X	X		000
4800	ON	ON	ON	OFF	0	0	0	1	X	X	X	X		020
2400	ON	ON	OFF	ON	0	0	1	0	X	X	X	X		040
1200	ON	ON	OFF	OFF	0	0	1	1	X	X	X	X		060
600	OFF	ON	ON	ON	1	0	0	0	X	X	X	X		200
300	OFF	ON	ON	OFF	1	0	0	1	X	X	X	X		220
200	OFF	OFF	ON	OFF	1	1	0	1	X	X	X	X		320
150	OFF	ON	OFF	ON	1	0	1	0	X	X	X	X		240
110	OFF	OFF	ON	ON	1	1	0	0	X	X	X	X		300
100	OFF	OFF	OFF	ON	1	1	1	0	X	X	X	X		340
75	OFF	ON	OFF	OFF	1	0	1	1	X	X	X	X		260
50	OFF	OFF	OFF	OFF	1	1	1	1	X	X	X	X		360

## Note:

Input and output baud rates are selected by the same IOX instruction. If the A register is set to octal value 14 before the IOX instruction is executed, 110 baud will be selected for input, and 9600 baud will be selected for output. To get 110 baud on both the input and output channel, the octal value 314 should be placed in the A register before the IOX instruction is executed.

## IDENT CODES AND INTERRUPT MECHNAISM

## Ident Codes

The ident codes are binary coded by the switches in position 1E, with 0 corresponding to ON and 1 corresponding to OFF.

*EXAMPLES:*

Ident code	1E7	1E6	1E5	1E4	1E3	1E2	1E1
0 <sub>8</sub>	ON	ON	ON	ON	ON	ON	ON
1 <sub>8</sub>	ON	ON	ON	ON	ON	ON	OFF
2 <sub>8</sub>	ON	ON	ON	ON	ON	OFF	ON
60 <sub>8</sub>	ON	OFF	OFF	ON	ON	ON	ON
77 <sub>8</sub>	ON	OFF	OFF	OFF	OFF	OFF	OFF
155 <sub>8</sub>	OFF	OFF	ON	OFF	OFF	ON	OFF

All ident codes from 0 to 177<sub>8</sub> can be selected.

## Interrupt Mechanism

What is needed for a device to give an interrupt?

First of all the device must be ready for a transfer, i.e. status bit 3 must be on. For input this means that a whole character is received by the input buffer, and is ready to be read into the A register. For output it means that it is possible to place at least one more character in the output buffer. Secondly, interrupt on ready for transfer must be enabled. It means that a 1 is written into the control register bit 0 (which also is status register bit 0). The AND function of Ready for Transfer and Ready for Transfer Interrupt Enabled is gated to "wire-or" lines, separate for input and output. Input is connected to interrupt level 12 (terminal 35) and output is connected to interrupt level 10 (terminal 27).

When an interrupt is detected (dependent on the status in CPU and the program), the CPU usually responds by executing an IDENT instruction for the interrupting level. The level shift and interrupt mechanism in the CPU will not be described here. What is usually seen on the card is that sooner or later the INIDENT signal (terminal 7) will occur with the correct level code (determined by Bus Address bits 0 and 1 (terminals 32 and 33)). The timing here is that the Bus Address bits occur before signal occurs. Now, one part of the schotky data selector/multiplexer (74S157) in position 13A is used as a latch, freezing the status of the INT signal at the moment INIDENT occurs. If it is a 1, TINT will be a 1. This in turn results in INPUT and CONNECT back to the CPU, and the interrupt enable flip-flop for the selected level is cleared by CLINT (13A7) gated through the 74157 circuit in position 11A. (11A4 or 11A7). As the interrupt flag is AND function of the enable flip-flop and the Ready for Transfer status, the flag is cleared when the enable flip-flop is cleared.

Together with CONNECT and INPUT back to the CPU, the Ident Code is gated to the Data Bus (DB 0-7).

The ident code is identical for input and output channel.

## D.2 SPECIFICATION OF TAPE READER INTERFACE

Standard device number 0400 (0400-0403)<sub>8</sub>  
 Number of device number 4  
 Standard interrupt level 12<sub>10</sub>  
 Standard ident number 2

### *Control Word IOX Device Number + 3:*

Bit 0	Enable interrupt on ready for transfer
Bit 1	Not used
Bit 2	Activate device (start reading next character on tape)
Bit 3	Test
Bit 4	Device clear
Bits 5-15	Not used

### *Status Word IOX Device Number + 2:*

Bit 0	Interrupt enabled on ready for transfer
Bit 2	Read active
Bit 3	Reader ready for transfer (character read)

IOX device no. + 1	Not used
-----------------------	----------

### *Data Read IOX Device Number + 0:*

Read character. The same character may be read several times if desired.

### *TEST:*

When bit 3 in the control word is set to 1, the interface may be tested without reader.

If bit 2 is also set to 1, the interface will give "ready for transfer" after a while.

If "ready for transfer" is constantly 1, the data register will increment for each time IOX device no. + 3 (control word write) is used, and then it is possible to test the data patch.

### D.3 SPECIFICATION OF THE PAPER TAPE PUNCH INTERFACE

Standard device number 0410 (0410-0413)<sub>8</sub>  
 Number of device number 4  
 Standard interrupt level 10<sub>10</sub>  
 Standard ident no. 2

*Write Control Word IOX Device Number + 3:*

Bit 0	Enable interrupt
Bit 1	Not used
Bit 2	Activate device (punch character now in buffer)
Bit 3	Test
Bit 4	Device clear
Bits 5-15	Not used

*Read Status Word IOX Device Number + 2:*

Bit 0	Interrupt enabled
Bit 2	Device activate
Bit 3	Device ready

*Write data word IOX Device no. + 1.*

Write the 8 A-register bits to be punched in a buffer register.

*Read data IOX Device number + 0:*

Only used under test.

It is not wise to write a character into the buffer if the punch is not ready.

#### **TEST:**

The interface may be tested without punch.

When bit 3 in the control word is one, the buffer register may be read back by IOX device number. If the interface is activated, it will become "ready for transfer" after a while.

## D.4 SPECIFICATIONS OF LINE PRINTER INTERFACE FOR CDC 9380

Standard device number 0430 (0430-0433)<sub>8</sub>.  
 Number of device number 4.  
 Standard interrupt level 10<sub>10</sub>.  
 Standard ident number 3.

### *Write Control Word IOX Device Number + 3:*

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate device (print character now in buffer)
Bit 3	Test
Bit 4	Device and interface clear
Bit 5-15	Not used

### *Read Status Word IOX Device Number + 2:*

Bit 0	Interrupt enabled on ready
Bit 1	Interrupt enabled on error
Bit 2	Not used
Bit 3	Ready for transfer
Bit 4	Error, bit 5 or 6 set
Bit 5	Line printer not ready
Bit 6	Out of paper
Bit 7	Compressed pitch
Bit 8	LP9 is on, to indicate to the controller that data on the lines is format information and is interpreted as control code
Bit 9	Inhibit, illegal character in buffer
Bit 10	Not used
Bit 11	Band detect
Bit 12	Band detect

Bit 11	Bit 12	Type of band
0	0	128 characters
1	0	96 characters
0	1	64 characters
1	1	48 characters

Note! This interface is only handling 64, 96 character printers.

Bit 13-15 Not used

Write Data Word IOX DEV NO + 1

Writes a character in the buffer register.

All character codes 0-37<sub>8</sub> are illegal and ignored by the interface, except following control codes:

- 11<sub>8</sub> : HT (Gives space in CDC controller)
- 12<sub>8</sub> : LF
- 14<sub>8</sub> : FF
- 15<sub>8</sub> : CR
- 20<sub>8</sub> - 33<sub>8</sub> VFU channels give LP9 and disable LP5
- 20<sub>8</sub> VFU channel 1 (FF)
- 21<sub>8</sub> VFU channel 2
- 33<sub>8</sub> VFU channel 12

Read Data Word IOX DEV NO

It is possible to read back the data written in the buffer register when running in test mode (bit 3 set in control word).

## D.5 SPECIFICATION OF CARD READER INTERFACE (DOCUMENTATION) FOR NORD-10/S

Standard device number 0420 (0420-0423)<sub>8</sub>.  
 Number of device number 4.  
 Interrupt level 12<sub>10</sub>.  
 Ident number 3.

### *Write Control Word IOX Device + 3:*

Bit 0	Enable interrupt on ready for transfer
Bit 1	Enable interrupt on error
Bit 2	Activate.): Feed one card. Clear end of card.
Bit 3	Test
Bit 4	Device clear. Clear interrupt flip-flop, overrun flip-flop. Continue feed flip-flop and set end of card.
Bit 5-8	Not used
Bit 9	Continuous feed): feed next card immediately.
Bit 10-15	Not used

### *Read Status Word IOX Device + 2:*

Bit 0	Interrupt enabled on ready for transfer
Bit 1	Interrupt enabled on error
Bit 2	Card reader active. Signal from card reader.
Bit 3	Ready for transfer): a column may be read. This bit is turned off by "read data" IOX DEV.
Bit 4	Bits 5-9 set, error.
Bit 5	Hopper check error set from card reader.
Bit 6	Light or dark error from card reader.
Bit 7	Motion check error from card reader.
Bit 8	Overrun, one column was lost because it was not read before the next column was strobed into buffer. Cleared by MASTER CLEAR.
Bit 9	End of card.
Bits 10-15	

Be aware that the card reader sends hopper check while reading the last card.



*Write Data IOX Device + 1:*

Only used for testing the interface without card reader.

*Read Data IOX Device:*

Read last column.

**TEST:**

The interface may be tested without card reader. When bit 3 in the control word is set to one, the interface is in "test mode".

An IOX Device + 1 will simulate a column ready by the interface, set ready for transfer and increment the data register.

An "end of card" is simulated by IOX Device + 1 and bit 5 is set to one.

## D.6 *NORD-10/S CDC HAWK DISK PROGRAMMING SPECIFICATIONS*

### *Disk Device Register Address:*

The codes below are relevant for disk system 1. Each disk system may consist of 4 units. For disk system 2 add  $10_8$  to the specified codes.

Read Core Address

IOX 500

Load Core Address

IOX 501

Read Sector Counter

IOX 502

Load Block Address

IOX 503

Read Status Register

IOX 504

Load Control Word

IOX 505

Seek Instruction

IOX 506

Load Word Count Register

IOX 507

The minimum number of words to be transferred is one sector, i.e.,  $200_8$  words, the maximum number of words is one track, i.e., 24 sectors ( $6000_8$  words).

Read Block Address

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (test mode), the instruction

IOX 506

will return the previously loaded block address to the A register.

**Control Word**

Bit 0	Enable interrupt on device ready for transfer
Bit 1	Enable interrupt on errors
Bit 2	Activate device
Bit 3	Test mode
Bit 4	Device clear
Bit 5	Address bit 16
Bit 6	Address bit 17
Bit 7-8	Not assigned
Bit 9	Unit select
Bit 10	Unit select
Bit 11	Device operation
Bit 12	Device operation
Bit 13	Marginal Recovery
Bit 14	Not assigned
Bit 15	Write format

**Unit Select Code:**

Bit 10	9	
0	0	Unit 0
0	1	Unit 1
1	0	Unit 2
1	1	Unit 3

**Device Operation Code:**

Bit 12	11	
0	0	Read transfer
0	1	Write transfer
1	0	Read parity
1	1	Compare

To format a disk, the switch for formatting has to be turned on, Write Transfer, and Write Format must be specified.

**Status Word**

Bit 0	Ready for transfer, interrupt enabled
Bit 1	Error interrupt enabled
Bit 2	Device active
Bit 3	Device ready for transfer
Bit 4	Inclusive OR of errors (status bits 5-11)
Bit 5	Write protect violate
Bit 6	Time out
Bit 7	Hardware error
Bit 8	Address mismatch
Bit 9	Parity error
Bit 10	Compare error
Bit 11	Missing clock error
Bit 12	Transfer complete
Bit 13	Transfer on
Bit 14	On cylinder
Bit 15	Bit 15 loaded by previous control word

**Interrupt**

The disk interrupt level is 11 and the ident number for the first disk system is 1.

## D.7 *NORD-10/S BIG-DISK PROGRAMMING SPECIFICATION (33 or 66M BYTE)*

### DISK DEVICE REGISTER ADDRESS

The codes below are relevant for disk system I. Each disk system may consist of 8 disk units. For disk system II add  $10_8$  to the specified codes.

#### *Read Core Address*

IOX 1540

#### *Load Core Address*

IOX 1541

#### *Read Seek Condition*

IOX 1542

#### *Load Block Address*

IOX 1543

#### *Read Status Register*

IOX 1544

#### *Load Control Word*

IOX 1545

#### *Load Word Count Register*

IOX 1547

The maximum number of words to be transferred are 16 sectors, 8K words.

#### *Read Block Address*

This instruction is implemented for maintenance purposes only. By first loading a control word with bit 3 (Test mode) the instruction

IOX 1546

will return the previous loaded block address to the A-register.

### DISK FORMAT

#### Disk Address

The 16 bit in the Block Address Register have the following meaning:

Bit	
0-3	Sector number, 16 sectors per track (512 <sub>8</sub> words pr. sector)
4-6	Surface number, 5 surfaces
7-15	Cylinder number, totally 411 cylinders (0-410)

The most significant bit (bit 15) in the Control word is used to extend the cylinder address to 10 bits, thus enabling a cylinder address of maximum 822 cylinders. This is only relevant for 66 Mbyte disks.

## CONTROL WORD

### Control Word Content

Bit	
0	Enable interrupt on device ready for transfer
1	Enable interrupt on errors
2	Activate device operation
3	Test mode/ Select unit
4	Device clear (clear the activate flip-flop) and controller error bits
5	Address bit 16
6	Address bit 17
7-9	Unit select (maximum 8 units)
10	Marginal recovery cycle
11-14	Device operation code
15	Extended cylinder address

### Select Unit

When a Control Word is loaded the disk unit number (0-7) has to be set up in bits 7-9. If the transfer is changed from one unit to another, the new unit must be selected with a special program sequence. Bit 3 in the Control Word, select unit bit (test bit) is used.

*Example, selects unit one:*

UNIT,	200	%	Unit one, one in bit 7-9
SE LUNIT,	LDA UNIT	%	Load unit number
	AAA 10	%	Set select unit bit, bit 3
	IOX 1545	%	Load Control Word
	SAA 20	%	Device clear to
	IOX LCW	%	Clear possible error status
	IOX 1544	%	Read status
	BSKP IF ZERO 150 DA	%	Test if unit ready
	JMP ERROR	%	No unit ready
		%	Continue

### Marginal Recovery Cycle

The marginal recovery cycle (control word bit 10) may be used in connection with read operation codes M0, M2 and M3 as defined in the following section. This control bit is included to be an aid in recovering marginal data. For consecutive read transfers with this bit set, the controller will cycle through the following conditions:

1	Marginal read	: Servo offset positive, data strobe early
2	Marginal read	: No servo offset, data strobe early
3	Marginal read	: Servo offset negative, data strobe early
4	Marginal read	: Servo offset positive, nominal data strobe
5	Marginal read	: Servo offset negative, nominal data strobe
6	Marginal read	: Servo offset positive, data strobe late
7	Marginal read	: No servo offset, data strobe late
8	Marginal read	: Servo offset negative, data strobe late
9=1	etc.	

### Device Operation

All device operation codes will be activated when the code is given together with bit 3 (activate device). For all codes except M6, the correct unit number must also be selected.

Bit	14	13	12	11		
	0	0	0	0	M0	Read transfer
	0	0	0	1	M1	Write transfer
	0	0	1	0	M2	Read parity transfer
	0	0	1	1	M3	Compare transfer
	0	1	0	0	M4	Initiate seek
	0	1	0	1	M5	Write format
	0	1	1	0	M6	Seek complete search
	0	1	1	1	M7	Return to zero seek

#### M0 *Read transfer:*

This operation causes the controller to transfer data from the disk to the computer memory. The number of blocks transferred depends upon the word count as defined by the Word Count Register.

#### M1 *Write transfer:*

Transfer of data from the computer memory to the disk.

#### M2 *Read parity transfer:*

The controller will check the parity on the address and data of the sectors specified. Data is transferred to the controller and the cyclic check word for both the address field and the data field of a sector is compared with the correct check word as generated by the controller. No data transfer to the computer memory is performed.

#### M3 *Compare transfer:*

This function is included to positively check the data written on the disk. During compare transfer the controller compared the data read from the disk and data from the computer memory is compared bit by bit. Mismatch causes compare error bit to be set.

**M4** *Initiate seek:*

This function is included to enable a unit to position the heads prior to a data transfer. The heads will be positioned according to the content of the Block Address Register. As soon as this function is accepted by the disk, the operation will be completed.

**M5** *Write format:*

Together with a switch on a card in the interface set, this function will cause the controller to write the address field within each sector.

**M6** *Seek complete search:*

This function will enable the controller to go in a waiting state until any unit has completed a seek. This function is independent of the unit select code in the control word.

**M7** *Return to zero seek:*

This will cause the selected disk to perform a seek to cylinder 0 and will also clear the seek error bit in the unit.

**Extended Cylinder Address:**

Bit 15 in the control word is used as an extension to the cylinder address in the Block Address Register. This extended bit is used to allow addresses of up to 822 cylinders.

**READ SEEK CONDITION (IOX 1542)****Bit 0-7**            **SEEK COMPLETE**

Seek complete status for unit 0-7. True if the unit has moved the heads to the correct cylinder or a seek error has occurred, and the heads are under the sector number prior to the one specified by the block address loaded before the initiate seek command. The seek complete status will only be set if an initiate seek command for that unit has first been issued.

Thus, after an initiate seek command is given, the SEEK COMPLETE bit for that unit will appear once per revolution after the unit is positioned on the correct cylinder, or a seek error has occurred. The condition will last until a transfer command is given.

**Bit 8-10**            **UNIT SELECT**

The unit number as loaded by the last control word.

## Bit 11            SEEK ERROR

Seek error for that selected unit. This signal indicates that the unit was unable to complete a move within 500 ms, or that the heads have moved to a position outside the recording field, or that an address greater than the maximum number of tracks has been selected.

This signal will only be cleared by performing a RETURN to ZERO command on that unit.

## READ STATUS

## Status word:

Bit 0	Ready for transfer interrupt enabled.
Bit 1	Error interrupt enabled.
Bit 2	Controller active.
Bit 3	Controller finished with a device operation
Bit 4	Inclusive or of errors (Bit 5-13).
Bit 5	Illegal load i.e. load while status bit 2 is true, or load of block address while the unit is not on cylinder.
Bit 6	Time out
Bit 7	Hardware error (Disk fault + missing read clocks + missing servo clocks).
Bit 8	Address mismatch
Bit 9	Parity error
Bit 10	Compare error
Bit 11	DMA channel error
Bit 12	Abnormal completion
Bit 13	Disk unit not ready
Bit 14	On cylinder
Bit 15	Extended cylinder address

## INTERRUPT

The disk interrupt level is 11 and the ident number for disk system I is 17 and for disk system II 20.



## D.8 PROGRAM SPECIFICATIONS FOR PERTEC 8000 and 9000 MAG-TAPE

Device no. and registers.

Device no. is 520-527 for first system.

Register:	IOX
Read Core Address	520
Load Core Address	521
Read Modus	522
Load Modus	523
Read Status	524
Load Control	525
In Test, Read previous loaded Modus (523)	526
Load Word Count	527
Interrupt Level	11

[Statement in sharp parantheses is equivalent meaning on Tandberg].

### Load Control Word (IOX 525)

Bit	
0	Enable interrupt on device ready for transfer
1	Enable interrupt on errors
2	Activate
3	Test mode
4	Device clear
5	Address bit 16
6	Address bit 17
7-10	Not used
11-12	Device operation code
13-14	These bits must be zero
15	On the fly operation, interrupt when tape-unit is deaccelerating

### 12-11

0 0	A normal operation given by the modus-code.
0 1	Not used
1 0	Rewind
1 1	Off line [Tandberg Rewind and unload]

## Read Status (IOX 524)

Bit	
0	The ready interrupt enabled
1	Error interrupt enabled
2	Device active
3	Device ready for transfer
4	Error, inclusive OR of bit 5-12
5	Control or modus word error. Trying to write on protected tape, tape unit not on-line, etc.
6	Bad data block
7	Tape mark detected
8	Not usable
9	End of tape detected
10	Word counter not zero
11	DMA-error
12	Overflow in read
13	Formatter busy [Tape busy]
14	Data busy [Formatter busy]
15	Bit 15 loaded by previous control word. On the fly operation, interrupt when bit 14 goes off.

## Load Modus (IOX 523)

Bit 0-8 a modus code

Bit	
0	Not used [556 BPI]
1	Not used [220 BPI]
2	Reverse
3	Write
4	Space/Erase
5	File mark
6	Edit [High speed]
7	Parity (7 tr.) [Parity 7 tr.] (even parity)
8	THR2 [Threshold]

Bits 2-5 are combined to give an operation

2	3	4	5	
0	0	0	0	Read forward
1	0	0	0	Read reverse
0	1	0	0	Write
0	0	1	0	Space forward
1	0	1	0	Space reverse
0	1	1	0	Erase
0	1	0	1	Write file mark
0	0	1	1	Search for file mark
1	0	1	1	Search reverse for file mark

Other combinations are not standard

Bit 6 Edit is used to overwrite one record between others.

Bit	
9-11	Not used
12-13	Tape unit no. (1 of 4) [One of 8 units on Tandberg]
14	Formatter no. (1 of 2) [One of 8 units on Tandberg]
15	Read odd no. of characters

Note: Odd no. of characters Modus 15 should not be used together with on-the-fly operation (control bit 15).

#### Read Modus (IOX 522)

Bit	
0	Online
1	Write enable ring present
2	Tape standing on load point
3	Hard error [CRC]
4	Corrected error [LRC]
5- 8	Undefined [no. of VRC]
9-15	Undefined



APPENDIX E

E.1

MODEL 33 ASR/KSR TELETYPE CODE (ASC II) IN BINARY FORM

HOLE PUNCHED = MARK = 1  
 NO HOLE PUNCHED = SPACE = 0

Most significant bit  
 Least significant bit  
 7 6 5 4 3 2 1 0

@	SPACE	NULL/IDLE						0	0	0	0	0
A	!	START OF MESSAGE						0	0	0	0	1
B	..	END OF ADDRESS						0	0	0	1	0
C	#	END OF MESSAGE						0	0	0	1	1
D	\$	END OF TRANSMISSION						0	0	1	0	0
E	%	WHO ARE YOU						0	0	1	0	1
F	&	ARE YOU						0	0	1	1	0
G	'	BELL						0	0	1	1	1
H	(	FORMAT EFFECTOR						0	1	0	0	0
I	)	HORIZONTAL TAB						0	1	0	0	1
J	*	LINE FEED						0	1	0	1	0
K	+	VERTICAL TAB						0	1	0	1	1
L	,	FORM FEED						0	1	1	0	0
M	-	CARRIAGE RETURN						0	1	1	0	1
N	.	SHIFT OUT						0	1	1	1	0
O	/	SHIFT IN						0	1	1	1	1
P	0	DCO						1	0	0	0	0
Q	1	READER ON						1	0	0	0	1
R	2	TAPE (AUX ON)						1	0	0	1	0
S	3	READER OFF						1	0	0	1	1
T	4	(AUX OFF)						1	0	1	0	0
U	5	ERROR						1	0	1	0	1
V	6	SYNCHRONOUS IDLE						1	0	1	1	0
W	7	LOGICAL END OF MEDIA						1	0	1	1	1
X	8	S 0						1	1	0	0	0
Y	9	S 1						1	1	0	0	1
Z	:	S 2						1	1	0	1	0
[	;	S 3						1	1	0	1	1
\	<	S 4						1	1	1	0	0
]	=	S 5						1	1	1	0	1
↑	>	S 6						1	1	1	1	0
←	?	S 7						1	1	1	1	1

0	0	Same
0	1	Same
1	0	Same
1	1	Same

RUB OUT ←

PARITY



## APPENDIX F

### CARD MODULES

#### F.1 *GENERAL*

Dimensions of card modules installed in NORD 10, NORD 10S, NORD 12, NORD 42 and NORD 50 designed before summer 1977 are given in Figure 1.

Dimensions of modules designed after summer 1977 are given in Figure 3.

#### F.2 *COORDINATE SYSTEMS*

To identify positions on the cards, two different coordinate systems are used, one to identify plated-through holes, and the other to identify component positions on the card.

##### F.2.1 *THROUGH-PLATING COORDINATES*

On Figure 1, the system used to identify through-platings is shown. Every hole except those close to the finger contacts is identified by a capital letter (A to V) and a number (1 to 53). The coordinates for the marked through-plating near the centre of the card is *K30*. The through-platings close to the finger contacts are identified by the corresponding finger contact number terminal on component side. It is written as a colon and an even number (0 to 98).

## F.2.2 COMPONENT COORDINATES

The coordinate system used for components is mainly for integrated circuits. These coordinates are written as a row number from 1 to 19 and then a letter for the column. Some of these numbers are printed on the card, and are partly shown in Figure 1. 1 is the row between plated-through holes A and B, 2 is the row between plated-through holes B and C, and so on. The letters, however, are not fixed to physical dimensions on the card, but are dependent on where on the card the integrated circuits are placed. The rules are that all integrated circuits in the column close to the finger contacts are column A. The next one B and so on. With normal size on the integrated circuits it is possible to use the letters from A to (and including) the letter F\*. IC's with 24 and 40 pins may cover for instance 3 and 4, B and C. The notation in this case is 3B. (Figure 2).

\*G for the later modules.

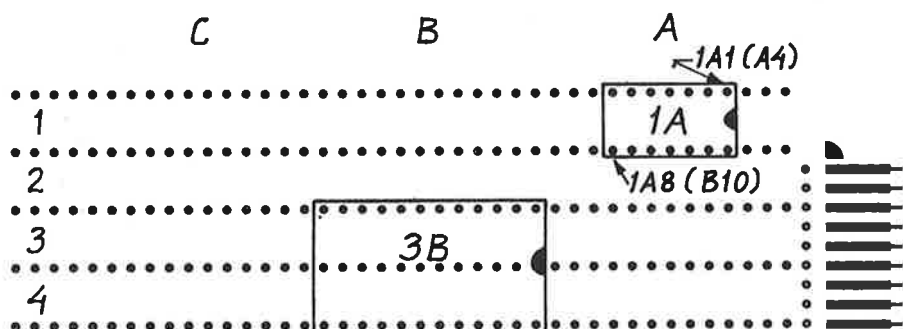


Figure 2: IC COORDINATES

The components coordinates are often used with an additional number to identify pin on the IC. In figure 1 the IC pin 1A1 is located in through-plating A4, and 1A8 is located in through-plating B10.

## F.3 CARD MODULES POWER-CONNECTION

### Voltage:

+5V  
GROUND (+5V)  
  
-5V  
GROUND (-5V)  
-12V  
GROUND (-12V)  
+12V  
GROUND (+12V)  
+24V  
GROUND (+24V)

### Finger-contact:

0,1,98,99  
2,3,96,97  
  
58,59  
56,57  
62,63  
60,61  
66,67  
64,65  
70,71  
68,69



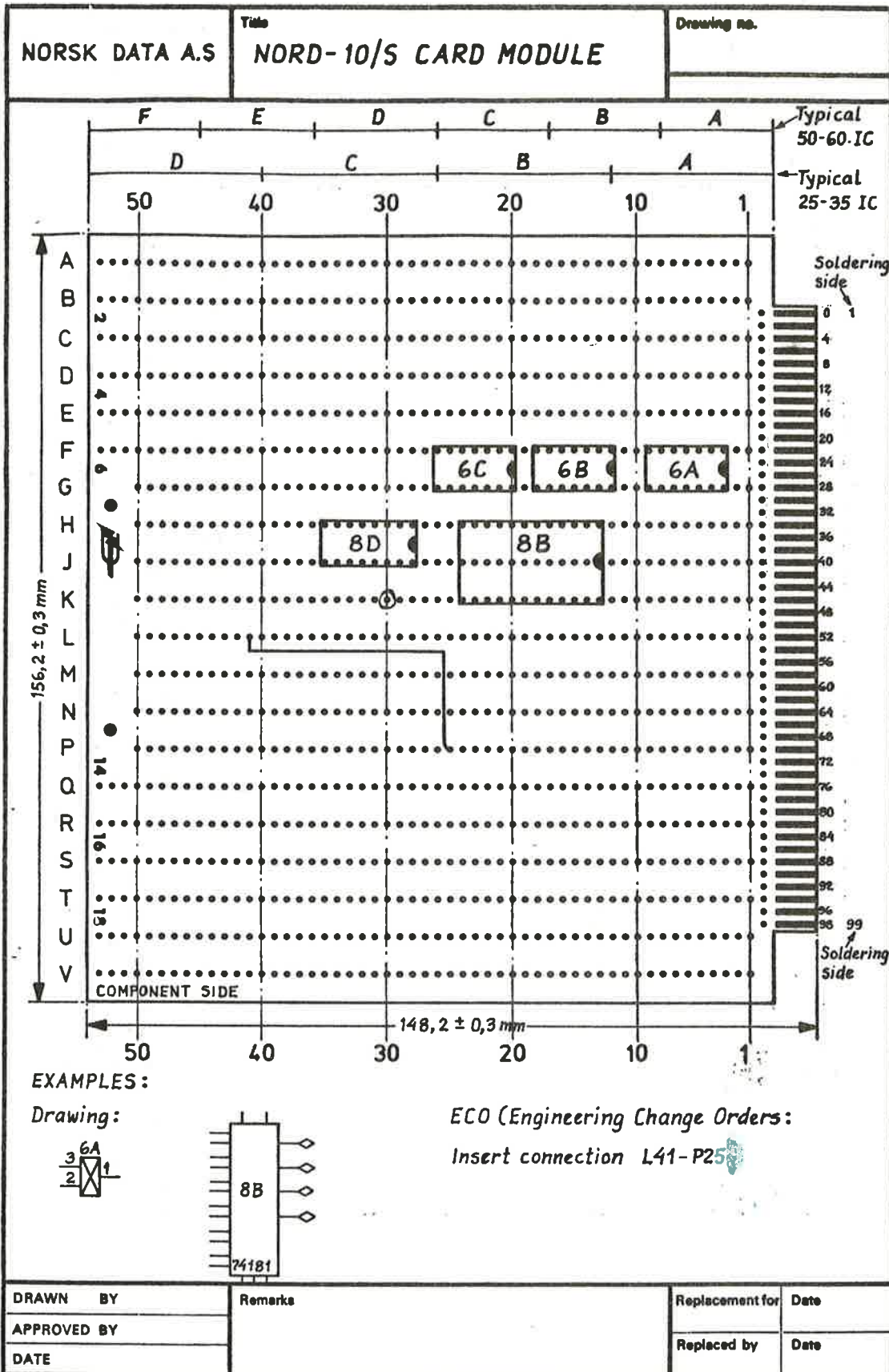


FIGURE 1

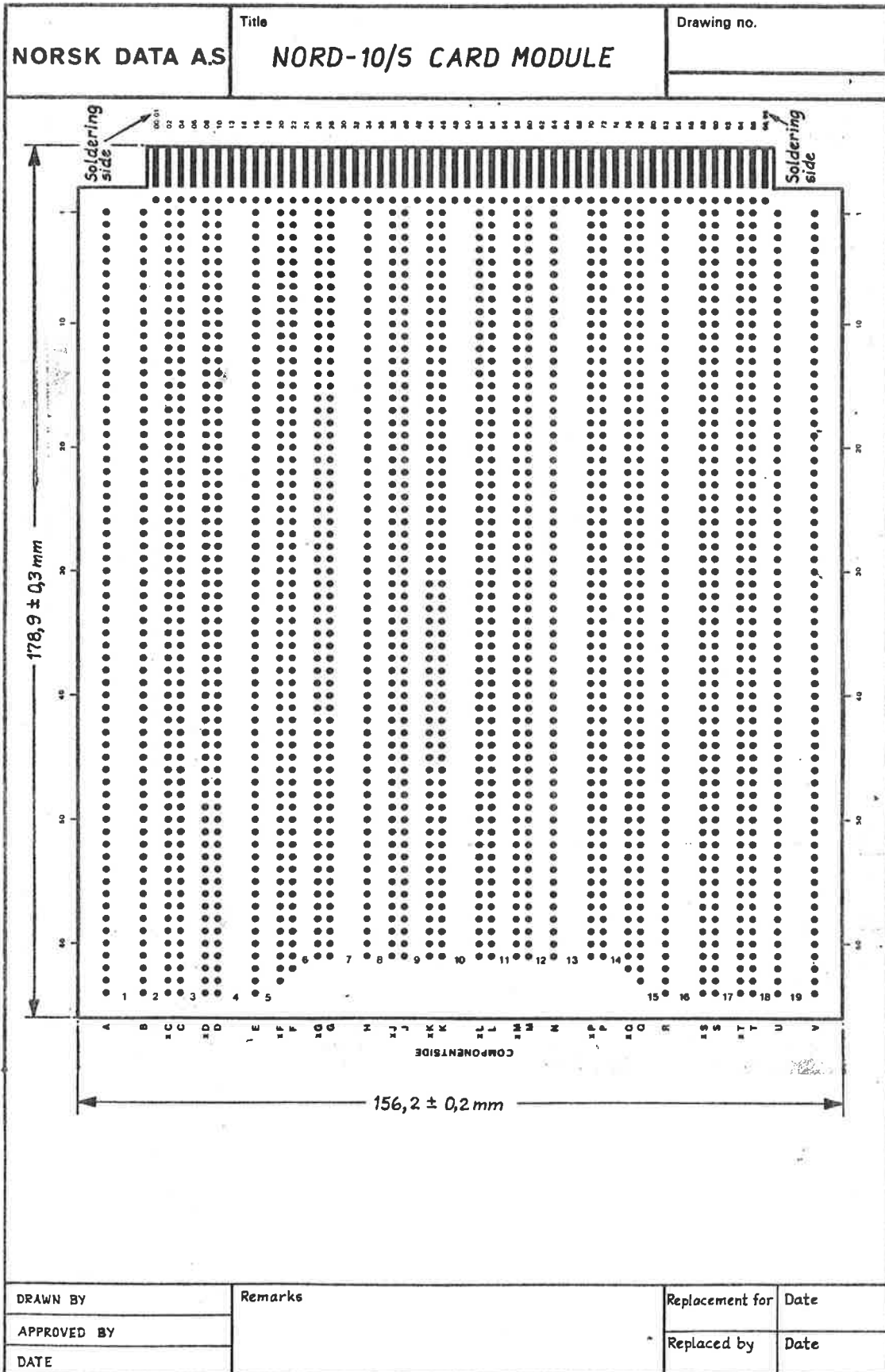


FIGURE 3

## APPENDIX G

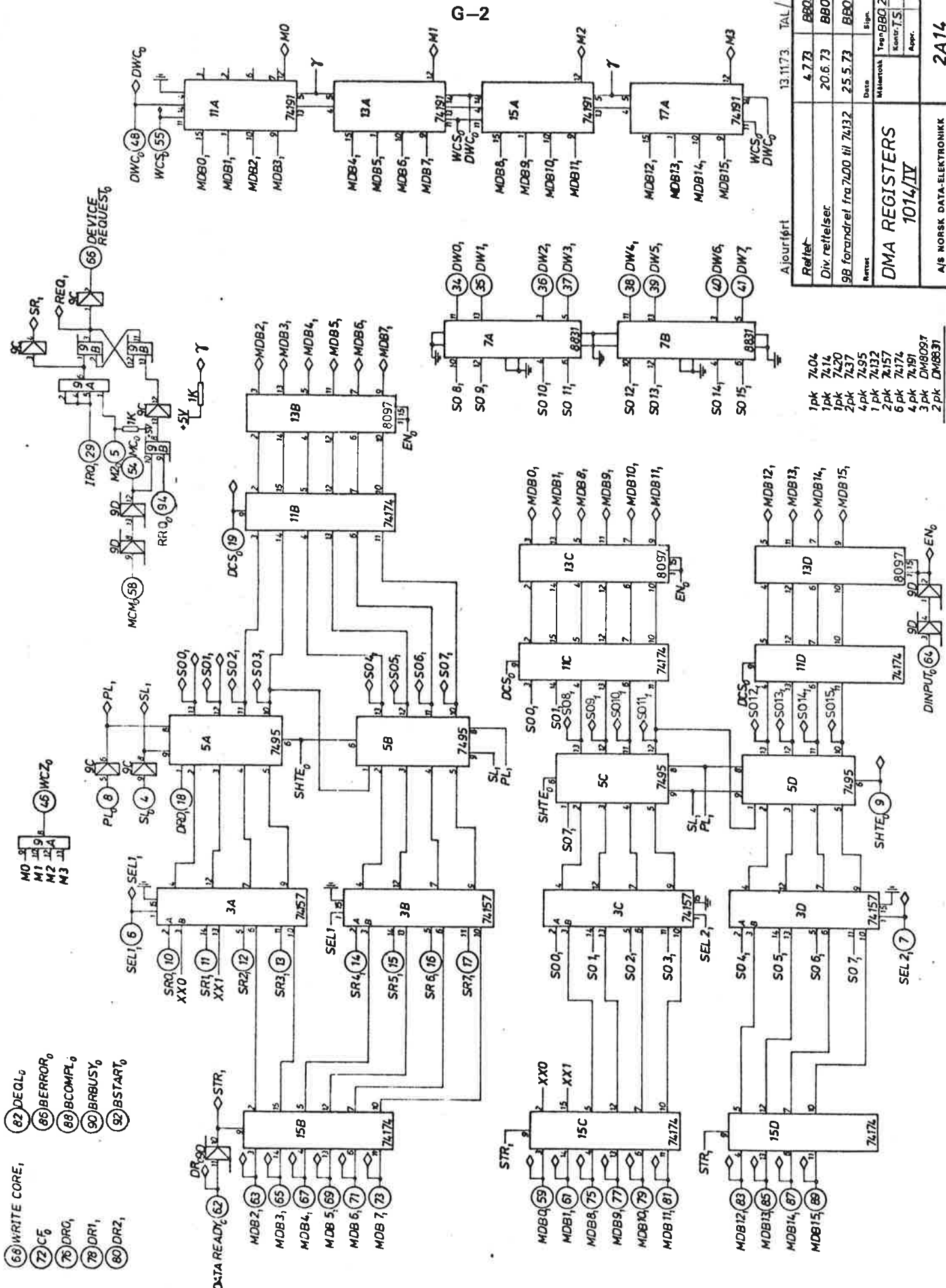
### DRAWINGS

*DRAWINGS:*

1014	DMA REGISTER
1022	BUS CONTROL
1043	CARD READER BUFFER (DOCUMENTATION)
1093	BRANCH TRANSCEIVER
1095	TERMINAL BUFFER
1096	DMA ADDRESS
1101	BRANCH CONTROL
1119	TRANSCEIVER ADDRESS
1125	TRANSCEIVER DATA
1127	TRANSCEIVER CONTROL
1130	CDC LINEPRINTER INTERFACE



- (66) WRITE CORE,
- (72) C<sub>6</sub>
- (76) DR<sub>0</sub>
- (78) DR<sub>1</sub>
- (80) DR<sub>2</sub>
- (82) DEQL<sub>0</sub>
- (86) BERR<sub>0</sub>
- (88) BCOMPL<sub>0</sub>
- (90) BRBUSY<sub>0</sub>
- (92) BSTART<sub>0</sub>

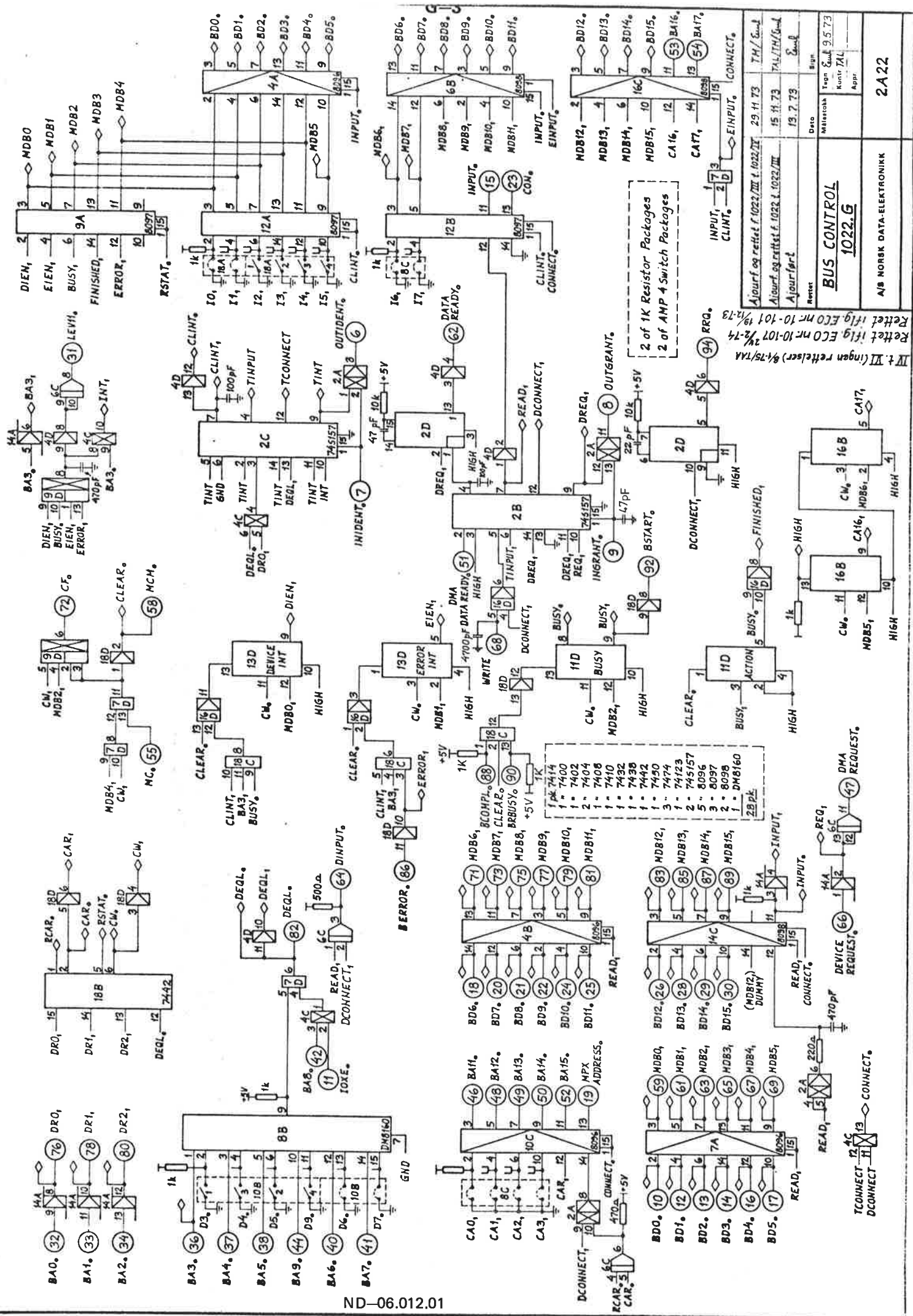


G-2

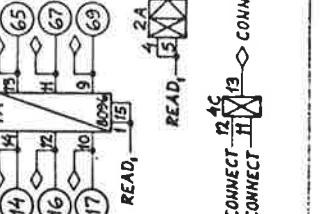
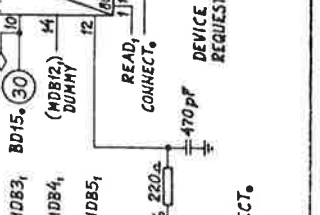
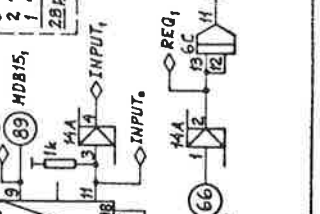
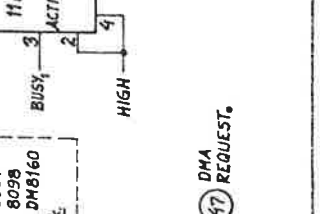
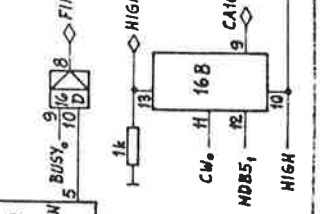
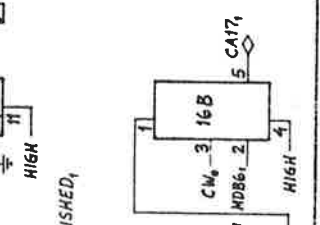
Ajourført		13.11.73	TAL / BBO
Refekt	Div. rettelsler	4.7.73	BBO
98 forandrel fra 74.00 til 74.132		20.6.73	BBO
Berevnet		25.5.73	BBO
DMA REGISTERS 1014/IV		Date	Sign.
		Måltavle	Tegn BBO 24.4.73
		Kontor-T.S.	
		Appr.	
A/S NORSK DATA-ELEKTRONIK		2A14	

- 1pk 7404
- 1pk 7414
- 1pk 7420
- 2pk 7437
- 4pk 7495
- 1pk 74132
- 2pk 74157
- 6pk 74174
- 4pk 74191
- 3pk DM8097
- 27pk DM8831
- 2stk JK





IV + VI (ingen Reteller) 8/75/TAL  
 Rettel i fig. ECONr-10-107 2/74  
 Rettel i fig. ECONr-10-101 12/73



Ajourført og rettet f. 1022/TAL f. 1022/TAL	29.11.73	T.H./Gund
Ajourført og rettet f. 1022 f. 1022/TAL	15.11.73	TAL/T.H./Gund
Ajourført	13.7.73	Gund
Rettet		Sign
Matrikelnr. Tegnr. Eksam. 9.5.73 Kunder TAL. Appr.		
<b>BUS CONTROL</b> <b>1022.5</b>		
AJS NORSK DATA-ELEKTRONIKK		
<b>2A22</b>		



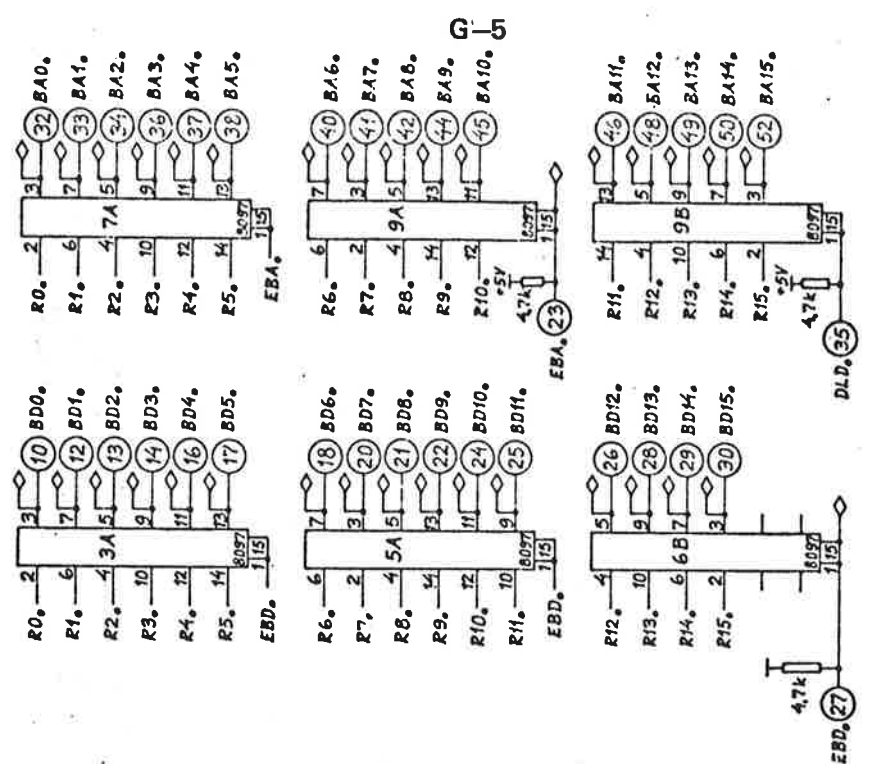
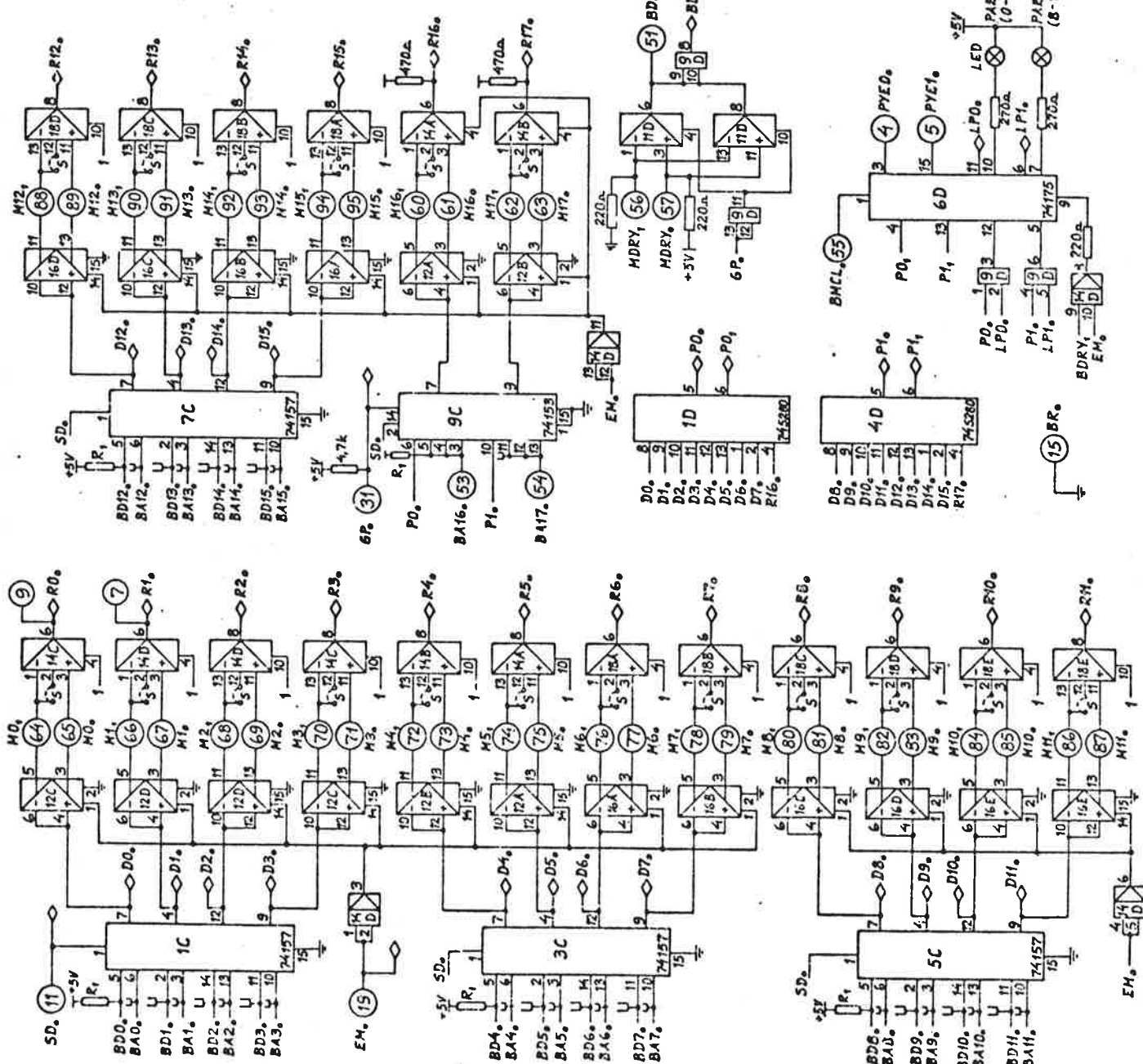






ACTUAL SIGNAL NAMES

USAGE	SIGNAL	DL.D.	EBA.	EBD.	EM.	6P.	BKCL.	SD.	BR.	BD.
BRANCH DATA		DLDB	DLDA	EBD.	EMD.	N.C.	GND	SBD.	DPR.	N.
BRANCH ADDRESS		N.C.	EBA.	N.C.	EMA.	N.C.	GND	SLD.	APR.	N.
DMA DATA		N.C.	N.C.	EDD.	EM.	GND	BKCL.	GND	BR.	BD.



- 1p. 7400
- 1. 7408
- 1. 74155
- 4. 74157
- 1. 74175
- 2. 745280
- 6. 8097
- 10. 8820A
- 9. 8831
- RI: 3. RES. 1K
- 38 PK

85 term.

NOTE: WHEN USED FOR DMA DATA, PREFERABLY REMOVE R1 AND INSERT STRAPS 5.

OPPRAT.I.O.M.E.C.O NR.10-318(C)	30.12.75	TAA. 10.
Patent 1093.B (ingeniørrettelser)	8.12.75	TAA.I.F.
Referat: polkspose.	2.7.75	2.1
Revisjon	10.11.75	10.11.75
BRANCH TRANSCEIVER		
1093.C		
A/S NORSK DATA-ELEKTRONIKK		

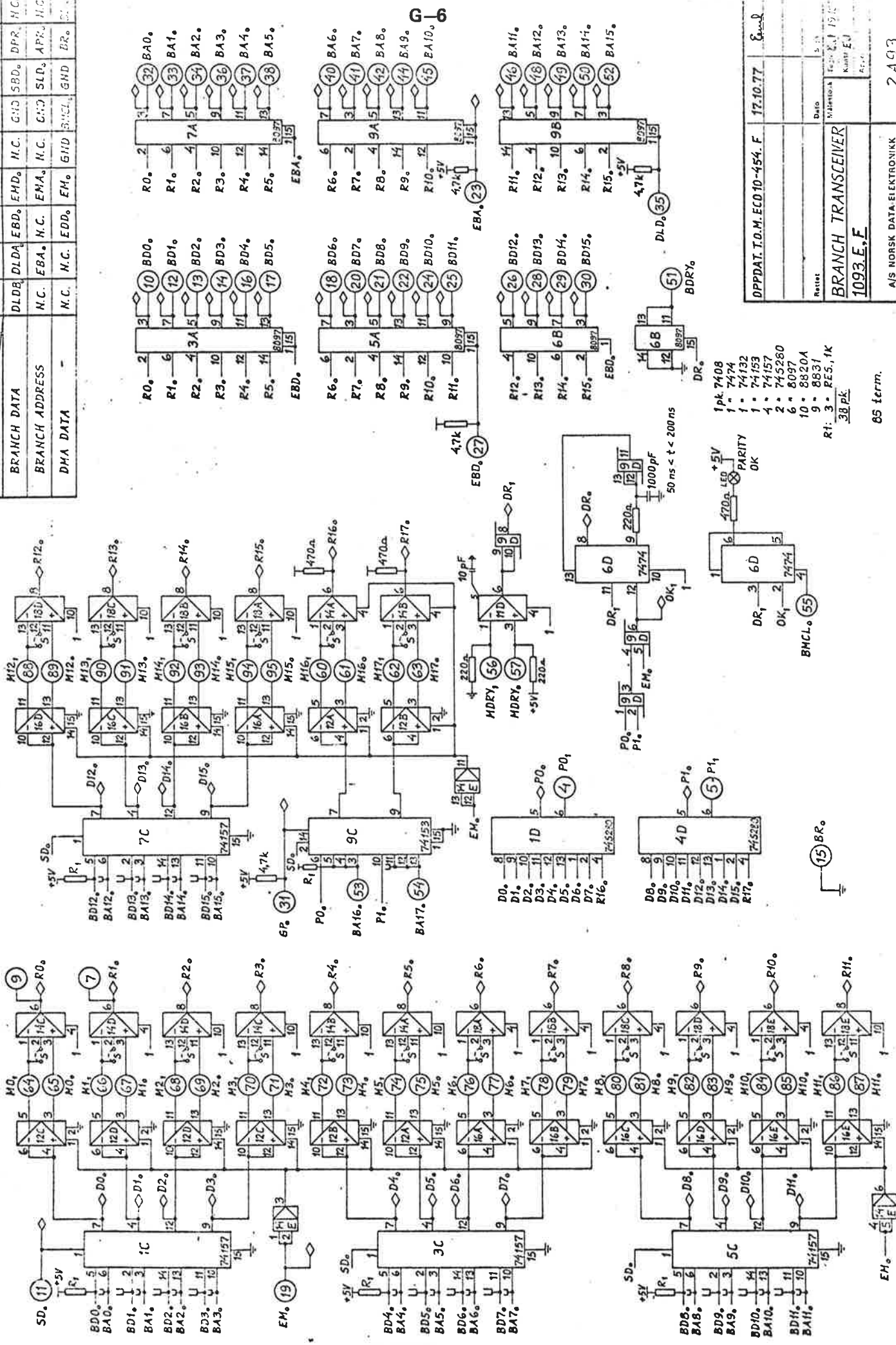
2A93



ACTUAL SIGNAL NAMES

USAGE	SIGNAL	DL.D.	EBA.	EBD.	EM.	GP.	BA.CL.	SD.	BR.
BRANCH DATA		DLDB	DLDA	EBD.	EMD.	M.C.	GND	SB.D.	DPR
BRANCH ADDRESS		N.C.	EBA.	N.C.	EMA.	N.C.	GND	SLD.	APR
DMA DATA		N.C.	N.C.	EDD.	EM.	GND	3.WCL.	GND	BR.

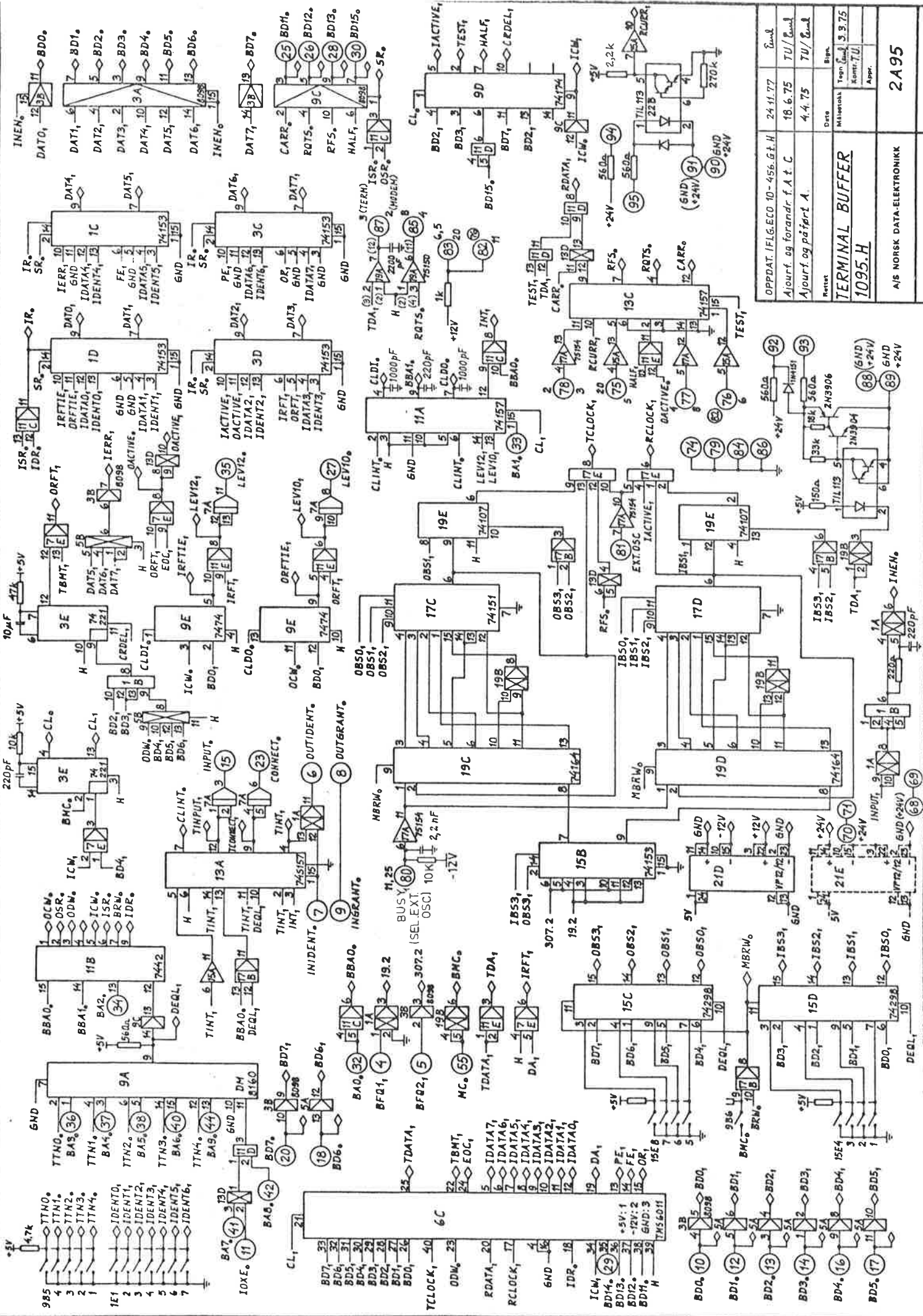
NOTE: WHEN USED FOR DMA DATA, PREFERABLY REMOVE R<sub>1</sub> AND INSERT STRAPS S.



OPPDAT. T.O.M. ECD 10-454. F	17.10.77
BRANCH TRANSCIEVER	
1093.E.F	
AIS NORSK DATA ELEKTRONIKK	2A93

- 1pk. 7408  
 1 - 7474  
 1 - 74132  
 1 - 74153  
 1 - 74157  
 2 - 745280  
 6 - 8097  
 10 - 8820A  
 9 - 8831  
 R1: 3 - RES., 1K  
 38 PK.

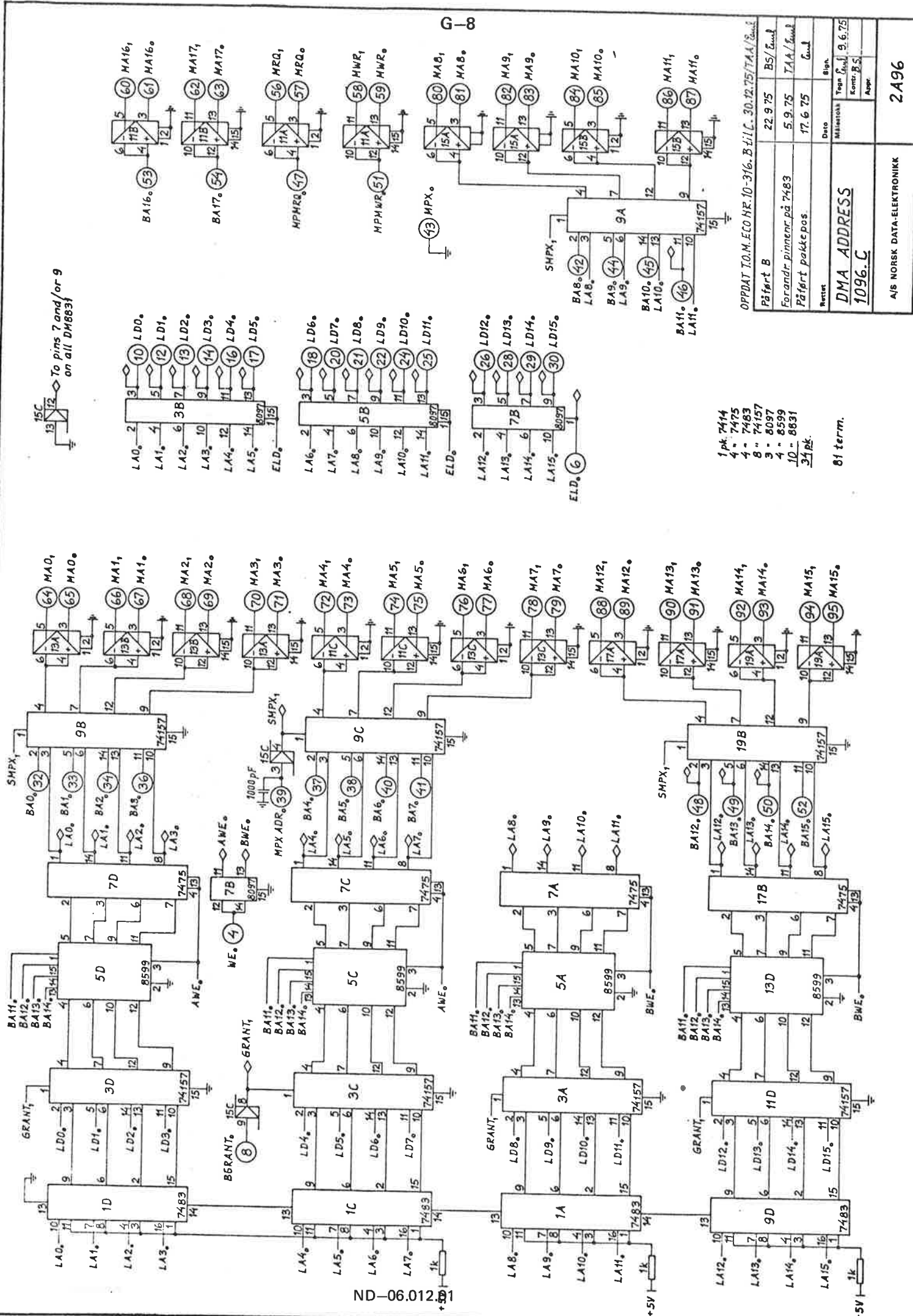




OPPDAT. IFLG.EC 10-456.G.T.H	24.11.77	Ømsl
Ajour.f. og forandr. f. a. t. c	18.6.75	TU/Ømsl
Ajour.f. og påført A.	4.4.75	TU/Ømsl
Revisert		
Materialer		Bilp.
Term.Ømsl		3.3.75
Ajour.f. og påført A.		
<b>TERMINAL BUFFER</b>		
<b>1095.H</b>		
AJS NORSK DATA-ELEKTRONIKK		
<b>2A95</b>		







15C  
To pins 7 and/or 9  
on all DM883

- 1 pk 7414
- 4 " 7475
- 4 " 7483
- 8 " 74157
- 4 " 8599
- 10 - 8831
- 34 pk.

81 term.

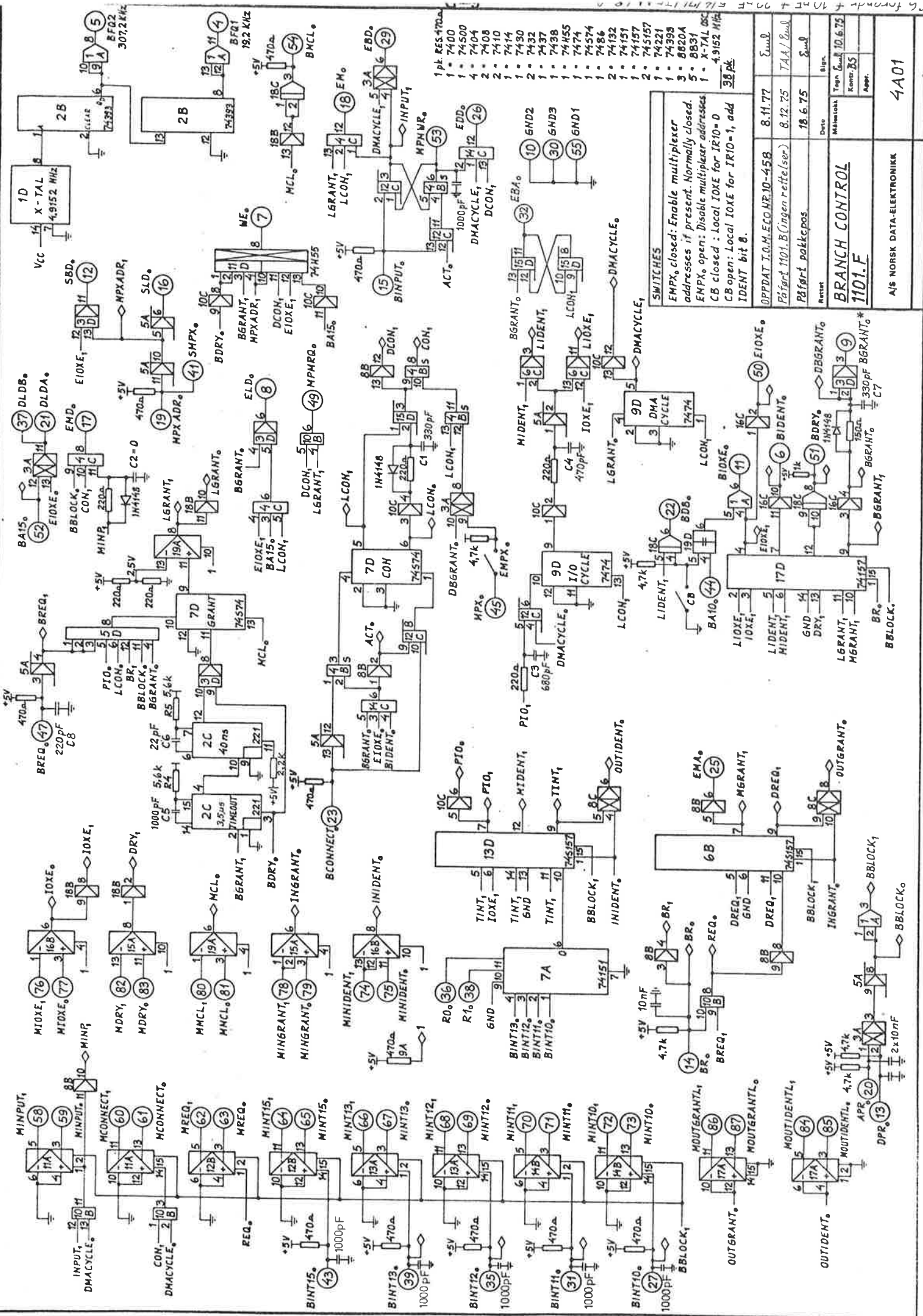
ND-06.012.01

OPPDAT I.O.M.ECO NR.10-316. B.U.L.C. 30.12.75/TAA/2001

Påført B	22.9.75	BS/Emil
Forandr. pinner på 7483	5.9.75	TAA/Emil
Påført pakkepos.	17.6.75	Emil
Revisert	Date	Sign.
	Måltattak	Tepp. Emil 9.6.75
		Kontroll B.S.
		Appr.
<b>DMA ADDRESS</b>		
<b>1096.C</b>		
2A96		

AIS NORSK DATA-ELEKTRONIKK



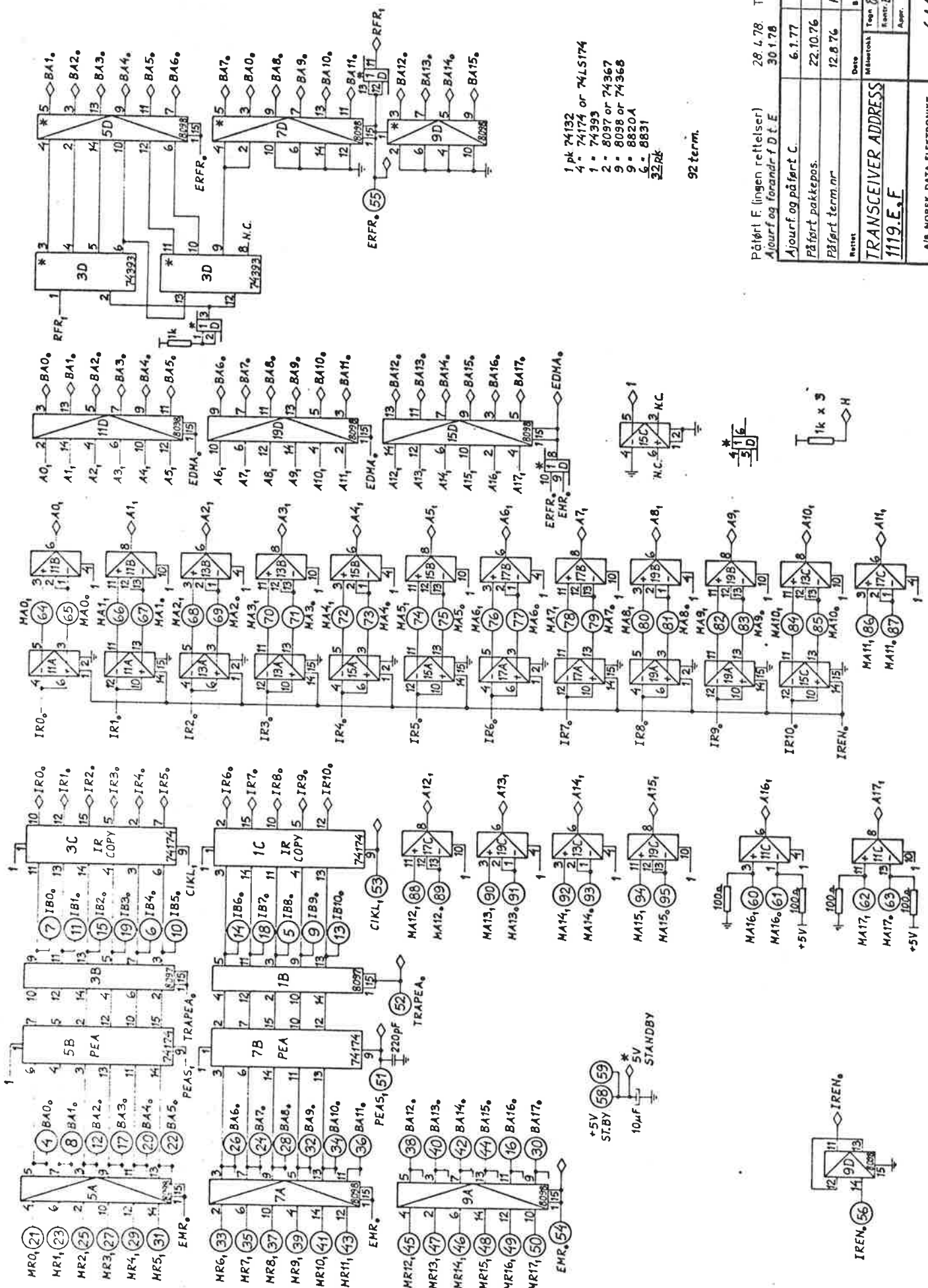


- 1 PL RES-470Ω
- 1 - 7400
- 1 - 74500
- 4 - 7404
- 2 - 7410
- 1 - 7414
- 1 - 7430
- 2 - 7432
- 1 - 7437
- 1 - 7438
- 1 - 74H55
- 1 - 7474
- 1 - 74574
- 1 - 7486
- 2 - 74132
- 1 - 74151
- 1 - 74157
- 2 - 74157
- 1 - 74221
- 1 - 74993
- 3 - 8820A
- 5 - 8834
- 1 - X-TAL OSC 4.9152 MHz

SWITCHES  
 EMPX, closed: Enable multiplexer addresses if present. Normally closed.  
 EMPX, open: Disable multiplexer addresses.  
 CB closed: Local IOXE for IRIO=0  
 CB open: Local IOXE for IRIO=1, add IDENT bit 8.

UPPDAT I.O.M. ECO NR 10-458	8.11.77	Sumbl
Påført 1101.B (ingen rettelse)	8.12.75	TAA / Sumbl
Påført pakkepos.	18.6.75	Sumbl
Revisert		
MM-skema	Tran. 6.10.75	
Kom. 85		
Appr.		
<b>BRANCH CONTROL</b>		
<b>1101.F</b>		
A/S NORSK DATA-ELEKTRONIKK		
<b>4A01</b>		





- 1pk 74132
- 4. 74174 or 74LS174
- 1. 74393
- 2. 8097 or 74367
- 9. 8098 or 74368
- 6. 8831
- 22Rk

92 term.

Påført F (ingen rettelser)	28.4.78	TEAA/BW								
Ajourført og forandret	30.1.78	HS/LSL								
Påført pakkepos.	6.1.77	HS/LSL								
Påført term.nr	22.10.76	HS/LSL								
Rettes	12.8.76	HS/LSL								
<table border="1"> <tr> <th>Dato</th> <th>Sign.</th> </tr> <tr> <td>14.5.76</td> <td></td> </tr> <tr> <td>14.5.76</td> <td></td> </tr> <tr> <td>14.5.76</td> <td></td> </tr> </table>			Dato	Sign.	14.5.76		14.5.76		14.5.76	
Dato	Sign.									
14.5.76										
14.5.76										
14.5.76										
<table border="1"> <tr> <th colspan="2">TRANSCIVEIVER ADDRESS</th> </tr> <tr> <td>1119.E.F</td> <td></td> </tr> </table>			TRANSCIVEIVER ADDRESS		1119.E.F					
TRANSCIVEIVER ADDRESS										
1119.E.F										
A/S NORSK DATA-ELEKTRONIK										
4A19										

Pin 7 and/or 9 on 8831 to H



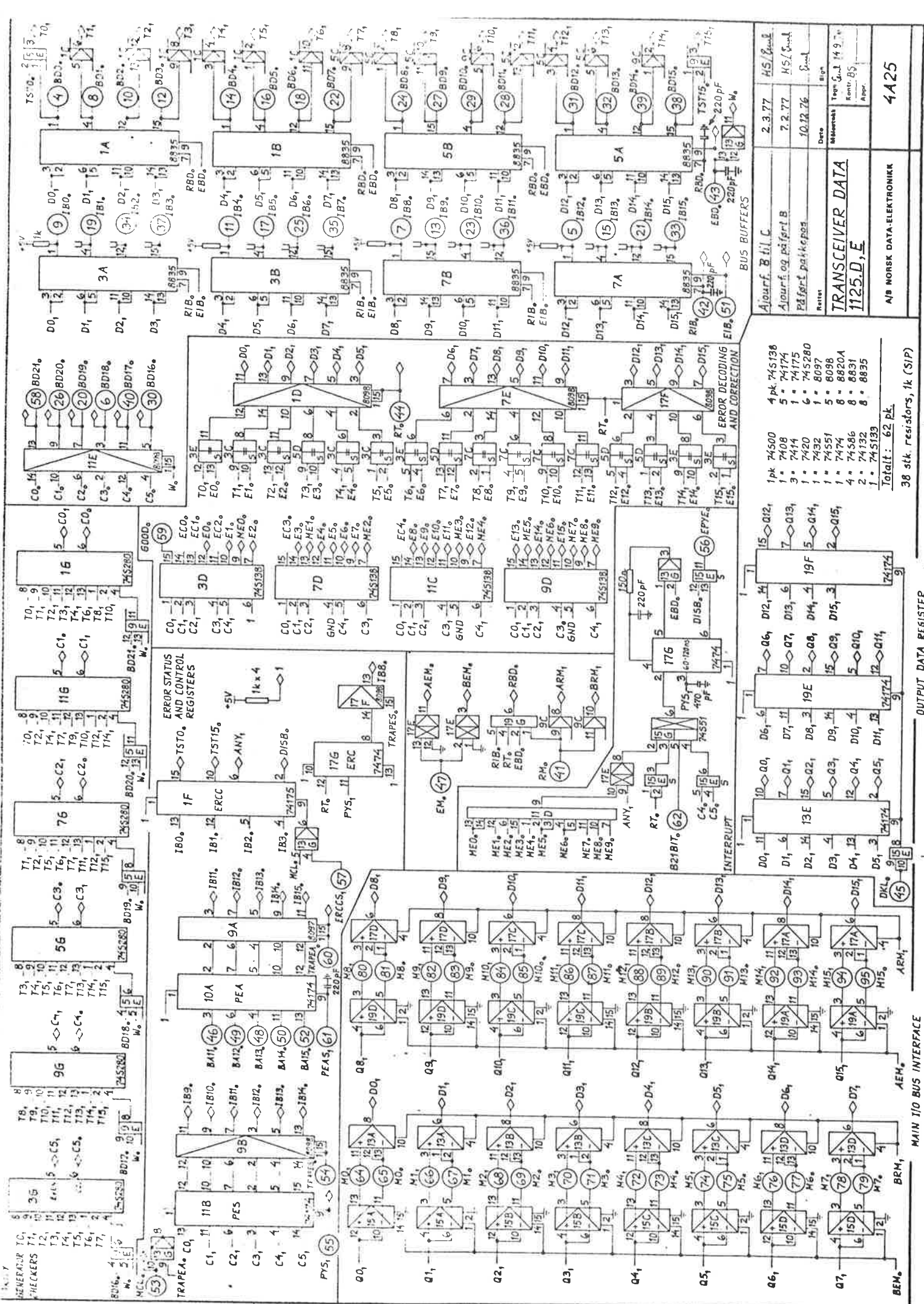


TABLE 1  
GENERAL IO CHECKERS  
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Ajourf. B til C	2.3.77	HS/200
Ajourf. og påført B	7.2.77	HS/200
Påført pakkeplan	10.12.76	HS/200
Navn: Målestørrelse: Tegning: Skala: Dato: Målestørrelse: Tegning: Skala:		
<b>TRANSCEIVER DATA</b>		
<b>1125.D.E.</b>		
A/S NORSK DATA-ELEKTRONIK		
4A25		

- 4pk 745136  
 5 " 74174  
 1 " 74175  
 6 " 745280  
 1 " 7420  
 1 " 7432  
 1 " 74551  
 1 " 7474  
 8 " 8820A  
 8 " 8831  
 2 " 74132  
 1 " 745133  
**Totalt : 62 pk.**

- 1pk 74500  
 1 " 7408  
 3 " 7414  
 1 " 745280  
 1 " 7420  
 1 " 7432  
 1 " 74551  
 1 " 7474  
 8 " 8820A  
 8 " 8831  
 2 " 74132  
 1 " 745133  
**Totalt : 62 pk.**

- 38 stk resistors, 1k (SIP)

- 4pk 745136  
 5 " 74174  
 1 " 74175  
 6 " 745280  
 1 " 7420  
 1 " 7432  
 1 " 74551  
 1 " 7474  
 8 " 8820A  
 8 " 8831  
 2 " 74132  
 1 " 745133  
**Totalt : 62 pk.**

- 38 stk resistors, 1k (SIP)

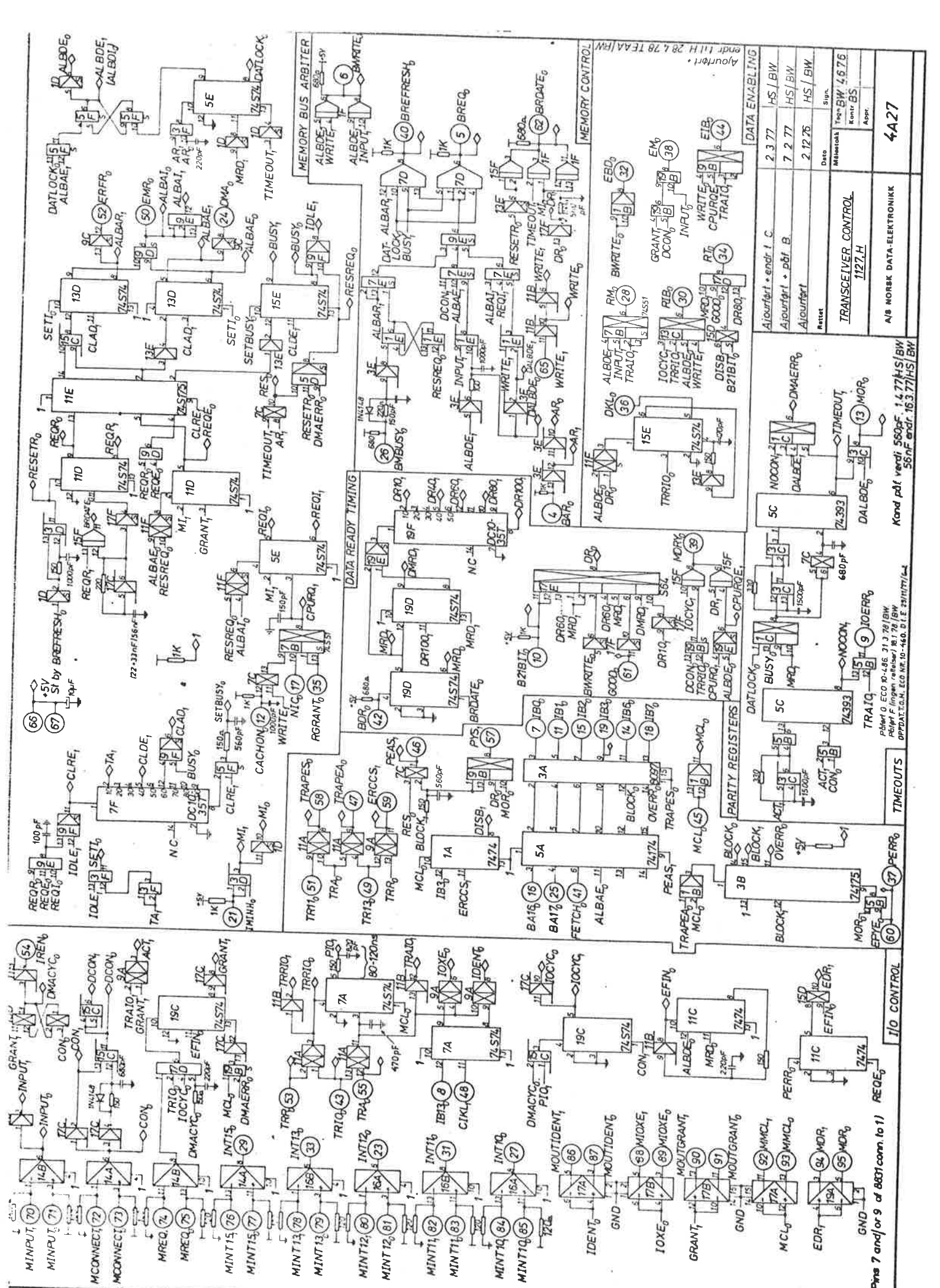
- 4pk 745136  
 5 " 74174  
 1 " 74175  
 6 " 745280  
 1 " 7420  
 1 " 7432  
 1 " 74551  
 1 " 7474  
 8 " 8820A  
 8 " 8831  
 2 " 74132  
 1 " 745133  
**Totalt : 62 pk.**

- 38 stk resistors, 1k (SIP)

- 4pk 745136  
 5 " 74174  
 1 " 74175  
 6 " 745280  
 1 " 7420  
 1 " 7432  
 1 " 74551  
 1 " 7474  
 8 " 8820A  
 8 " 8831  
 2 " 74132  
 1 " 745133  
**Totalt : 62 pk.**







Alourfert • enr i. C.  
 Alourfert • pbf B.  
 Alourfert

RESET  
 TRANSCEIVER CONTROL  
 1127.H

DATA ENABLING	HS / LBW
Alourfert • enr i. C.	2.3.77
Alourfert • pbf B.	7.2.77
Alourfert	2.12.76

Memoirek  
 Tech. BW 4.676  
 Kontr. BS

Date: \_\_\_\_\_  
 Sign.: \_\_\_\_\_

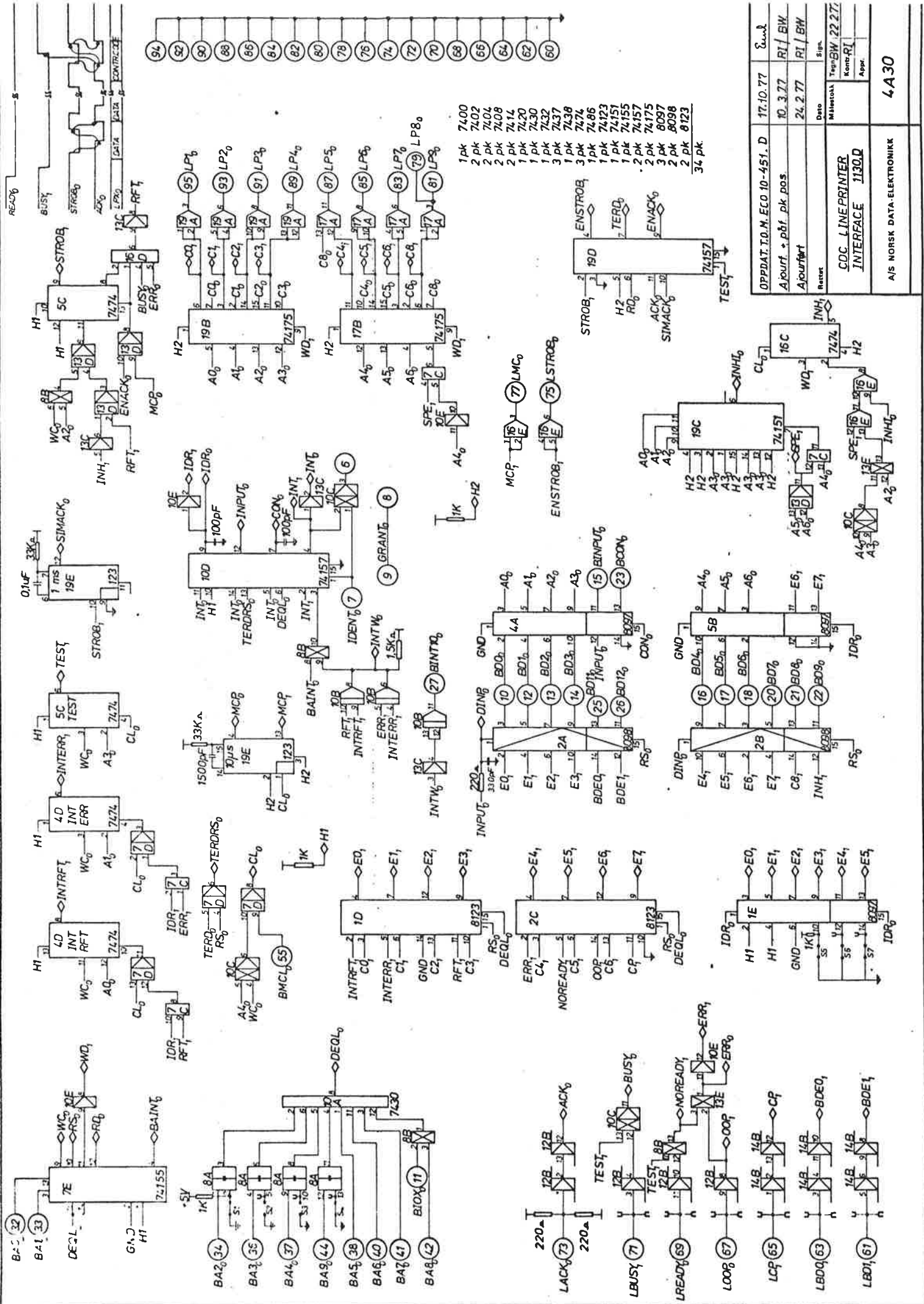
Kand pdf verdi 580pF, 1.477HS/BW  
 56nF enr. 163.77/HS/BW

P&M O. ECO 10-456. 31.7.76/BW  
 P&M F. N.M. (enr i. C.) 16.7.76/BW  
 APPROVAL: ECO. NO. 160. D.T.E. 27/11/77/14

TIMEOUTS  
 37 PERR<sub>0</sub>

I/O CONTROL  
 60 REQE<sub>0</sub>





- 1pk 7400
- 2pk 7402
- 2pk 7404
- 2pk 7408
- 1pk 7414
- 1pk 7420
- 1pk 7430
- 1pk 7432
- 3pk 7437
- 1pk 7438
- 3pk 7474
- 1pk 7486
- 1pk 74223
- 1pk 74151
- 1pk 74155
- 2pk 74157
- 2pk 74175
- 3pk 8097
- 2pk 8098
- 2pk 8123
- 34pk.

OPPDAT. T.O.M. ECO 10-451-D	17.10.77	Emil
Ajournt. + pak. pos.	10.3.77	RI / BW
Ajournt	24.2.77	RI / BW
Reviser		Sign.
COC LINEPRINTER INTERFACE 130.D		Temp. BW. 22.2.77
A/S NORSK DATA-ELEKTRONIKK		Appr.
4A30		



APPENDIX H

NORD-10 I/O SYSTEM HISTORIC OVERVIEW

BASIC I/O CONFIGURATION

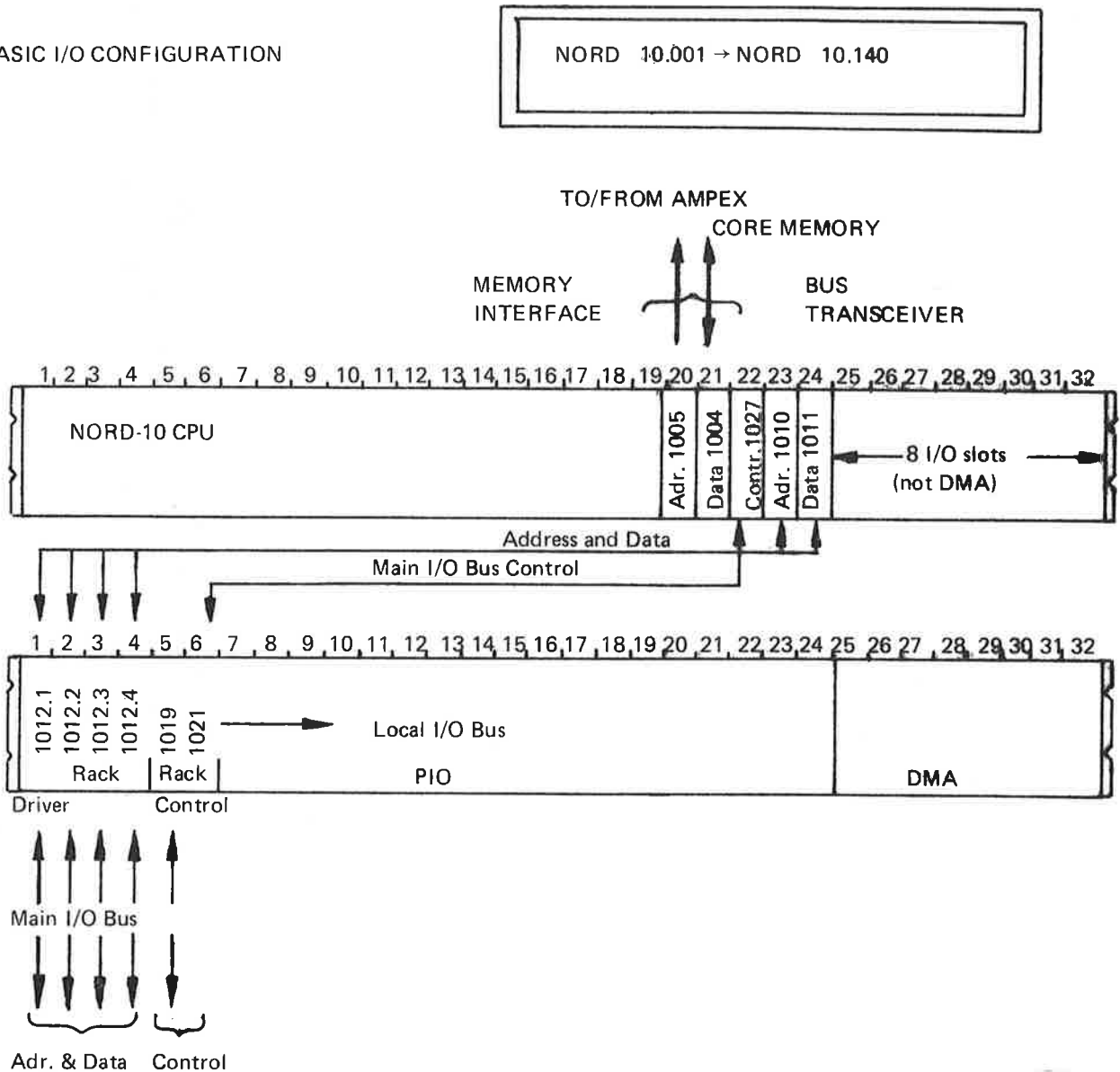


Figure 1.5: TYPICAL I/O CONFIGURATION  
NORD 10.001 - NORD 10.140

Main differences from N-10S:

- 8 I/O slots for PIO interfaces in the CPU-rack
- Possible to connect-customer equipment via the Main I/O BUS.
- No MPM channel available. All DMA transfer via the CPU.
- One rack-driver module 1012 contains; Drivers/receivers for 4 data and address bits and 4 bits of the Core Address-Register.

**MODULE 1012 RACK DRIVER**

- Transfer 4 bits of the Main I/O Data-bus MD
- Transfer 4 bits of the Main I/O Address-bus MA
- Convert 4 bits of the MD-bus to local tristate BD-bus
- Convert 4 bits of the MA-bus to local tristate BA-bus
- Contains 4 bits of the Core Address-Register
- Contains 4 bits of UPPER and LOWER address limit-register (Normally disabled)

Bit 0-3	4-7	8-11	12-15
1012.1	1012.2	1012.3	1012.4

**MODULE 1019 RACK CONTROL 1**

- Priority network for External/Local INTERRUPT and REQUEST
- Circuits for receiving/sending external control signals:  
(CONNECT, INPUT, REQUEST / IDENT, DRY, MCL)

**MODULE 1021 RACK CONTROL 2**

- Drivers/receivers for control signals to/from CPU
- Drivers/receivers for control signals to/from next I/O-rack
- Protect-registers address decoding
- Terminal oscillator generation (BFQ1 and BFQ2)

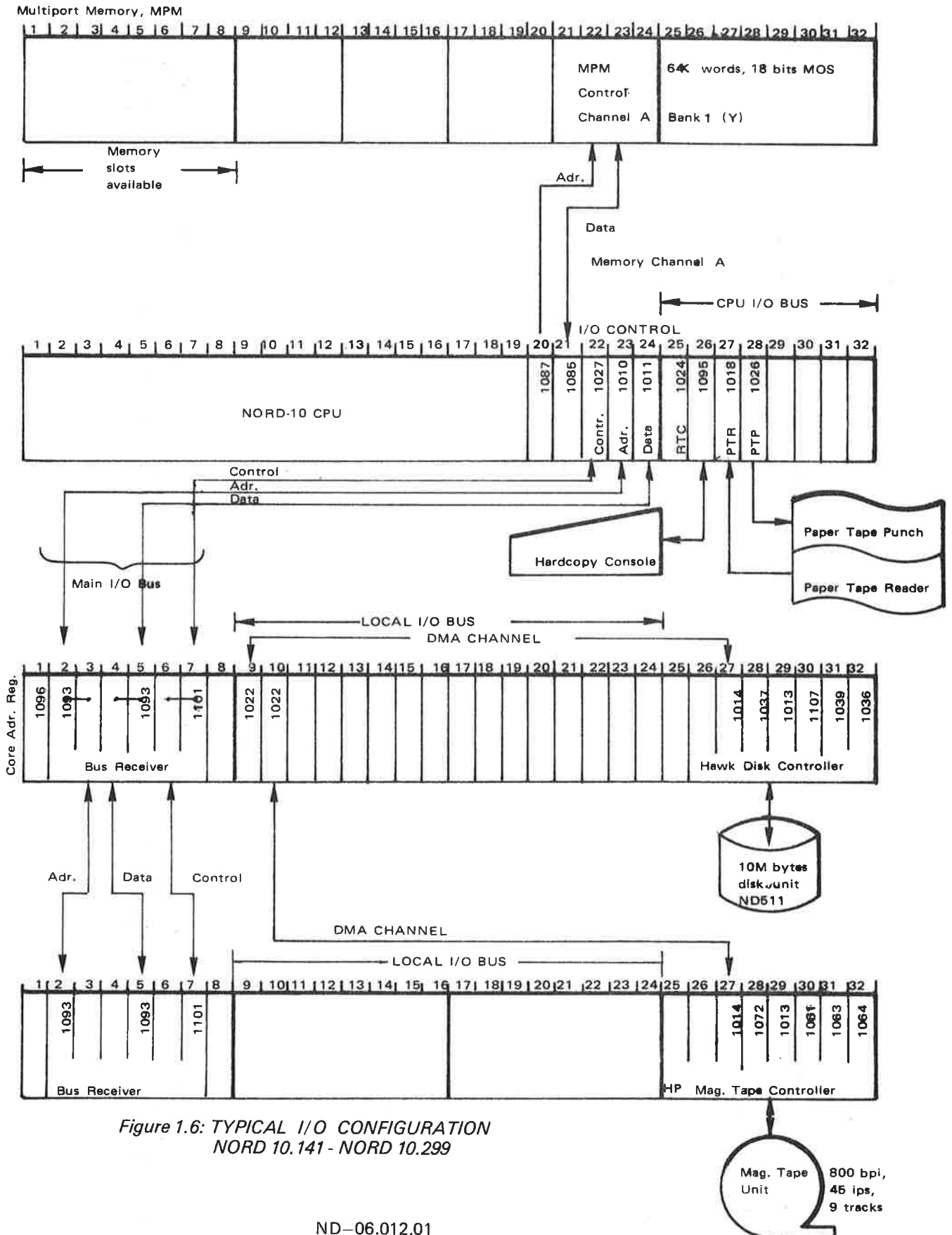
NORD 10.141 — NORD 10.299

The multiport-memory system, introducing the MOS-memory was designed in the summer 1975. To live up to the name of a DMA-transfer for mass storage interfaces, the BUS RECEIVER/BRANCHER was designed. Built into the system, is the possibility to perform a true Direct Memory Access. (The BUS BRANCHER.

Main differences from N-10/S:

- 8 I/O slots for PIO interfaces in the CPU-rack
- No Local Memory
- No Cache Memory
- During the DMA transfer via CPU, data is passed via the CPU data bus IB

**BASIC I/O CONFIGURATION**





BASIC I/O CONFIGURATION

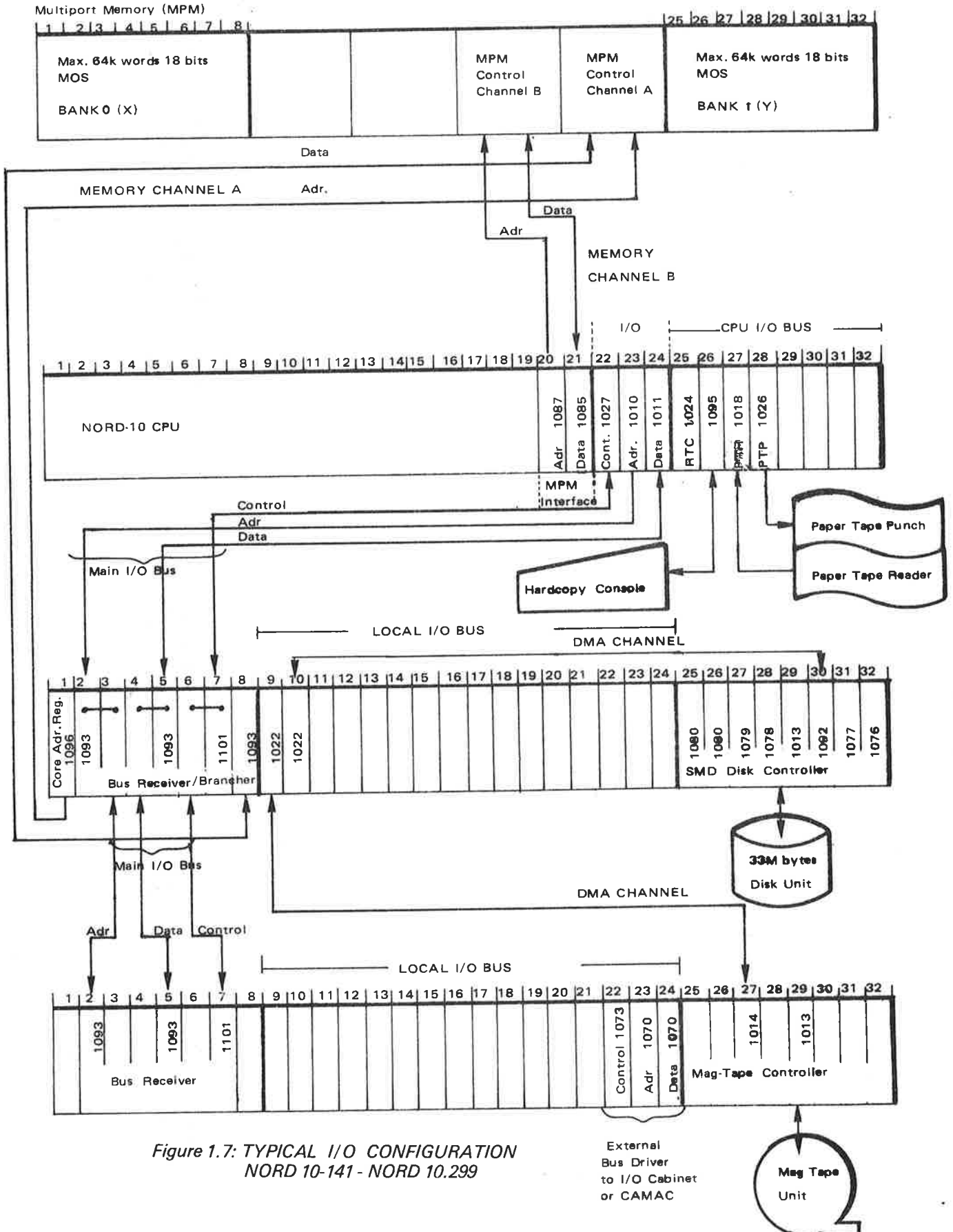
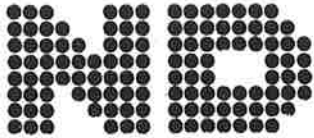


Figure 1.7: TYPICAL I/O CONFIGURATION  
NORD 10-141 - NORD 10.299



NORSK DATA A. S.

Lørenveien 57 - Postboks 163, Økern

OSLO 1

## COMMENT AND EVALUATION SHEET

ND-06.012.01

NORD-10/S INPUT/OUTPUT SYSTEM

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM

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**– we make bits for the future**

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