BIG MULTIPORT MEMORY SYSTEM

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1 BIG MULTIPORT MEMORY SYSTEM

1.1 *GENERAL*

The Big Multiport Memory System (referred to as BMPM) is a high speed flexible and modular memory system used for two major applications:

1. Increased memory band width to enable for higher total data transfer rates to and from memory.

2. Allow for multiprocessor and/or multi-device communication via a common memory system.

This is accomplished by using a number of independent memory banks accessed by a number of independent memory ports. The system is modular with respect to banks, channels and storage capacity.

Each memory channel has an address range of 2048K words and may be connected from 1 to 10 ports.

Single bit error correction and multiple error detection is standard.

A special service channel is provided for a number of operations and maintenance purposes.

1.2 *THE MEMORY SYSTEM*

A memory system (refer to Figure 1.1) is a collection of independent *banks,* each covering a definite address space. Every bank is linked together and to the outside world by *Channels.* The entrance for channels is called *Ports.* The Channels in the system are driver from *Sources.*

The Sources are interfaces between the memory system and the unit demanding access. In order to maintain a well-defined intersection the sources are not considered part of the memory system.

In addition to the ordinary channels a *special service channel* exists. All banks are linked to the service channel which is driven from an I/O interface.

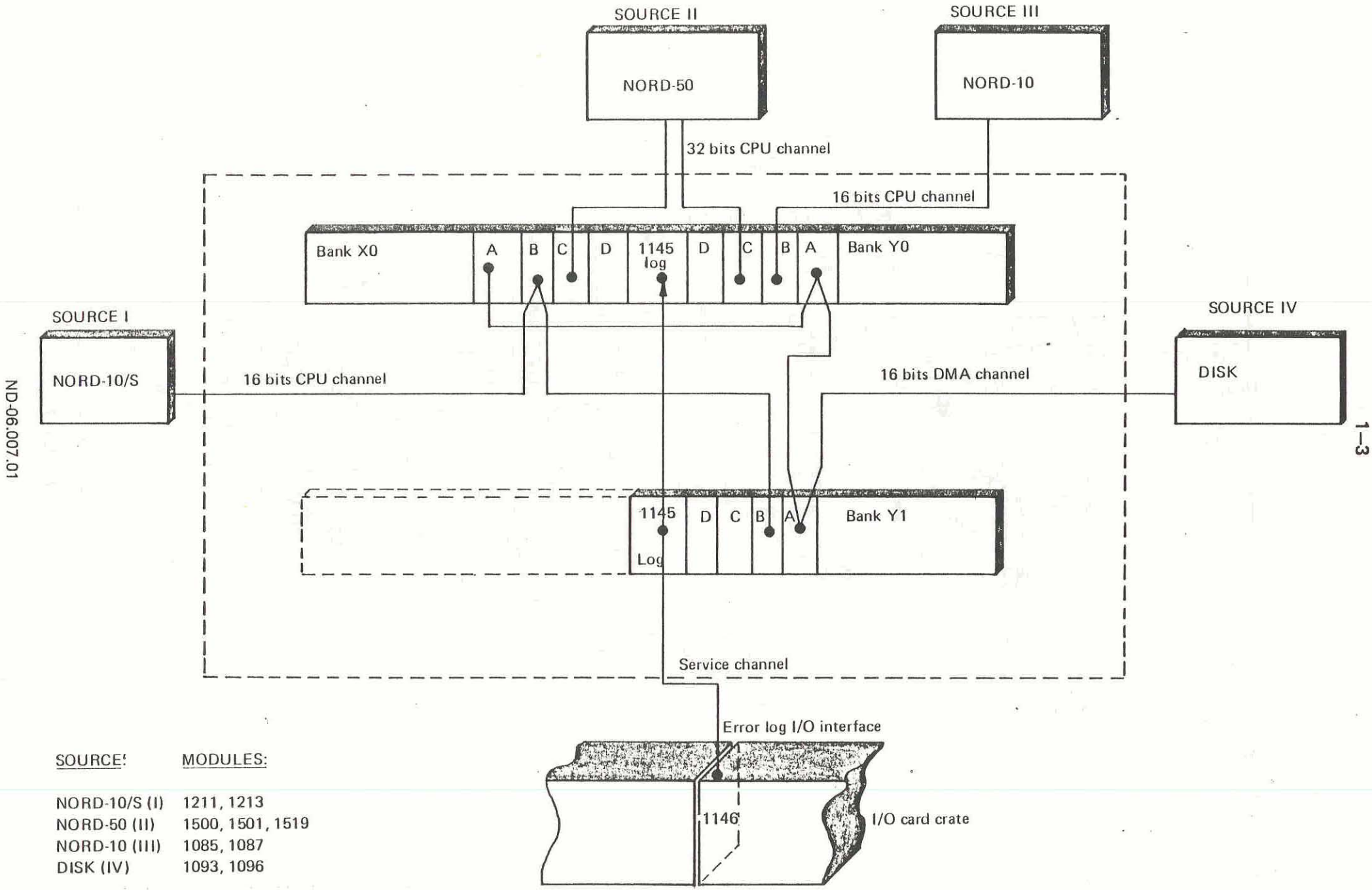
1.3 *SYSTEM PARTS*

1.3.1 *Crate*

For the following discussion refer to Figure 1.2.

Although the bank is logically the basic building block, the card rate is physically the basic unit, containing one or two banks, an X-bank and a Y-bank. This is done purely for space and wiring reasons. In BMPM there is no logic in common between the two banks as it is on the former model. Yet the service channel has common logic since it will always be connected in a predetermined manner.

A maximum of 8 crates can be used in a Memory system.



SOURCE:	MODULES:
NORD-10/S (I)	1211, 1213
NORD-50 (II)	1500, 1501, 1519
NORD-10 (III)	1085, 1087
DISK (IV)	1093, 1096

Figure 1.1: Multiport Configuration — Example

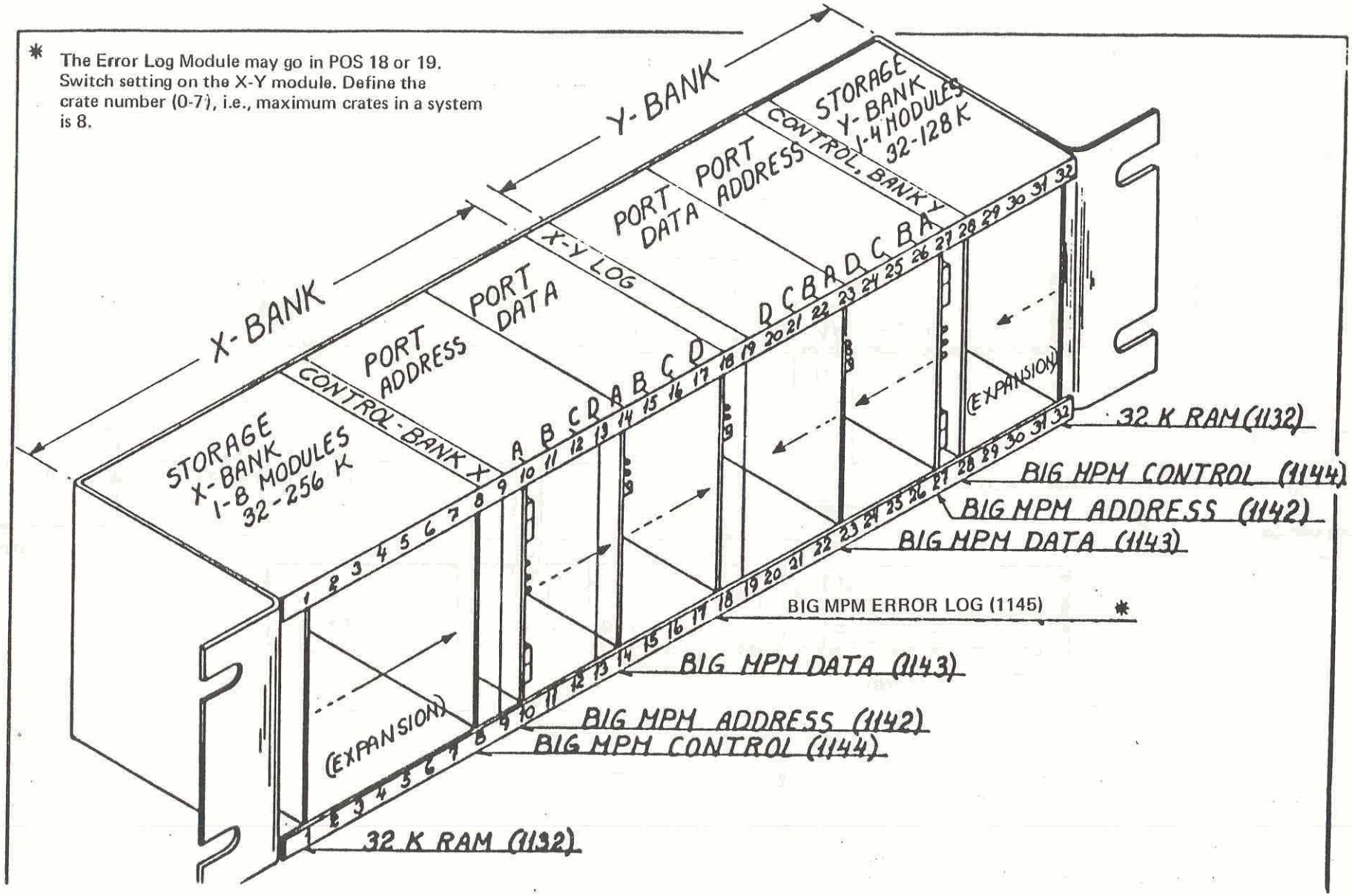


Figure 1.2: Multiport Memory (1 card crate)

1.3.2 *Bank*

A bank is an independent memory unit that can cycle by itself. It also has it's own timing and control logic.

Two banks can be located in one card crate, one X-bank and one Y-bank.

A complete bank consists of the following parts:

* Controller (1144)
* Storage (1132's)
* Ports (1142, 1143)
* Error logic (1145)

1.3.3 *Controller (1144)*

It is essential that a bank has a private controller which allows it to operate independent of other banks.

The controller solves two major tasks.

1. To serve as a "switchboard" between the ports on one side and the storage on the other

2. To refresh the MOS memory elements at regular intervals.

Since up to 4 ports (A - D) may access the same storage, a priority network allocates the storage to one port for one storage cycle at a time.

The ports and refresh are assigned a fixed priority which is, beginning at the highest priority:

New request from same port as previous one, REFRESH, PORT A, PORT B, PORT C, PORT D

When two ports make requests simultaneously the highest priority port will be served first.

Note! It is not possible for one high priority port to lock out the lower priority ones. The reason is that the request must toggle on and off.

Even if a channel is capable of absorbing everything it could get from memory, it must withdraw the request for a moment to prepare for the next. At that very moment the lower priority port will be granted access.

However, *two* high priority ports are able to lock the bank for lower priority ports.

Periodic refresh is necessary in MOS memories to avoid decline of information. This is accomplished by regularly accessing all memory cells. These accesses (one each 15 *vs*) may be treated similar to accesses from the ports.

The refresh request circuitry and refresh address counter is located in the controller (1144).

1.3.4 *Storage (1132's)*

An X-bank has room for 8 storage modules and a Y-bank has room for 4 storage modules. Each module contains 32K x 21 memory cells (bits). Hence, one X-bank is sufficient to cover all NORD-10/S' primary storage requirements of 256K words.

Internally in the bank the address range is always from 0 in 32K increments up to 256K. Hence, an address transformation is normally required at each port. (Refer to Section 1.4 regarding addressing.)

The 18 address bits required for a 256K address range are used as shown in Figure 1.3.

The *memory integrated circuits (MIC)* contain *16K x 1 bit.* Hence, two MIC's are needed per data bit on a 32K module. Since storage of 21 data bits are required each storage module contains 42 MIC's. The 5 extra bits are used by the control code attached to the 16 data bits. (Error checking and correction is described in Section 1.5.)

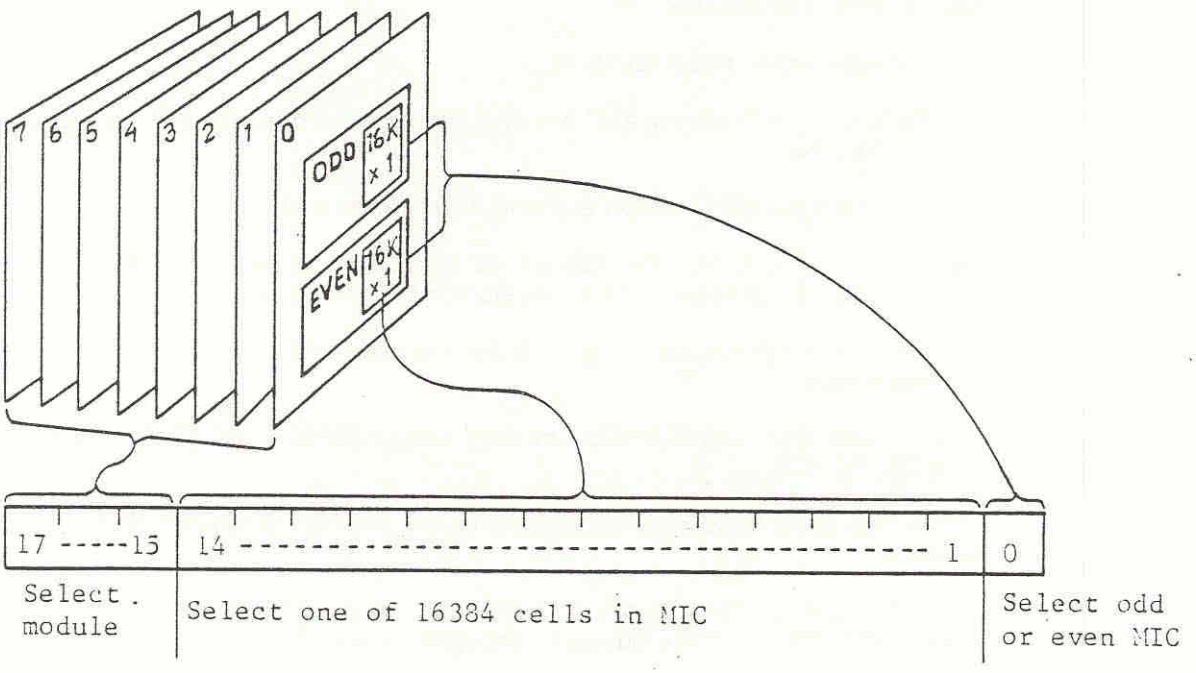


Figure 1.3: Use of Internal Bank Address

1.3.5 *Port (1142, 1143)*

A port is the entrance for a channel to a bank. A bank holds from 1 to 4 ports (A - D). A port consists of receivers for addresses and transmitters and receivers for data and control lines.

Up to 10 ports can be linked together (daisy chained) by a channel, i.e., a source can access up to 10 banks of storage.

A port consists of a data (1143) and an address (1142) module. A port carries out two major functions:

1. Select a bank for the source and convert the channel address to a local bank address (1142).

2. — Generate a 5 bit control code to be attached to data during write and
   — check the data against the control code during read.

Each port defines the address range for a bank (1142). (Refer to Section 1.4.) Normally, the address range is the same as seen from the different ports, but for special purposes they will be different. One such example is the NORD-10/NORD-50 communication using BMPM as a common memory.

1.3.6 *Channel*

In the memory system a Channel is physically a pair of cables. One cable carries address and request signals while the other carries *data* and *ready* signals. With the word channel we will normally mean a *16 bit data* channel. It is, however, possible to define a *32 bit* channel consisting of one address cable and two data cables. Since all ports are 16 bits wide, two ports are required in that case. A 32 bits channel is illustrated in Figure 1.1.

All channels meet only one type of port. Hence, all sources must conform to the same *specifications* when requesting memory.

It is normally possible to connect several banks to one channel.

Every port has one input and one output connector for each cable, which allows *daisy chaining* of up to 10 ports. At the end of the chain a *termination* plug is mounted.

Note! The two banks in the same crate have their ports daisy chained internally. Figure 1.4 shows signals appearing on a channel.

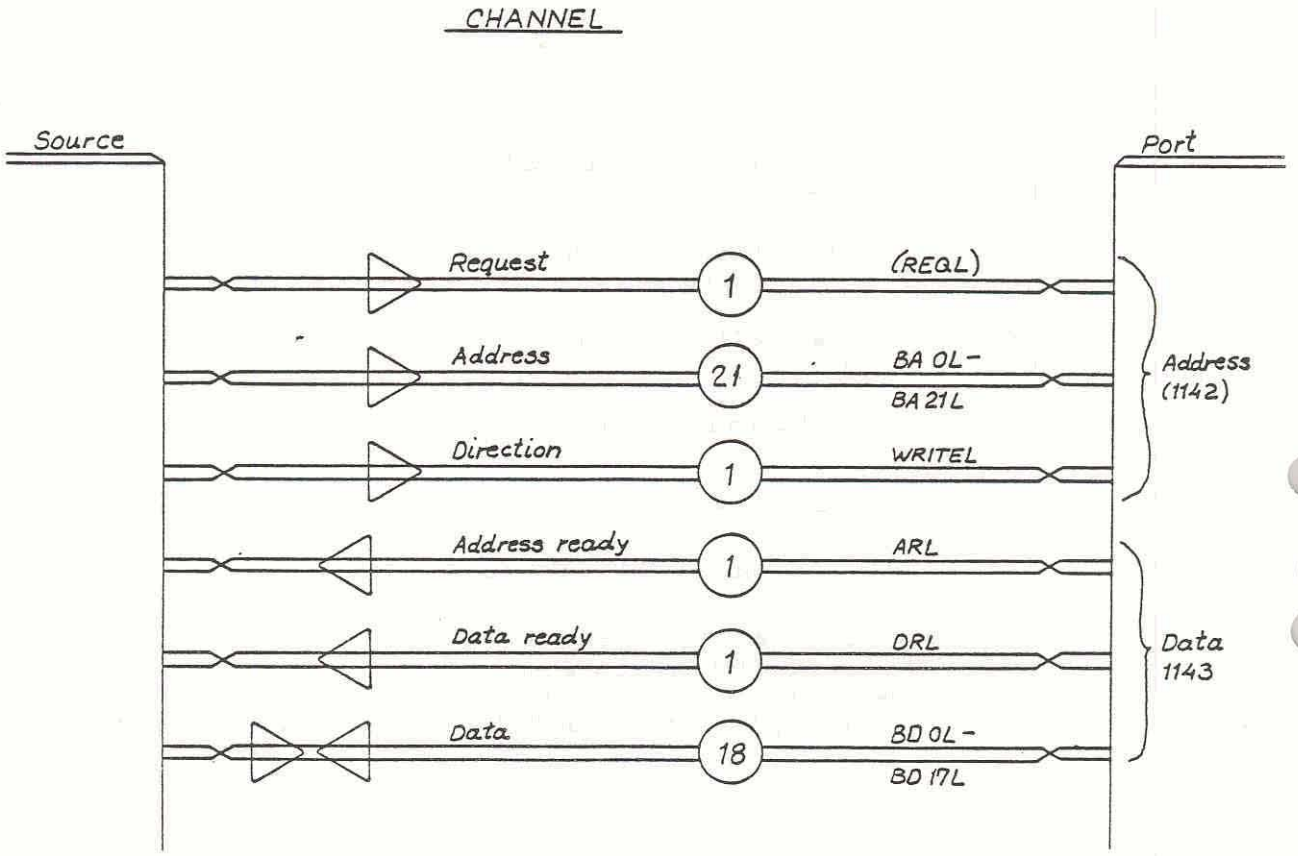


Figure 1.4: Channel Signals

Note 1: A 32 bits channel consists of one address cable and two data cables.

Note 2: Up to 10 ports may be chained to one source. The cables must be terminated in the last port.

Note 3: Transmitters and receivers in the ports meet the RS-422 specifications. (Refer to Appendix E.)

1.3.7 *Source*

A Source can be any kind of electronic unit which is capable of communicating with BMPM over a channel. Examples of sources can be: NORD-10, NORD-10/S, NORD-50 or DMA interfaces. The sources must conform to the channel specifications (refer also to Figure 1.1).

1.3.8 *Service Channel*

The service channel consists of an error log module (1145) located in the BMPM, an error log I/O interface module (1146) located in the NORD-10/S input/output system and a cable connecting those two modules together. BMPM will thus be regarded as an I/O device as seen from NORD-10/S.

The error log module (1145) is logically divided into two parts, one serves the X-bank and the other the Y-bank. Each part contains an error log memory. All errors (single or multiple) occurring in the bank and detected by the ports (1143's), will be recorded in this special memory. The error log memory is organized as a 512 x 1 bit memory where the address is a pointer to the failing memory integrated circuit (MIC).

A thumb wheel switch located on this module defines the crate number (0 - 7).

The service channel can perform the following four functions:

1. (Action: 00), Refer to Figure 1.5.

   Scan the error log memory for a failing bit. The error log memory address where the failing bit is found (pointer to the failing MIC) is transferred to a one-word scan register located in the error log I/O interface (1146).

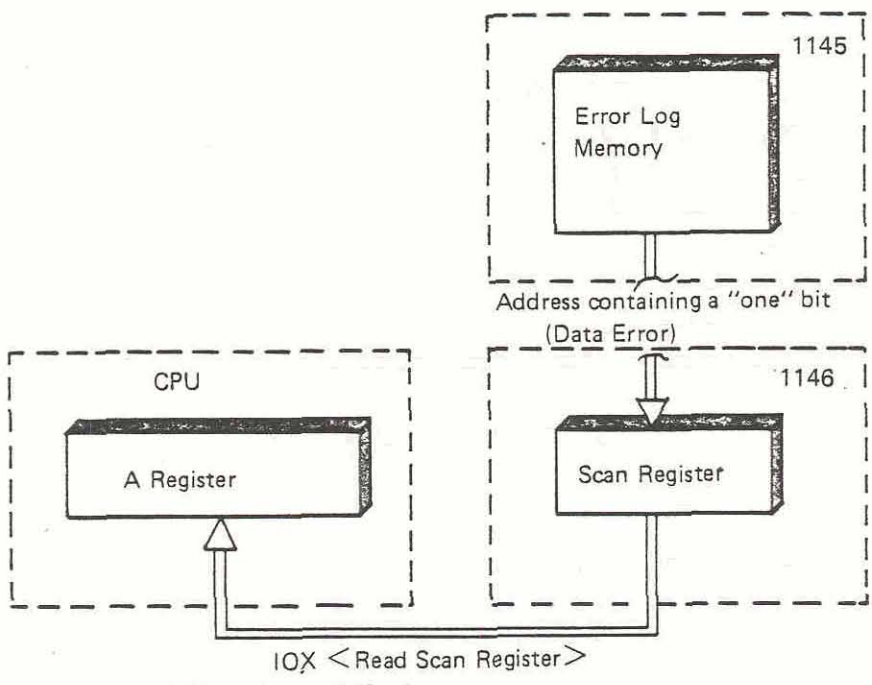


Figure 1.5: Scan Error Log

2. (Action: 01), Refer to Figure 1.6.

   Scan the present ports for bank address range setting. This operation will also give the information whether the ports have detected an error or not.

Steps 1 and 2 are feed-back information from the BMPM and will be written into the scan register located in the error log I/O interface (1146). This will be transferred to the A register of the CPU by execution of an IOX <Read Scan Register> (IOX 750).

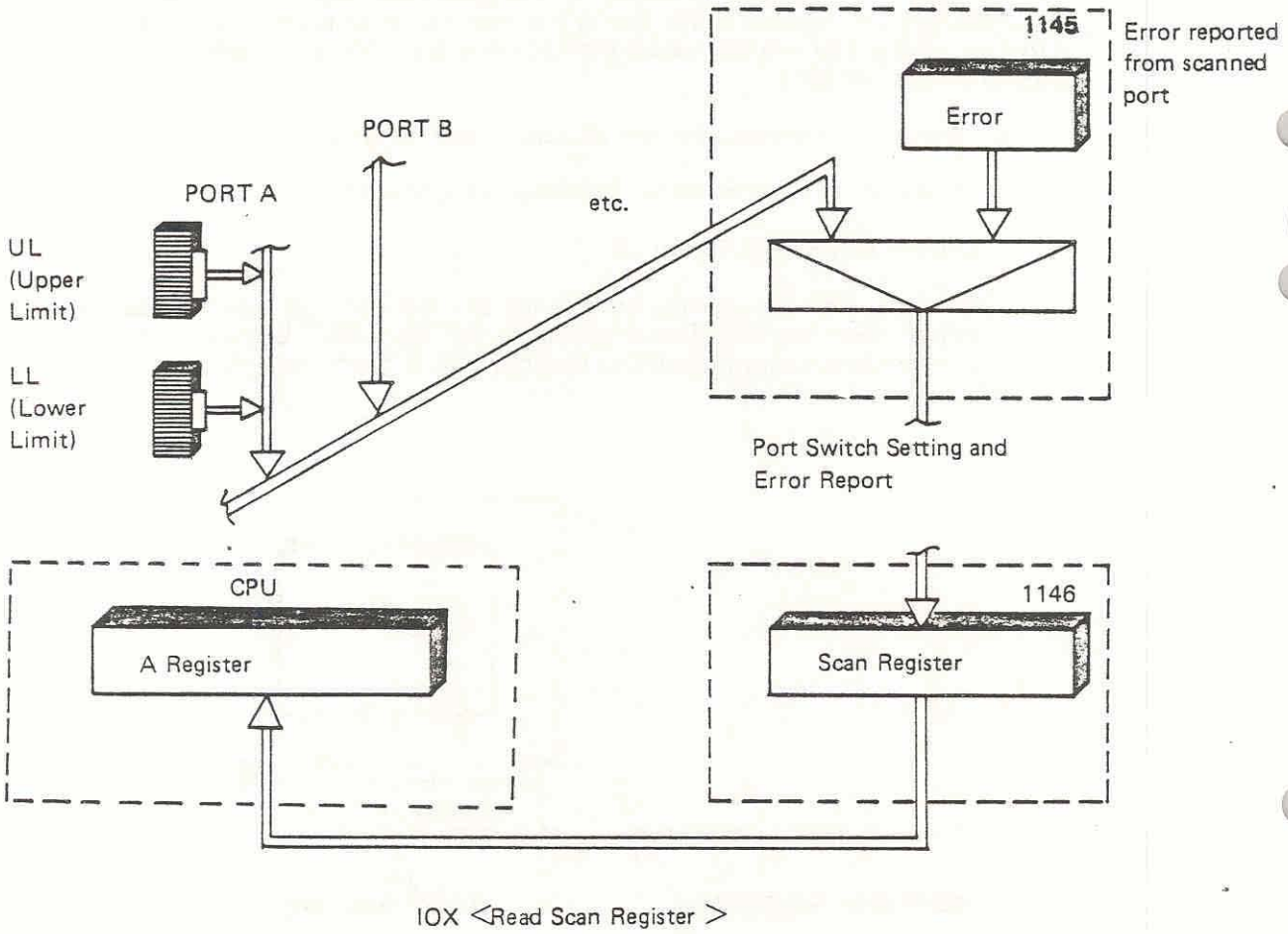


Figure 1.6: Scan Port Status

3. (Action: 10), Refer to Figure 1.7.

   Set the content of the error correction control register (ECC) located in the data module (1143) of the ports.

4. (Action: 11), Refer to Figure 1.8.

   Execute test access. A read or write operation can be simulated without a channel connected.

Steps 3 and 4 are control information for the BMPM. The control information is transferred from the A register in the CPU to the command register located in the error log I/O interface (1146) by executing an IOX <Load Command Register> (IOX 751). From this register the control information is sent to BMPM via the error log module (1145).

Information regarding detailed description of programming specifications and word formats is given in Chapter 3.

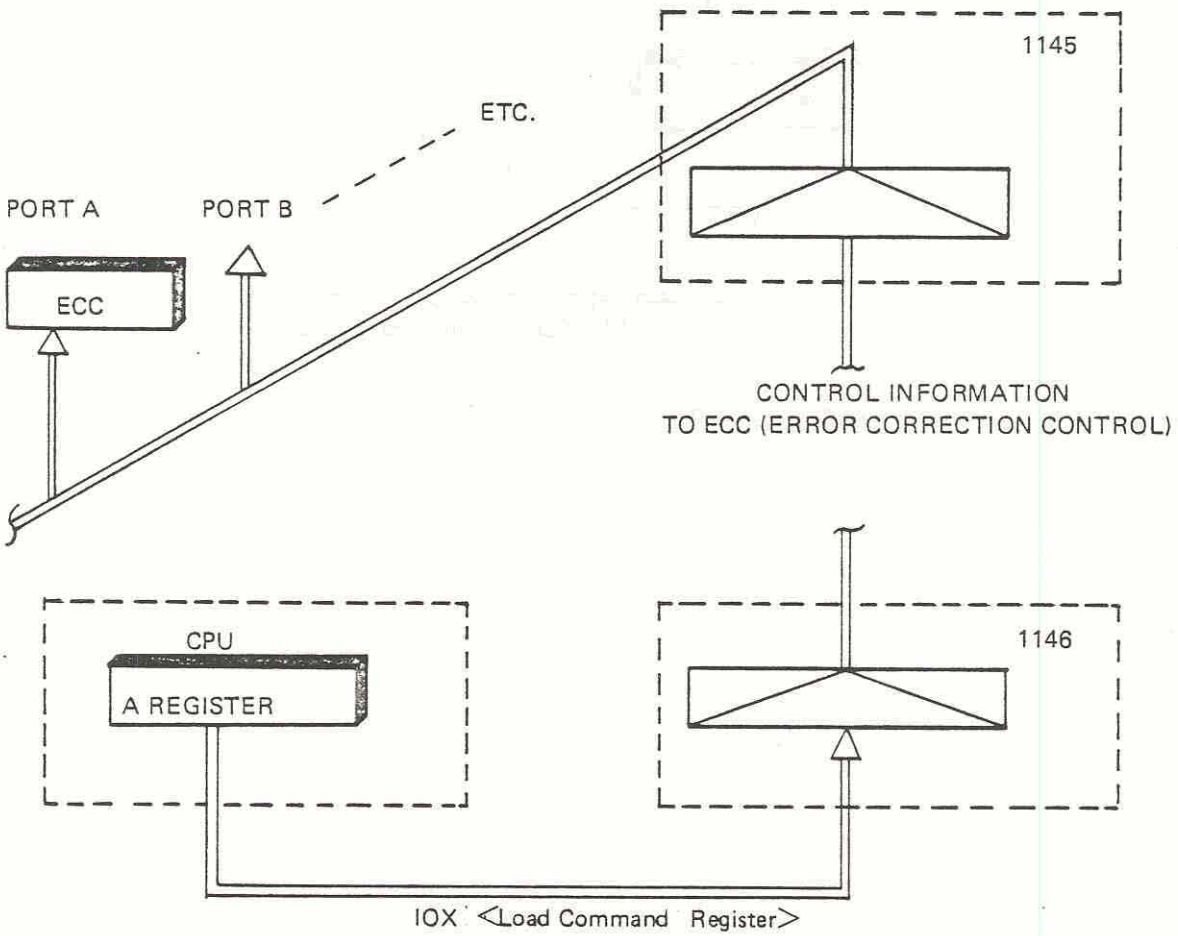


Figure 1.7: Write ECC Register

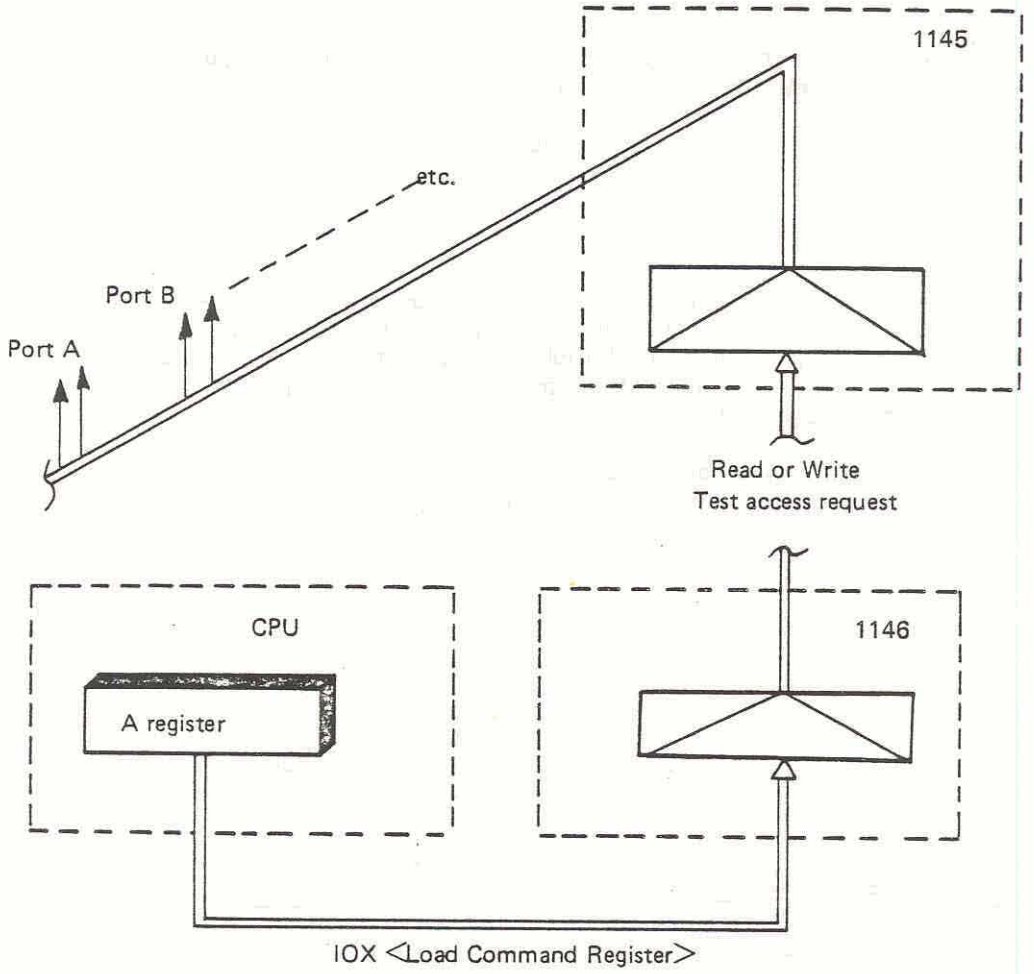


Figure 1.8: Execute Test Access

1.4 *ADDRESSING*

1.4.1 *Address Conversion*

The total address range of a channel is 2048K (21 address bits). Since each bank has a range of 256K, 8 banks are necessary to cover the complete range. Hence, the 3 most significant address bits could be decoded for bank selection.

However, since the minimum size of a bank is 32K (1 storage module) it is desirable that one has a resolution of 32K for selection. Hence, the 6 most significant bits are needed for decoding of 32K banks.

Straight decoding requires banks of equal size, so to permit banks of different sizes a more flexible method is required.

Each port has therefore a set of limit switches which define the address range the port will respond to.

One pair determines lower limit, LL, and one pair determines upper limit, UL. Each pair holds a two-digit octal number. Refer to the chart in Figure 1.9 for the corresponding address range.

When a request appears on the channel, all ports test the address against their limit switches. The request shall have access if:

$LL \leqslant \text{Channel Address} < UL$

Inside all banks the address range is 0 - 256K, so the channel address must normally be transformed to an internal bank address which is offset by the lower limit (LL).

This transformation is performed at the port, and it is a simple subtraction:

Bank Address = Channel Address — Lower Limit

Accordingly, channel address equal to lower limit is directed into bank address 0.

Observe that two channels *may* access the same memory cell although their channel addresses are *different*. Address skew between channels should be avoided as much as possible since it makes the system very opaque both from a hardware and software point of view.

Max. no. of card crates: 8
Max. no. of ports per crate: 8
i,e. max. no. of ports(8x8): 64
If each source uses only one bank
max. no. of sources: 64

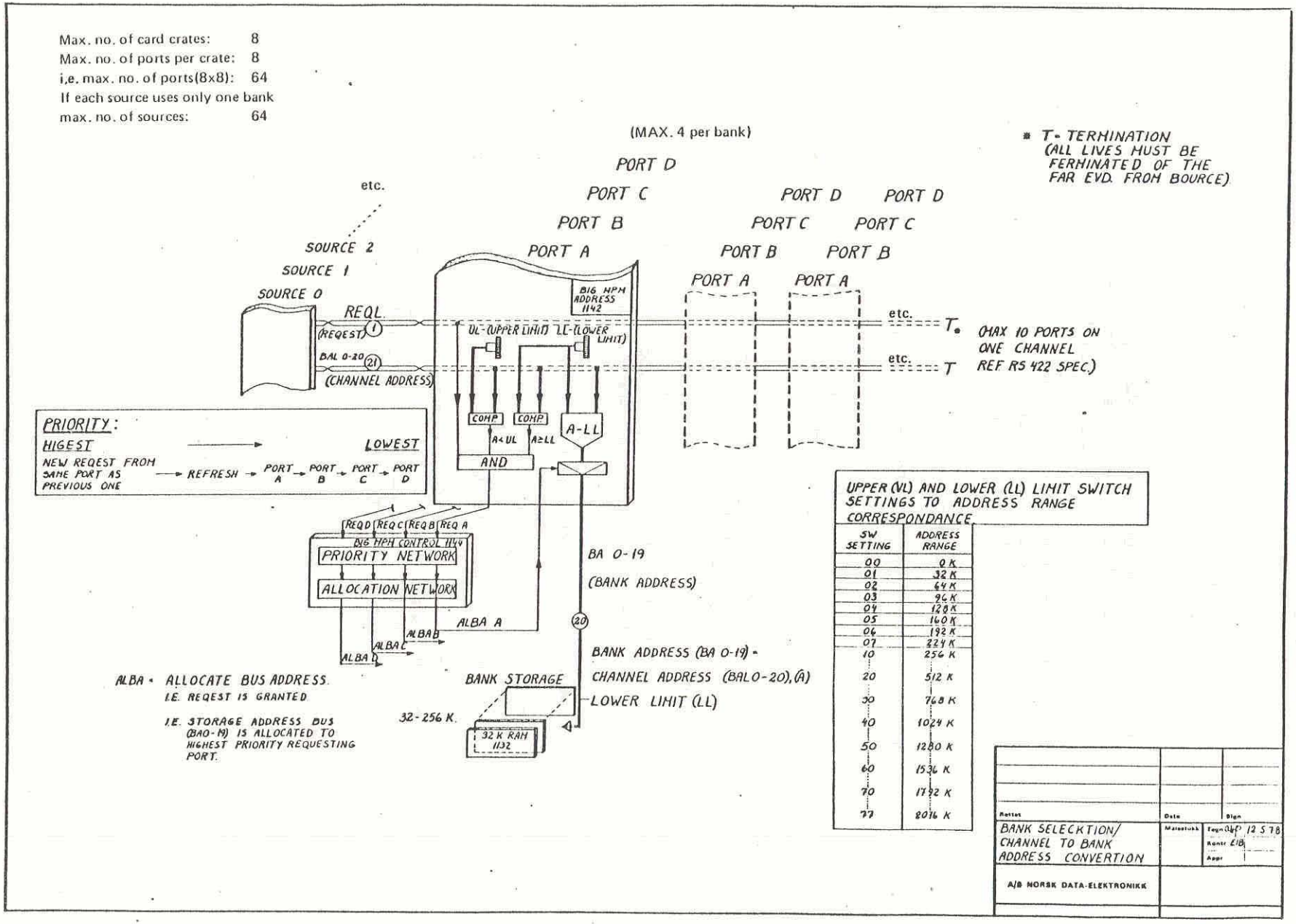


Figure 1.9: Bank Selection/Channel to Bank Address Conversion

1.4.2 *Bank Selection*

For the following discussion refer to Figure 1.9.

When a source places an address on the bus together with a Request all the ports linked together by the channel will examine the channel address. The port (1142) that finds the channel address within its limits (LL ⩽ A < UL) will forward the request to the controller (1144).

Since the 4 ports associated with a given bank operate completely asynchronously with respect to each other, a priority network is required. The highest priority port will then be allocated to storage for one memory cycle. The bank address = (channel address — lower limit) will then be enabled onto the local bank address bus.

For further information regarding storage to port communication refer to Figure 1.10.

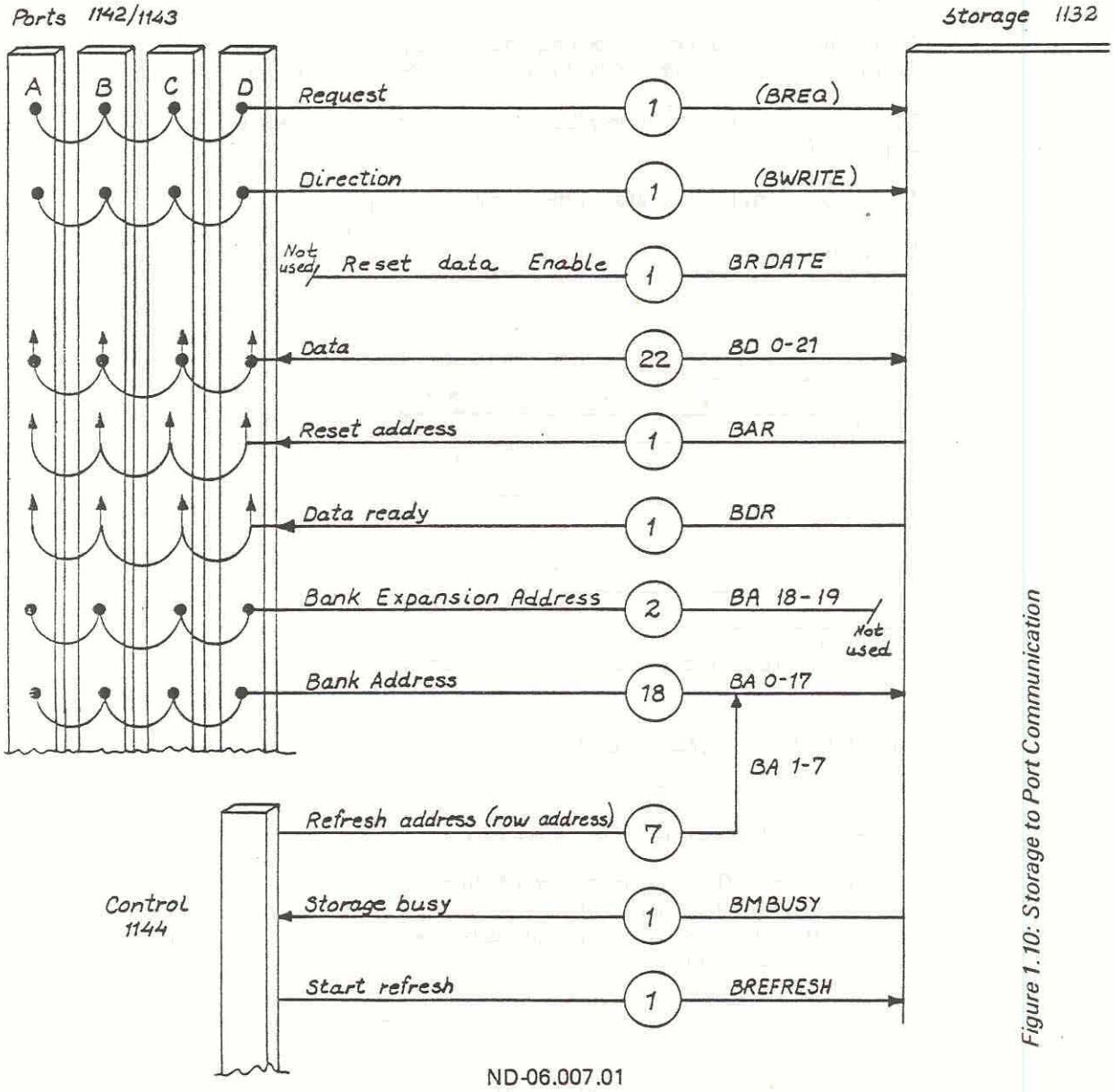


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Figure 1.10: Storage to Port Communication

1.4.3 *Interleave (Shifted Address)*

To increase memory band width an interleave techique can be used. However, it is only meaningful in a pipeline system where a new request is issued before the previous is serviced.

In a less critical sense "interleave" is used to designate shifting of the address bits.

If the address is rotationally shifted one place to the right, bit 0 will receive position 20, bit 20 position 19 and so on. The effect is that all even addresses will seem to lie between 0 and 1024K while all odd addresses will appear as lying between 1024K and 2048K.

Two consecutive addresses (as seen from program) will therefore lie in different banks. The band width benefit expectation from this shifting is greatly exagerated when memory accesses are not pipelined.

However, interleaving is necessary when 16 bit and 32 bit channels are to communicate.

Two 16 bit words, at consecutive addresses, may be read as *one 32 bit* word when the two 16 bit words *reside in different banks.* (See Figures 1.12 and 1.13.)

The address shifting is performed by modifying the address cable as shown in Appendix C.

The concept may be illustrated in the following example.

Example:

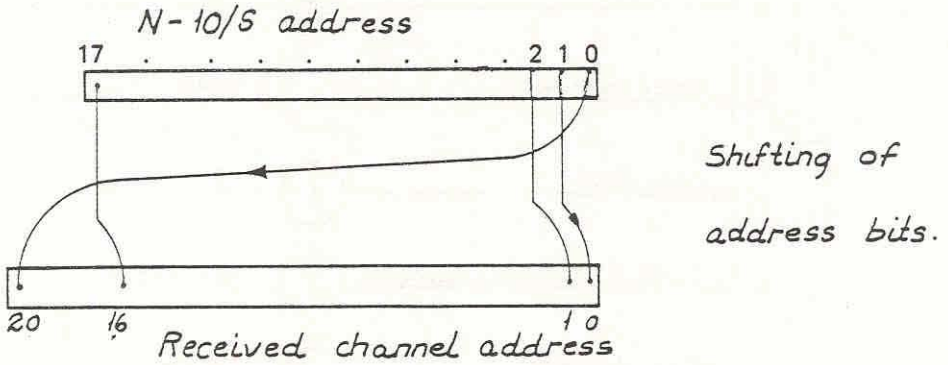


Figure 1.11: Shifting of Address Bits

Address bit number 20 is used to select a bank.

Assuming NORD-10/S is storing 4 words in memory in consequtive locations (as seen from NORD-10/S) the lowest bit on the issued address will toggle and alternating banks will be selected. If the issued addresses are 0, 1, 2 and 3, the received addresses would be:

Received Address:	Word No.:
0 0 0 0 0 0 0	(1)
4 0 0 0 0 0 0	(2)
0 0 0 0 0 0 1	(3)
4 0 0 0 0 0 1	(4)

etc.

The following illustration will show how the four words will be stored.

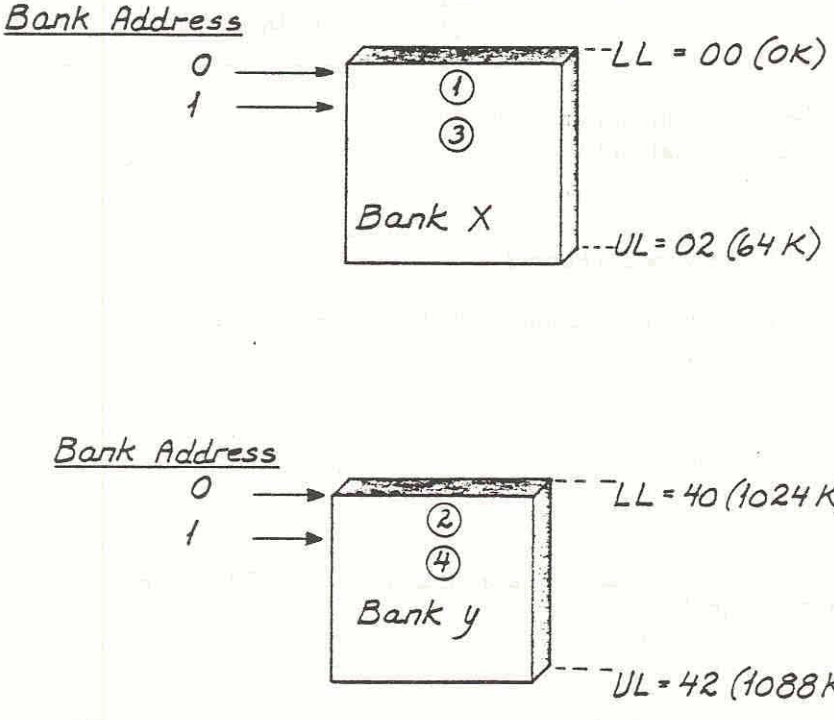


Figure 1.12: The Banks as Seen from NORD-10/S

When NORD-50 reads those 4 NORD-10/S words, it regards the same two banks as one bank with double word length. The 4 16 bit words will then be read as two 32 bit words.

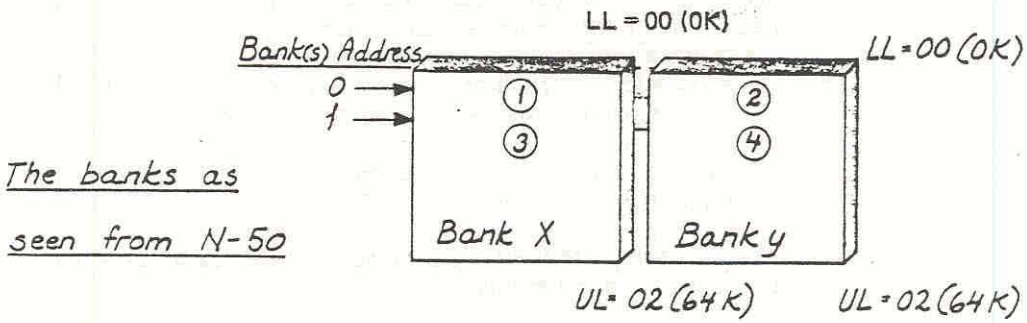


Figure 1.13: The Banks as Seen from NORD-50

1.5 *DATA*

1.5.1 *Format*

As seen from the source (NORD-10/S), the standard BMPM data width is the 16 bits associated with 2 odd parity bits, one for lower, one for upper byte.

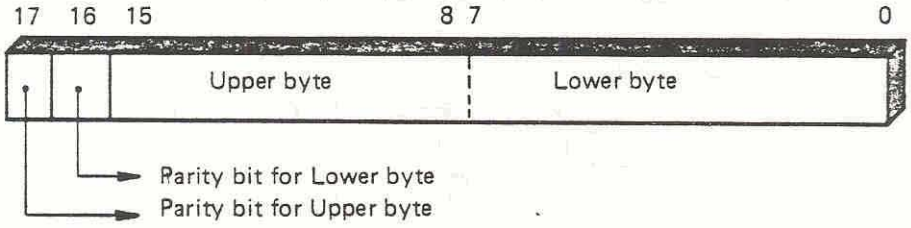


Figure 1.14: Channel Data Format

This makes the BMPM compatible with the former model.

1.5.2 *Data Protection*

Data is protected by means of a 5 bit control code. Error correction is therefore standard in BMPM.

1.5.2.1 General about Error Detection and Correction

In an error correcting memory 5 parity bits are stored in addition to the normal 16 data bits. These 5 bits are parities formed by the data bits in a unique way. Each port has its private error correction network in order to load the common memory resources as little as possible. The two source-generated parity bits are skipped and 5 new control bits are generated. The port could have checked the parity of write data but hardly informed the system in a proper way. It could have reported "Hey, I have seen an error", but it is impossible for the system to decide what action to take on such information. The reason for error would probably be a faulty cable, which would be detected by reading anyhow.

Although many people find error correction obscure, the practical treatment is quite straight forward and is shown in Figure 1.21.

For the sake of clarity, generation and checking are shown separately although they actually have common circuitry.

The following 5 parities serve as control bits and are generated at each *write* access.

C0 = 0 ⊕ 1 ⊕ 2 ⊕ 3 ⊕ 4 ⊕ 6 ⊕ 8 ⊕ 10
C1 = 0 ⊕ 2 ⊕ 4 ⊕ 7 ⊕ 9 ⊕ 10 ⊕ 12 ⊕ 14
C2 = 1 ⊕ 2 ⊕ 5 ⊕ 7 ⊕ 11 ⊕ 12 ⊕ 15
C3 = 3 ⊕ 4 ⊕ 5 ⊕ 6 ⊕ 7 ⊕ 13 ⊕ 14 ⊕ 15
C4 = 8 ⊕ 9 ⊕ 10 ⊕ 11 ⊕ 12 ⊕ 13 ⊕ 14 ⊕ 15

They are stored together with the 16 data bits in memory.

When data is *read* the parity of the 21 bit word is checked. If no errors have been introduced all parities are *unchanged* which gives the error code 00000 = GOOD. The 5 bits in the error code are called syndrome bits. If GOOD does not show up there must be a single bit or a multiple bit error.

How can these five bits really point out the faulty bit? The reason is that two different data bits never contribute in the same manner in *all* parities. For example, bit 2 is a part of C0, C1 and C2. If bit 2 has been changed (inverted) since generation C0, C1 and C2 will also be inverted. Hence, the error code 00111 is produced instead of the GOOD code 00000 which means no bit changed. Referance to Figure 1.15 will show that, in fact, 00111 is the error code for bit 2. Since error in bit 1 changes C0 and C2, 00101 is the error code for bit 1, etc.

It is important to note that only error in *one bit at a time* is assumed.

Since 21 bits can produce only 21 single error codes the remaining codes must be caused by *errors in some combination of two or more bits.* Those errors cannot be corrected and are therefore fatal to the system.

A decoder is used to decide which of the 31 possible errors has occurred (see Figure 1.15).

In case it is a single bit error the correspondig bit is inverted by an EXCLUSIVE-OR gate.

In case a *multiple error* is detected a FATAL ERROR signal is generated. This signal *inverts the otherwise correct parity bit 16.*

Accordingly, multiple errors force a parity error which is detected by a normal parity check in the source. Single bit errors are (of course) not reported to the source. However, all errors are written in the error log (1145).

The theory for error correction is also covered in Section II.6 of the manual "NORD-10/S Functional Description (ND-06.009).

	S4	S3	S2	S1	S0	No Error	Single Data Error	Single Error Error	Multiple Errors
0	0	0	0	0	0	Good			
1	0	0	0	0	1			C0	
2	0	0	0	1	0			C1	
3	0	0	0	1	1		E0		
4	0	0	1	0	0			C2	
5	0	0	1	0	1		E1		
6	0	0	1	1	0				ME0
7	0	0	1	1	1		E2		
10	0	1	0	0	0			C3	
11	0	1	0	0	1		E3		
12	0	1	0	1	0				ME1
13	0	1	0	1	1		E4		
14	0	1	1	0	0		E5		
15	0	1	1	0	1		E6		
16	0	1	1	1	0		E7		
17	0	1	1	1	1				ME2
20	1	0	0	0	0			C4	
21	1	0	0	0	1		E8		
22	1	0	0	1	0		E9		
23	1	0	0	1	1		E10		
24	1	0	1	0	0		E11		
25	1	0	1	0	1				ME3
26	1	0	1	1	0		E12		
27	1	0	1	1	1				ME4
30	1	1	0	0	0		E13		
31	1	1	0	0	1				ME5
32	1	1	0	1	0		E14		
33	1	1	0	1	1				ME6
34	1	1	1	0	0		E15		
35	1	1	1	0	1				ME7
36	1	1	1	1	0				ME8
37	1	1	1	1	1				ME9

Figure 1.15: Syndrome Decoding

1.5.2.2. Write

During a store operation the port (1143) will receive the data in the format as indicated in Figure 1.14.

The two parity bits are not processed in any manner by the port. Based on the 16 data bits a 5 bits control code is generated and sent to memory with the data. This is illustrated in Figure 1.16.

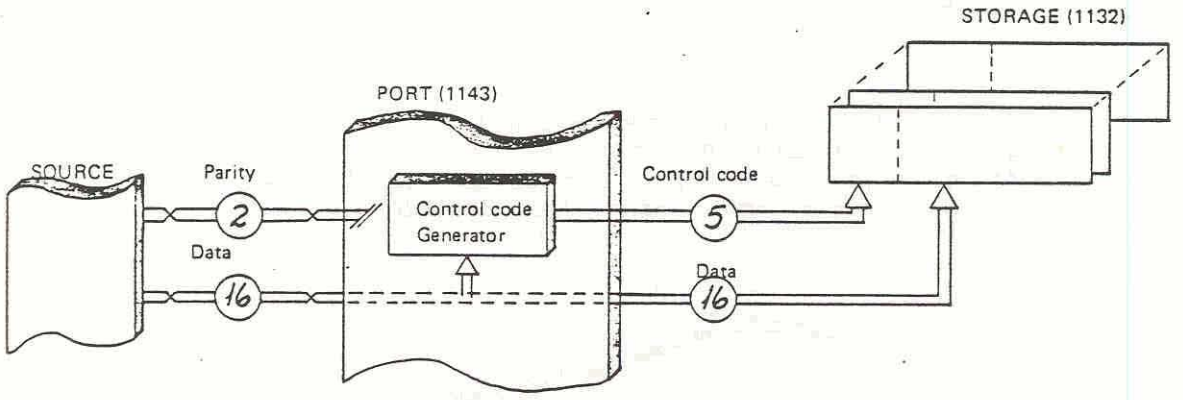


Figure 1.16: Data Flow on Write

Note! Addressing and bank selection is not covered here.

1.5.2.3 Read

During a read operation the addressed data is received from the selected storage by the port (1143). Working on the 16 data bits, a new control code is generated and compared with the one stored with the data. If they are equal, the data is accepted as Good data.

The difference (exclusive OR) between the "new" and the "old" control code is called the syndrome. If the syndrome is equal to 0, the data is Good. As the control codes are checked, two parity bits are generated in the port (1143) and sent to the source with the data. See Figure 1.17.

1.5.2.4 Single Data Error

If a single data bit is failing, the 5 bits syndrome (exlusive OR of "new" and "old" control code) will be different from zero ($\neq 0$) where the syndrom (code) is a pointer to the failing bit. The failing bit is corrected (inverted) and the correct parity bits wil be generated and sent to the source with the correct data. The syndrome ($\neq 0$) will be sent to the error log module (1145) to indicate where and what type of error has occurred. See Figure 1.18.

1.5.2.5 Single Control Code Error

Using the same type of memory for storing the control code, a single bit can also be failing in the code. The syndrome (code) will also here be a pointer to which control bit that was failing. No data need be corrected for this type of error. The synfrome is sent to the error log module (1145).

1.5.2.6 Multiple Error

A multiple error is a type of error where more than one bit is failing within the 21 bits field. In this case the data cannot be corrected. To indicate that the data is not correct, the parity bit for the lower byte is forced false (BDL 16). The syndrome is here also sent to the error log module (1145). See also Figure 1.19.

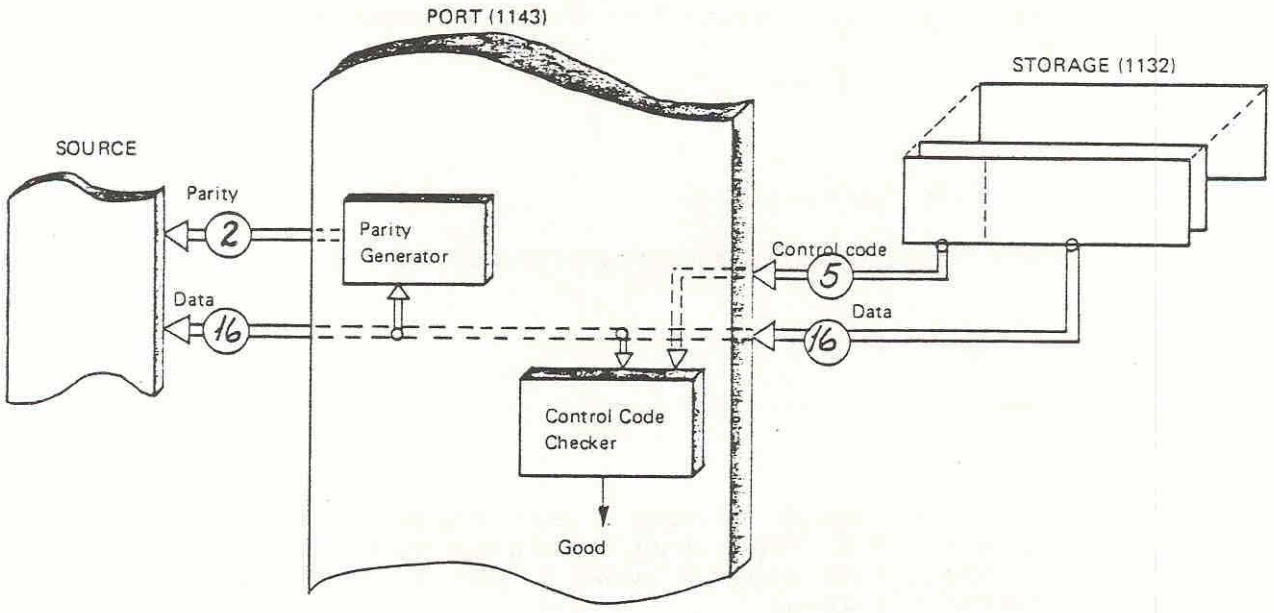


Figure 1.17: Reading Data (No Error)

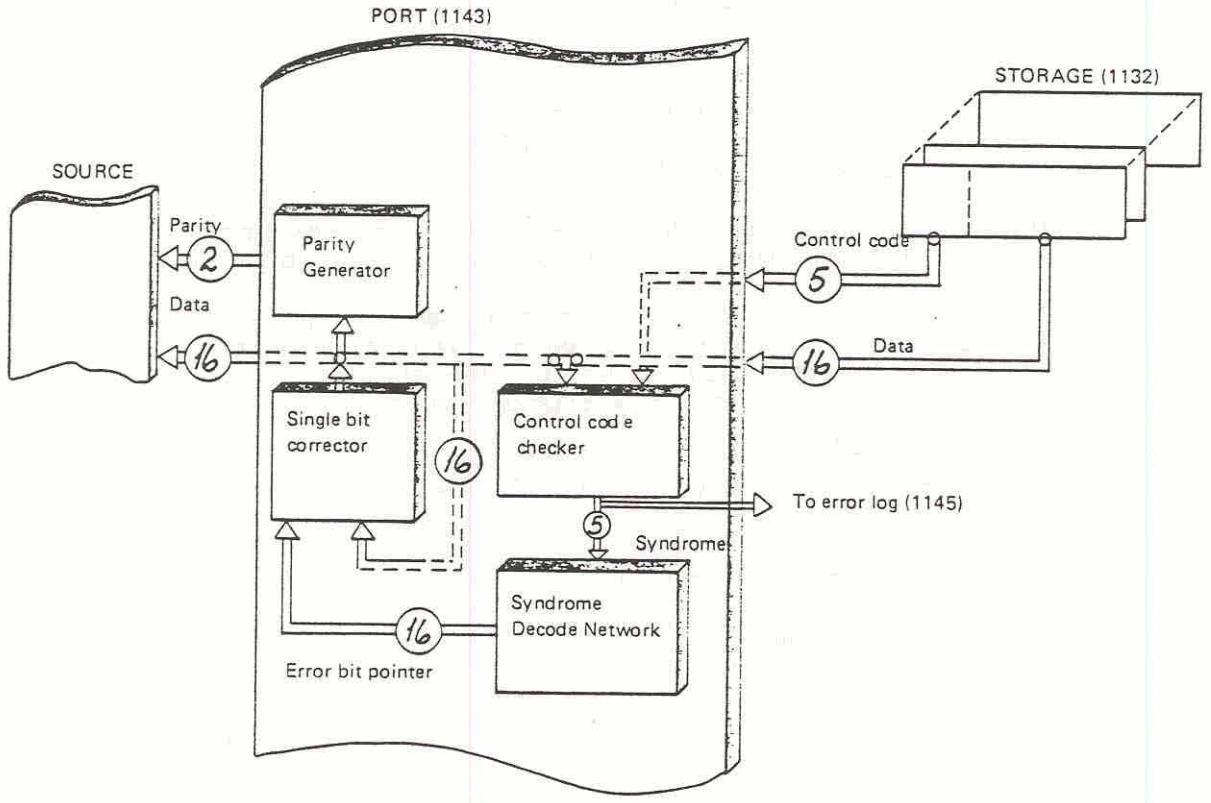
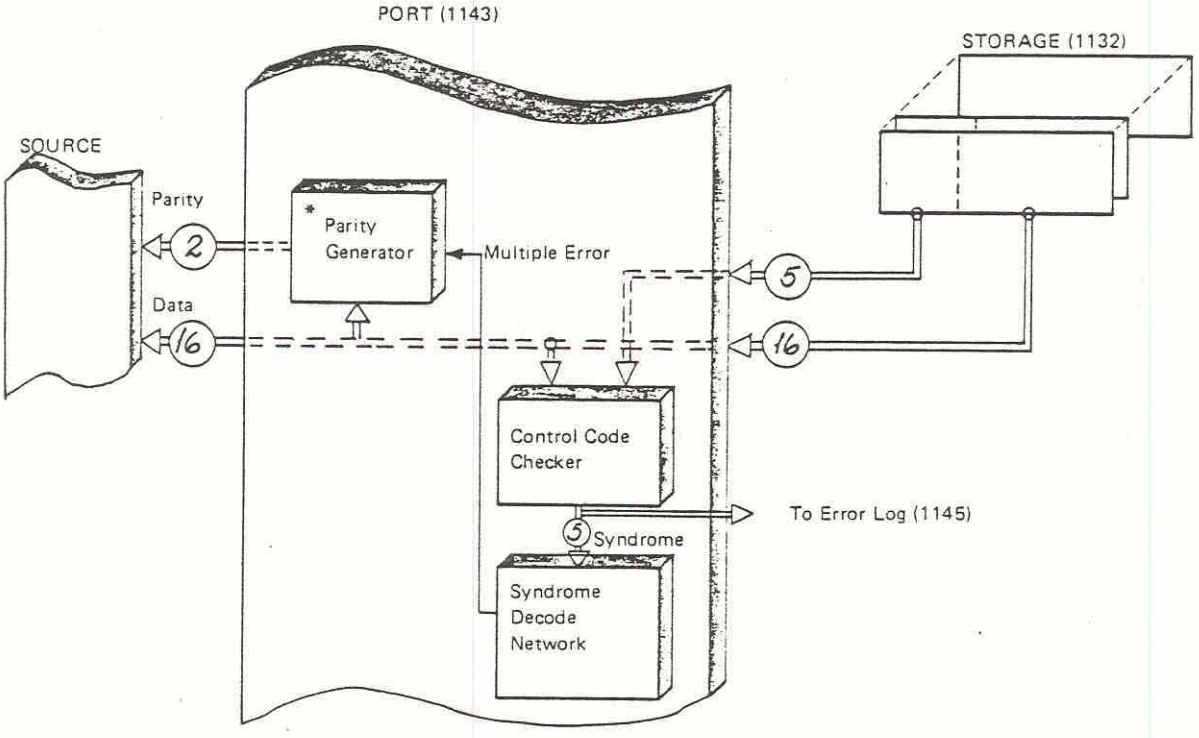


Figure 1.18: Reading Data (Single Error)



* when multiple error is detected parity bit for lower byte is forced false (BDL 16)

Figure 1.19: Reading Data (Multiple Error)

1.5.3 *Control and Error Reporting*

We have already discussed that single bit errors are detected and corrected internally in the BMPM. If multiple errors occur, the data cannot be corrected, and parity bit for lower byte is forced false.

If NORD-10/S is the source, an internal interrupt is generated which forces the CPU to level 14. It is, however, of interest to be aware of a single bit error also.

Over the service channel and the I/O system a failure in BMPM may generate interrupt to level 13 at the time of occurrance. By selecting the proper bit mask for the error correction control register (ECC), we can decide whether interrupt is disabled, single bit errors or multiple errors should generate interrupt.

At the time of the failure (interrupt) the syndrom is sent to the error og (1145). By reading the error log memory the system will know what type and where the error occurred.

See detailed description in Chapter 3.

Refer also to Figure 1.20 for further details.

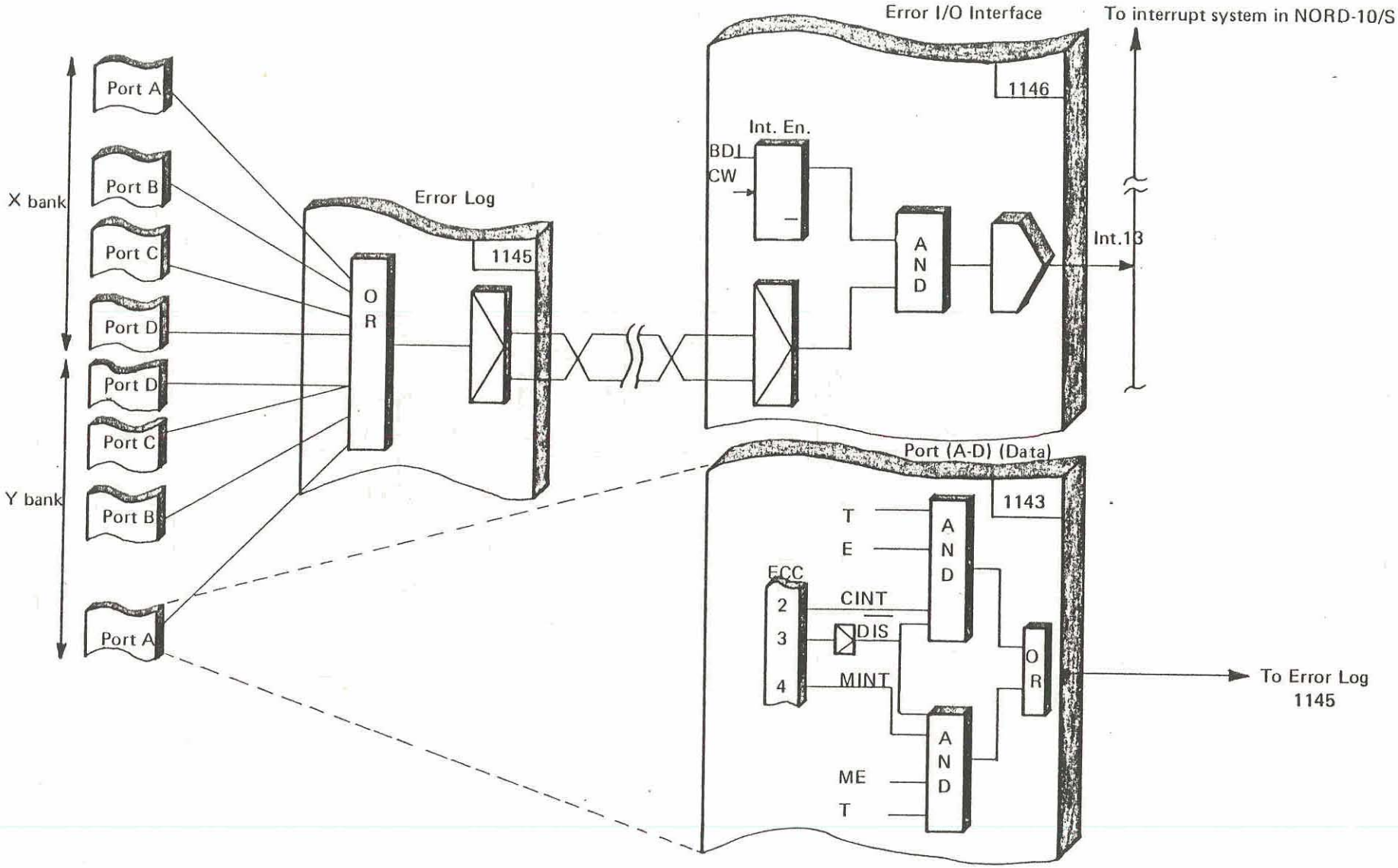


Figure 1.20: I/O Interrupt System in NORD-10/S

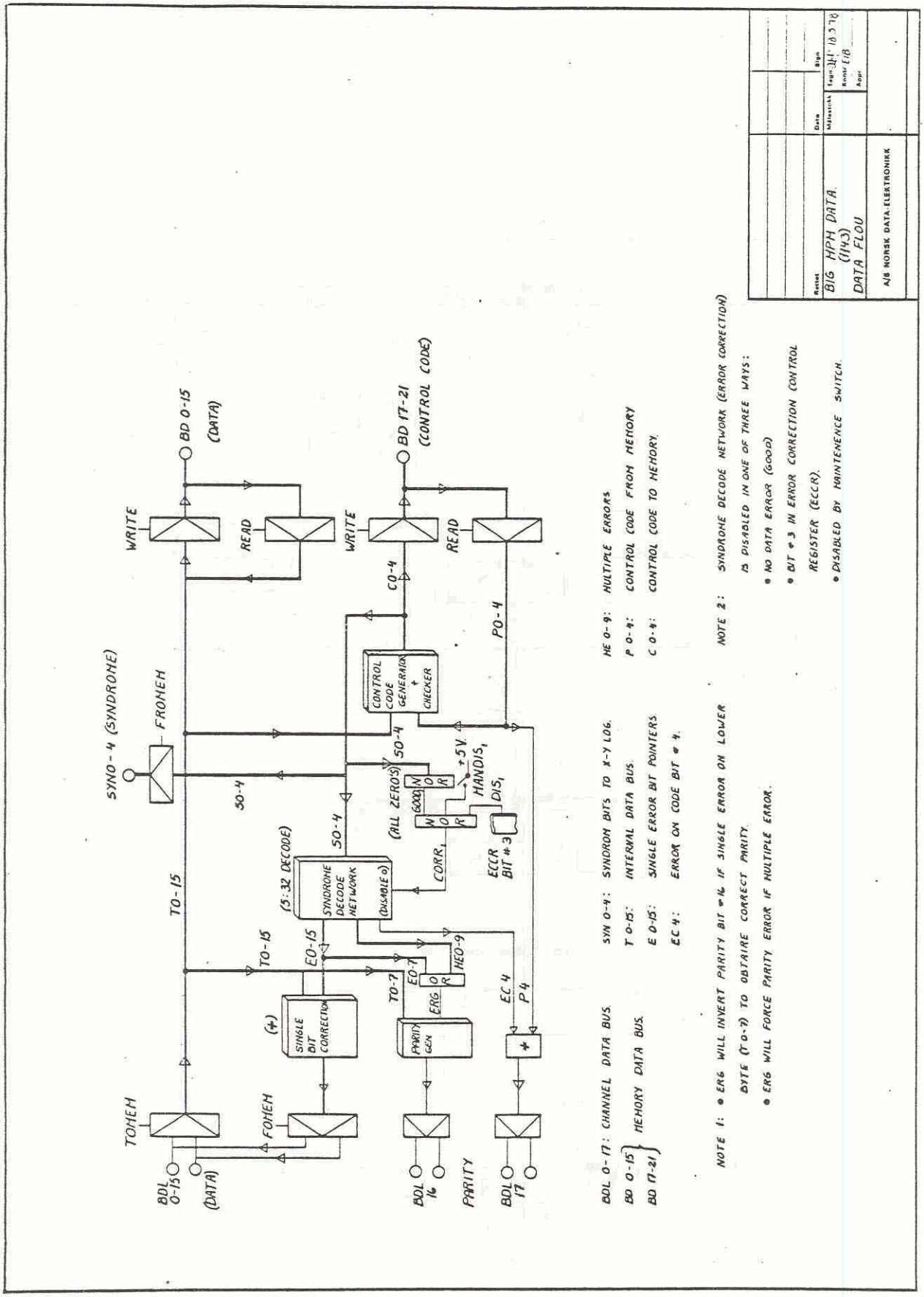


Figure 1.21: Big MPM Data (1143) — Data Flow

2 MEMORY CHANNEL SPECIFICATIONS

A 16 bits channel consists of one address cable, one data cable and two termination plugs. A 32 bit channel consists of one address cable, two data cables and three termination plugs. The specifications herein concern a 16 bit channel, unless otherwise noted. The channel source must fulfill the electrical and logical requirements stated below.

2.1 *HARDWARE SPECIFICATIONS*

2.1.1 *Signal Standard*

The channel signals are carried on differential lines conforming to CCITT-V.11 or RS-422 standard. See Figure 2.1 and Appendix E for further details.

Recommended line drivers and receivers are: AMD 26LS31 and AMD 26LS32 or equivalent.

2.1.2 *Cable*

Cables may be 120 ohm twisted pairs or flat cable. Maximum total length of a channel is 15 m. This limitation is due to requirement of signal quality at 10M baud.

2.1.3 *Connector*

Cables may be connected either direct to backwiring posts or via an optional plug panel. The backwiring connectors may be one of the following:

For twisted pairs;

BERG 65051-011, 2 x 26 position latch housing

BERG 47712, discrete female sockets

For flat cables;

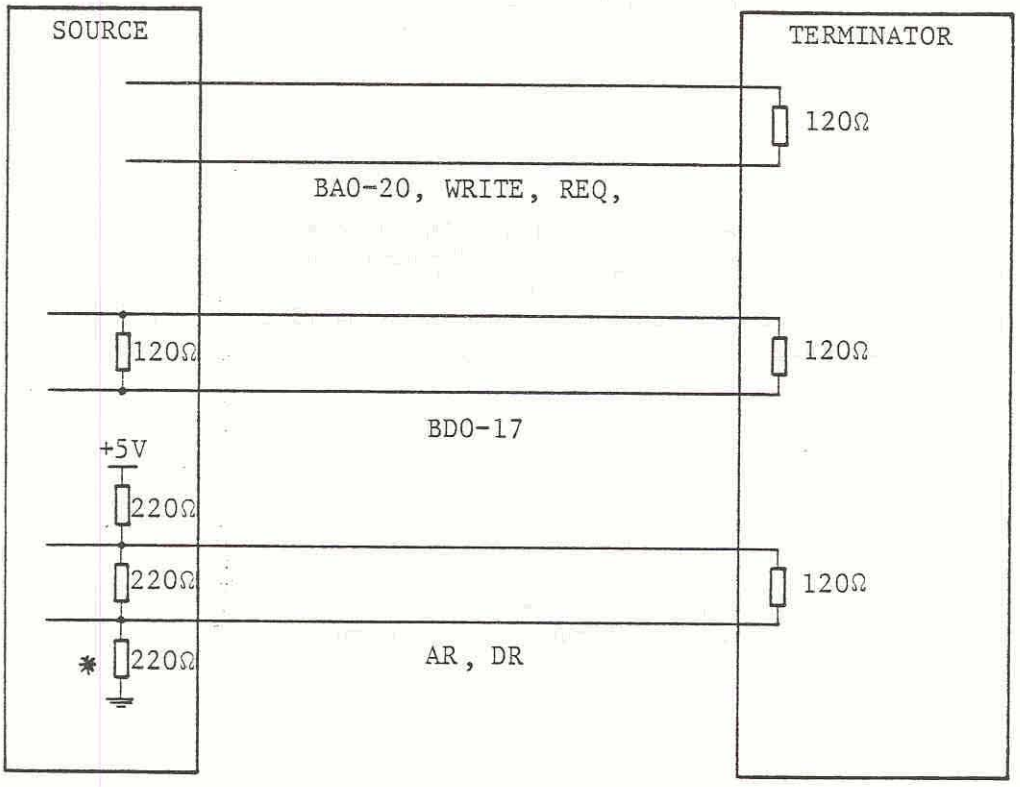
3M 3307, 2 x 25 position socket connector

3M 3404, keying header

2.1.4 *Termination*

All cables longer than 1 meter or between two cabinets shall be terminated at the end of the daisy chain (far end from source). Each differential pair shall be linked with a 120 Ω resistor mounted on a suitable connector (see Appendix C.6).

On the source module of the data cable further termination has to be performed. The termination scheme is summarized in Figure 2.1.



* Provisional. May be subject to change.

Figure 2.1: Termination of Memory Channel Signals

2.2 *SIGNAL DESCRIPTION*

Complete signal lists are found in Appendix C.2 and C.3. Below is a description of signals as seen from the source.

For the following discussion refer also to Figure 1.4.

2.2.1 *Address Cable Signals*

BA 0-17:	18 output address signals for normal NORD-10 address range
BA 18-20:	3 output address signals for extended address range
REQ:	output pulse to request access
WRITE:	output signal indicating data direction. WRITE = true means write to memory. WRITE = false means read from memory.

2.2.2 *Data Cable Signals*

BD 0-15:	16 bi-directional data signals
BD 16-17:	2 bi-directional signals indicating odd parity of lower and upper byte respectively
AR:	Input signal, address ready. Indicates that the request is accepted by a bank and that another request may be issued.
DR:	Input signal, data ready. Indicates that write data is accepted by bank or that data read from memory is valid on data lines.

2.3 *CHANNEL TIMING*

Timing diagrams and requirements are shown in Figures 2.2, 2.3A and 2.3B.

2.3.1 *Access and Cycle Times*

Access time at the port, measured as time between REQ and DR, assuming no latency.

Write: 200 ns maximum

Read: 450 ns maximum if data is good
500 ns maximum if data is corrected

Description:	Name:	Min.:	Type:	Max.:	Unit:
Address set-up time	t_{AS}	0			
Write data set-up time	t_{DS}	−75			ns
Write command before write data enabled	t_{WS}	70			ns 1)
Write data hold time	t_{DH}	0			
Write command hold time	t_{WH}	0			
Address hold time	t_{AH}	0			
Address ready pulse width	T_{ARP}	60	90		ns
Request pulse width	t_{RP}	50		∞	ns
Data ready pulse width	T_{DRP}	70	100		ns
End of address ready to next request	t_{RAR}	0			
Access time from Request to Address Ready	T_{AACC}			200	ns 2)
Write data access time	T_{WACC}			200	ns 2)
Write cycle time	T_{WCYC}	380			ns
Read command set-up time	t_{RS}	−30			ns
Read data disabled after Read Command false	T_{RDIS}	25		70	ns 1)
Read data valid before Data Ready	T_{DVAL}	0			
Read data access time (no error)	T_{RACC}			450	ns 2)
Read data access time (1 bit corrected)	T_{RACC}			500	ns 2)
Read cycle cycle time	T_{RCYC}	380			ns

Figure 2.2: Memory Channel Timing Specifications Measured at Port Terminals

1) Write signal should be put true as soon as possible after each read access in order to disable data driver at port.

2) Access times in case there is no waiting time due to previous accesses in the bank. Minimum cycle-time will limit write access time.

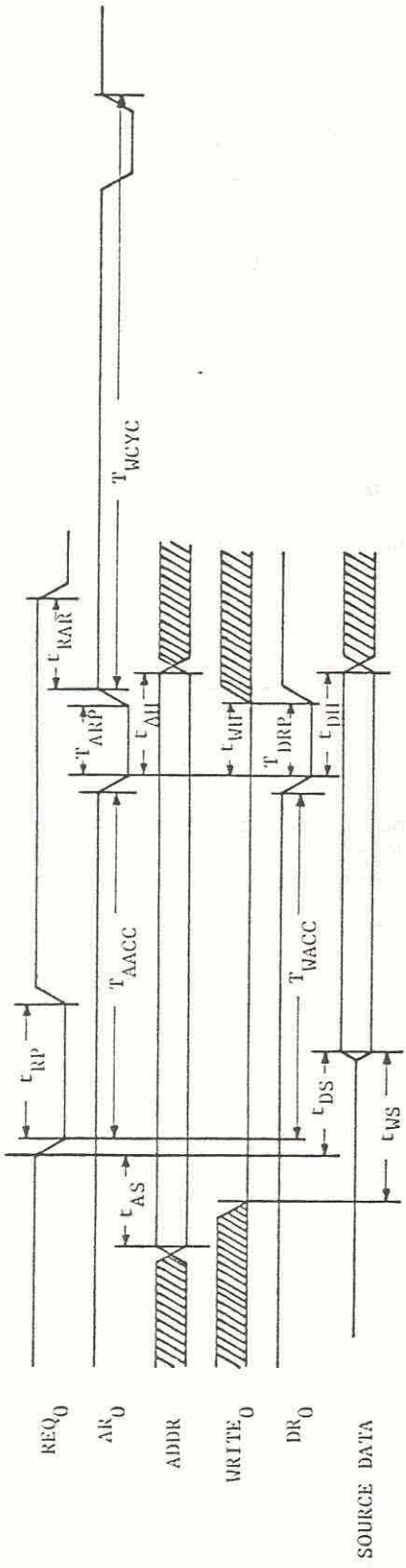


Figure 2.3A: Memory Channel Write Access Timing

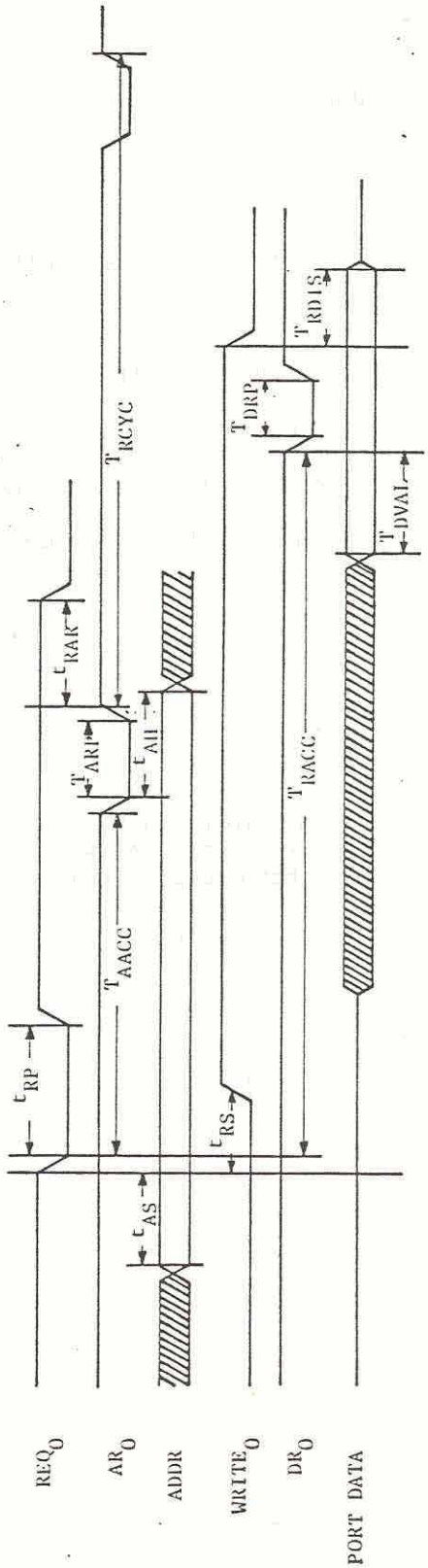


Figure 2.3B: Memory Channel Read Access Timing

Cycle time at the port, measured as time between two AR. Next REQ at trailing edge of AR.

Write: 380 ns maximum in same address. May decrease to 300 when accessing alternate modules.

Read: 380 ns maximum.

2.3.2 *Latency*

Due to different activities in the bank there may be a certain waiting time in addition to the regular access time. Maximum waiting will occur when two succeeding accesses attend the same memory integrated circuit.

1. Maximum waiting time when one higher priority port has access: 480 ns.
2. Maximum waiting time when two higher priority ports have access: ∞.
3. Maximum waiting time due to refresh: 520 ns.
4. Maximum waiting time due to previous access from same port: 180 ns.

The above numbers arise from worse case conditions which are seldom experienced.

2.3.3 *Timeout*

Missing answers AR and DR from a channel may be due to "memory out of range" or "memory inhibit" caused by power fail in a bank. It is therefore mandatory that the channel source has a timeout mechanism.

Minimum length is 10 μs.

2.4 *32 BITS CHANNEL*

A 32 bits channel is obtained by accessing two banks simultaneously from one source. The addresses and requests are the same in both banks as the address cable is common. Two data cables will each supply half of the 32 bits word (see Figure 2.4). As the source receives a double set of ready signals, which may be out of phase, there must be a provision to wait for the slowest response.

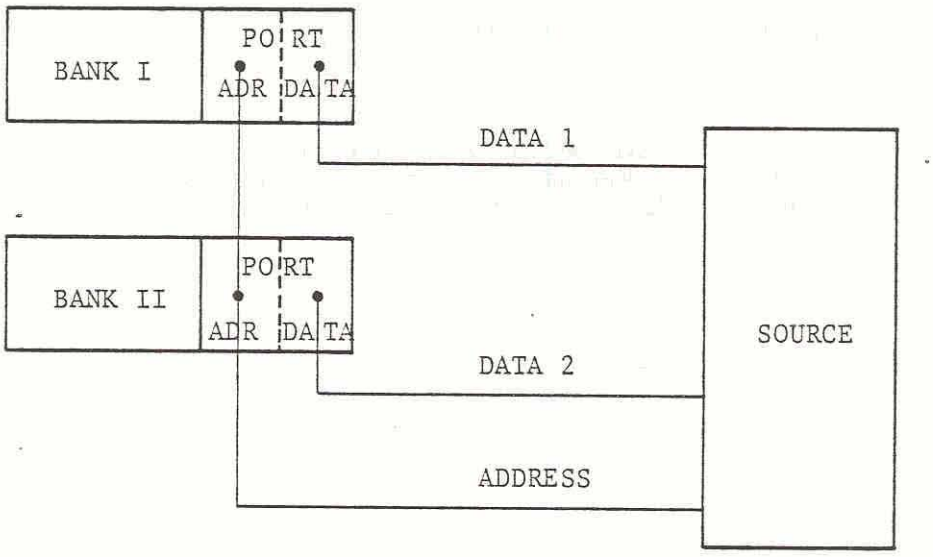


Figure 2.4: Two 16 Bit Banks Accessed as One 32 Bit Bank

2.5 *INDICATORS*

The data modules have two red indicators which normally shall be off. The upper warns that an error is detected. The lower warns that the error correction network is disabled either manually or by program.

The address modules have three yellow indicators of general information value. The upper indicates that the last request was accepted by the port. The middle indicates that the request was granted by the bank control. The lower indicates that a storage module has answered. These indicators light up until cleared by the next request on the channel.

2.6 *ADDRESS RANGE SWITCH*

The address range which a port shall respond to is determined by two sets of switches on the address module.

The upper set determines upper limit in 32K increments. The lower set determines lower limit in 32K increments. See Section 5.1 for further details.

2.7 *DISABLE ERROR CORRECTION SWITCH*

The data modules have a switch for manual disable of error correction. Operating the switch will also clear the error indicator. The switch is intended for maintenance purposes and failure will result if operated during an access.

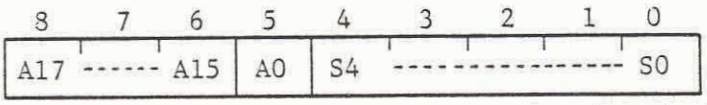
3 SERVICE CHANNEL SPECIFICATIONS

3.1 *GENERAL*

3.1.1 *Error Log (1145)*

Each port contains an error checking and correction circuitry which detects all *single bit* and alot of *multiple bit errors.* (Turn to the manual "NORD-10/S Functional Description" for further information.)

When an error is detected by a port, the 5 *syndrome* bits which identify the error are forwarded to the *error log* module. This module has a *512 x 1 bit log memory.* The 9 bits address to the log is composed of the following parts:



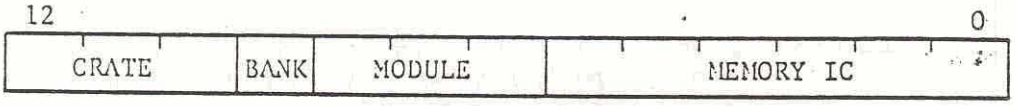
S 0-4:	Syndrome bits indicate failing data bit (or eventually multiple error)
A0:	Address bit that indicates even or odd block on failing module
A 15-17:	Address bits that identify the failing module

It is apparent that this 9 bit address is sufficient to point out the failing memory integrated circuit (MIC). In a 256K memory bank there are 336 MIC's hence every MIC has an *associated cell* in the log. Every time an MIC fails the corresponding cell is *set to 1.* The log will only indicate fail or not fail and not the number of fails.

Each time the log is read it is cleared and it is possible to obtain a good error statistic by reading the log many times.

3.1.2 *Error Log I/O Interface*

The error logs are not ordinary working memory and therefore they need a *dedicated interface* to read them. The interface is a normal I/O module obeying a number of IOX instructions. An IOX command *initiates scanning* of the error log in a bank, bit for bit. If 1 is hit on the address together with bank and crate number it is returned to the CPU. This information uniquely *identifies* all MIC's in a 16 bank system.



The log channel also serves other service purposes which described later. Refer also to Figure 3.1.

3.2 *PROGRAMMING SPECIFICATIONS*

3.2.1 *Device Number*

Fixed wired device numbers are 750 - 753.

3.2.2 *Interrupt Level = 13_{10}*

Interrupt is only caused by error conditions, i.e., status bit 1 and status bit 4 = 1.

3.2.3 *Ident Code = 5*

Fixed wire.

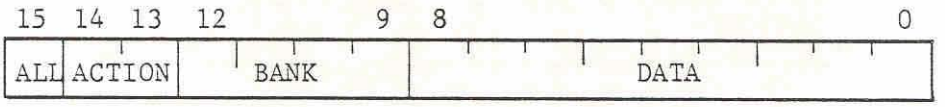
3.2.4 *Load Command Register = IOX 751*

The command is loaded but the result depends on status bit 2.

If status bit 2 = 0 (scan not active), clear status bit 3 (ready for transfer). Execute command.

If status bit 2 = 1 (scan active), abort scan. Such termination is possible, but should be done only when *absolutely* necessary.

The format is:



Bits 0-8: Data associated with actions 10 and 11. Unused in action 00 and 01 (see Section 3.3).

Bits 9-12: Bank address where bits 10-12 are crate numbers (see Section 3.4.5). bit 9 = 0 means X-bank and bit 9 = 1 means Y-bank.

Bits 13-14: Action caused in selected bank.

14	13	
0	0	Initiate scan of error log
0	1	Initiate scan of port status
1	0	Load error correction control register
1	1	Execute a test access

The actions are further described in Section 3.3.

Bit 15: Address all banks.

If bit 15 and bit 14 = 1 perform action in ALL banks regardless of bits 9-12.

Otherwise use bits 9-12 as bank address. (The purpose is to allow setting of all error correction control registers in one instruction.)

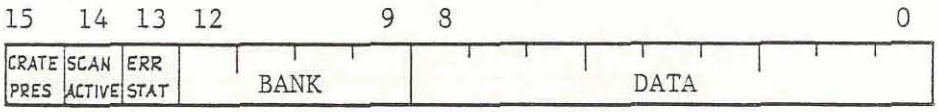
3.2.5 *Read Scan Register = IOX 750*

Reading of this register is only meaningful after initiation of a scan (action 00 or 01 of command register).

If status bit 2 = 1 (scan active): Clear status bit 3 (ready for transfer). Read register.

If status bit 2 = 0 (scan not active): Read register with data bits 0-8 = 0.

The format is:



Bits 0-8: Data resulting from actions 00 and 01 (see Section 3.3).

Bits 9-12: Bank address where bits 10-12 are crate numbers bit 9 = 0 means X-bank and bit 9 = 1 means Y-bank. (These bits are the same as loaded by the last command.)

Bit 13: Error status.

During a scan of port status (action 01) the bit indicates whether there has been an error at the port. Used for further identification of error interrupts (see Section 3.3). Bit 13 = 1 during scan of error log (action 00).

Bit 14: Scan active.

If bit = 1 the addressed bank is busy scanning its error log or port status. The bit is identical to status bit 2.

Set: Initiate scan by action 00 or 01 of command register.
Clear: At end of scan. Change of command register (incorrect!).

Bit 15: Crate present.

Use to separate missing crates from present crates with empty error log.

Set: The crate addressed by last scan command is present.
Clear: The crate addressed by last scan command did not answer.

3.2.6 *Read Status Register = IOX 752*

Since the interface is always ready for transfer in less than 100 *vs* neither of the data instructions (IOX 750-751) can cause interrupt. The only sources of interrupt are memory errors detected by the ECC system at each port.

The meaning of the status bits are:

Bit 1: Error interrupt enabled.

Set: Control word bit 1 = 1.
Clear: Control word bit 1 = 0. Control word bit 4 = 1. Serviced IDENT PL 13. Master Clear.

Bit 2: Scan active.

If bit = 1 the addressed bank is busy scanning. The bit will be 1 during the whole scan period even when valid data is transferred to the interface. Hence it is *not* inverse of status bit. 3.

Set: Initiate scan by action 00 or 01 of command register.
Clear: At end of scan. Change of command register.

Bit 3: Ready for transfer, RFT. RFT does not cause interrupt.

Set: Status bit 2 = 0. (Always ready when scan is passive. Status bit 2 = 1 and valid data present in interface. Control word bit 4 = 1 (device clear). Master Clear.

Clear: Status bit 2 = 1 and valid data not found yet (but investigation is in progress).

Bit 4: Memory error.

An OR function of the error signals from all ports of all banks. The individual contributions are enabled by *error correction control register.*

Set: Single or multiple memory error detected and enabled for interrupt at the port. Control word bit 3 = 1 (set to test mode).
Clear: Scanning of port status of the failing bank. Test mode is cleared by:
Device Clear
Services IDENT PL13
Master Clear.

3.2.7 *Load Control Register = IOX 753*

Bit 1: Enable interrupt on memory error

Bit 4: Device clear.

Set RFT = 1, Terminate scan, Clear Test mode.

Device clear has no influence on memory error signals which must be cleared by scanning of port status.

3.3 *DETAILED DESCRIPTION OF COMMANDS*

Besides handling error interrupt, the interface provides execution of four command actions.

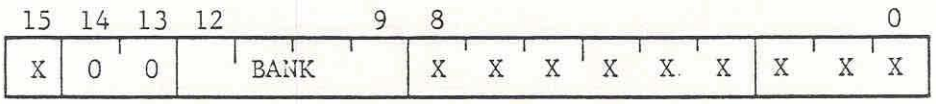
The actions are either *direct* or *scan.* When a scan is initiated by a command it must be allowed to terminate before another command is started.

To find out when the scan register content is valid, status bit 3 must be read repeatedly. (Make a loop with error exit after 100 *vs* without finding status bit 3 = 1.)

3.3.1 *Action 00: Initiate Scan of Error Log*

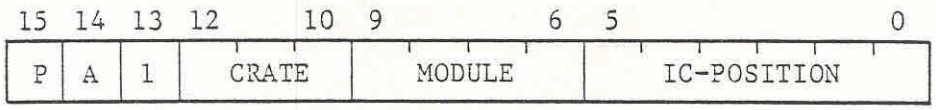
See also Figures 3.3 and 3.4.

Load the command register with the following content:



The interface will be set to scan mode (status bit 2 = 1. The addressed log module now searches through its error log and looks for error bits set. When status bit 3 changes to 1 the location of the error is transferred to the scan register. Eventually end of scan is reached without any errors detected.

The format of the error information is:



The information is here divided in a slighly different manner compared to what is stated in Section 3.1.1.

IC POSITION: 6 bits code showing the failing memory IC. Conversion between code and physical position is stated in Appendix B.1.

MODULE: 4 bits code showing the slot of the failing memory module. Conversion between code and physical slot is stated in Appendix B.2..

CRATE: 3 bits code identifying the crate number displayed on log module in slog 18 or 19.

A Scan active.

A = 1: More data will come
A = 0: End of scan. A new command is required to start another scan. Value of MODULE and IC POSITION is insignificant. (Bits 0-8 = 0).

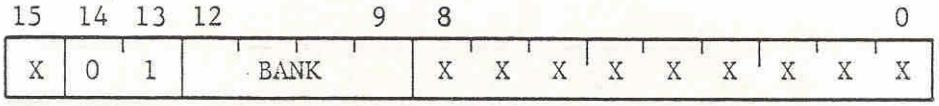
P Crate present.

P = 0: Addressed crate does not answer. Scan aborted.
P = 1: Crate hale and hearty.

3.3.2 *Action 01: Intiate Scan of Port Status*

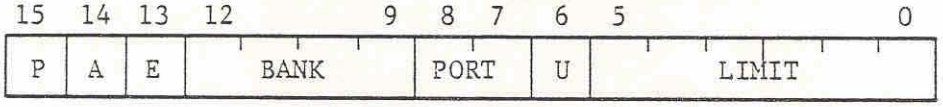
See also Figures 3.6 and 3.7.

Load the comand register with the following content:



The above will put the interface in scan mode. The addressed bank will look over its ports and report which are there and what their address ranges are.

The format of the port status is:



LIMIT: Value of the range limit on thumb wheel switches of port address module.

U: Upper limit if U = 1.
Lower limit if U = 0.

PORT: 2 bits code indicting port. 0 - 3 means A-D respectively. Appendix B.3 shows in which slots the respective range switches are found.

BANK: 4 bits code constituted by one bit (9) indicating X or Y and 3 bits (10-12) identifying crate number displayed on log module in slot 18 or 19.

E: Bit telling whether an error signal has been issued from the current port.

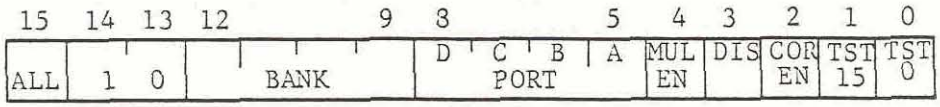
A, P: The meaning of these bits are the same as stated in Section 3.3.1: Action 00.

Timing diagram for SCAN operation (ERROR LOG and PORT STATUS) is given in Figure 3.9 and 3.10.

3.3.3 *Action 10: Load Error Correction Control Register, ECC*

Each port has an error correction control register. It is similar (not equal!) to the corresponding CPU register for local memory access.

The format of the command is:



TST0: Invert polarity of correction code bits 0 and 1, which correspond to error in data bit 0 (see below).

TST15: Invert polarity of correction code bits 2, 3 and 4, which correspond to error in data bit 15 (see below).

COREN: Enable error interrupt on single bit errors.

DIS: Disable error correction and clear error indicator on data card (same function as the disable switch).

MULEN: Enable error interrupt on multiple errors.

PORT ABCD: 4 bits port address where each port has a corresponding bit. This allows access to all ports simultaneously.

BANK: Bank address as described in Section 3.3.2.

ALL: Address all banks regardless of the bank bits 9 - 12 if ALL = 1. ALL affects only the bank address not the port addresses (which may be accessed simultaneously).

Example:
To enable interrupt on multiple errors in the complete system simultaneously, the following command word is suitable:

1 4 0 7 6 0

Note! At power-up and after a power-fail the ECC registers are set to 0.

3.3.3.1 Test Error Correction

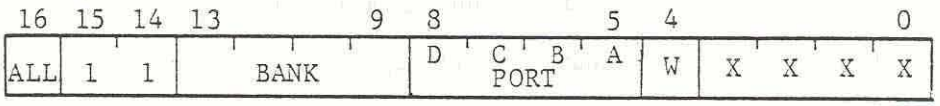
Error in data bit 0 is reported by means of the code 00011_2. A forced inversion of bits 0 and 1 in the correction bits of otherwise correct data will exhibit error in data bit 0. At the same time a forced inversion of correction bits 2, 3 and 4 produce error code 11100 which accuses data bit 15 of being faulty.

But, what will happen if both the correction bits are inverted when written into and read from memory? Since two inversions are equivalent to no inversion, data will appear faultless. Thus, only the writing or the reading port should be in test mode in order to simulate errors.

3.3.4 *Action 11: Execute Test Accesses*

It is possible upon command to produce test requests at a port without attaching a channel.

The format of the command word is:



PORT, BANK and ALL work in the same manner as described in the previous Section, 3.3.3.

If W = 1 a write access results and if W = 0 a read access results.

3.3.4.1 Address and Data of Test Accesses

How much information that can be drawn from a test access depends on whether the cable is connected or not.

When neither an address nor a data cable are connected the port will experience address = 777777 and write data = 0. The range switches must therefore be:

Lower limit: ⩾7
Upper limit: ⩽ 10

In order to forward the request to the bank. By means of the test mode (independantly set for each channel) it is possible to put an "error label" on selected data words. The labelled data word can be traced from and to specific ports. Furthermore, it is possible to follow the produced error to the log and to the I/O and interrupt system.

Even if the channel is connected to a physical source which sends out an unpredictable data and address, some information may still be extracted.

First, initialize the bank with the correct correction codes via an appropriate port. Then set test bit 0 or 15 on the port under test and perform the test access. It is immaterial what address and data is used. If this access produces error interrupt and correct the error code in the log very much of the port hardware works properly.

3.4 *HARDWARE SPECIFICATIONS*

The service channel is physically one cable linking all Error log modules to an I/O interface module. It has nothing in common with the ordinary memory channels. The main task is to read the log memories, but it serves also other purposes as described in Section 3.3.

3.4.1 *Electrical Standard*

The channel carries 20 uni- and bi-directional differential lines conforming to RS-422 standard.

Cables may be 120 Ω twisted pair of flat cables. For further details refer to Section 2.1.

3.4.1.1 Termination

All cables longer than 1 meter (or between cabinets) shall be terminated at the end of the daisy chain by a plug with 120 ohm resistor between each differential pair.

Bi-directional and input signals are also terminated on the interface module.

3.4.2 *Service Channel Signals*

A complete plug list is found in Appendix C.4. For the following discussion refer to Figures 3.1 and 3.2. The meaning of the signals are:

B0-8:	9 bi-directional data signals.
B9-14:	6 output command signals.
B15:	1 bi-directional control/ status signal
LIOX:	Output signal indicating that command and data are valid from interface at output command. Handshake signal for LDRY during input of scan data.
ACT:	Input signal. Answer from addressed module that it is present and is active with a scan.
LDRY:	Input signal. "Data Ready" signal sent from active module telling about valid scan data. It shakes hands with LIOX in scan mode.
LINT:	Input signal warning that an error is detected "somewhere". Causes interrupt if enabled.

3.4.3 *Channel Timing*

Timing diagrams and requirements are shown in Figure 3.1 to 3.12.

3.4.4 *Error Indicator*

Each LOG module has a red indicatgor lamp internally connected to the LINT signal. Indicates that an error has been detected in the crate. It is cleared by scanning of port status.

3.4.5 *Crate Number Switch*

The LOG module has a ten position thumb wheel switch defining a 3 bit crate number, 0-7. Position 8-9 puts the module off-line. The number is used for maintenance identification and is not required for normal memory accesses.

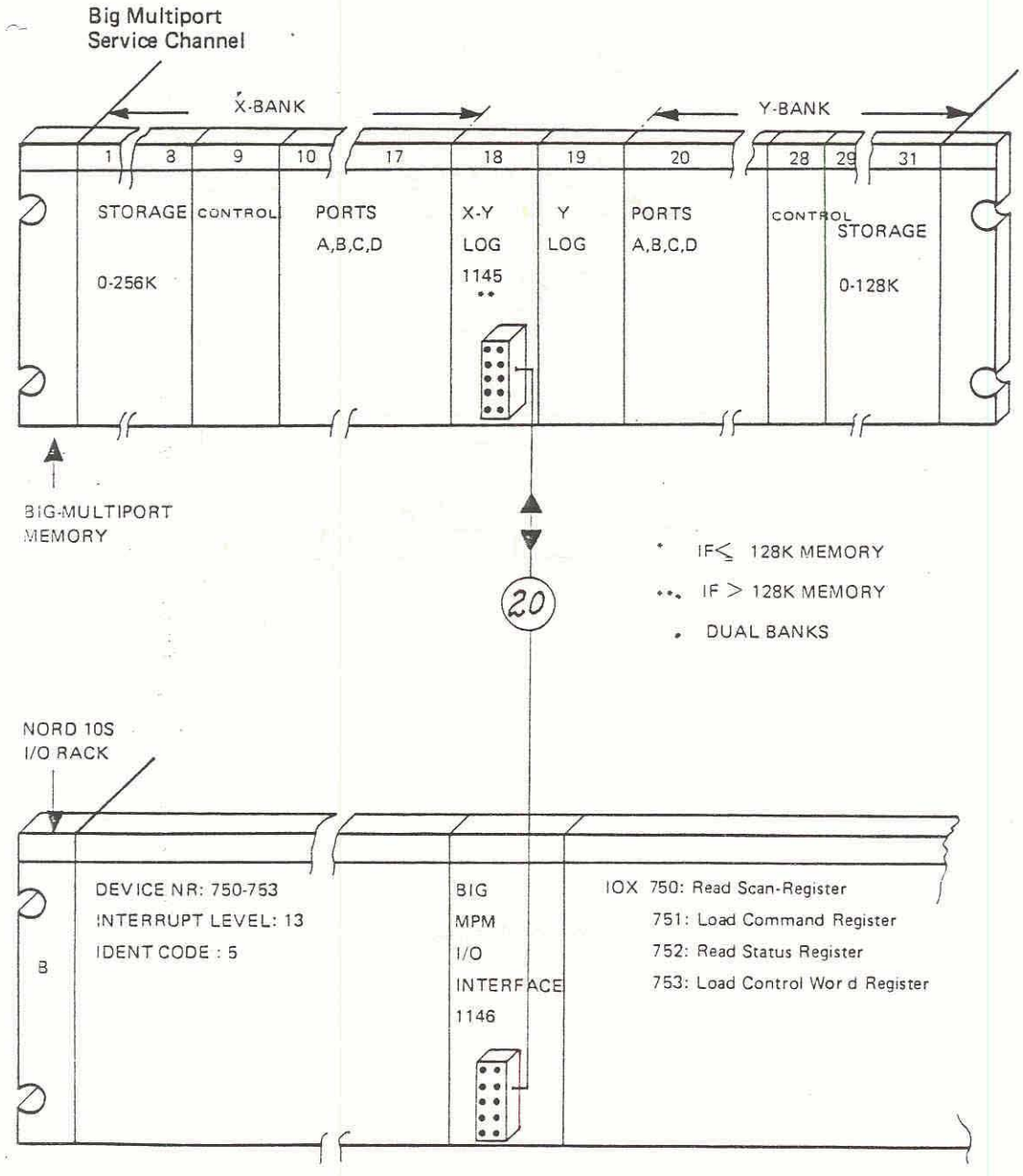


Figure 3.1: BMPM Service Channel

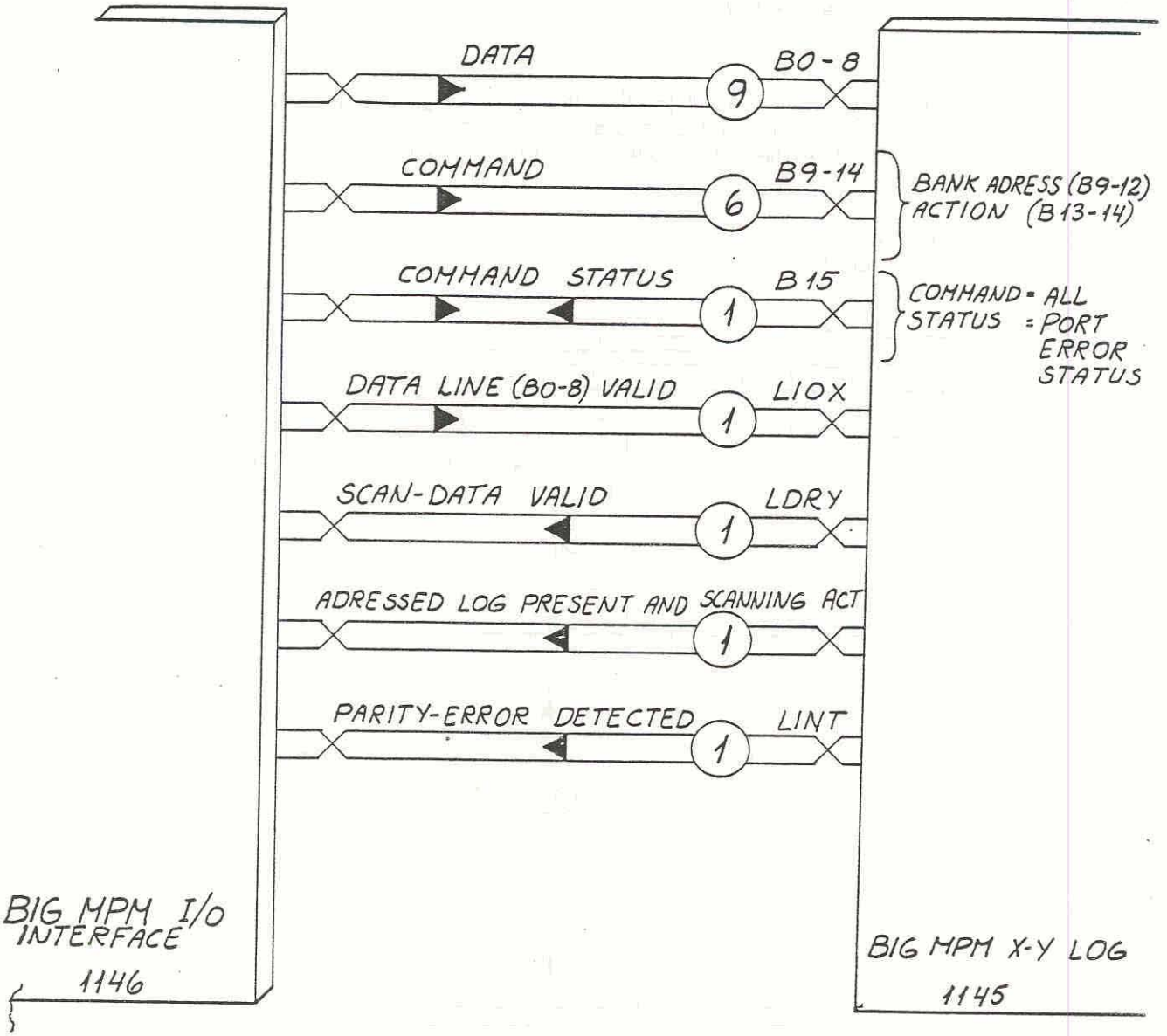


Figure 3.2: I/O Module to Error Log Module Communication

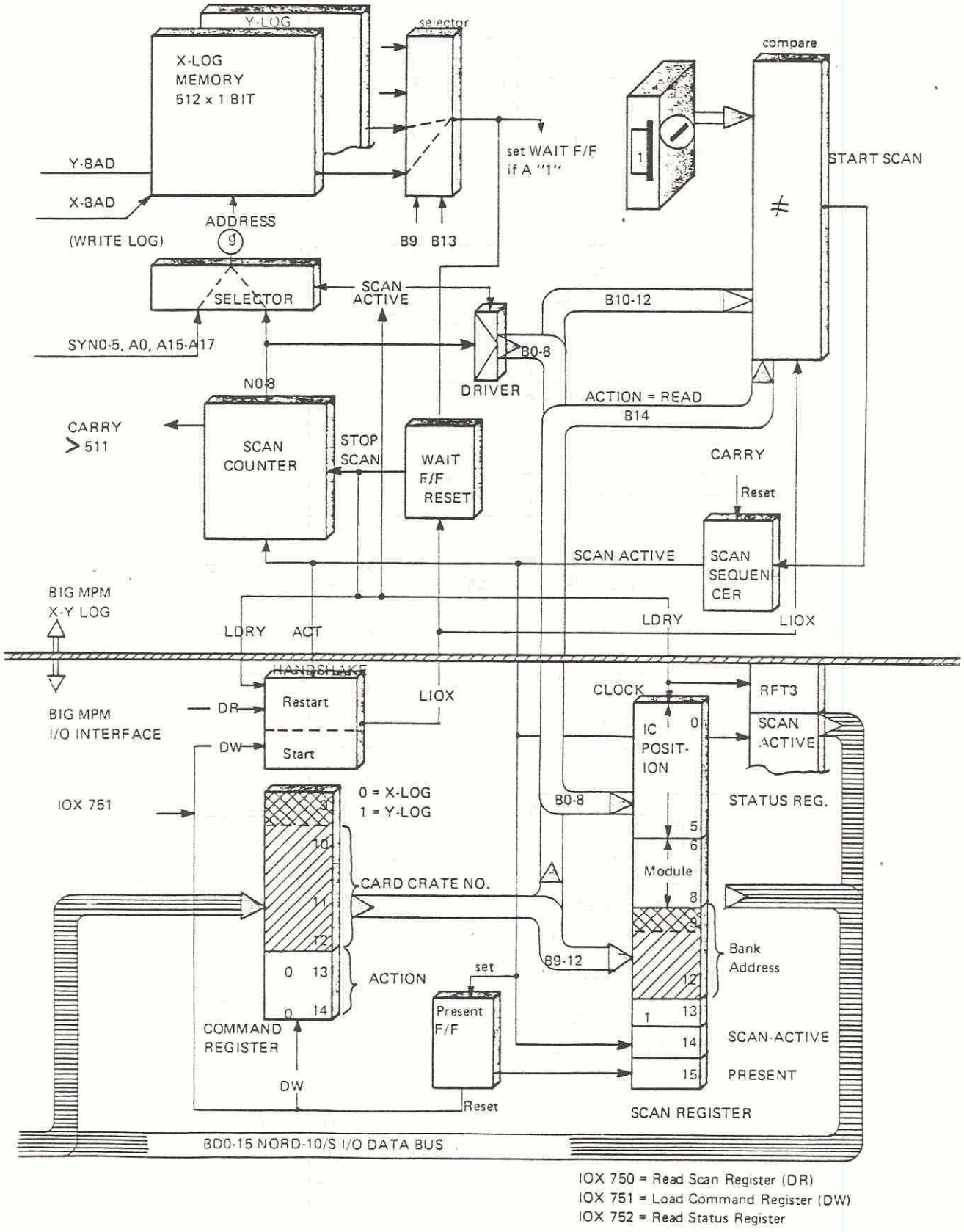


Figure 3.3: Scan of Error Log — Block Diagram

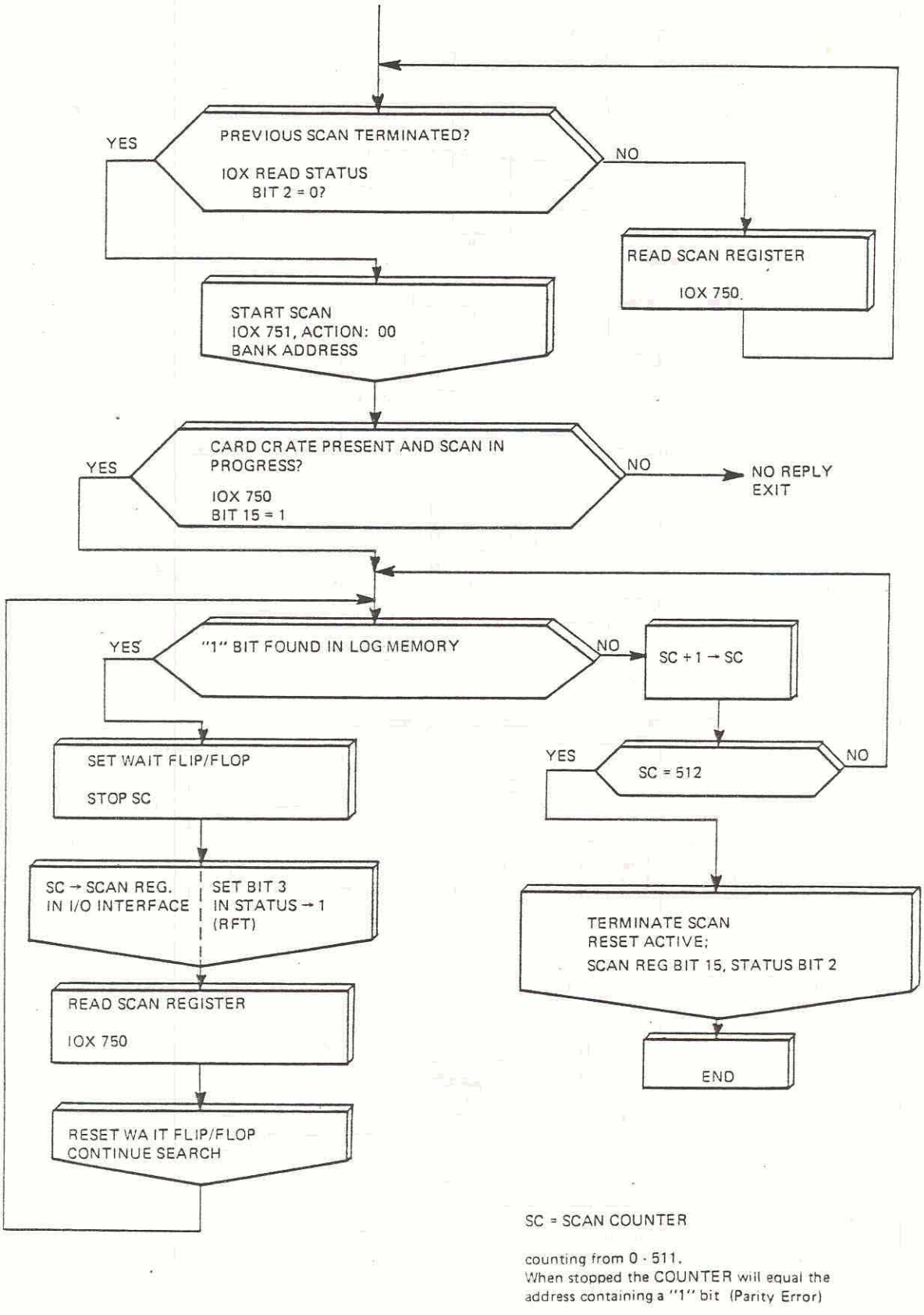


Figure 3.4: Action: 00 Scan of Error Log — Flow Diagram

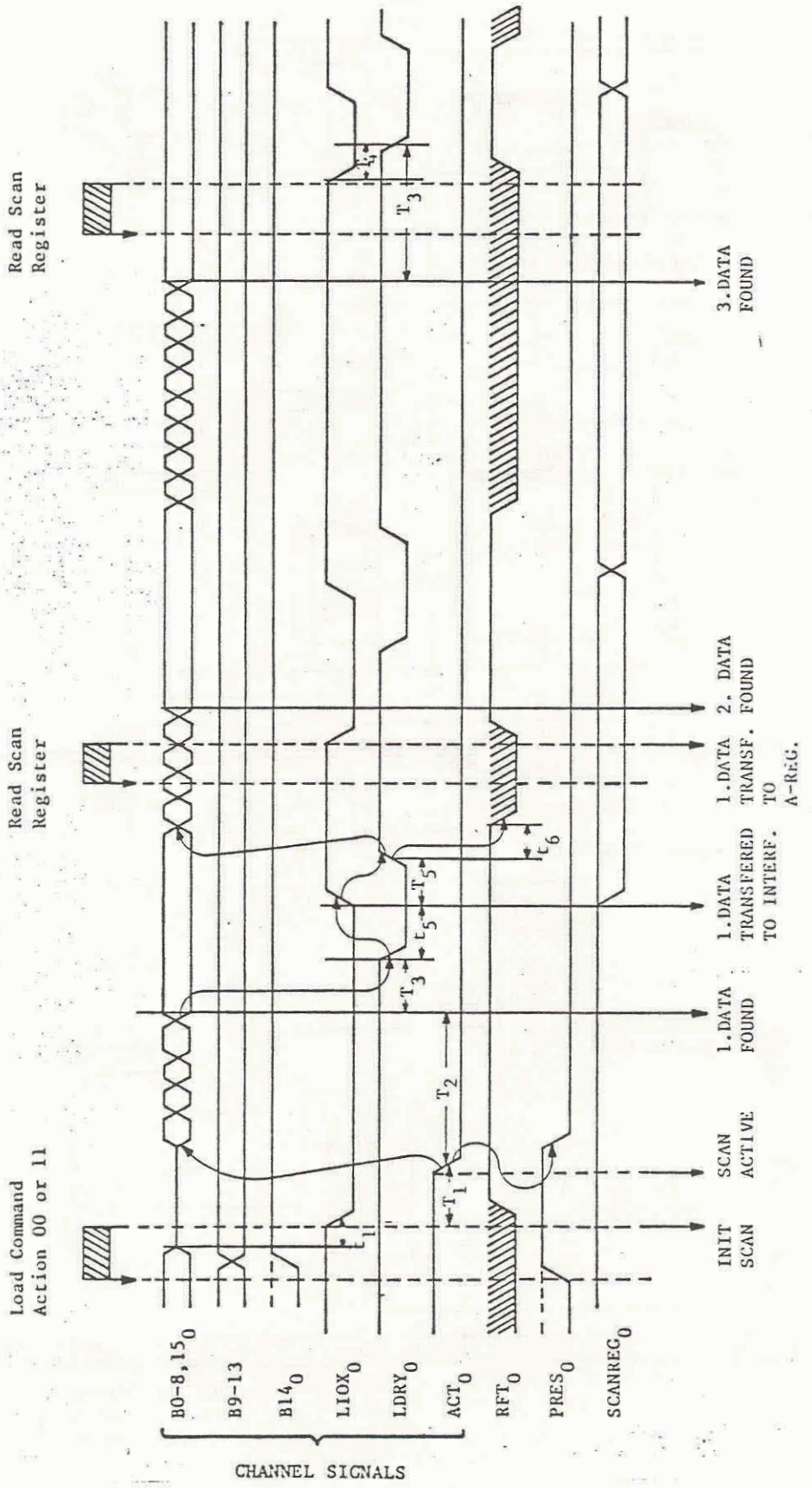
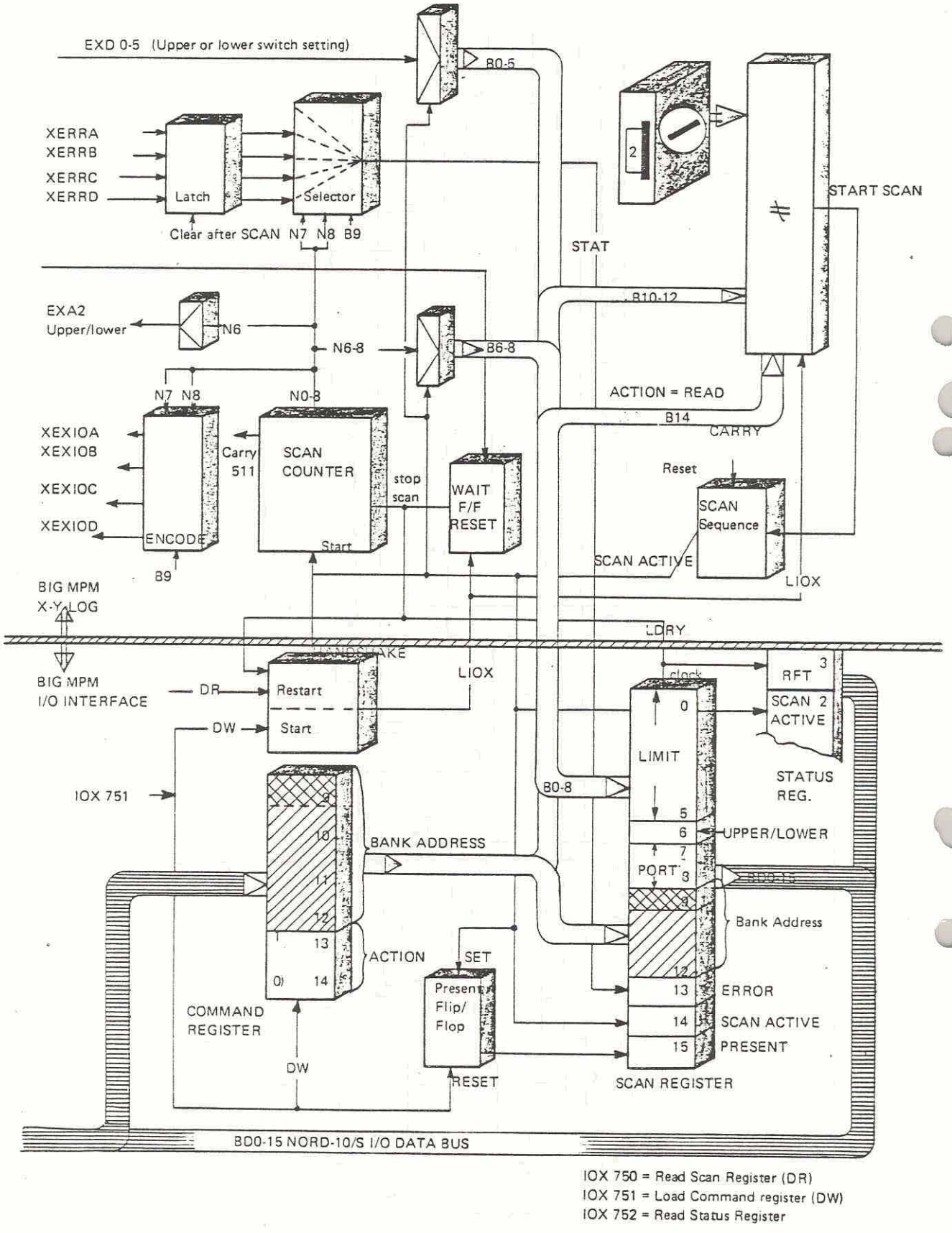


Figure 3.5: Beginning and Continuation of a Scan (termination is shown in Figure 3.10)



IOX 750 = Read Scan Register (DR)
IOX 751 = Load Command register (DW)
IOX 752 = Read Status Register

Figure 3.6: Scan of Port Status — Block Diagram

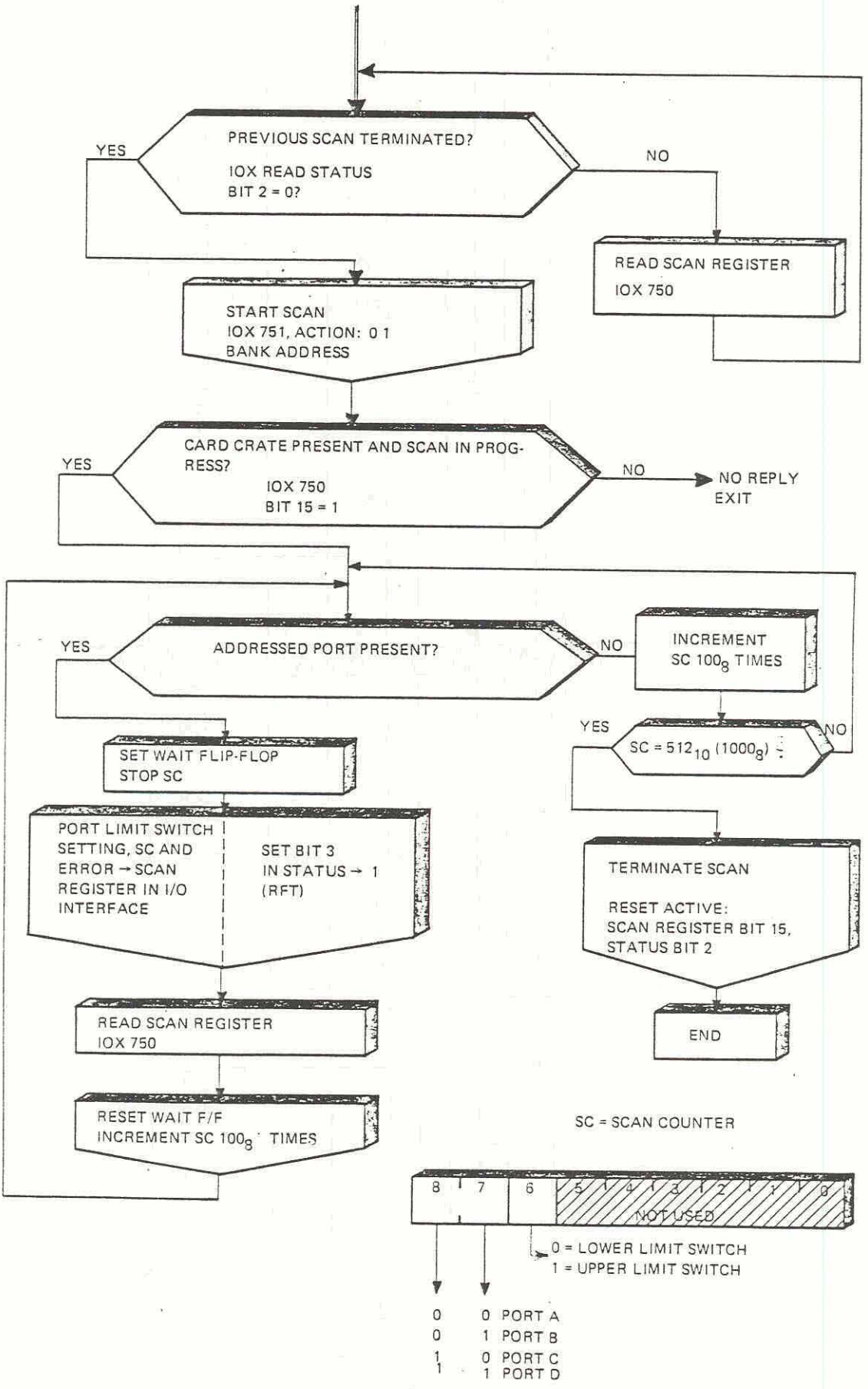


Figure 3.7: Action: 01 Scan of Port Status — Flow Diagram

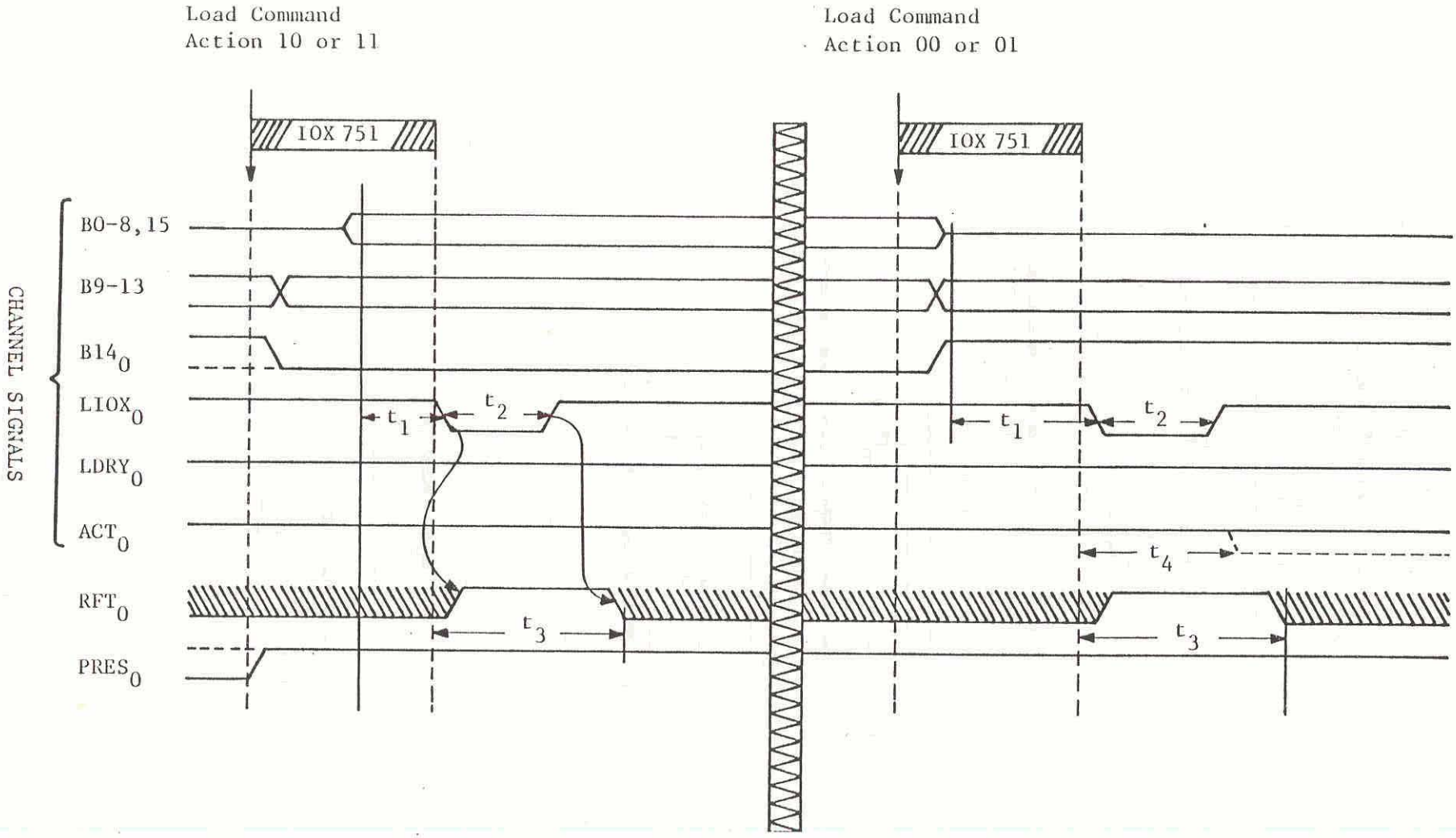


Figure 3.8: Execution of Actions 10 or 11. No answer expected from channel.

Figure 3.9: Execution of Actions 00 or 01. Addressed bank did not answer by assetting ACT with t_4 = 400 ns after LIOX.

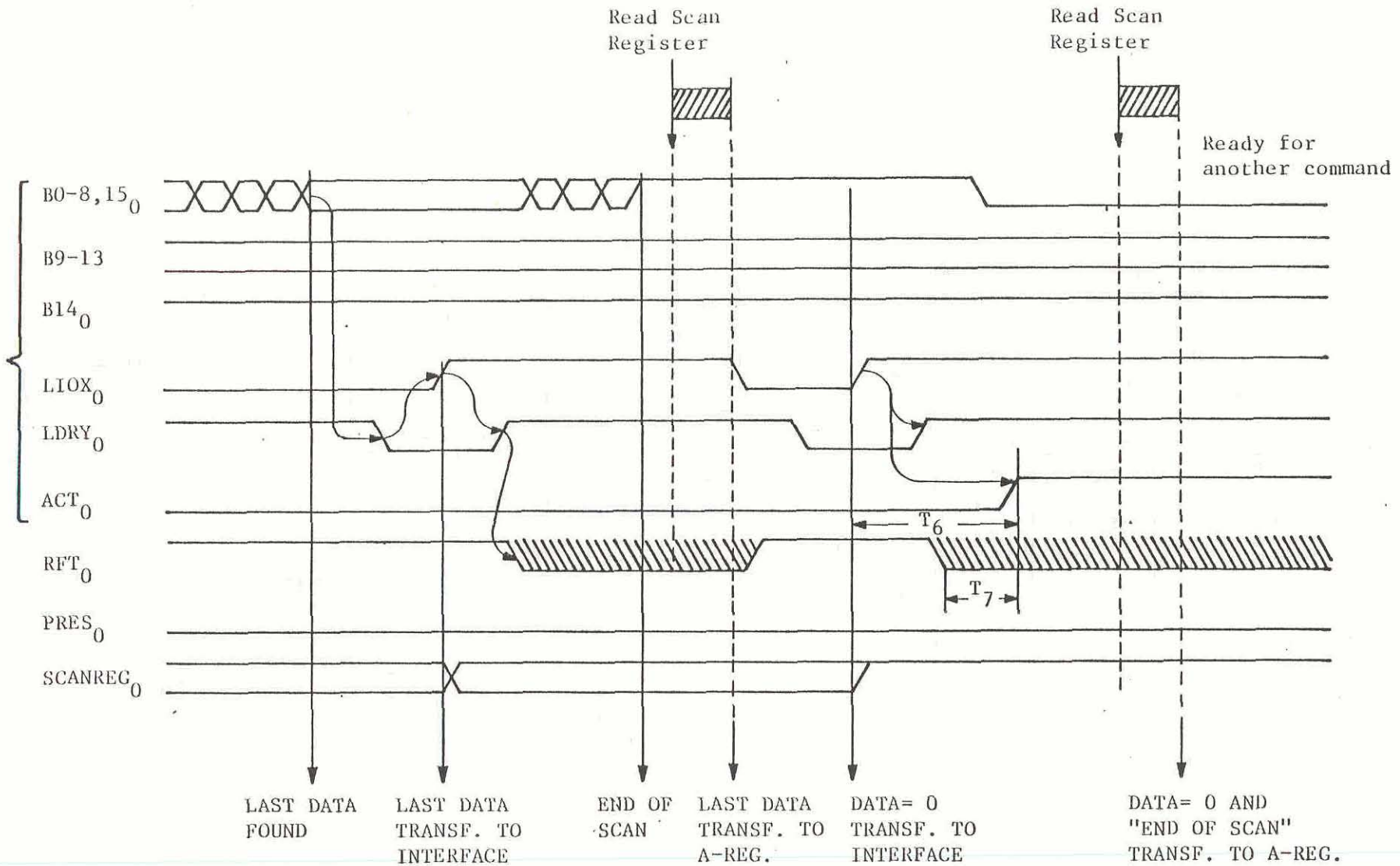


Figure 3.10: Termination of a Scan
(diagram continues from Figure 3.5)

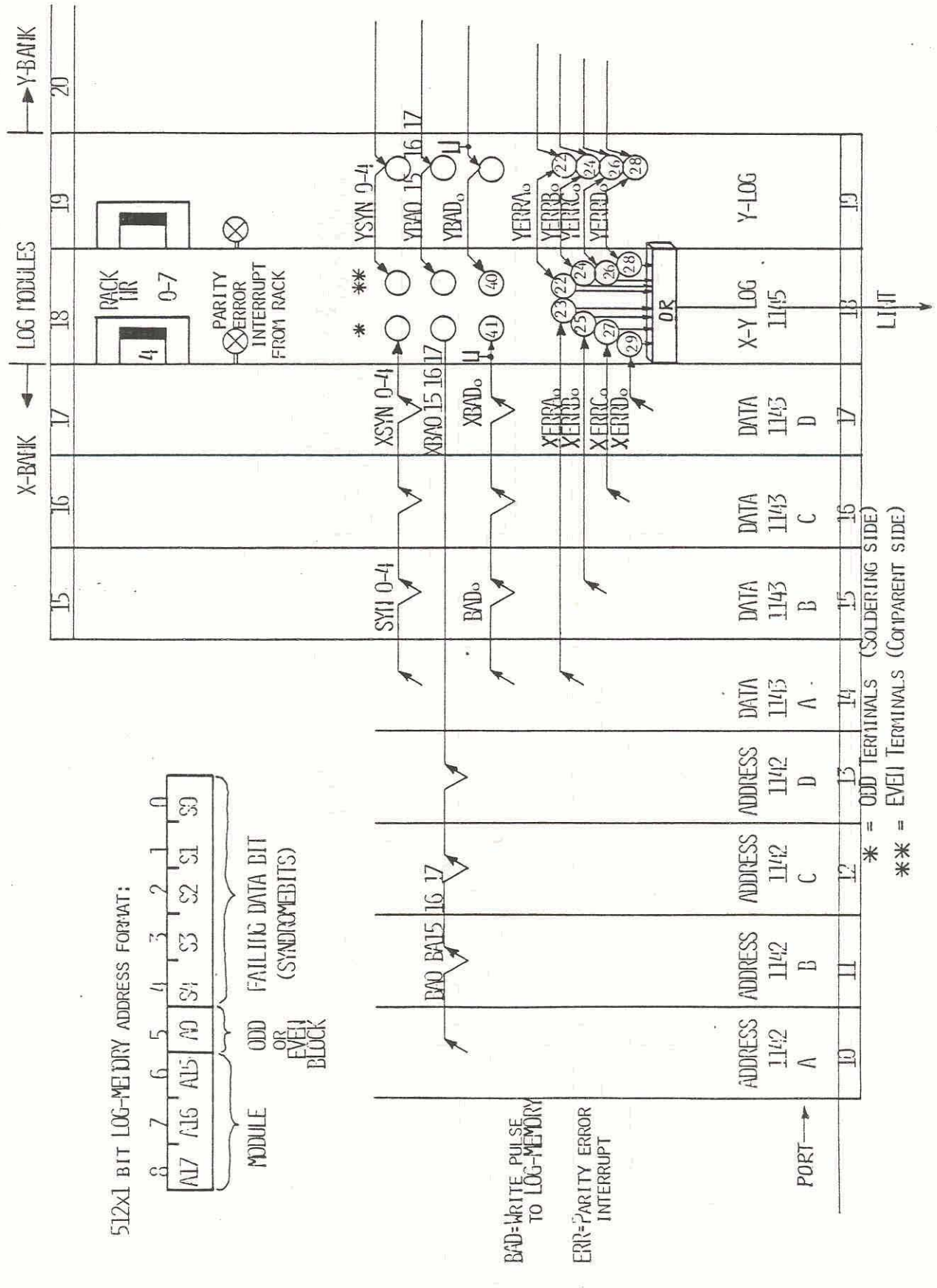


Figure 3.11: Error Log Module/Port Communication

ND-06.007.01

Description	Name	Min	Typ	Max	Unit
Data stable before LIOX	t_1	200		1000	ns
Length of LIOX (scan passive)	t_2	450		650	ns
Time from command to ready again (scan passive)	t_3			700	ns
Time from LIOX to ACT if interface shall detect "crate present"	t_4			400	ns
LIOX untrue after LDRY true	t_5		60	100	ns
LDRY untrue to RFT true	t_6		50	80	ns
Time from LIOX to ACT (exklusive cable delay)	T_1		170		ns
Time from ACT to first scandata or between two scandatas	T_2			85	µs
Scandata stable before LDRY	T_3	90	110		ns
LDRY true after LIOX true	T_4	60		∞	ns
LDRY untrue after LIOX untrue	T_5		70	110	ns
ACT untrue after last LIOX untrue	T_6		130	200	ns
ACT untrue after last RFT true	T_7		25	75	ns

Figure 3.12: Service Channel Timing Specifications according to Figure 3.1 - 3.4.

Times are measured at interface terminals. Times named by t are determined by interface, while times named by T are determined by log module.

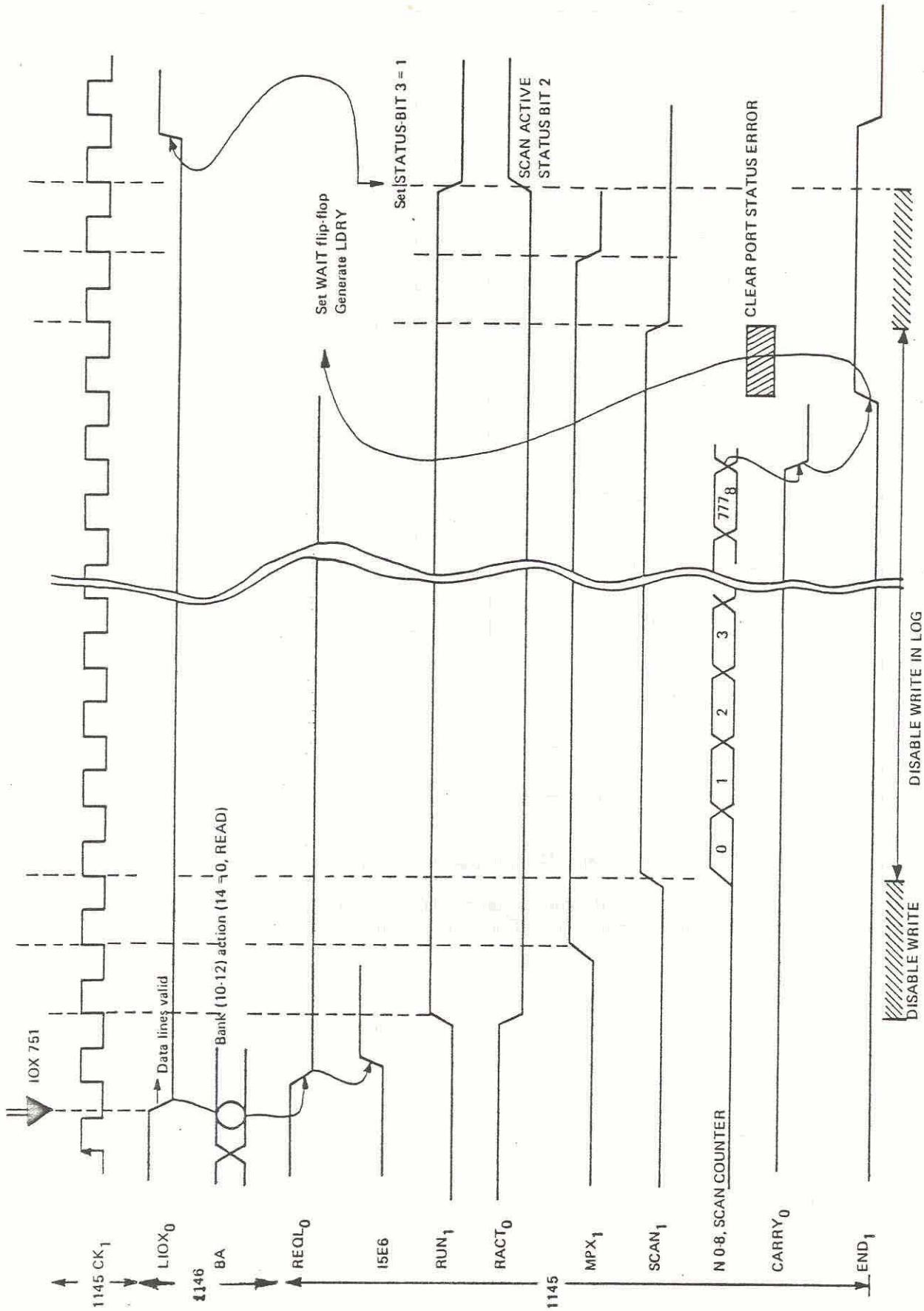


Figure 3.13: Start/Stop of Scan (no error found)

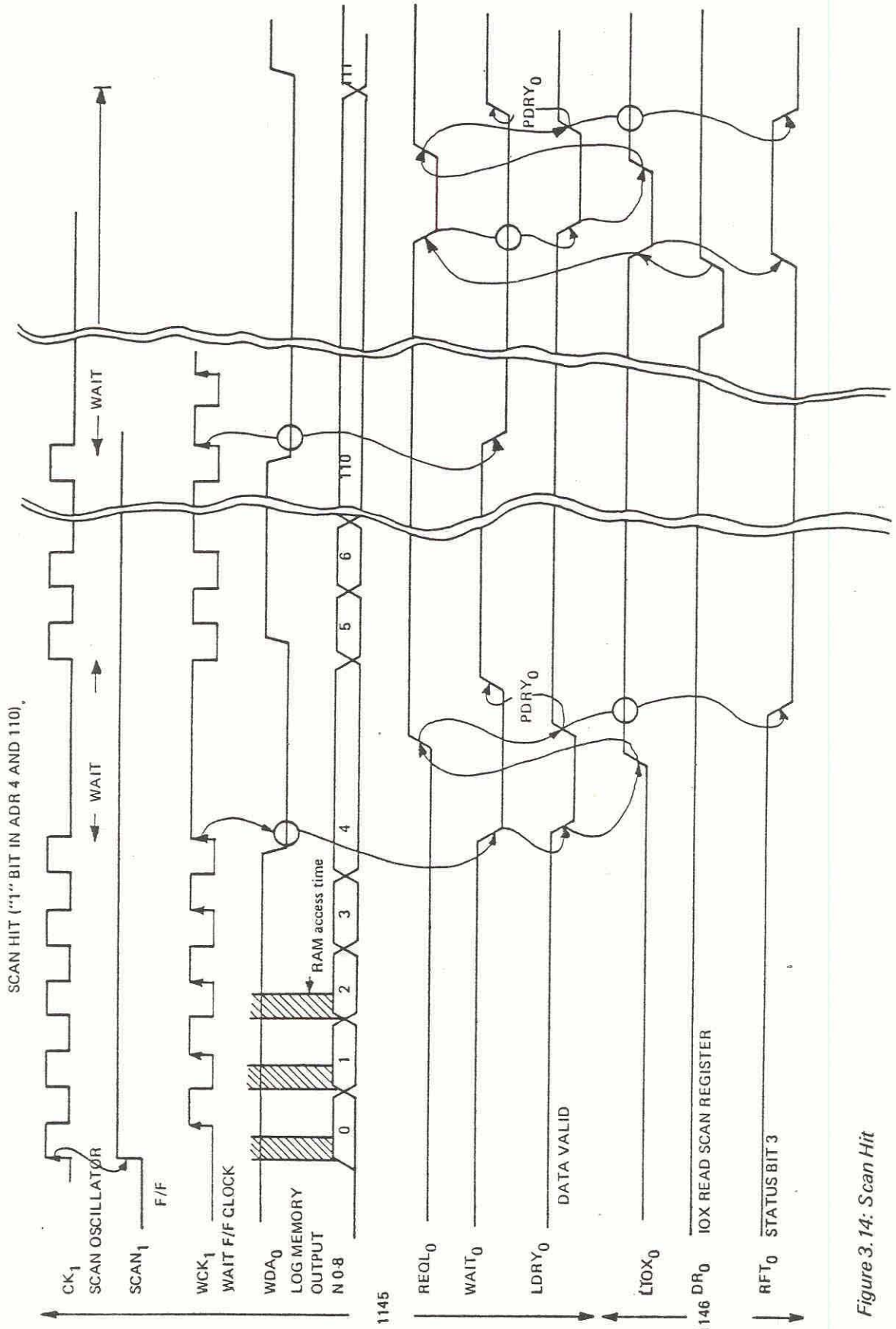


Figure 3.14: Scan Hit

4 CONTROL CHANNEL SPECIFICATIONS

4.1 *FUNCTIONAL DESCRIPTION*

The purpose of the control channel is to distribute a synchronous refresh signal and 5 memory inhibits between banks.

4.1.1 *Memory Inhibit/Power Fail*

When a memory bank loses its main 5V power a memory inhibit signal, CMI, arrives from the power supply. The purpose is to inhibit all but refresh accesses to the bank. In order to maintain data while main power has disappeared, 5V, −12, and + 12V stand-by power keeps vital circuitry alive.

While main power is down CMI will clear and inhibit requests from all ports. When normal power conditions return all old requests are "forgetten".

When a system is powered from different supplies a single memory channel may lose power while the bank is still going strong. Each memory channel must therefore supply a separate signal which inhibits the attached port.

When the memory channel source has common power supply to the bank, a separate inhibit signal is *not necessary*.

4.1.2 *Refresh Synchronization*

It may be advantageous to synchronize refresh in two banks which are connected to a 32 bit channel. (However, the benefits are marginal.) Via the control channel up to 8 banks may be synchronized to the same refresh oscillator. To do so one bank must be selected as a master which transmits the refresh oscillator to a number of slaves.

Master, slaves and independents are selected by backwiring straps as described in Section 5.2.2.

4.2 *ELECTRICAL SPECIFICATIONS*

Memory inhibits are single ending signals, low true, twisted with ground. Each receiver offers a standard TTL load with a pull-up and filter capacitor.

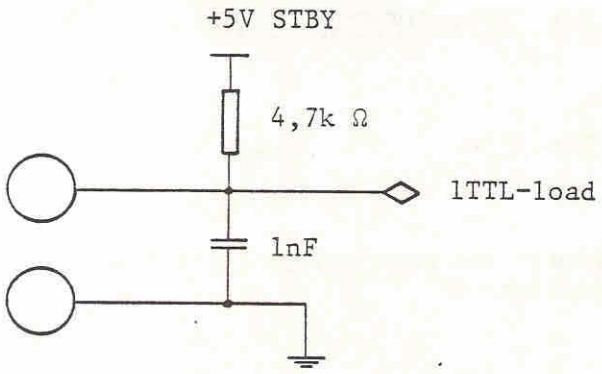


Figure 4.1: Electrical Specifications

No external termination shall be used.

The refresh oscillator is transmitted on a differntial pair from driver DS 8831 to receivers DS 8820A. Termination is only required when the signal is brought out of the cabinet of the master.

4.3 *CHANNEL SIGNALS*

The meaning of the signals are:

CMI:	Memory inhibit from the power supply of the bank.
REFOSC:	Refresh oscillator sent from a "master bank".
MIA - MID:	4 individual memory inhibits from the power supplies of the memory channel sources A-D.

5 INSTALLATION

5.1 *SWITCH SETTING*

5.1.1 *Address Range Selection*

The address range has to be defined at each port of a bank. On address module 1142, two pairs of thumb wheel switches define lower and upper address limits.

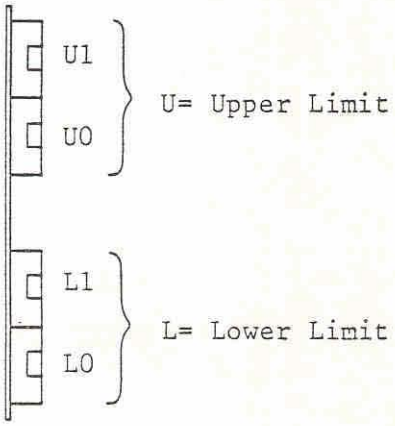


Figure 5.1: Limit Switches

The switch range is 0-9 but 8 and 9 are unused (they correspond to 0 and 1 respectively). The switch setting for some limits are shown in Figure 5.2.

Be careful that the 2 address ranges do not overlap on the same channel.

If a channel shall have access to the whole bank, then

U-L = Number of 32K modules in bank.

For Example:

With access to 0 - 256K in a bank, the limits shall be: U = 10_8, L = 0 and U-L = 8 modules.

Limit:	Address:
00	0
01	32K
02	64K
03	96K
04	128K
05	160K
06	192K
07	224K
10	256K
:	:
20	512K
:	:
30	768K
:	:
40	1024K
:	:
50	1280K
:	:
60	1536K
:	:
70	1792K
:	:
77	2016K

Figure 5.2: Limit Switch Setting

5.1.2 *Crate Number Setting*

In order to determine the exact position of a failing memory IC, the crates must be numbered uniquely. On the log module 1145 (or 1157) a 0-9 thumb wheel switch is mounted.

0-7 defines crate number
8-9 means crate disregarded by I/O interface

It is immaterial which number is assigned which crate, provided all are different.

5.1.3 *Manual Disabling of Error Correction*

For maintenance purposes it may be desireable to disable error correction at a port. On all data modules 1143, a disable switch is mounted.

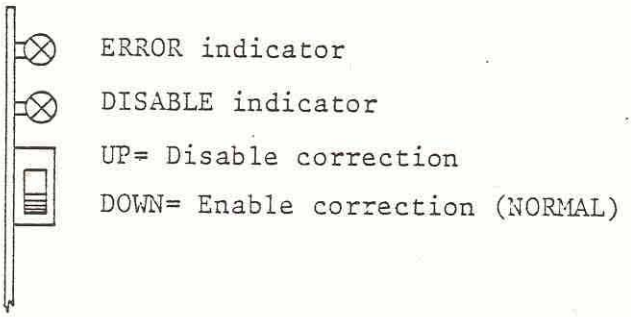


Figure 5.3: Indicators

Normally the switch shall be in the down position (correction enabled) and both indicators turned off.

Note that the disable indicator may be lighted even if the switch is turned down when correction is disabled by program (see Chapter 3).

The error indicator may be cleared by toggling the switch once.

5.2 *CONTROL CHANNEL CONNECTION*

5.2.1 *Memory Inhibit*

In each bank there are up to 5 separate memory inhibit signals, MI, that must be handled. Each port must receive a MI from the power supply which feeds the channel source (refer to Figure 5.4).

Channels which have power supply in common with the crate need no separate MI. Thus, in a normal single computer system only CMI is necessary.

5.2.2 *Refresh Synchronization*

It is possible to synchronize the refresh on several banks. To do so, one bank must be selected as a *master* which transmits the refresh oscillator to a number of *slaves*. The control channel contains a pair of lines (92-93) which is intended for distribution of the refresh oscillator signal.

To participate as a master or a slave one track in the printed backwiring must be broken. Be careful to appoint only *one* master.

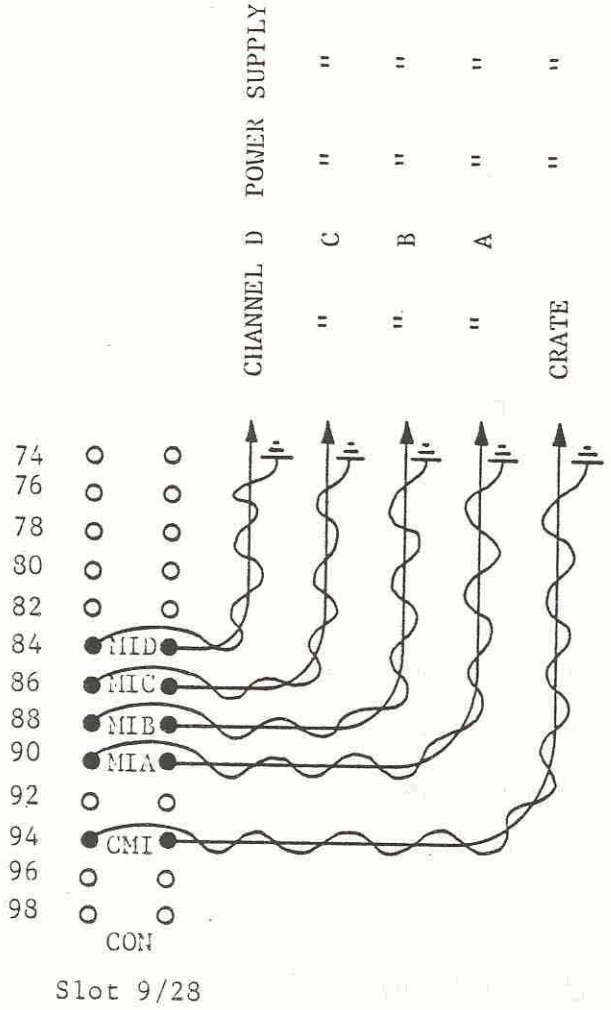


Figure 5.4: Memory Inhibits Connections in Backwiring

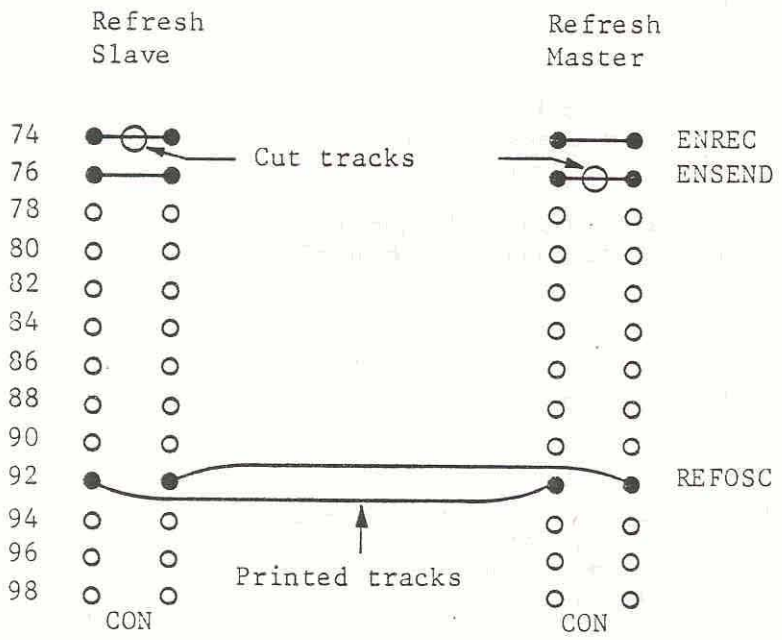


Figure 5.5: Refresh Synchronization at Control Modules in Slot 9 or 28.

Asynchronous independent bank	Do nothing (normal)
Synchronous master bank	Break at control plug 76-77
Synchronous slave bank	Break at control plug 74-75

Figure 5.6: Three Modes of Refresh Operation for a Bank

5.3 *CHANNEL EXPANSION*

5.3.1 *Daisy Chaining*

Linking a channel between several banks is performed by daisy chained cables. Hence, two joining plugs for entrance and exit are available for each cable.

Note! All channels between two banks in one crate are internally daisy chained.

Figurer 5.7 shows which plug fields are internally connected.

Entrance and exit may be exchanged since all connections are 1:1.

	Slots:	Terminal Range:
Port A Address	10 - 27	95 - 50
Port A Data	14 - 23	95 - 56
Port B Address	11 - 26	95 - 50
Port B Data	15 - 22	95 - 56
Port C Address	12 - 25	95 - 50
Port C Data	16 - 21	95 - 56
Port D Address	13 - 24	95 - 50
Port D Data	17 - 20	95 - 56
Maintenance Channel	18 - 19	95 - 56
Control Channel	9 - 28	95 - 84

Figure 5.7: Internally Connected Plug Fields Used for Channel Expansion

It is strictly forbidden to carry out other signals than those stated in "terminal range" in Figure 5.7.

For Example:

If 25 pairs of flat cables are used the forbidden signal wires must be properly broken.

5.3.2 *Termination*

All systems with channel cable length of more than 1 meter (or between cabinets) shall be terminated. Thus, single bank systems (ND-143, ND-144) contained in one cabinet do not need termination but all others do. The terminal plug is put on the last free contract at the end of the channel. Except for the control channel all signal pairs shall be terminated in 120 Ω. On the control channel only the REF OSC signal (pair 92 - 93) shall be terminated if synchronized refresh is used and brought out of the cabinet.

5.4 *CONFIGURATION STRUCTURE*

There are 4 basic bank configurations: ND-143, 144, 146 and 158 which may be expanded by ports ND-145, 147 and storage modules ND-156.

The modules that constitute the various ND numbers are shown in Appendix F. This appendix also shows the proper slot numbers for each module. The primary positions are shown with a bold frame. Expansion possibilities are indicated by a light frame.

Note! ND-146 and 158 require extra wire-wrap backwiring unless a separate flat cable plug panel is used.

APPENDIX A

BMPM TO MPM COMPARISON

Big multiport memory (BMPM) compared to the former model of multiport memory (MPM). Below are short statements regarding the differences and similarities between the two models:

1. Same concept and design philosophy.
2. Improved electrical specifications allow 10 ports per channel on BMPM compared to 4 ports on MPM.
3. Signal definitions and timing requirements of the channel are the same.
4. BMPM access time are somewhat faster.
5. BMPM ports may be connected to existing MPM channels.
6. One port serves one bank in BMPM while it serves two in MPM.
7. BMPM address range is 2048K while it is 256K in MPM.
8. Resolution of port address limits are 32K on BMPM while 8K on MPM.
9. Bank sizes, in one crate, are 256K and 128K in BMPM compared to 2 x 64K in MPM.
10. BMPM has error correction as standard (stored data has 16 + 5 bits) while MPM has dual parity error detection (stored data has 16 + 2 bits).
11. 8K memory modules (1094) ND-152 cannot be used in BMPM. 32K memory modules (1132) ND-156 can be used in MPM but requires modification of refresh (ECO issued).
12. In contrast to MPM, BMPM features a special maintenance channel for reporting of errors, reading of address range switches and general test purposes.

APPENDIX B

CONVERSION CHARTS

B.1 *CONVERSION BETWEEN LOGICAL CODE AND PHYSICAL POSITION OF FAULTY IC'S ON 1132 MODULE*

IC CODE	1132 COORDINATES	IC CODE	1132 COORDINATES
0	- No error	40	- No error
1	1 0 B	41	10 D
2	17 C	42	17 E
3	3 B	43	3 D
4	6 B	44	6 D
5	13 C	45	13 E
6	- Mult. error in B or C	46	- Mult. error in D or E
7	4 C	47	4 E
10	1 C	50	1 E
11	10 C	51	10 E
12	- Mult. error in B or C	52	- Mult. error in D or E
13	6 C	53	6 E
14	4 B	54	4 D
15	9 B	55	9 D
16	3 C	56	3 E
17	- Mult. error in B or C	57	- Mult. error in D or E
20	9 C	60	9 E
21	19 C	61	19 E
22	14 B	62	14 D
23	11 B	63	11 D
24	7 B	64	7 D
25	- Mult. error in B or C	65	- Mult. error in D or E
26	7 C	66	7 E
27	- Mult. error in B og C	67	- Mult. error in D or E
30	14 C	70	14 E
31	- Mult. error in B or C	71	- Mult. error in D or E
32	1 3 B	72	13 D
33	- Mult. error in B or C	73	- Mult. error in D or E
34	16 C	74	16 E
35	- Mult. error in B or C	75	- Mult. error in D or E
36	- Mult. error in B or C	76	- Mult. error in D or E
37	- Mult. error in B or C	77	- Mult. error in D or E

B.2 *CONVERSION BETWEEN LOGICAL CODE AND PHYSICAL SLOT OF FAULTY STORAGE MODULES*

MODULE CODE	CRATE SLOT	MODULE CODE	CRATE SLOT
0	1	10	32
1	2	11	31
2	3	12	30
3	4	13	29
4	5	14	
5	6	15	Unassigned
6	7	16	
7	8	17	

B.3 *PHYSICAL POSITION OF RANGE LIMIT SWITCHES INDICATED BY THE BANK/PORT CODE*

BANK/PORT CODE 987	PORT	CRATE SLOT
000	XA	10
001	XB	12
010	XC	14
011	XD	16
100	YA	27
101	YB	25
110	YC	23
111	YD	21

APPENDIX C

CABLE AND WIRING LISTS

Figure C.1: Memory Channel — Address

Figure C.2: Memory Channel — Data

Figure C.3: Service Channel

Figure C.4: Control Channel

Figure C.5: Wire Wrapping on ND-146

Figure C.6: Terminal Plug

Figure C.7: Memory Channel — Address Interleave Cable

A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Memory Channel Addresses at Port	Drawing no. I

NO.	SIGNAL	POLARITY	ADDRESS PORT 1:1 cable	ADDRESS PORT Interleave cable		
1	BA15L	0	BERG 95	93		
	BA15L	1	" 94	92		
2	BA14L	0	" 93	91		
	BA14L	1	" 92	90		
3	BA13L	0	" 91	89		
	BA13L	1	" 90	88		
4	BA12L	0	" 89	87		
	BA12L	1	" 88	86		
5	BA11L	0	" 87	85		
	BA11L	1	" 86	84		
6	BA10L	0	" 85	83		
	BA10L	1	" 84	82		
7	BA9L	0	" 83	81		
	BA9L	1	" 82	80		
8	BA8L	0	" 81	79		
	BA8L	1	" 80	78		
9	BA7L	0	" 79	77		
	BA7L	1	" 78	76		
10	BA6L	0	" 77	75		
	BA6L	1	" 76	74		
11	BA5L	0	" 75	73		
	BA5L	1	" 74	72		
12	BA4L	0	" 73	71		
	BA4L	1	" 72	70		
13	BA3L	0	" 71	69		
	BA3L	1	" 70	68		
14	BA2L	0	" 69	67		
	BA2L	1	" 68	66		
15	BA1L	0	" 67	65		
	BA1L	1	" 66	64		
16	BA0L	0	" 65	51		
	BA0L	1	" 64	50		
17	BA17L	0	" 63	61		
	BA17L	1	" 62	60		
18	BA16L	0	" 61	95		
	BA16L	1	" 60	94		
19	WRITEL	0	" 59	59		
	WRITEL	1	" 58	58		
20	REQL	0	" 57	57		
	REQL	1	" 56	56		
21	BA18	0	" 55	63		
	BA18	1	" 54	62		
22	BA19	0	" 53	55		
	BA19	1	" 52	54		
23	BA20	0	" 51	53		
	BA20	1	" 50	52		

Standard differential channel

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	Signals 1–20 are Standard Signals 21–23 are Extended Addresses	Replaced by	Date
DATE			

A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Memory Channel Data at Port	Drawing no. II

NO.	SIGNAL	POLARITY	DATA PORT			
1	BD15L	0	BERG 95			
	BD15L	1	" 94			
2	BD14L	0	" 93			
	BD14L	1	" 92			
3	BD13L	0	" 91			
	BD13L	1	" 90			
4	BD12L	0	" 89			
	BD12L	1	" 88			
5	BD11L	0	" 87			
	BD11L	1	" 86			
6	BD10L	0	" 85			
	BD10L	1	" 84			
7	BD9L	0	" 83			
	BD9L	1	" 82			
8	BD8L	0	" 81			
	BD8L	1	" 80			
9	BD7L	0	" 79			
	BD7L	1	" 78			
10	BD6L	0	" 77			
	BD6L	1	" 76			
11	BD5L	0	" 75			
	BD5L	1	" 74			
12	BD4L	0	" 73			
	BD4L	1	" 72			
13	BD3L	0	" 71			
	BD3L	1	" 70			
14	BD2L	0	" 69			
	BD2L	1	" 68			
15	BD1L	0	" 67			
	BD1L	1	" 66			
16	BD0L	0	" 65			
	BD0L	1	" 64			
17	BD17L	0	" 63			
	BD17L	1	" 62			
18	BD16L	0	" 61			
	BD16L	1	" 60			
19	ARL	0	" 59			
	ARL	1	" 58			
20	DRL	0	" 57			
	DRL	1	" 56			

Standard differential channel

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Service Channel	Drawing no. III

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)			
1	B15L	0	BERG 95			
	B15L	1	" 94			
2	B14L	0	" 93			
	B14L	1	" 92			
3	B13L	0	" 91			
	B13L	1	" 90			
4	B12L	0	" 89			
	B12L	1	" 88			
5	B11L	0	" 87			
	B11L	1	" 86			
6	B10L	0	" 85			
	B10L	1	" 84			
7	B9L	0	" 33			
	B9L	1	" 82			
8	B8L	0	" 31			
	B8L	1	" 80			
9	B7L	0	" 79			
	B7L	1	" 78			
10	B6L	0	" 77			
	B6L	1	" 76			
11	B5L	0	" 75			
	B5L	1	" 74			
12	B4L	0	" 73			
	B4L	1	" 72			
13	B3L	0	" 71			
	B3L	1	" 70			
14	B2L	0	" 69			
	B2L	1	" 68			
15	B1L	0	" 67			
	B1L	1	" 66			
16	B0L	0	" 65			
	B0L	1	" 64			
17	LINTL	0	" 63			
	LINTL	1	" 62			
18	LDRYL	0	" 61			
	LDRYL	1	" 60			
19	ACTL	0	" 59			
	ACTL	1	" 58			
20	LIOXL	0	" 57			
	LIOXL	1	" 56			

Standard differential channel

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Control Channel	Drawing no.: IV

NO.	SIGNAL	POLARITY	PLUG BERG (CPU POS.)			
1	CMI	0	BERG 95			
	CMD		" 94			
2	REFOSC	0	" 93			
	REFOSC	1	" 92			
3	MIA	0	" 91			
	GND		" 90			
4	MIB	0	" 89			
	GND		" 88			
5	MIC	0	" 87			
	GND		" 86			
6	MID	0	" 85			
	GND		" 84			
7			"			
			"			
8			"			
			"			
9			"			
			"			
10	ENSEND	0	" 77	} Connected in backwir.	STRAPS FOR REFRESH SYNCHRONIZING	
	GND	1	" 76			
11	ENREC	0	" 75	} Connected in backwir.		
	GND	1	" 74			
12		0	"			
		1	"			
13		0	"			
		1	"			
14		0	"			
		1	"			
15		0	"			
		1	"			
16		0	"			
		1	"			
17		0	"			
		1	"			
18		0	"			
		1	"			
19		0	"			
		1	"			
20		0	"			
		1	"			

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Wire Wrapping on ND-146	Drawing no.: V

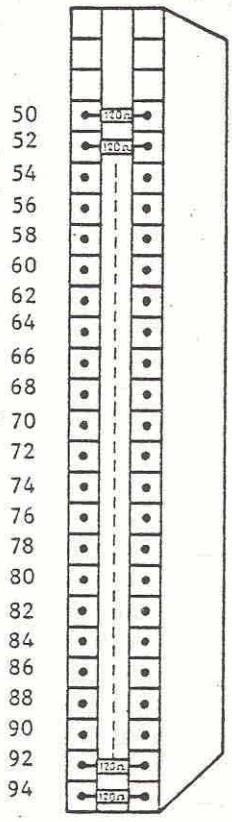
XDDAT - YDDAT	XCDAT - YCDAT	XBDAT - YBDAT	XADAT - YADAT
17:56 - 20:56	16:56 - 21:56	15:56 - 22:56	14:56 - 23:56
17:57 - 20:57			
⋮	⋮	⋮	⋮
17:94 - 20:94			
17:95 - 20:95	16:95 - 21:95	15:95 - 22:95	14:95 - 23:95

XDADR - YDADR	XCADR - YCADR	XBADR - YBADR	XAADR - YAADR
13:56 - 24:56	12:56 - 25:56	11:56 - 26:56	10:56 - 27:56
⋮	⋮	⋮	⋮
13:95 - 24:95	12:95 - 25:95	11:95 - 26:95	10:95 - 27:95

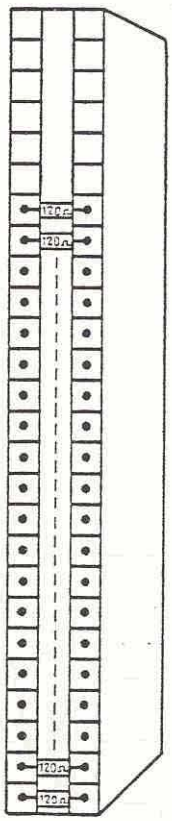
In all 8 groups 40 wires are wrapped 1:1 between pins of same number.

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

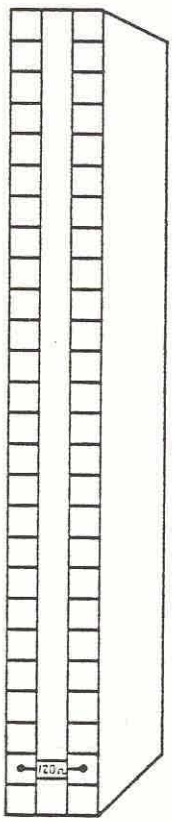
A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Termination Plugs	Drawing no.: VI



23 resistors, 120 Ω
Memory Channel Address



20 resistors, 120 Ω
Memory Channel Data
Maintenance Channel

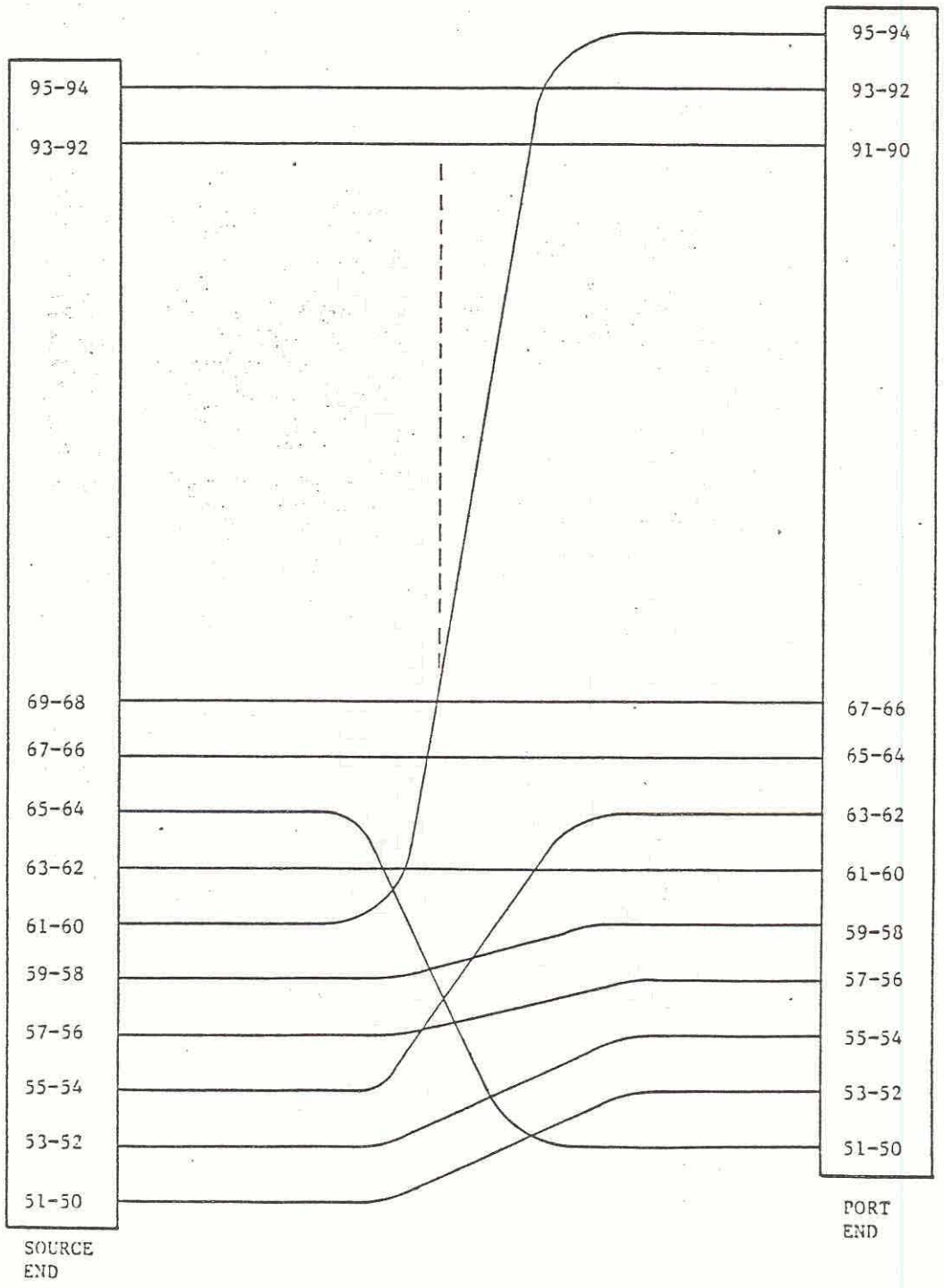


1 resistor, 120 Ω
Control Channel

Housings are 2 x 26 pins BERG 65051-011

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

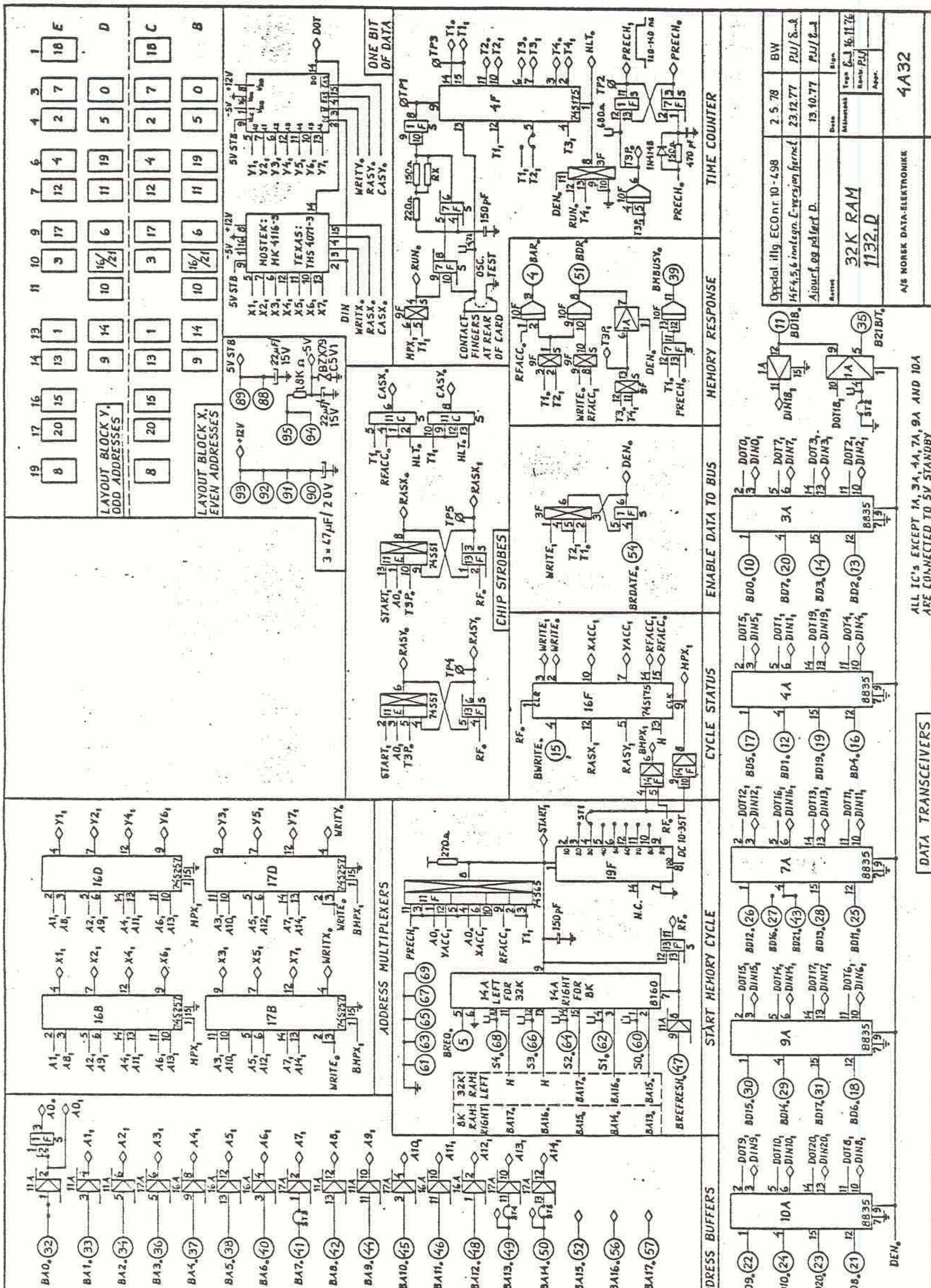
A/S NORSK DATA-ELEKTRONIKK	Title: BMPM Memory Channel Addresses at port One Way Interleave	Drawing no. VII

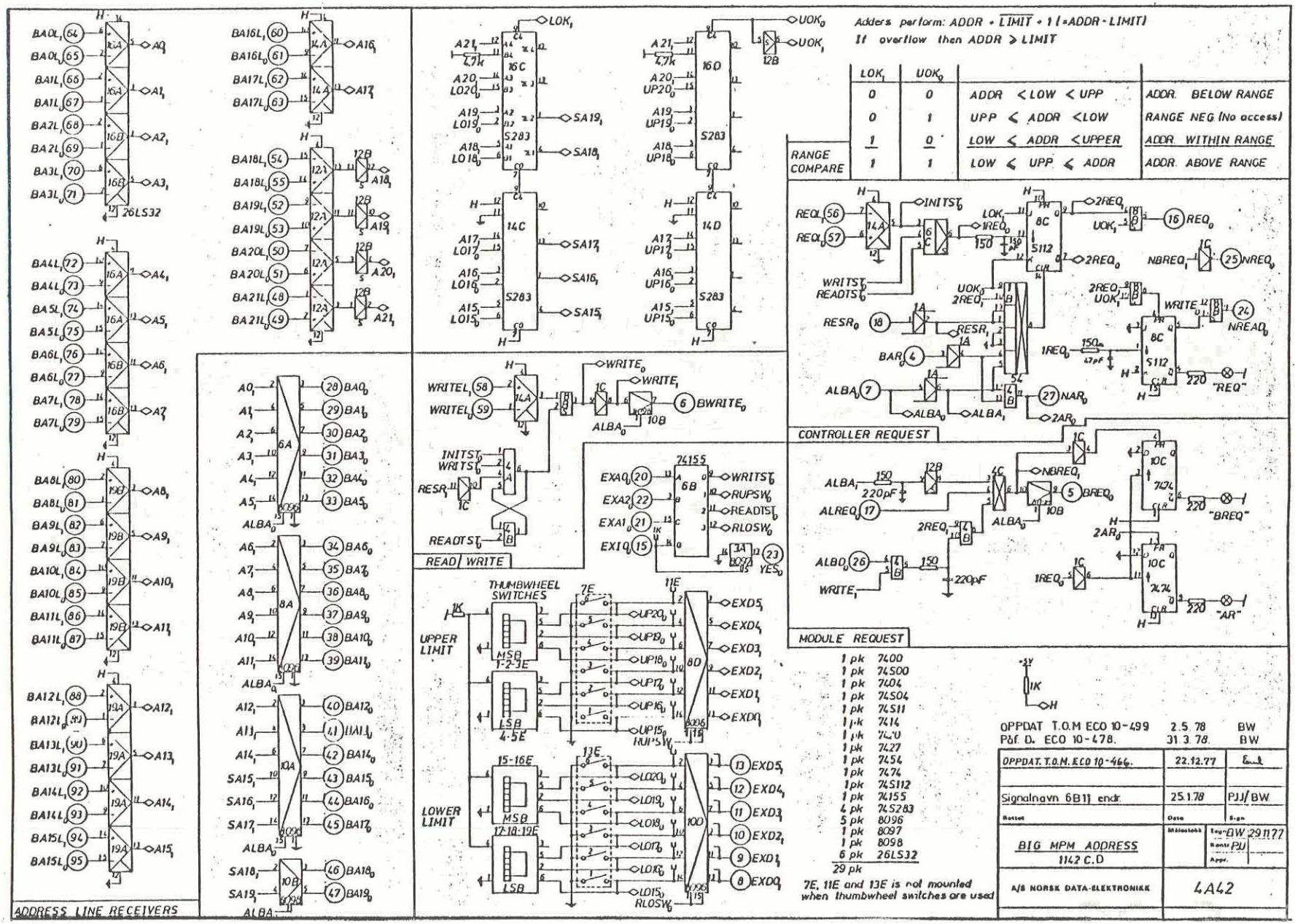


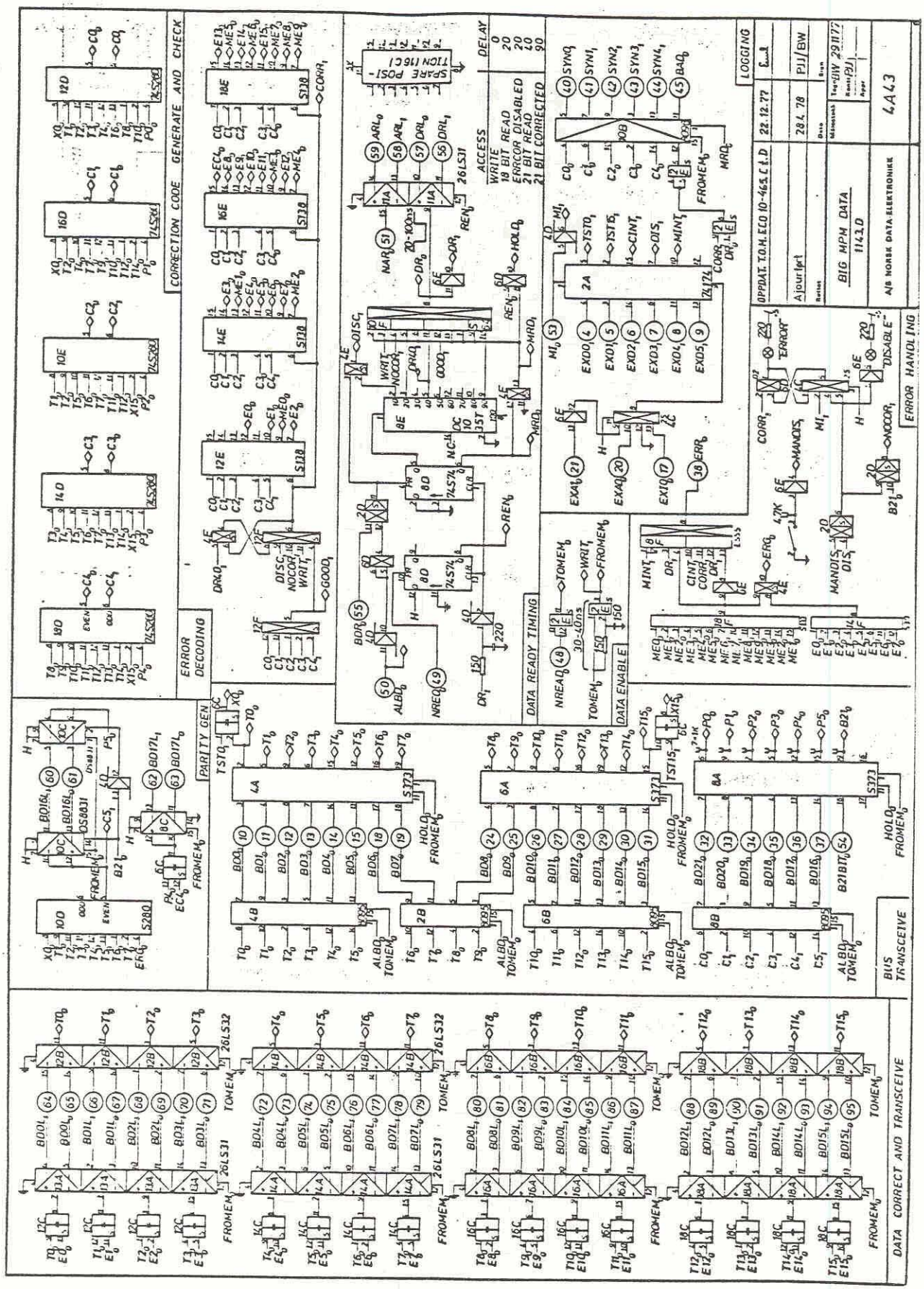
DRAWN BY	Remarks	Replacement for	Date
APPROVED BY	Cable appearance		
DATE		Replaced by	Date

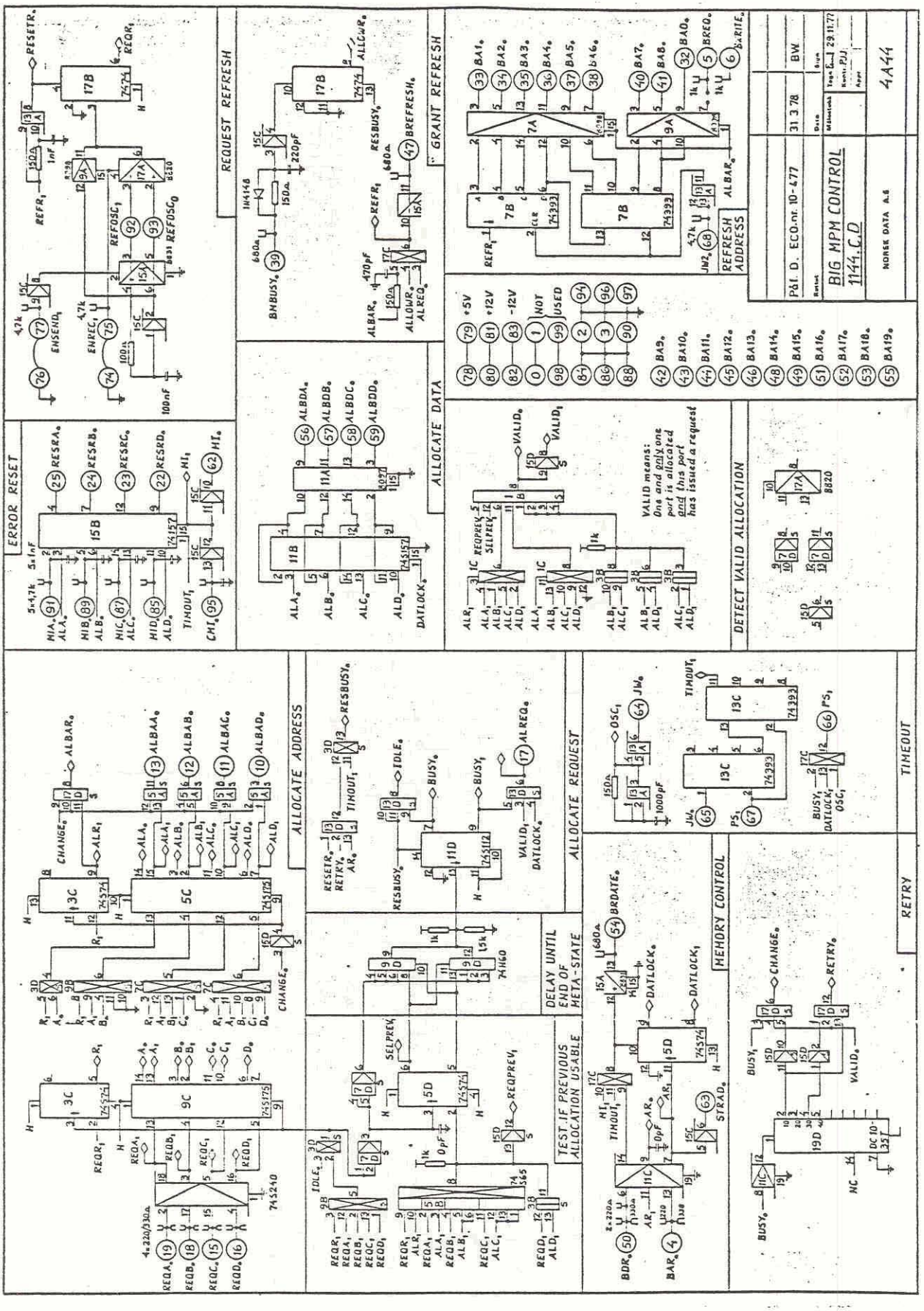
APPENDIX D

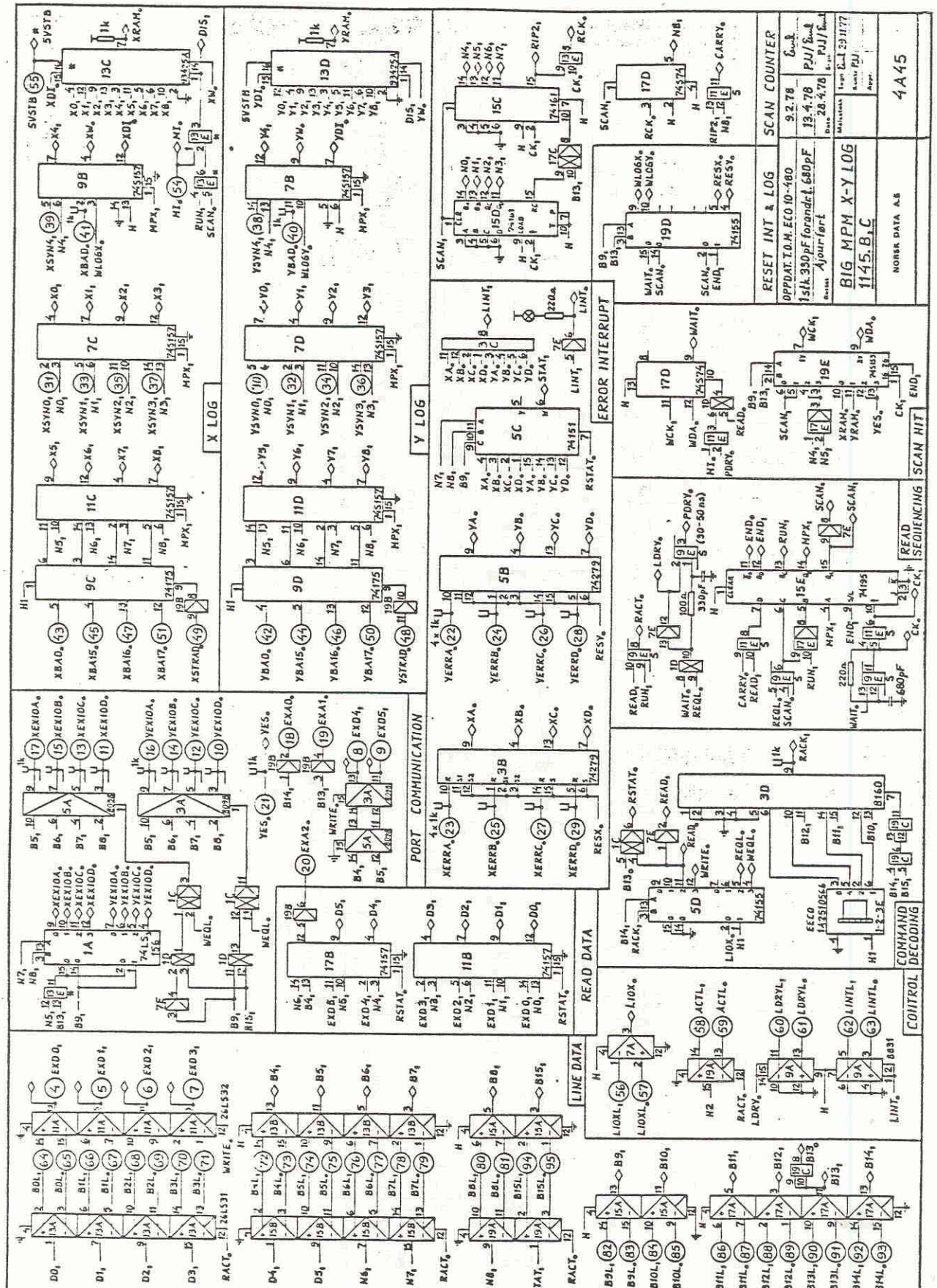
LOGIC DIAGRAMS

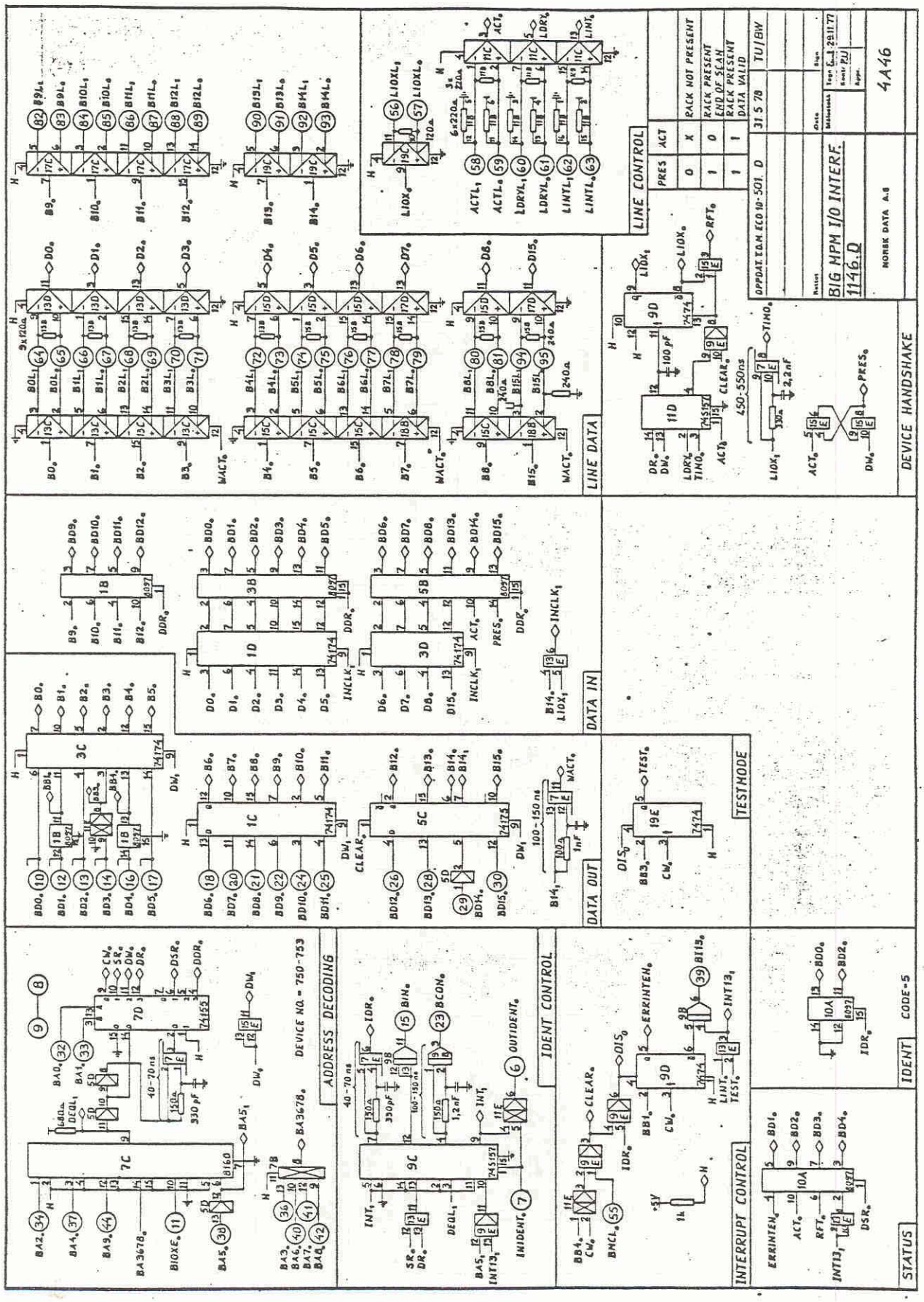

ADDRESS BUFFERS
ADDRESS MULTIPLEXERS
START MEMORY CYCLE
CYCLE STATUS
CHIP STROBES
ENABLE DATA TO BUS
MEMORY RESPONSE
TIME COUNTER
ONE BIT OF DATA
DATA TRANSCEIVERS
LAYOUT BLOCK Y, ODD ADDRESSES
LAYOUT BLOCK X, EVEN ADDRESSES
ALL IC's EXCEPT 1A, 3A, 4A, 7A, 9A AND 10A ARE CONNECTED TO 5V STANDBY
32K RAM
1132.D
4A32
A/S NORSK DATA-ELEKTRONIKK

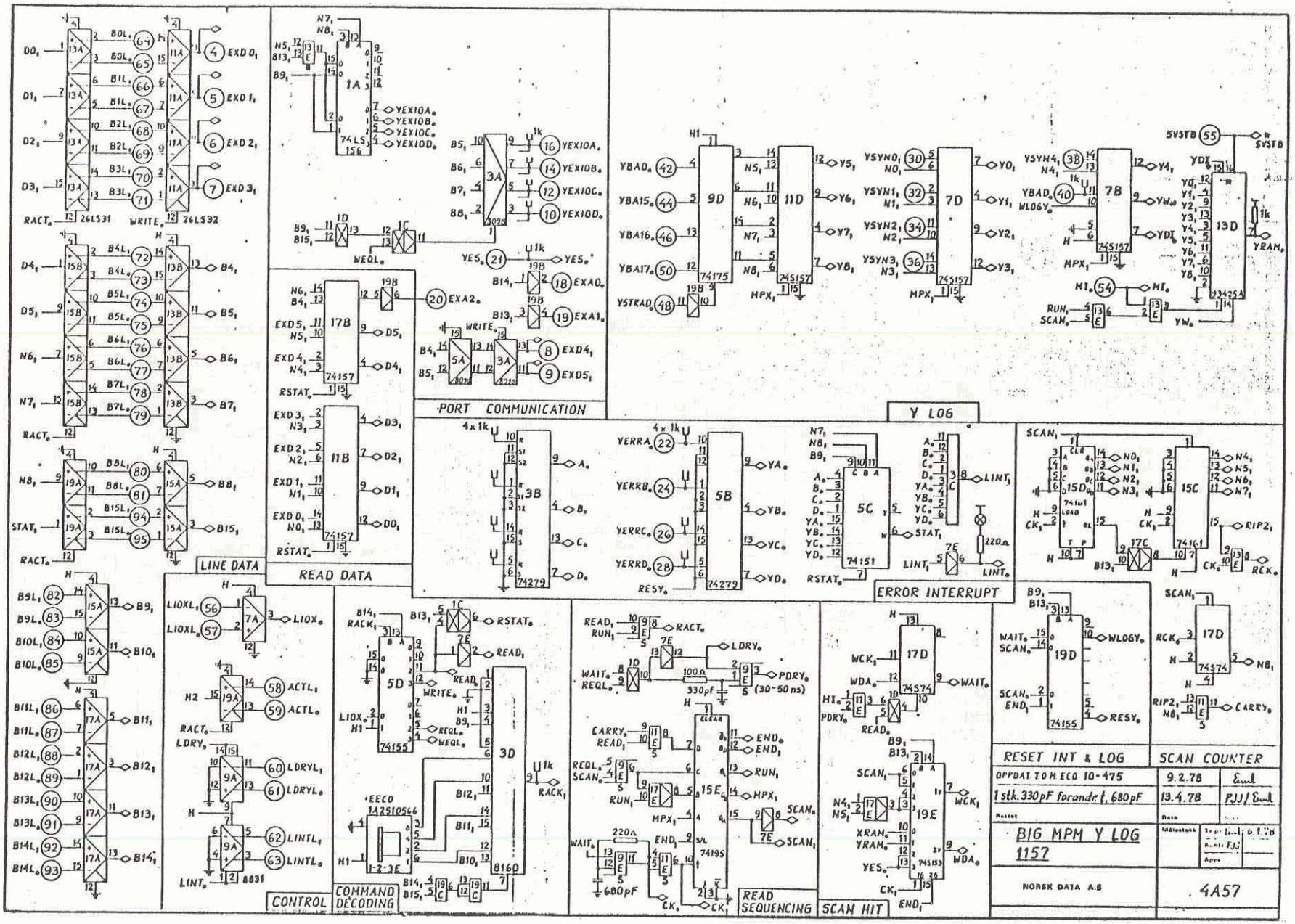

ADDRESS LINE RECEIVERS
26LS32
Adders perform: ADDR + $\overline{LIMIT}$ + 1 (=ADDR - LIMIT)
If overflow then ADDR > LIMIT
LOK1
UOK0
UOK1
RANGE COMPARE
LOK1 UOK0
0 0 ADDR < LOW < UPP — ADDR. BELOW RANGE
0 1 UPP < ADDR < LOW — RANGE NEG (No access)
1 0 LOW < ADDR < UPPER — ADDR. WITHIN RANGE
1 1 LOW < UPP < ADDR — ADDR. ABOVE RANGE
CONTROLLER REQUEST
MODULE REQUEST
READ/WRITE
THUMBWHEEL SWITCHES
UPPER LIMIT
LOWER LIMIT
7E, 11E and 13E is not mounted when thumbwheel switches are used
1 pk 7400
1 pk 74S00
1 pk 7404
1 pk 74S04
1 pk 74S11
1 pk 7414
1 pk 7420
1 pk 7427
1 pk 7454
1 pk 7474
1 pk 74S112
1 pk 74155
4 pk 74S283
5 pk 8096
1 pk 8097
1 pk 8098
6 pk 26LS32
29 pk
OPPDAT T.O.M ECO 10-499 2.5.78 BW
Pdf. D. ECO 10-478. 31.3.78. BW
OPPDAT. T.O.M. ECO 10-466. 22.12.77
Signalnavn 6B11 endr. 25.1.78 PJJ/BW
BIG MPM ADDRESS 1142 C.D
A/S NORSK DATA-ELEKTRONIKK
4A42


CORRECTION CODE GENERATE AND CHECK
ERROR DECODING
PARITY GEN
DATA READY TIMING
DATA ENABLE
ERROR HANDLING
DATA CORRECT AND TRANSCEIVE
BUS TRANSCEIVE
ACCESS
DELAY
WRITE 0
18 BIT READ 20
ERRCOR DISABLED 20
21 BIT READ 20
21 BIT CORRECTED 90
LOGGING
APPDAT. T.O.H. ECO 10-465 C.I.D
22.12.77
28.4.78
Ajourført
PJJ/BW
BIG MPM DATA
1142.D
A/S NORSK DATA ELEKTRONIKK
4.A.43


ERROR RESET
REQUEST REFRESH
GRANT REFRESH
ALLOCATE DATA
DETECT VALID ALLOCATION
ALLOCATE ADDRESS
ALLOCATE REQUEST
DELAY UNTIL END OF META-STATE
TEST IF PREVIOUS ALLOCATION USABLE
MEMORY CONTROL
RETRY
TIMEOUT
REFRESH ADDRESS
VALID means: One and only one port is allocated and this port has issued a request
BIG MPM CONTROL
1144.CD
NORSK DATA A.S
4A44


BIG MPM X-Y LOG
1145.B.C
NORSK DATA A.S
4A45
RESET INT & LOG
SCAN COUNTER
X LOG
Y LOG
ERROR INTERRUPT
PORT COMMUNICATION
READ DATA
LINE DATA
CONTROL
COMMAND DECODING
READ SEQUENCING
SCAN HIT


BIG HPM I/O INTERF.
1146.0
4.446
NORSK DATA A.S
DEVICE HANDSHAKE
LINE DATA
LINE CONTROL
DATA IN
DATA OUT
TESTMODE
ADDRESS DECODING
IDENT CONTROL
INTERRUPT CONTROL
STATUS
IDENT CODE=5
RACK NOT PRESENT
RACK PRESENT
END OF SCAN
DATA VALID
TU/BW


LINE DATA
READ DATA
PORT COMMUNICATION
Y LOG
ERROR INTERRUPT
CONTROL
COMMAND DECODING
READ SEQUENCING
SCAN HIT
RESET INT & LOG
SCAN COUNTER
BIG MPM Y LOG
1157
NORSK DATA A.S
4A57
OPPDAT TO H ECO 10-475
1 stk. 330pF forandr. t. 680pF
9.2.78
13.4.78
Eml
PJJ/Eml

APPENDIX E

RS-422 STANDARDS

E.1 *SUMMARY OF EIA RS-422 STANDARD FOR A BALANCED DIFFERENTIAL INTERFACE*

A. Line Driver

Open Circuit Voltage (either logic state)
- Differential: $|V_{do}| \leq 6.0V$
- Common Mode: $|V_{cmo}| \leq 3.0V$

Differential Output Voltage (across 100 ohm load)
- Either logic state: $|V_d| \geq \max(0.5V_{do}, 2.0V)$

Output Impedance
- Either logic state: $R_G \leq 100$ ohms

Mark-Space Level Symmetry (across 100 ohm load)
- Differential: $|V_{dS}| - |V_{dM}| \leq 0.4V$
- Common Mode: $|V_{cmS}| - |V_{cmM}| \leq 0.4V$

Output Short Circuit Current (to ground)
- Either Output: $|I_{SC}| \leq 150mA$

Output Leakage Current (power off)
- Voltage Range: $-0.25V \leq V_x \leq +6.0V$
- Either Output at V_x: $|I_X| \leq 100\mu A$

Rise and Fall Times (across 100 ohm load)
- T = Baud Interval: $(t_r, t_f) \leq \max(0.1T, 20ns)$

Ringing (across 100 ohm load)

Definitions

$V_{dSS} = V_d$ (steady state)

$V_{SS} = V_{dS} - V_{dM}$ (steady state)

Limits (either logic state)
- Percentage: $|V_d - V_{dSS}| \leq 0.1V_{SS}$
- Absolute: $2.0V \leq |V_d| \leq 6.0V$

B. Line Receiver

Signal Voltage Range
- Differential: $|V_d| \leq 6.0V$
- Common Mode: $|V_{cM}| \leq 7.0V$

Single-Ended Input Current (power ON or OFF)
- Either Input at V_x: $|V_x| = 10V$
- Other Input Grounded: $|I_V| \leq 3.25mA$

Single-Ended Input Bias Voltage (other input grounded)
- Either Input Open Circuit: $|V_B| \leq 3.0V$

Single-Ended Input Impedance (other input grounded)
- Either Input: $R_L \geq 4000$ ohms

Differential Threshold Sensitivity
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$
- Either Logic State: $|V_T| \leq 200mV$

Absolute Maximum Input Voltage
- Differential: $|V_d| \leq 12V$
- Single-Ended: $|V_x| \leq 10V$

Input Balance (threshold shift)
- Common Mode Voltage Range: $|V_{cm}| \leq 7.0V$

Differential Threshold (500 ohms in series with each input)
- Either Logic State: $|V_t| \leq 400mV$

Termination (optional)
- Total Load Resistance (differential): $R_T > 90$ ohms

Multiple Receivers (bus applications)

Up to 10 receivers allowed. Differential threshold sensitivity of 200mV must be maintained.

Hysteresis (optional)

As required for applications with slow rise/fall time at receiver, to control oscillations.

Fail Safe (optional)

As required by application to provide a steady MARK or SPACE condition under open connector or driver power OFF condition.

C. Interconnecting Cable

Type

Twisted Pair Wire or Flat Cable Conductor Pair

Conductor Size
- Copper Wire (solid or stranded): 24 AWG or larger
- Other (per conductor): $R \leq 30$ ohms/1000 ft.

Capacitance
- Mutual Pair: $C \leq 20pF/ft.$
- Stray: $C \leq 40pF/ft.$

Pair-to-Pair Cross Talk (balanced)
- Attenuation at 150KHz: $A \geq 40dB$

E.2 *EIA STANDARD RS-422*

Recommendation V.11

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR GENERAL USE WITH INTEGRATED CIRCUIT EQUIPMENT IN THE FIELD OF DATA COMMUNICATIONS [5]

(Geneva, 1976)

1. *Introduction*

This Recommendation deals with the electrical characteristics of the generator, receiver and interconnecting leads of a differential signalling (balanced) interchange circuit with an optional d.c. offset.

The balanced generator and load components are designed to cause minimum mutual interference with adjacent balanced or unbalanced interchange circuits (see Recommendation V.10) provided that waveshaping is employed on the unbalanced circuits.

In the context of this Recommendation, a balanced interchange circuit is defined as consisting of a balanced generator connected by a balanced interconnecting pair to a balanced receiver. For a balanced generator the algebraic sum of both the outlet potentials, with respect to earth, shall be constant for all signals transmitted; the impedances of the outlets with respect to earth shall be equal. The degree of balance of the interconnecting pair is a matter for further study.

Annexes are provided to give guidance on a number of application aspects as follows:

Annex 1 Cables and terminations

Annex 2 Compatibility with other interfaces

Annex 3 Multipoint operation

Note. – Generator and load devices meeting the electrical characteristics of this Recommendation need not operate over the entire signalling rate range specified. They may be designed to operate over narrower ranges to satisfy requirements more economically, particularly at lower signalling rates.

Reference measurements are described which may be used to verify certain of the recommended parameters but it is a matter for individual manufacturers to decide what tests are necessary to ensure compliance with the Recommendation.

2. *Field of application*

The electrical characteristics specified in this Recommendation apply to interchange circuits operating with data signalling rates up to 10 Mbit/s, and are intended to be used primarily in Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE) implemented in integrated-circuit technology.

This Recommendation applies to new work and is not intended to apply to DCE implemented in discrete component technology, for which the electrical characteristics covered by Recommendation V.28 are more appropriate.

---

[5] This Recommendation is also designated as X.27 in the Series X Recommendations.

Typical points of application are illustrated in Figure 1/V.11.

Whilst the balanced interchange circuit is primarily intended for use at the higher signalling rates, its use at the lower rates may be necessary in the following cases:

1) where the interconnecting cable is too long for proper unbalanced circuit operation;
2) where extraneous noise sources make unbalanced circuit operation impossible;
3) where it is necessary to minimize interference with other signals.

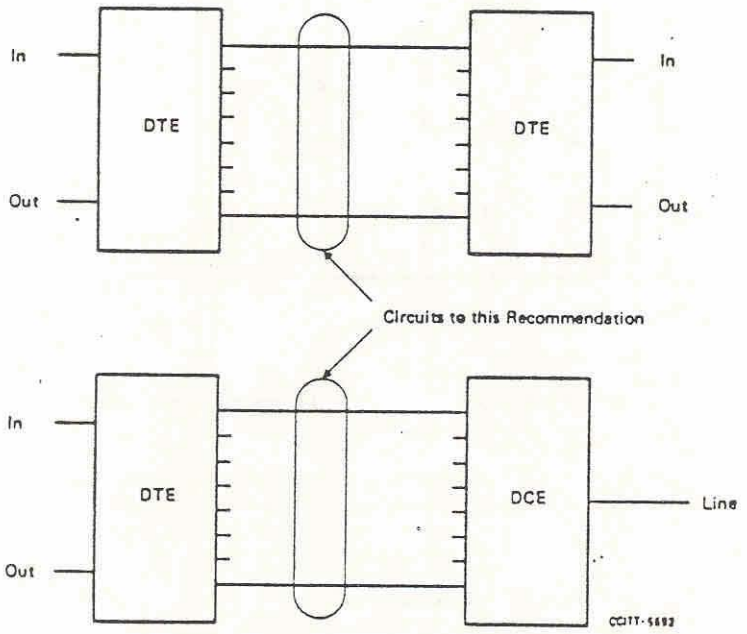
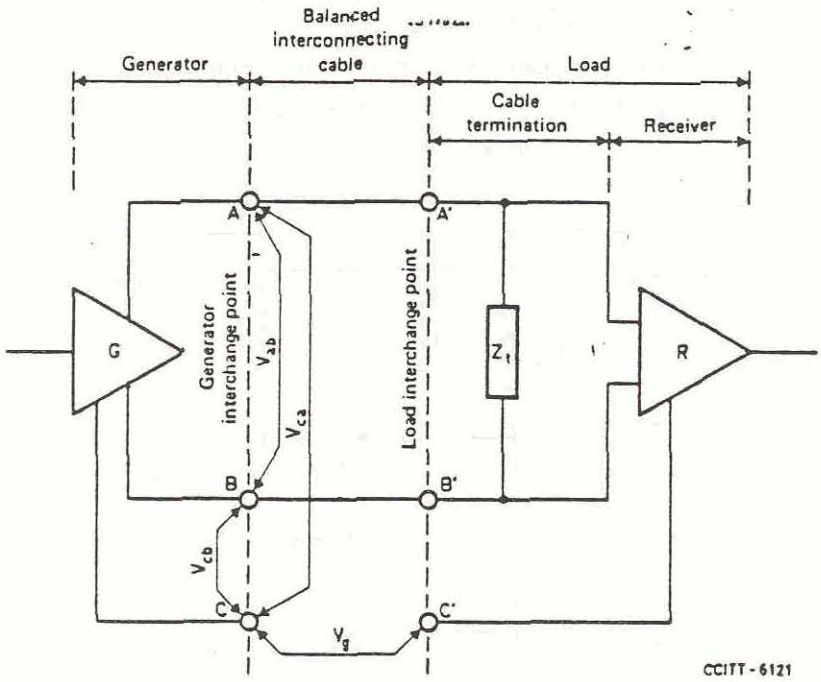


FIGURE 1/V.11 – Typical applications of balanced interchange circuits

3. *Symbolic representation of interchange circuit* (Figure 2/V.11)



V_{ab} = generator output voltage between points A and B
V_{ca} = generator voltage between points C and A
V_{cb} = generator voltage between points C and B
Z_t = cable termination impedance
V_g = ground potential difference
A, B and A', B' = interchange points
C, C' = zero volt reference interchange points

FIGURE 2/V.11 – Symbolic representation of a balanced interchange circuit

Note 1. – Two interchange points are shown above. The output characteristics of the generator, excluding any interconnecting cable, are defined at the "generator interchange point". The electrical characteristics to which the receiver must respond are defined at the "load interchange point".

Note 2. – Point C may be connected to C' by CCITT Recommendation V.24 Circuit 102 and to protective ground if required by national regulations.

4. *Generator polarities and receiver significant levels*

4.1 *Generator*

The signal conditions for the generator are specified in terms of the voltage between output points A and B shown in Figure 2/V.11.

When the signal condition 0 (space) for data circuits or ON for control and timing circuits is transmitted, the output point A is positive with respect to point B. When the signal condition 1 (mark) for data circuits or OFF for control and timing circuits is transmitted, the output point A is negative with respect to point B.

4.2 *Receiver*

The receiver differential significant levels are shown in Table A/V.11 below, where $V_{A'}$ and $V_{B'}$ are respectively the voltages at points A' and B' relative to point C':

TABLE A/V.11 – Receiver differential significant levels

	$V_{A'} - V_{B'} < -0.3$ V	$V_{A'} - V_{B'} > +0.3$ V
Data circuits	1	0
Control and timing circuits	OFF	ON

5. *Generator*

5.1 *Resistance and offset voltage*

1. The total generator resistance between points A and B shall be equal to or less than 100 ohms and adequately balanced with respect to point C. (It is left for further study as to the degree of balance required both statically and dynamically.)

2. The magnitude of the generator d.c. offset voltage (see 5.2.2 below) shall not exceed 3 V under all operating conditions.

5.2 *Static reference measurements*

The generator characteristics are specified in accordance with measurements illustrated in Figure 3/V.11 and described in 5.2.1 to 5.2.4 below.

5.2.1 *Open-circuit measurement* (Figure 3a)/V.11)

The open-circuit voltage measurements are made with a 3900 ohm resistor connected between points A and B. For either binary state, the magnitude of the differential voltage (V_0) shall not be more than 6.0 volts, nor shall the magnitude of V_{0a} and V_{0b} be more than 6.0 volts.

5.2.2 *Test-termination measurement* (Figure 3b)/V.11)

With a test load of two resistors, each 50 ohms, connected in series between the output points A and B, the differential voltage (V_t) shall not be less than 2.0 volts or 50% of the magnitude of V_0, whichever is greater. For the opposite binary state the polarity of V_t shall be reversed (V_t). The difference in the magnitudes of V_t and V_t shall be less than 0.4 volts. The magnitude of the generator offset voltage V_{0s} measured between the centre of the test load and point C shall not be greater than 3.0 volts. The magnitude of the difference in the values of V_{0s} for one binary state and the opposite binary state shall be less than 0.4 volts.

Note. – Under some conditions this measurement does not determine the degree of balance of the internal generator impedances to point C. It is left for further study whether additional measurements are necessary to ensure adequate balance in generator output impedances.

5.2.3 *Short-circuit measurement* (Figure 3c)/V.11)

With the output points A and B short-circuited to point C, the currents flowing through each of output points A or B shall not exceed 150 milliamperes for either logical condition.

5.2.4 *Power-off measurements* (Figure 3d)/V.11)

Under power-off condition with voltages ranging between +0.25 volt and −0.25 volt applied between each output point and point C, as indicated in Figure 3d)/V.11, the magnitude of the output leakage currents (I_{xa} and I_{xb}) shall not exceed 100 microamperes.

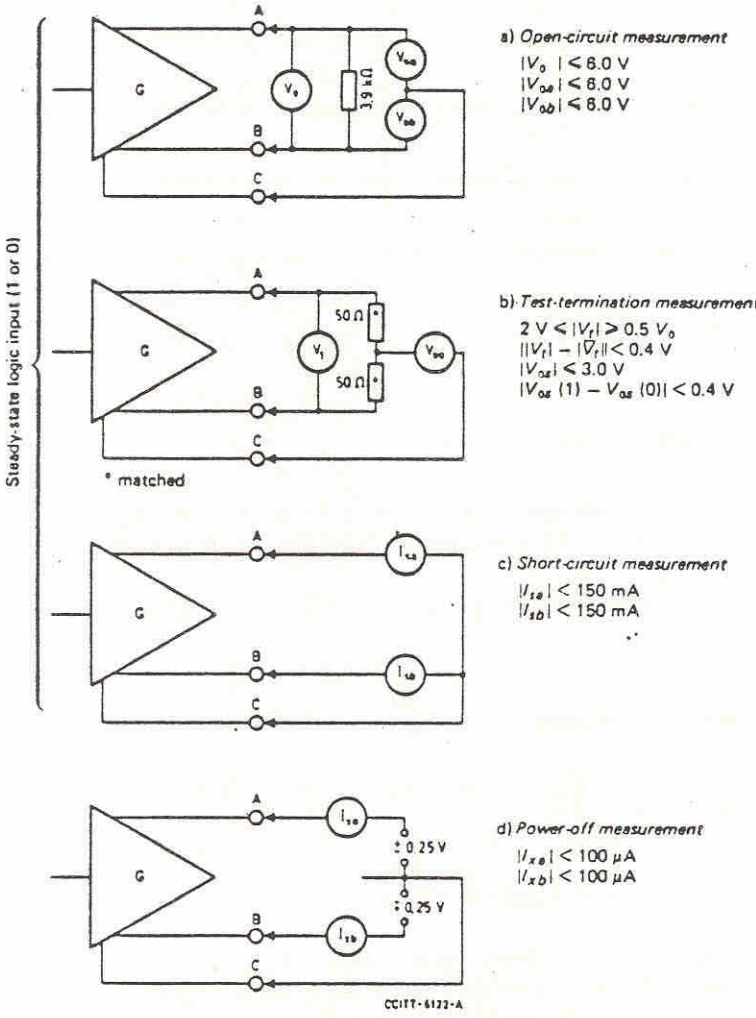
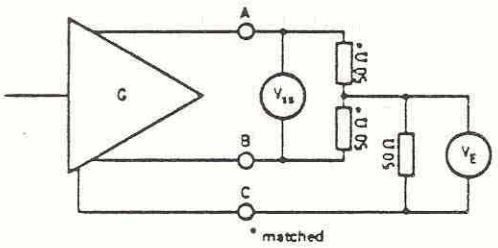


FIGURE 3/V.11 – Generator-parameter reference measurements

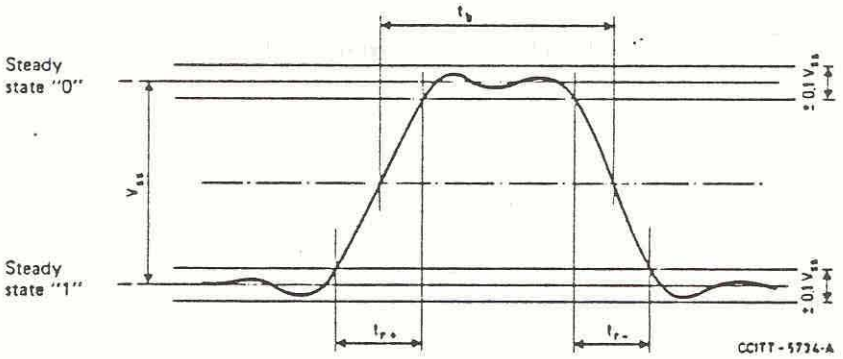
5.3 *Dynamic voltage balance and rise time* (Figure 4/V.11)

With the measurement configuration shown in Figure 4/V.11, a test signal with a nominal signal element duration t_b and composed of alternate ones and zeros, shall be applied to the input. The change in amplitude of the output signal during transitions from one binary state to the other shall be monotonic between 0.1 and 0.9 V_{ss} within 0.1 of t_b or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{ss} from the steady state value.

The resultant voltage due to imbalance (V_E) shall not exceed 0.4 V peak-to-peak (the value of V_E is provisional and is subject to further study to determine whether voltage peaks of very short duration should be included).



V_E < 0.4 V peak-to-peak (provisional)
V_{ss} = difference between signal steady-state voltages



t_b = nominal duration of the test signal element
for $t_b \geq 200$ ns, $t_r \leq 0.1\ t_b$
for $t_b < 200$ ns, $t_r \leq 20$ ns

FIGURE 4/V.11 – Generator dynamic balance and rise time measurement

6. *Load*

6.1 *Characteristics*

The load consists of a receiver (R) and an optional cable termination resistance (Z_t) as shown in Figure 2/V.11. The electrical characteristics of the receiver are specified in terms of the measurements illustrated in Figures 5/V.11, 6/V.11 and 7/V.11 and described in 6.2, 6.3 and 6.4 below. A circuit meeting these requirements results in a differential receiver having a high input impedance, a small input threshold transition region between -0.3 and $+0.3$ volts differential, and allowance for an internal bias voltage not to exceed 3 volts in magnitude. The receiver is electrically identical to that specified for the unbalanced receiver in Recommendation V.10.

6.2 *Receiver input voltage – current measurements* (Figure 5/V.11)

With the voltage $V_{i,a}$ (or $V_{i,b}$) ranging between -10 volts and $+10$ volts, while $V_{i,b}$ (or $V_{i,a}$) is held at 0 volt, the resultant input current $I_{i,a}$ (or $I_{i,b}$) shall remain within the shaded range shown in Figure 5/V.11. These measurements apply with the power supply of the receiver in both the power-on and power-off conditions.

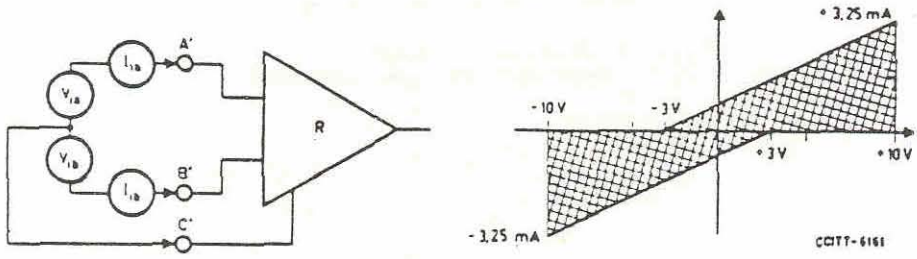


FIGURE 5/V.11 – Receiver input voltage-current measurements

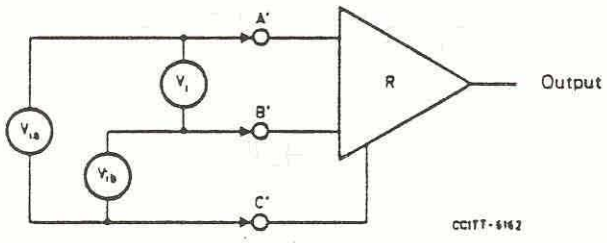
6.3 *D.c. input sensitivity measurements* (Figure 6/V.11)

Over the entire common mode voltage (V_{cm}) range of +7 volts to −7 volts, the receiver shall not require a differential input voltage (V_i) of more than 300 millivolts to assume correctly the intended binary state. Reversing the polarity of V_i shall cause the receiver to assume the opposite binary state.

The maximum voltage (signal plus common mode) present between either receiver input and receiver signal ground shall not exceed 10 volts nor cause the receiver to malfunction. The receiver shall tolerate a maximum differential signal of 12 volts applied across its input terminals without being damaged.

In the presence of the combinations of input voltages V_{ia} and V_{ib} specified in Figure 6/V.11, the receiver shall maintain the specified output binary state and shall not be damaged.

Note. – Designers of terminal equipment should be aware that slow signal transitions with noise present may give rise to instability or oscillatory conditions in the receiving device; therefore, appropriate techniques should be implemented to prevent such behaviour. For example, adequate hysteresis may be incorporated into the receiver to prevent such conditions.



Applied voltages		Resulting input voltage	Output binary state	Purpose of measurement
V_{ia}	V_{ib}	V_I		
−12 V	0 V	−12 V	(not specified)	To ensure no damage to receiver inputs
0 V	−12 V	+12 V		
+12 V	0 V	+12 V		
0 V	+12 V	−12 V		
+10 V	+ 4 V	+ 6 V	0	To guarantee correct operation at V_I = 6 V (maintain correct logic state)
+ 4 V	+10 V	− 6 V	1	
−10 V	− 4 V	− 6 V	1	
− 4 V	−10 V	+ 6 V	0	
				300 mV threshold measurement
+0.30 V	0 V	+0.3 V	0	V_{cm} = 0 V
0 V	+0.30 V	−0.3 V	1	
+7.15 V	+6.85 V	+0.3 V	0	V_{cm} = +7 V
+6.85 V	+7.15 V	−0.3 V	1	
−7.15 V	−6.85 V	−0.3 V	1	V_{cm} = −7 V
−6.85 V	−7.15 V	+0.3 V	0	

FIGURE 6/V.11 Receiver input sensitivity measurement

6.4 *Input balance test* (Figure 7/V.11)

The balance of the receiver input resistance and bias voltages shall be such that the receiver shall remain in the intended binary state under the conditions shown in Figure 7/V.11 and described as follows:

a) with V_i = +720 millivolts and V_{cm} varied between −7 and +7 volts;

b) with V_i = −720 millivolts and V_{cm} varied between −7 and +7 volts;

c) with V_i = +300 millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable signalling rate. (This condition is provisional and subject to further study.);

d) with V_i = −300 millivolts and V_{cm} a 1.5 volt peak-to-peak square wave at the highest applicable signalling rate (This condition is provisional and subject to further study).

Note. – The values of V_i are provisional and are the subject of further study.

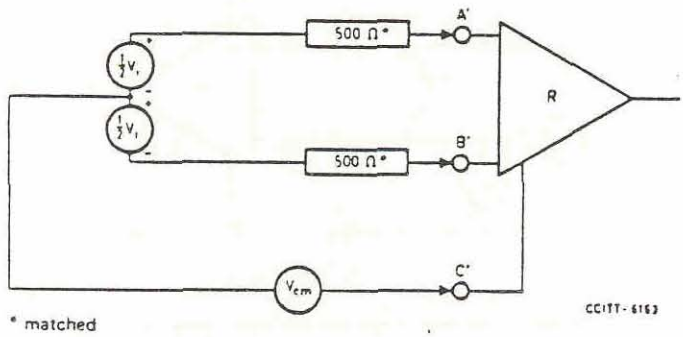


FIGURE 7/V.11 – Receiver input balance test

6.5 *Terminator*

The use of a terminator is optional depending upon the specific environment in which the interchange circuit is employed (see Annex 1). In no case shall the total load resistance be less than 100 ohms.

7. *Environmental constraints*

In order to operate a balanced interchange circuit at signalling rates ranging between 0 and 10 Mbit/s, the following conditions apply:

1) For each interchange circuit a balanced interconnecting pair is required.

2) Each interchange circuit must be appropriately terminated (see Annex 1).

3) The total common-mode voltage at the receiver must be less than 7 volts peak. This value is provisional and is subject to further study.

The common mode voltage at the receiver is the worst case combination of:

a) generator-receiver ground-potential difference (V_g, Figure 2/V.11);

b) longitudinally induced random noise voltage measured between the receiver points A' or B' and C' with the generator ends of the cable A, B and C joined together; and

c) generator bias voltage, if any.

Unless the generator is of a type which generates no bias voltage, the sum of *a)* and *b)* above, which is the element of the common mode voltage due to the environment of the interchange circuit, must be less than 4 volts peak.

8. *Circuit protection*

Balanced generator and load devices complying with this Recommendation shall not be damaged under the following conditions:

1) generator open circuit;

2) short-circuit between the conductors of the interconnecting cable;

3) short-circuit between either or both conductors and point C and C'.

The above faults 2) and 3) might cause power dissipation in the interchange circuit devices to approach the maximum power dissipation that may be tolerable by a typical integrated circuit (IC) package. The user is therefore cautioned that where multiple generators and receivers are implemented in a single IC package, only one such fault per package might be tolerable at any one time without damage occurring.

The user is also cautioned that the generator and receiver devices complying with this Recommendation might be damaged by spurious voltages applied between their input or output points and points C and C' (Figure 2/V.11). In those applications where the interconnecting cable may be inadvertently connected to other circuits, or where it may be exposed to a severe electromagnetic environment, protection should be employed.

9. *Detection of generator power-off or circuit failure*

Certain applications require detection of various fault conditions in the interchange circuits, e.g.:

1) generator in power-off condition;

2) receiver not interconnected with a generator;

3) open-circuited interconnecting cable;

4) short-circuited interconnecting cable;

5) input signal to the load remaining within the transition region (± 300 millivolts) for an abnormal period of time.

When detection of one or more fault conditions is required by specific applications, additional provisions are required in the load and the following items must be determined:

a) which interchange circuits require fault detection;

b) what faults must be detected;

c) what action must be taken when a fault is detected, e.g. which binary state must the receiver assume?

The method of detection of fault conditions is application-dependent and is therefore not further specified.

ANNEX 1

(to Recommendation V.11)

Cable and terminations

No electrical characteristics of the interconnecting cable are specified in this Recommendation. Guidance is given herein concerning operational constraints imposed by the length, balance and terminating resistance of the cable.

1. *Cable*

Over the length of the cable, the two conductors should have essentially the same values of:

1) capacitance to ground;

2) longitudinal resistance and inductance;

3) coupling to adjacent cables and circuits.

2. *Cable length*

The maximum permissible length of cable separating the generator and the load in a point-to-point application is a function of the data signalling rate. It is further influenced by the tolerable signal distortion and the environmental constraints such as ground potential difference and longitudinal noise. Increasing the distance between generator and load might increase the exposure to ground potential difference.

As an illustration of the above conditions, the curves of cable length versus data signalling rate in Figure 8/V.11 may be used for guidance.

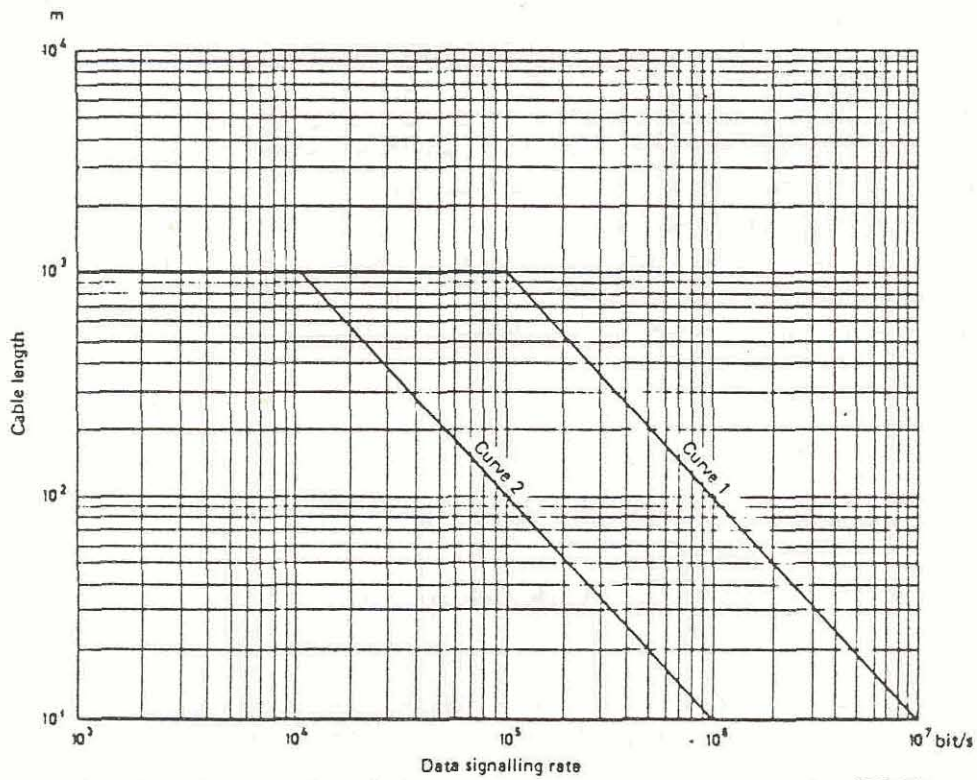
These curves are based upon empirical data using twisted pair telephone cable (0.51 mm wire diameter) both unterminated and terminated in a 100 ohm resistive load. The cable length restrictions shown by the curves are based upon the following assumed signal quality requirements at the load:

1) signal rise and fall time equal to, or less than, one-half the duration of the signal element;

2) a maximum voltage loss between generator and load of 6 dB.

At the higher signalling rates (see Figure 8/V.11) the sloping portion of the curves shows the cable length limitation established by the assumed signal rise and fall time requirements. The cable length has been arbitrarily limited to 1000 metres by the assumed maximum allowable loss of 6 dB.

These curves assume that the environmental limits specified in this Recommendation have been achieved. At the higher signalling rates these conditions are more difficult to attain due to cable imperfections and common-mode noise. Operation within the signalling rate and distance bounds of Figure 8/V.11 will usually ensure that distortion of the signal appearing at the receiver input will be acceptable. Many applications, however, can tolerate much greater levels of signal distortion and in these cases correspondingly greater cable lengths may be employed.



Curve 1 : terminated interchange circuit
Curve 2 : unterminated interchange circuit

FIGURE 8/V.11 - Data signalling rate vs cable length for balanced interchange circuit

Experience has shown that in many practical cases the operating distance at lower signalling rates may extend to several kilometres.

For synchronous transmission where the data and signal element timing are transmitted in opposite directions, the phase relationship between the two may need to be adjusted to ensure conformity with the relevant requirements of signal quality at the interchange point.

3. *Cable termination*

The use of a cable termination is optional and dependent on the specific application. At the higher signalling rates (above 200 kbit/s) or at any signalling rate where the cable propagation delay is of the order of half the signal element duration a termination should be used to preserve the signal rise time and minimize reflections. The terminating impedance should match as closely as possible the cable characteristic impedance in the signal spectrum.

Generally, a resistance in the range of 100 to 150 ohms will be satisfactory, the higher values leading to lower power dissipation.

At the lower signalling rates, where distortion and rise-time are not critical, it may be desirable to omit the termination in order to minimize power dissipation in the generator.

ANNEX 2

(to Recommendation V.11)

Compatibility with other interfaces

1. *Compatibility of Recommendation V.10 and Recommendation V.11 interchange circuits in the same interface*

The electrical characteristics of Recommendation V.11 are designed to allow the use of unbalanced (see Recommendation V.10) and balanced circuits within the same interface. For example, the balanced circuits may be used for data and timing whilst the unbalanced circuits may be used for associated control circuit functions.

2. *Recommendation V.11 interworking with Recommendation V.10*

The basic differential receiver specifications of Recommendations V.10 and V.11 are electrically identical. It is therefore possible to interconnect an equipment using Recommendation V.10 receivers and generators on one side of the interface with an equipment using Recommendation V.11 generators and receivers on the other side of the interface. Such interconnection would result in the interchange circuits according to Recommendation V.11 in one direction and interchange circuits according to Recommendation V.10 in the other direction. Where such interworking is contemplated, the following technical considerations must be taken into account:

2.1 Interconnecting cable lengths are limited by performance of the circuits working to the Recommendation V.10 side of the interface.

2.2 The optional cable termination resistance (Z_t), if implemented, in the equipment using Recommendation V.11 must be removed.

3. *Recommendation V.11 interworking with Recommendation V.35*

Equipment having interchange circuits according to Recommendation V.11 is not intended for interworking with equipment having interchange circuits according to electrical characteristics of Recommendation V.35.

ANNEX 3

(to Recommendation V.11)

Multipoint operation

It is considered that further study is required before parameters for this application can be precisely defined and this Annex, giving provisional figures, is intended as a guideline for this study.

1. *General*

The point-to-point interchange circuit arrangement of one generator and one load might be expanded to a multipoint arrangement by adding generators, receivers or both, at interchange points along the interconnecting cable, as shown in Figures 9/V.11 and 10/V.11.

Only one generator at a given time would present its differential voltage at its interchange point. All other generators would be isolated by an appropriate control, and assume the high impedance state defined below. All receivers would be continuously in an operating condition.

In multipoint configuration, one or more terminators might be required at the cable end or at interchange points, depending on the application. The combined load impedance presented to any active generator by other generators, receivers, cable and terminators, must not be less than 100 ohms.

The operation of a multipoint arrangement must not be perturbed by any of its components when they are either in a high impedance state or a power-off state [6]. The generators and receivers must tolerate without damage the transmitted signals with their maximum amplitude within the specified limits.

Generators on the same multipoint line must have the same nominal d.c. offset voltage in order to operate correctly. However, generators with different d.c. offsets could be used on the same line provided that these differences be compensated at the common reference point.

2. *Configurations*

Several topological arrangements are to be considered:

- cluster of circuits at the end of a line;
- multidrop line;
- star configuration.

Figure 9/V.11 illustrates a cluster configuration. Each line should be correctly terminated at the receiving end in order to avoid reflections and leads from that point to the receivers kept as short as possible.

Figure 10/V.11 illustrates a multidrop line. The presence of several generators along the line imposes the need to terminate the line correctly at both ends to avoid reflections. The length of the tapping connections along the line must be short enough to avoid mismatching of the main line. A length corresponding to a propagation delay of 1% of the unit interval of the signals seems to be an acceptable limit for the length of the tapping connection.

This tolerable propagation delay and other configurations are to be studied further.

The guidelines on cable length given in Figure 8/V.11 of Annex 1, assuming the same environmental conditions, apply equally to multipoint arrangements. Above 1 or 2 Mbit/s, however, the environmental conditions may be more difficult to control.

---

[6] In the power-off state of any device it is assumed that the supply collapses to zero and is replaced by a very low impedance or short circuit.

3. *High impedance state*

3.1 *Static measurements*

When in the high impedance state and with test loads of 50 ohms connected between each generator output point and point C, the magnitude of the voltage V_h measured between points A and B shall not exceed 4 mV whatever the logical condition of the generator input data lead (Figure 11/V.11).

When the generator is in the high impedance state, with voltages ranging between −6 V and +6 V applied between each output point and point C, as indicated in Figure 12/V.11, the magnitude of the output leakage currents I_{xa} and I_{xb} shall not exceed 150 μA.

The same condition applies under power-off condition.

3.2 *Dynamic measurements*

During transitions of the generator output between the low impedance state and the high impedance state, the differential signal measured across a 100 ohm test load connected between the generator points A and B shall be such that the change in amplitude goes from 10% to 90% of the steady state voltage in less than 10μs.

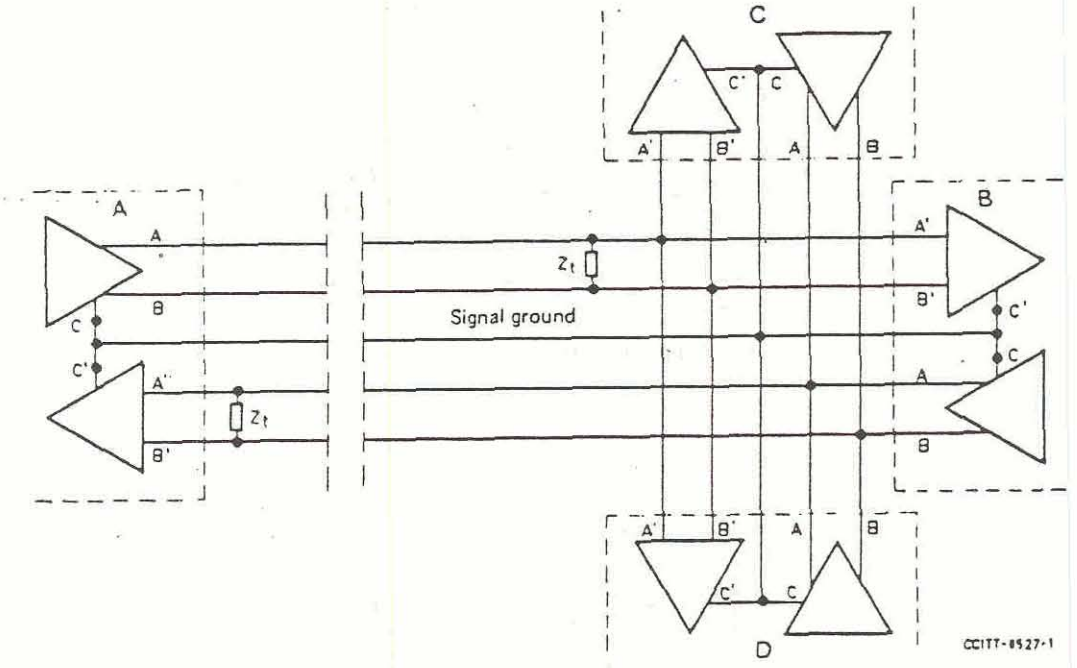


FIGURE 9/V.11 – Clustered multipoint configuration

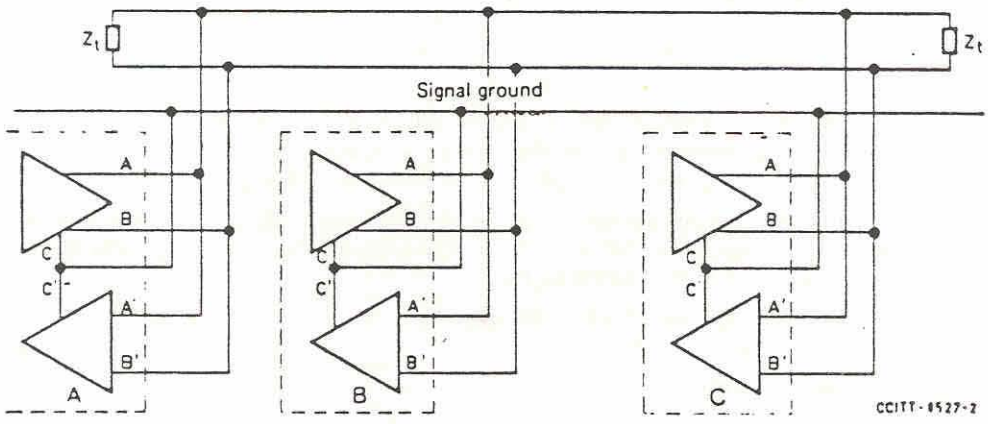


FIGURE 10/V.11 Distributed multipoint configuration

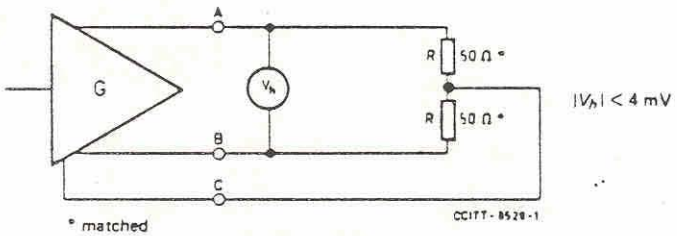


FIGURE 11/V.11 High impedance state static measurement

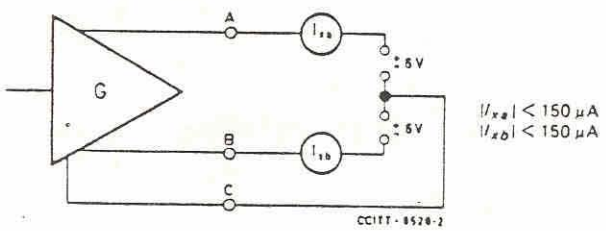


FIGURE 12/V.11 Generator output leakage current measurement

APPENDIX F

CONTENT OF DEFINED ND NUMBERS

	CRATE+	WIREWRAP			YES	YES			
	BACKWIRING	PC-BOARD	6017	6017	6017	6017			
1	STORAGE	0- 32K							1132
2		32- 64K							1132
3		64- 96K							1132
4		96-128K							1132
5		128-160K							1132
6		160-192K							1132
7		192-224K							1132
8		224-256K							1132
9	CONTROL			1144	1144	1144			
0	ADDRESS	PORT A		1142	1142	1142			
11		B					1142	1142	
12		C					1142	1142	
13		D					1142	1142	
14	DATA	PORT A		1143	1143	1143			
15		B					1143	1143	
16		C					1143	1143	
17		D					1143	1143	
18	LOG	X-Y		1145	1145	1145			
19		Y	1157						
20	DATA	PORT D					1143	1143	
21		C					1143	1143	
22		B					1143	1143	
23		A	1143		1143	1143	1143		
24	ADDRESS	PORT D					1142	1142	
25		C					1142	1142	
26		B					1142	1142	
27		A	1142		1142	1142	1142		
28	CONTROL		1144		1144	1144			
29	STORAGE	92-128K							1132
30		64- 92K							1132
31		32- 64K							1132
32		0- 32K							1132
	CONTENT OF CRATE SLOTS		ND-143 128K BANK	ND-144 256K BANK	ND-146 DUAL BANKS	ND-158 128K/32 BIT BANK	ND-145 ADD SINGLE PORT	ND-147,190 ADD DUAL PORT	ND-156 32K RAM

BANK X

BANK Y

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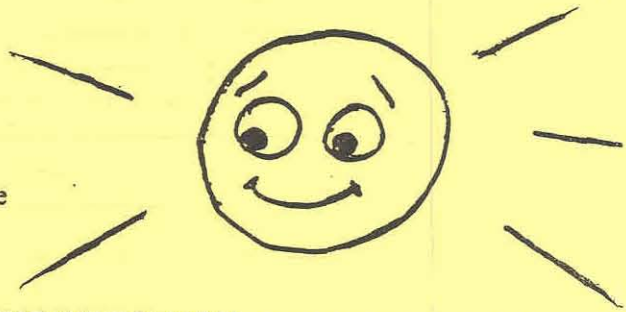

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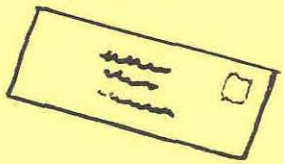

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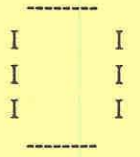
Answer from Norsk Data _____

Answered by _____ _____ _____ _____ Date _____



Norsk Data A.S.

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