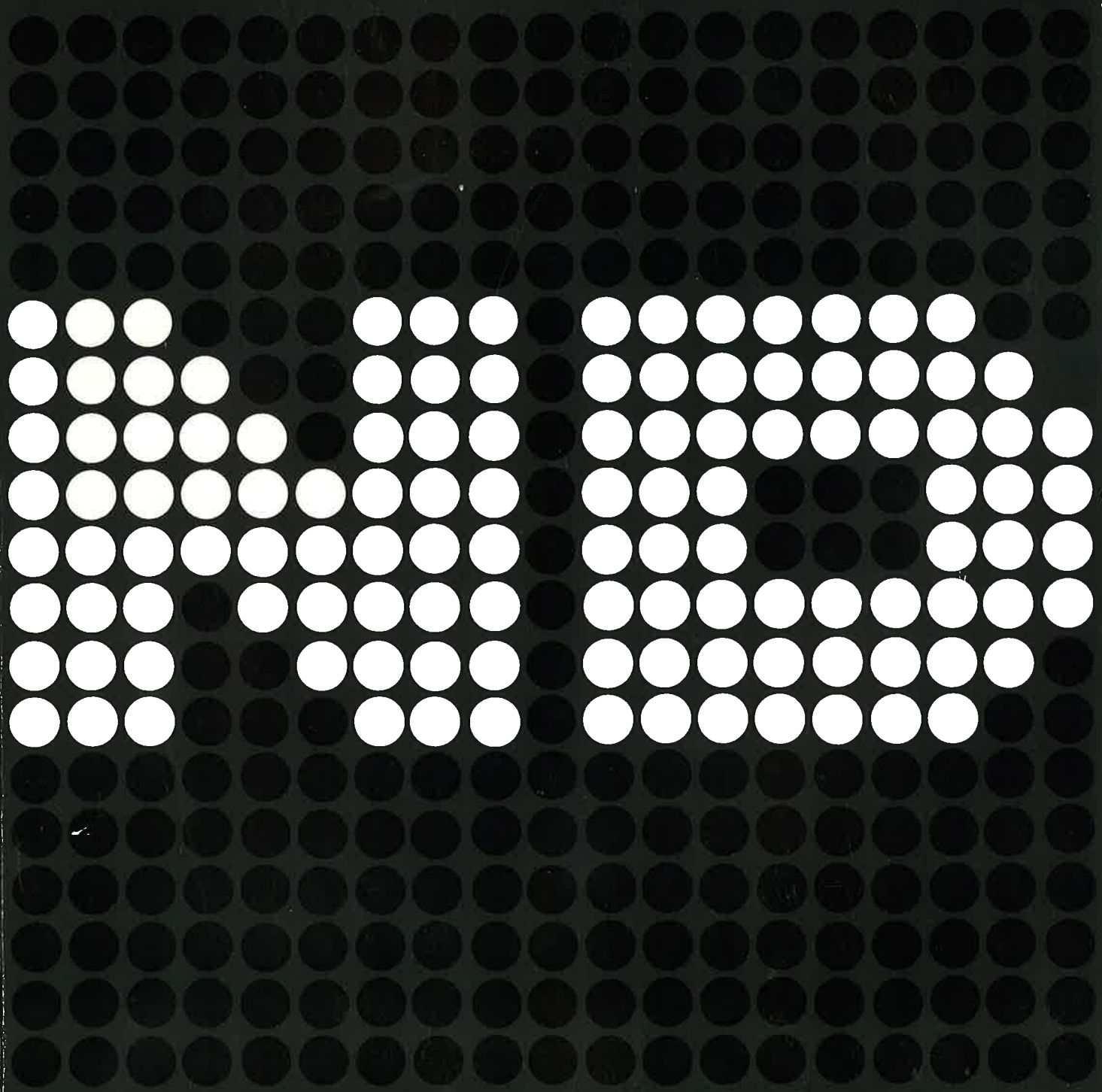
NORD-10

Input/Output System

A/S NORSK DATA-ELEKTRONIKK



NORD-10

Input/Output System

REVISION RECORD

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1 GENERAL DESCRIPTION

The NORD-10 I/O system consists of two different I/O systems. One compatible with the NORD-1 I/O controlled by the IOT-instruction (160000) and a new system controlled by the IOX-instruction (164000). The NORD-1 I/O system is included to give old customers the ability of connecting already well-proven custom-designed equipment to a NORD-10 CPU.

Only the I/O system controlled by the IOX instruction will be covered in this manual.

In NORD-10 all I/O device interface cards are made to a common standard. The cardrack contains a prewired bus with a number of identical interface slots permitting any mix of devices without changing the backwiring and plug-panel. Device plugs are also made to a common standard.

This system permits the use of printed backplane wiring for all wiring within one cardrack. Cable connectors are plugged directly into the backplane or to front end connectors mounted on the circuit board.

Devices with interface integrated in the CPU (first card rack) can be operated via the A-register. When the I/O-system is expanded with another cardrack, all devices in the second rack may be programmed for transfer of characters (words) one by one via the A-register or for block transfer directly to memory. (Mass storage, card reader, high speed modem etc.)

An optional rack controller which permits control of the devices from two different CPU's (multi-machine environment) will also be available.

NORD-10 - General system

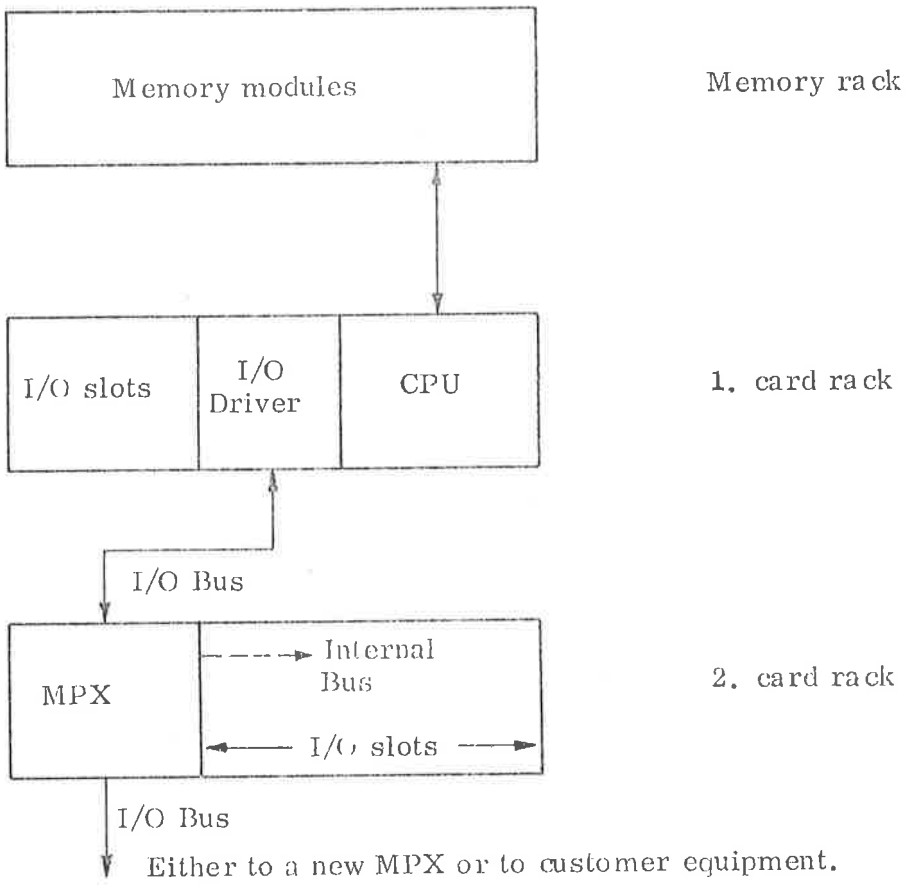


Fig. 1.

All card rack modules shown in figure 1 are 19" standard rack modules. One memory module holds up to 32K memory. The maximum size memory is 256K. The first card rack contains the CPU and ten standard I/O slots. All the main I/O operated by program control - such as consol teletype, paper tape reader, paper tape punch, card reader, lineprinter, display, operator panel, real time clock etc. - will be contained in the first rack.

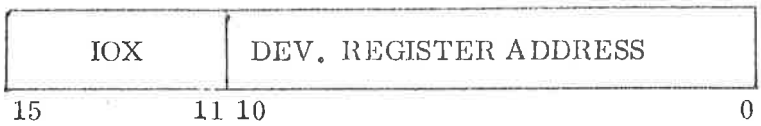
The connection between the first rack and the second rack is a general I/O Bus which will be described in detail below. The internal bus in the 2. card rack is logicly the same general I/O Bus only separated by electronic switches. Each new card rack

requires a multiplexer (MPX) that contains necessary rack buffer and control and also 16 memory address registers to be used by the local I/O devices in that rack. Thus in case of DMA transfer the individual device need not supply the memory address as this is integrated in the MPX.

The position of the device interface in the card rack determines the interrupt priority of the device. If several devices within one rack are connected to the same interrupt level, the device closest to the MPX has the highest priority within that level. Also if two devices in the same card rack competes for a Direct Memory Access - the device closest to the MPX has the highest priority and will win.

2 IOX-INSTRUCTION

All program controlled transfer between the CPU A-register and external devices is controlled by using the IOX-instruction. The IOX-instruction is loaded into the instruction register IR of the CPU, which in turn generates the I/O timing and enables the selection of the approriate device. The IOX-instruction has the following format:



IR:

Bit 15-11: IOX instruction = Octal value 164000

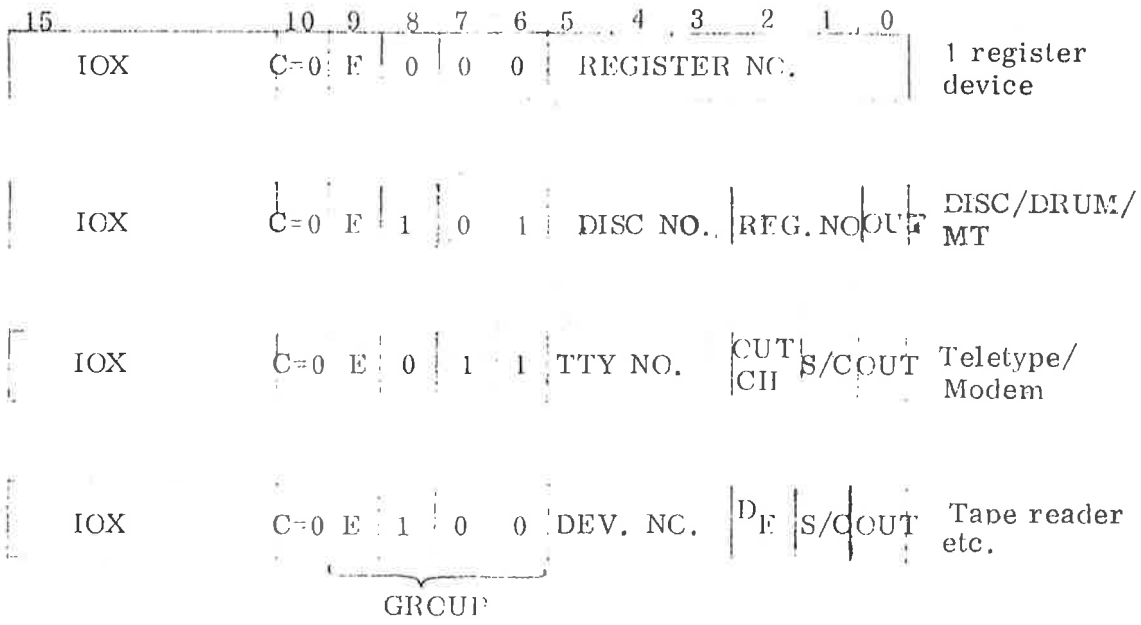
Bit 10-0: 11 bits define the different device register addresses. A maximum of 2^{11} i.e. 2048 register addresses may be specified.

The 2048 register addresses define an upper limit to the number of registers that may be addressed - some registers may require two register addresses, one for reading and one for loading. Different devices will, however, require different number of device addresses. Thus the maximum number of physical devices that may be connected will depend upon the specific configuration of devices.

Simple devices will usually require at least three different instructions (addresses), load status / control register, read status / control register and read or write data buffer register. More complex devices like magnetic tape units may need up to 8 instructions. Instructions for one and the same device are assigned successive device register addresses.

2.1 Recommended Device Addresses

Device address used for A/S Norsk Data-Elektronikk produced equipment on a standard I/O bus follows a preset assignment. The format for the different groups of devices is as follows:



C = 0	ND produced equipment
C = 1	Customer produced equipment
E =	extension
Group:	
0 (10)	Directly controlled registers
1 (11)	Modem (spare for group 2 & 3)
2 (12)	Alfanumeric display (spare for group 1 & 3)
3 (13)	Teletype (spare for group 1 & 2)
4 (14)	Paper tape etc.
5 (15)	Mass storage devices
6 (16)	Plotter, Intercore or other DMA-device
7 (17)	Miscellaneous (not exclusive, i.e. same number may be used for different device)

DISC NO.:

0	DISC I	(4 units)
1	DISC II	(4 units)
2	Mag. tape I	(4 units)
3	Mag. tape II	(4 units)
4	Drum I	(1 unit)
5	Drum II	(1 unit)
6	Drum III	(1 unit)
7	Drum IV	(1 unit)

REG. NO.: Different registers within the mass memory control.

0	Core address register
1	Sector-block address register
2	Status-control register
3	Word count register

OUT CH = 1	Output channel	} full duplex TTY
OUT CH = 0	Input channel	
S/C = 1	Status or control register	
S/C = 0	Data register	
OUT = 1	Output	
OUT = 0	Input	

3 EXTERNAL INTERRUPT IDENTIFICATION

The NORD-10 has a multiprogram system based on a 16 level priority interrupt system. Each program level has a complete set of registers. Out of these 16 levels five different levels are available to external devices. These levels are:

15		reserved extremely fast user I/O
13	}	Normal external
12	}	devices
11	}	
10	}	

Several different interrupt sources may be connected to the interrupt levels 10, 11, 12 and 13.

To identify which device is interrupting a "who are you" type of instruction is used. This returns an 8 bit identification number from the interrupting device to the A-register. The instruction is called

IDENT

and belongs to the MIS-group of instructions.

Each physical device is given a unique interrupt identification number. These numbers will range from zero to 255. There is no functional correspondance between these numbers and the device register addresses used to control the devices. - Each device uses only one interrupt identification number while it may use several register addresses.

For level 15, which is exclusively reserved user I/O, there is no identification system, and interrupt identification is obtained by reading a status wor

The detailed description of the function of the IDENT instruction is given in the section INTERRUPT HANDLING.

4 I/O BUS ARCITECTURE

The general layout of the I/O Bus System is shown in figure 2. One of the important features with this structure is the electronic separation of the bus in each branch point such as the I/O Multiplexer and the I/O Driver.

At the I/O Driver there are provisions to manually disconnect either the external I/O bus or the internal CPU I/O bus or both. If an external device by malfunctioning is jamming the bus, the ability to disconnect the external bus at the I/O driver will allow the CPU and its local devices to operate. If an internal device by malfunctioning is jamming the local CPU I/O bus it will be possible to run a memory check program with the internal bus disconnected - thus verifying the origin of the error.

Furthermore within each Multiplexer there are provisions to protect the system from being influenced by malfunctioning devices. This is done by giving each Multiplexer the possibility to disconnect the busses branched from the Multiplexer by program control.

One device register is reserved for this purpose in each Multiplexer. Two of the bits in this register will define which of the busses to disconnect, the internal bus controlled by the Multiplexer or the external bus branching off to a lower priority Multiplexer or to customer devices.

I/O BUS ARCHITECTURE

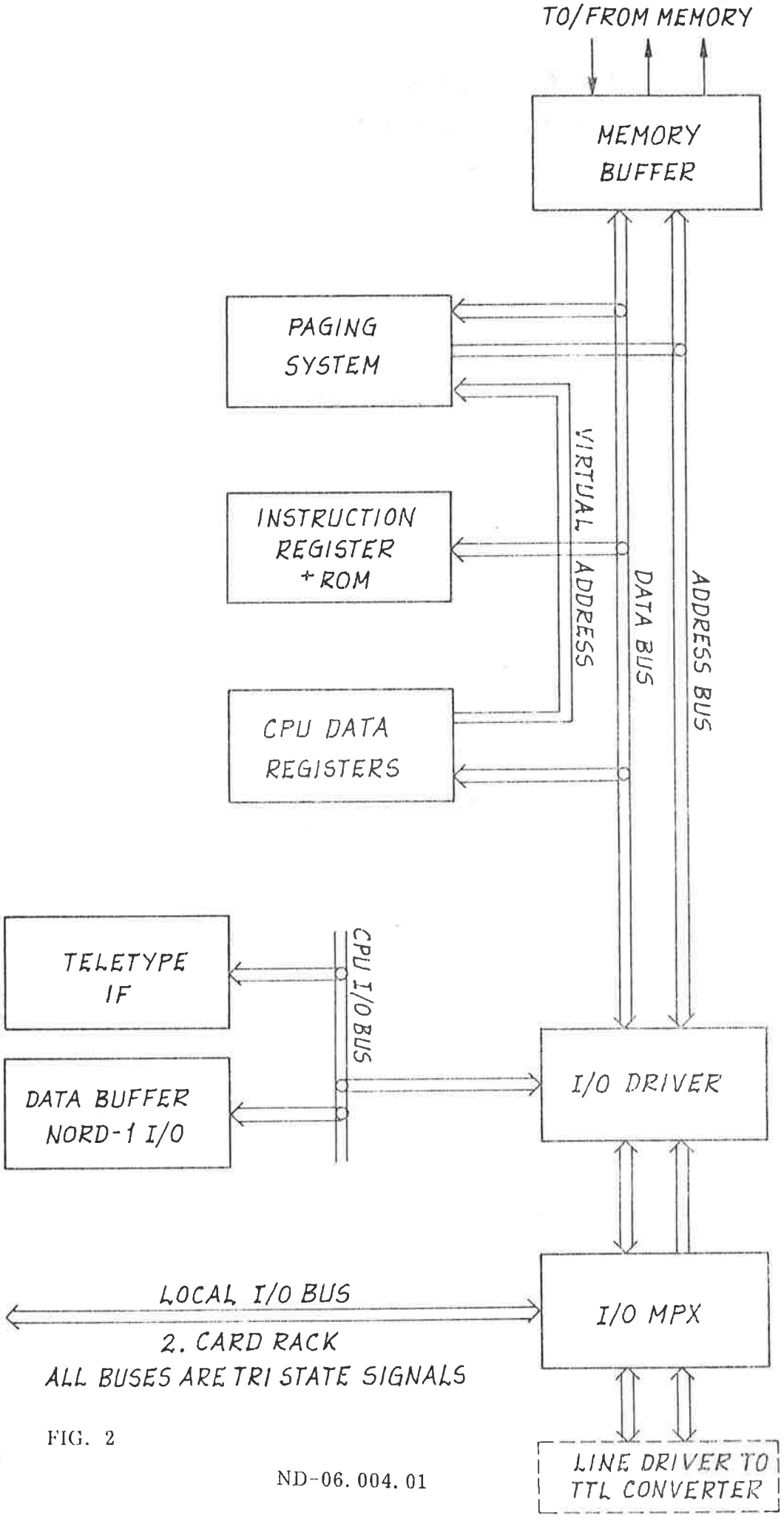


FIG. 2

5 I/O BUS SIGNALS

Table 5.1 lists the different signals on the I/O Bus:

NO. OF LINES	NAME	SOURCE		
		MEMORY BUFFER	CPU	DEVICE
16	DATA	x	x	x
18	ADDRESS		x	x
5	* INTERRUPT			x
1	IOXE		x	
1	CONNECT			x
1	INIDENT		x	x
1	OUTIDENT			x
1	INPUT			x
1	INGRANT			x
1	OUTGRANT			x
1	* DMA REQUEST			x
1	DMA DATA READY	x		
1	MPX ADDRESS			x
1	MASTER CLEAR		x	

Table 5.1

* These lines are open collector signals in the internal bus, as several sources may oporate these lines simultaneously. The rest of the signals are generated by tri-state logic.

6 PROGRAMMED INPUT/OUTPUT

6.1 Bus Signals

The following signals on the I/O Bus are relevant for programmed input/output:

DATA

ADDRESS

IOXE

CONNECT

INPUT

MASTER CLEAR

16 DATA Source: Device or CPU	16 lines carrying the data information from the CPU or from the device depending upon the control signal INPUT.
16 ADDRESS Source: CPU	Bit 0-10: Gives the value of the 11 least significant bits of the CPU instruction register, i.e. the device register address during an IOX-instruction.
Source: Device	Bit 11-14: These bits are used only for loading a core address into the corresponding register in the Multiplexer, and selects one of sixteen registers.
Source: Device	Bit 15: A strobe pulse for the specific MPX core address register if the same conditions as for ADDRESS bits 11-14 above are true.
1 IOXE Source: MPX	IOX enabling time signal, acts as a master enable signal during the relevant IOX instructions. This signal is defined as $(IOXE_{CPU} \cdot IR\ 10_X)$ X = 0 or 1 depends on a strapping in the MPX.
1 CONNECT Source: Device	A device answer on the IOXE signal indicating that the IOXE signal has been received and that the device has decoded the ADDRESS bits 0-10 and recognized one of its device register addresses. CONNECT has to be returned within a specified time (max 5 μs) otherwise the CPU will generate an internal interrupt on level 14.

1 INPUT Source: Device	Defines the direction of the data lines. INPUT true; data transferred from device to CPU A-register. INPUT false; data transferred from CPU A-register to device.
1 MASTER CLEAR Source: CPU	Used to clear the logic in the device controllers.

6.2 Data Transfer

A programmed data transfer on the I/O Bus is initiated as follows:

The IOXE signal together with the ADDRESS bits 0-10 connects a specific device to the bus. This is confirmed by the device by returning the CONNECT signal. The type of transfer depends upon the control signals INPUT.

6.2.1 Input

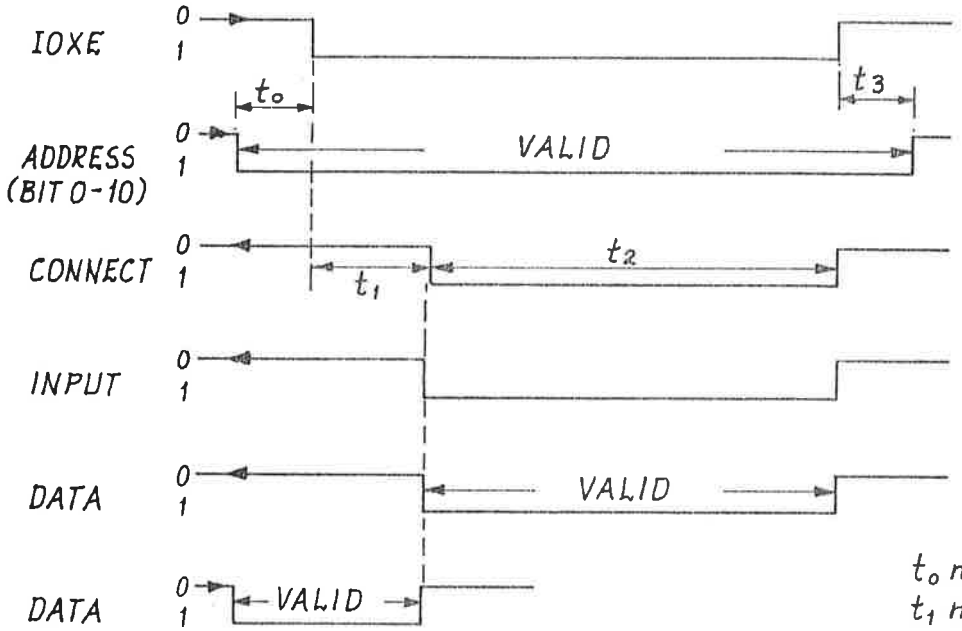
If the transfer is an input transfer i.e. data transferred from the device to the CPU, the device will together with returning the CONNECT signal also return the INPUT control signal and enable data on the DATA lines. The DATA lines has to remain stable during the rest of the IOXE signal. As soon as the IOXE signal drops, the CONNECT and INPUT signal have to be dropped. The timing sequence is shown in figure 3.

As shown in the figure it may be possible to perform both an output and an input transfer on the same IOXE. This is done by delaying the CONNECT and INPUT signal until the DATA from the CPU has been strobed by the device.

6.2.2 Output

After receiving the IOXE signal as for input, the data from the CPU may be strobed into a device register. This strobe pulse could be identical to the CONNECT signal. The timing sequence is shown in figure 4.

PROGRAMMED INPUT FROM DEVICE



t_0 min. 200 ns
t_1 min = 0
t_1 max = 5 µs
t_2 ≈ 200 ns
t_3 min. 200 ns
t_4 min. 100 ns
t_4 max. = CONNECT

Fig. 3

PROGRAMMED OUTPUT TO DEVICE

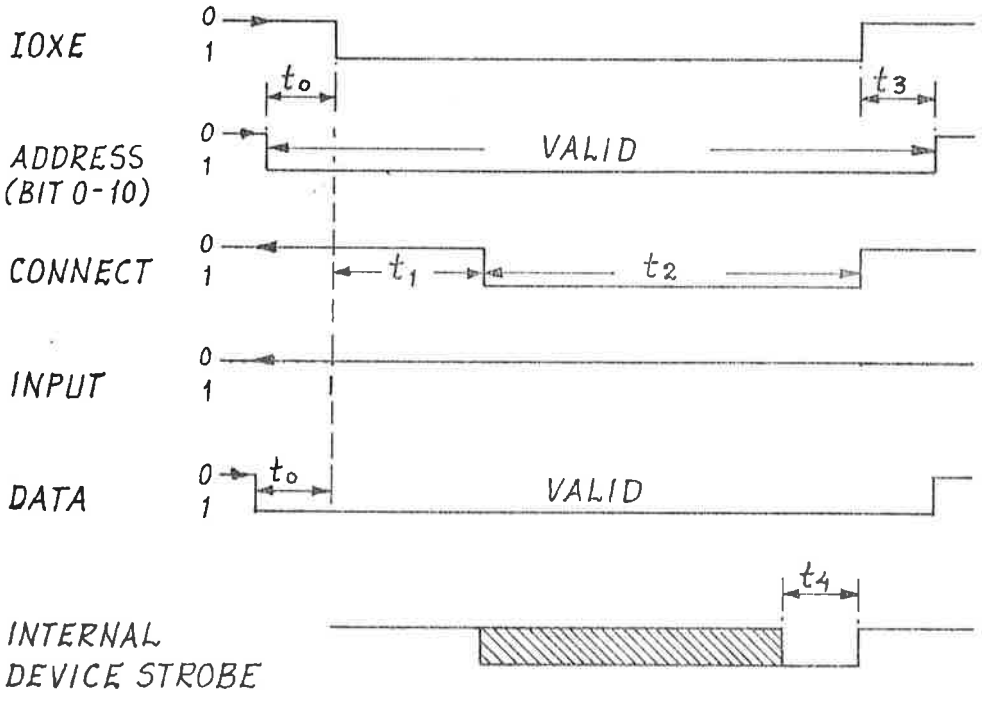


Fig. 4

→ To device

← From device

7 INTERRUPT IDENTIFICATION SEQUENCE

7.1 Bus Signals

The following signals on the I/O Bus are relevant during an interrupt sequence:

DATA

ADDRESS

INTERRUPT

INIDENT

OUTIDENT

CONNECT

INPUT

MASTER CLEAR

8 DATA
Source:
Device:

Bit 0-7: The value of these lines are equal to the specific INTERRUPT IDENTIFICATION NO. for the device. Each physical device is given a unique interrupt identification number.

6 ADDRESS
Source:
CPU

Bits 0-1: Give a coded value for the external interrupt level where the program is seeking to identify an interrupt. The code is as follows:

Bit 1 0

0 0 - Interrupt level 10

0 1 - Interrupt level 11

1 0 - Interrupt level 12

1 1 - Interrupt level 13

Source:
CPU

Bits 2-5: Give the value of the external interrupt level where the program is seeking to identify an interrupt. The code is as follows:

Bit 5432

0001 - Interrupt level 10

0010 - Interrupt level 11

0100 - Interrupt level 12

1000 - Interrupt level 13

5 INTERRUPT Source: Device	One line for each external interrupt level (10, 11, 12, 13 and 15). When the device wants the CPU attention one of these lines are grounded - set true. The level has to remain true until the device has been serviced by the IDENT instruction for the specific level.
1 INIDENT Source: CPU and device	This signal is generated at the CPU as a decoding of one of the four IDENT instructions.
1 OUTIDENT Source: Device	A signal transmitted to the next device's INIDENT pin if the device did not generate an INTERRUPT or the interrupt code did not correspond to the interrupt level of the device.
1 CONNECT Source: Device	A device answer on the INIDENT indicating that the device that gave the INTERRUPT has recognized the INIDENT and found the code for the interrupt level to correspond to the level of its specific interrupt.
1 INPUT Source: Device	A line indicating that the connected device is returning its DEVICE IDENTIFICATION NO. on the DATA lines bit 0-7.
1 MASTER CLEAR Source: CPU	Used to clear the logic in the device controllers.

7.2 Interrupt Sequence

The first device receiving the INIDENT is the first device in the interrupt priority chain. If this device gave no interrupt or the INIDENT signal was for a different level, the device will send the INIDENT signal as the OUTIDENT from this device. The next device in the priority chain will now receive this signal as its INIDENT. This daisy chaining will continue until the device that gave the interrupt recognizes the INIDENT and finds that the code for the interrupt level ADDRESS BITS 0-5 corresponds to the level for the specific device. This device will not transmit an OUTIDENT signal. The device will instead return a CONNECT and INPUT signal to the CPU.

Figure 5 illustrates the daisy chaining mechanism of the INIDENT/ OUTIDENT signals.

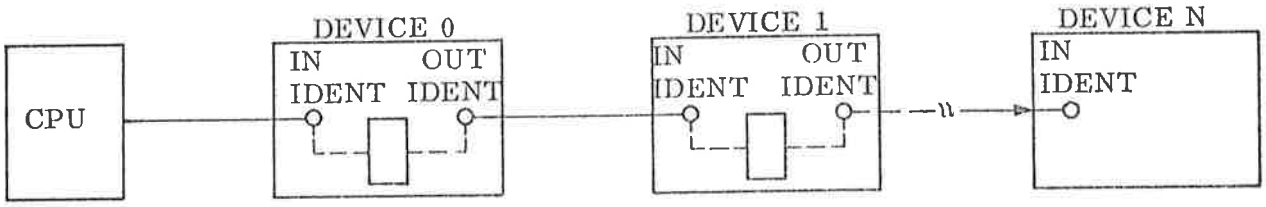
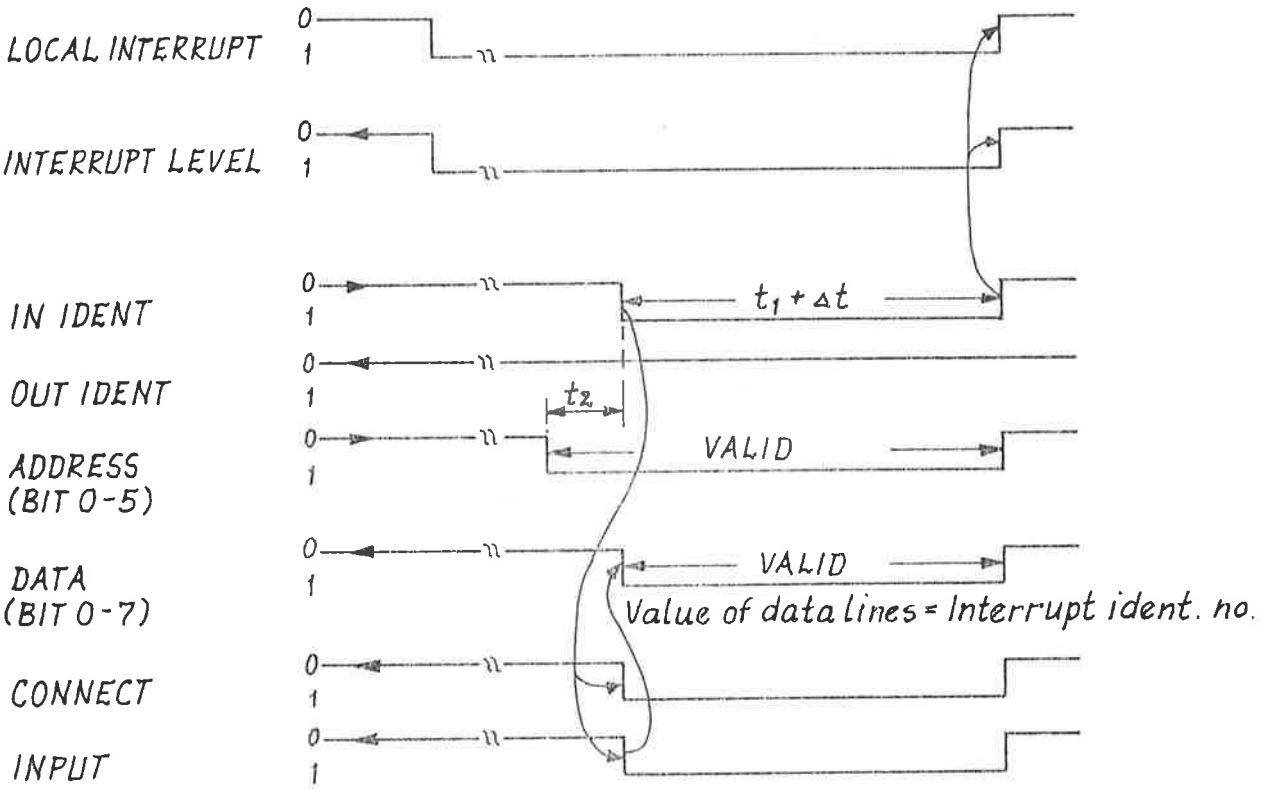


Fig. 5.

The timing diagram for the interrupt sequence of an interrupting device, is shown in figure 6. Likewise a timing diagram for a non-interrupting device is shown in figure 7.

INTERRUPT SERVICE ROUTINE FOR A DEVICE GENERATING LOCAL INTERRUPT



$t_1 \approx 200$ ns

Δt Depends upon device physical position

Δt max = max delay of gating in device controllers and max line delay.

t_2 min. 200 ns

Fig. 6

INTERRUPT SERVICE ROUTINE FOR A DEVICE WITHOUT A LOCAL INTERRUPT

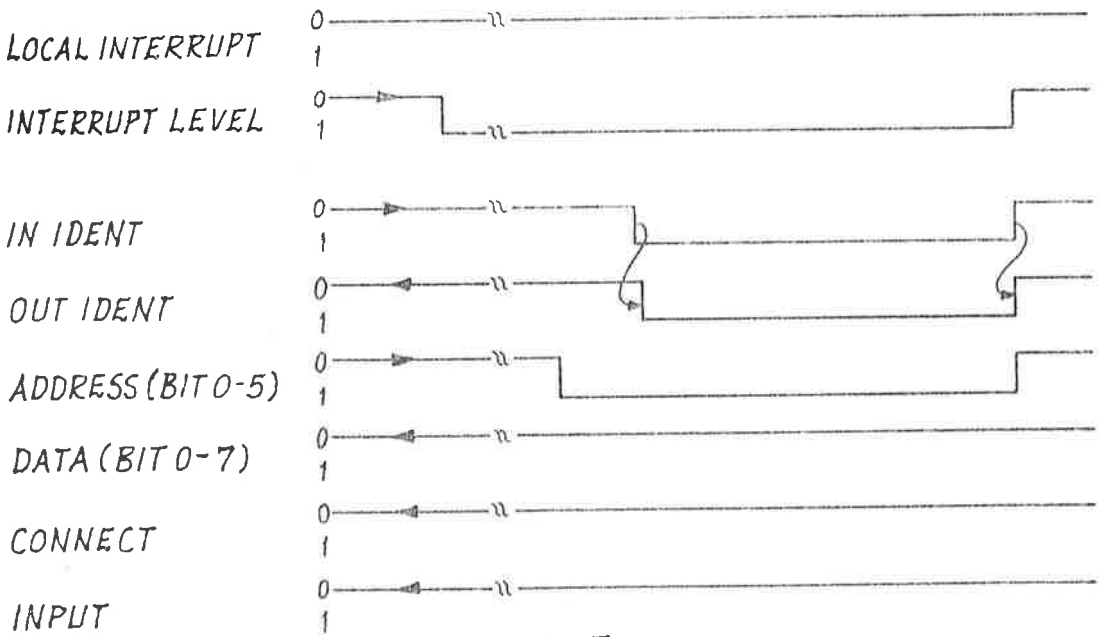


Fig. 7

8 DMA INPUT/OUTPUT

8.1 Bus Signals

The following signals on the I/O Bus are relevant for DMA input/output:

DATA

ADDRESS

INGRANT

OUTGRANT

DMA REQUEST

CONNECT

DMA DATA READY

MPX ADDRESS

INPUT

MASTER CLEAR

16 DATA Source: Device or memory	16 lines carrying the data information from the memory or from the device. Direction depends upon the control signal INPUT.
18 ADDRESS Source: Device	These lines have different meaning depending on the control signal MPX ADDRESS. MPX ADDRESS: true. Bit 11-14: Gives the address of the specific core address register within the Multiplexer. I.e., if a DMA device uses core address register 15, the address bits 11-14 should all be true (1111)=15 when DMA REQUEST is sent to the memory. MPX ADDRESS: false. Bit 0-15: Gives the memory address for the DMA transfer within one 64K memory block. Bit 16-17: Gives the memory block address, i.e., if more than 64K memory is used only one out of four memory blocks of 64K can be specified from a device within a complete data transfer. Thus ADDRESS bit 16-17 will remain static during the complete transfer while ADDRESS bit 0-15 will be counting per word.

1 INPUT Source: Device	A control signal indicating whether the request is for input or for output.
1 CONNECT Source: Device	A signal confirming receipt of INGRANT, and that address and data are enabled onto the bus.
1 INGRANT Source: MPX and device	This signal is generated at the MPX as a response to a DMA REQUEST and indicates that the device receiving this signal is granted the I/O Bus.
1 OUTGRANT Source: Device	A signal transmitted to the next device's INGRANT pin if the transmitting device did not generate a REQUEST.
1 DMA REQUEST Source: Device	A request for receiving the I/O Bus for a DMA transfer.
1 DMA DATA READY Source: Memory buffer	A control signal from the memory. This signal indicates that the DATA lines may be strobed in case of OUTPUT. (The ADDRESS to the memory buffer may also be changed after receiving this signal.)
1 MPX ADDRESS Source: Device	A control signal indicating whether the device is using a MPX core address register.
1 MASTER CLEAR Source: CPU	Used to clear the logic in the device controllers.

8.2 Data Transfer

A DMA data transfer on the I/O Bus is initiated as follows:

A device indicates that a DMA transfer is wanted by generating the DMA REQUEST signal. The MPX will then return an INGRANT signal to the device as soon as the I/O Bus is free. The first device to receive the INGRANT signal is the first device in the DMA priority chain. If this device did not generate the DMA REQUEST, it will transmit the INGRANT signal as the OUTGRANT signal from this device. The daisy chaining mechanism for the INGRANT/OUTGRANT signal is identical to the one for INIDENT/OUTIDENT as described in the section Interrupt Sequence.

8.2.1 DMA Output

After a DMA REQUEST has been placed on the bus the device is waiting for an INGRANT signal. As soon as this is received (the delay depends upon where the device is positioned in the priority chain) it is used as an enabling signal for the ADDRESS, MPX ADDRESS and CONNECT.

A device with a REQUEST to be processed, will inhibit the sending of the OUTGRANT signal.

If the device is using one of the MPX core address registers, the ADDRESS bits 11-14 have to be enabled, giving the address of this register.

If the device is using its own core address register, the ADDRESS bits 0-17 gives the memory address from where the data word is fetched.

The device will then receive a DMA DATA READY signal from the Memory Buffer indicating that the DATA bits 0-15 are valid and may be strobed.

The leading edge of the DMA DATA READY signal should be used for clocking of the local data buffer register.

Once the DMA DATA READY has been received the memory address need not be valid any more, thus the MPX may use this signal as an increment pulse for the core address register of the device. (The trailing edge of CONNECT may also be used.)

The timing sequence for DMA output is shown in figure 8 and figure 9.

DMA OUTPUT TO DEVICE USING MPX CORE ADDRESS REGISTER

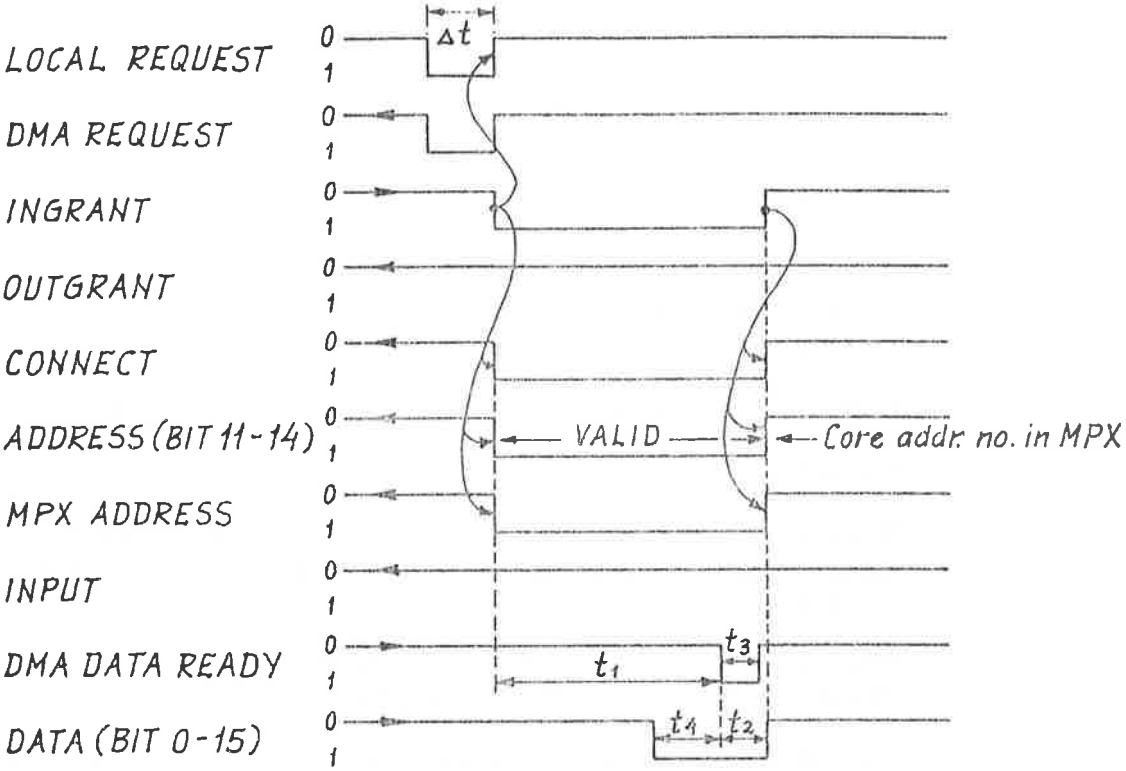


Fig. 8

→ to device

← from device

$0 < \Delta t \lesssim \Delta t_{max}$

Δt_{max} increases with DMA and I/O load

$t_{access} + 200\,ns < t_1 \lesssim t_{cycle} + 200\,ns$

$20\,ns < t_2 \lesssim 100\,ns$

$t_3 \approx 100\,ns$

$25\,ns < t_4 \lesssim 200\,ns$

DMA OUTPUT TO DEVICE USING LOCAL CORE ADDRESS REGISTER

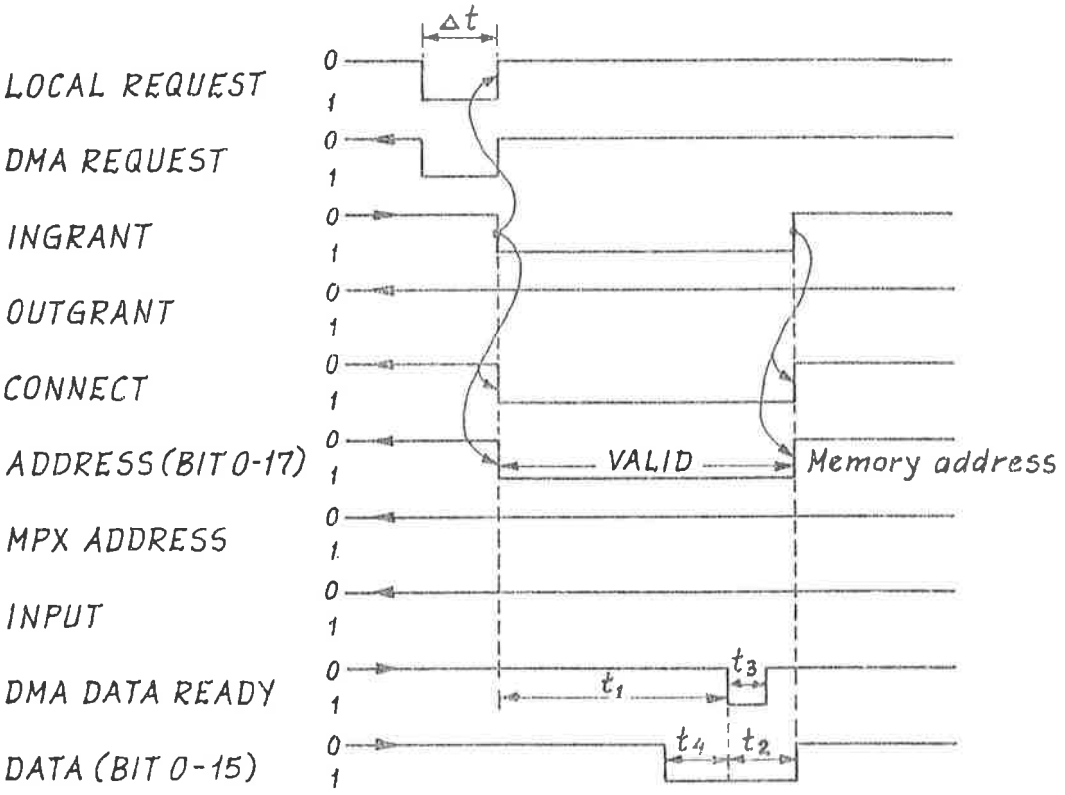


Fig. 9

8.2.2 DMA Input

The device having placed a DMA REQUEST on the line will wait for the INGRANT signal. This is used as an enable signal for the MPX ADDRESS, ADDRESS, DATA, INPUT and CONNECT signals.

If the device is using one of the MPX core address registers, ADDRESS bits 11-14 have to be enabled giving the address of this register.

If the device is using its own core address register, the ADDRESS bits 0-17 give the Memory Address to where the data word is transferred.

When the INGRANT signal is turned off, address and data have been strobed into the Memory Buffer, and should be disabled.

The timing sequence for a DMA output is shown in figure 10.

8.3 DMA Sequence for a Device that has not generated a Request

If a device of lower priority has generated a DMA REQUEST, the higher priority devices have to be active during the DMA sequence. The higher priority devices have to transmit the INGRANT signal to the OUTGRANT signal so that the device requesting a DMA sequence will receive an INGRANT signal. This daisy chaining mechanism is the same as shown for interrupt in figure 5.

The timing sequence for the DMA daisy chaining is shown in figure 11.

DMA INPUT FROM DEVICE USING LOCAL CORE ADDRESS REGISTER

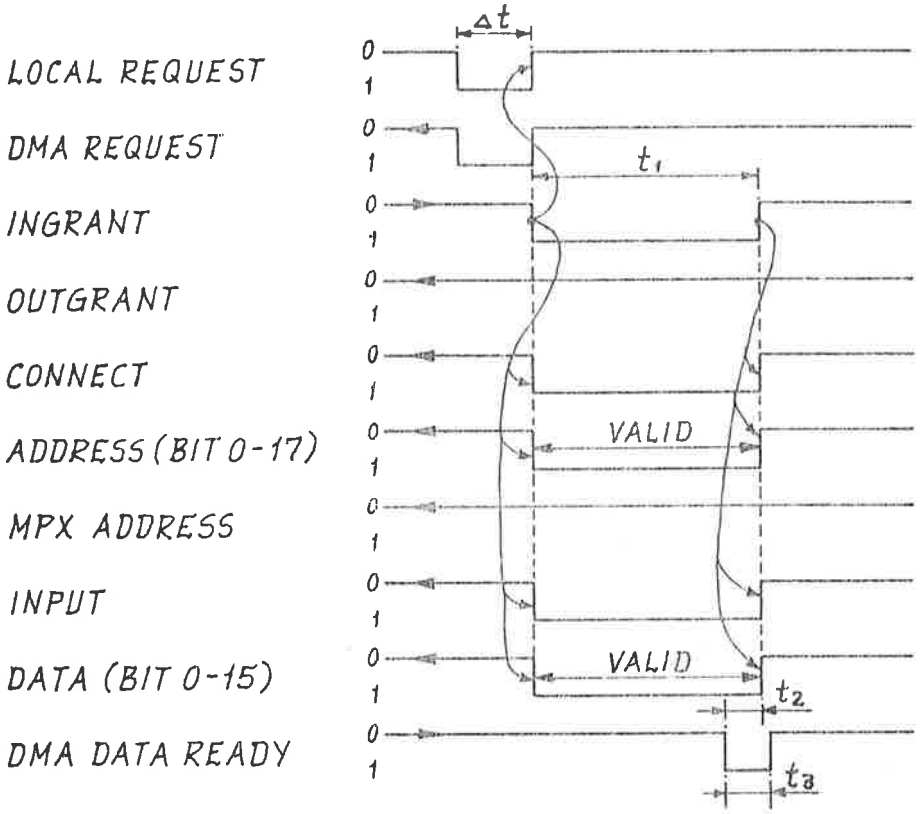


Fig. 10

$0 < \Delta t \lesssim \Delta t_{max}$
Δt_{max} increases with DMA and I/O load
$300\,ns < t_1 \lesssim t_{cycle} + 200\,ns$
$20\,ns < t_2 \lesssim 100\,ns$, $t_3 \approx 100\,ns$

DMA SERVICE ROUTINE FOR A DEVICE NOT GIVING LOCAL REQUEST

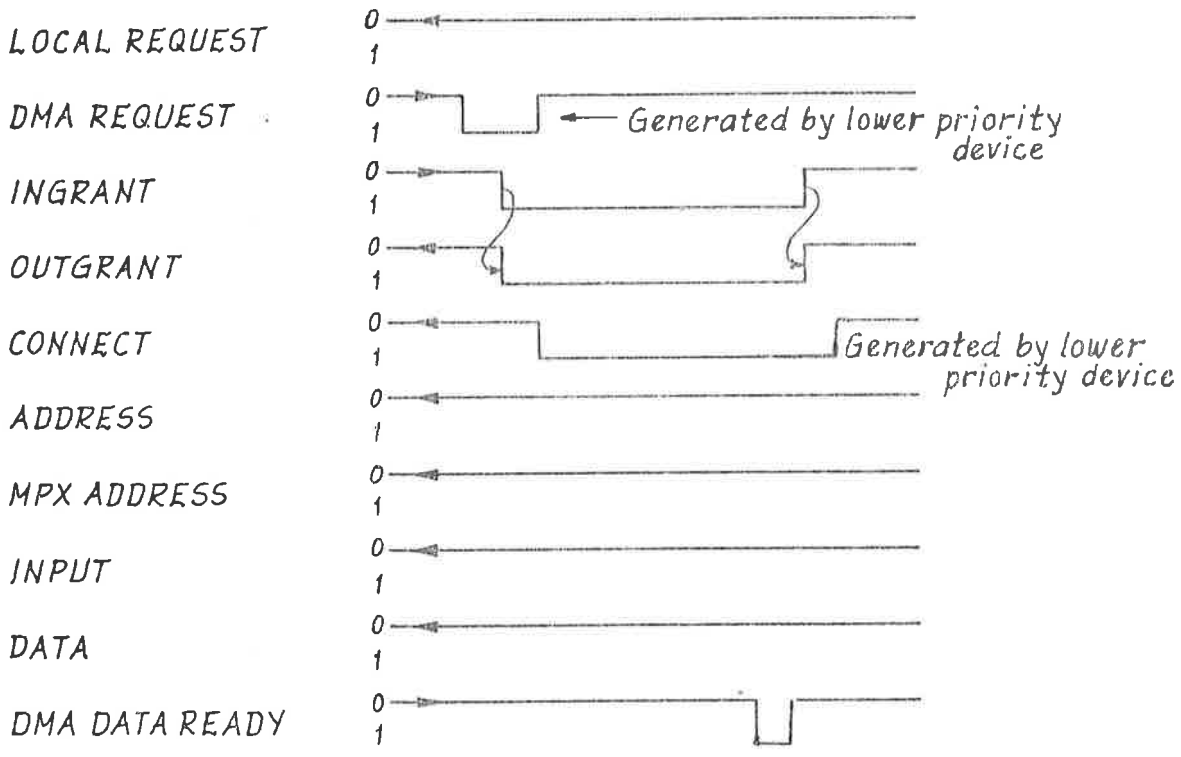


Fig. 11

9 TECHNICAL SPECIFICATIONS

9.1 Cables

Three cables are used for I/O connections outside the CPU-cabinet, one each for data, address and control. Each cable has 20 twisted pairs, with 120Ω impedance.

9.2 Signal Levels

Internal I/O Bus signals are TRI-STATE TTL for all signals except interrupt lines and DMA request line, which are open collector TTL.

Logical "1" signal: $0 \leq S \leq 0,4V$

Logical "0" signal: $2,4 \leq S \leq 5V$

The drive (sink) capability of each driver should be 30 mA.

The load on each input terminal should not be more than 0,1 mA in high state and 1,6 mA in low state. External I/O Bus signals supplied on cables are twisted pair differential line drivers/receivers using the DM 8820/8831 or equivalent.

9.3 Card Module Specifications

9.3.1 General Description

The modules are a 100-terminal edge connector with contact fingers on 0.1" grid.

The module board dimensions relevant to its mounting in card-frame are given in figure 12 page 9-2.

The contact area of the module is specific, based on use with a 50 + 50 terminal connector with 0.1" spacing, symmetrically located relative to the board centerline.

There are a number of 100-pin connectors available, differing only slightly in mechanical dimensions. Only the corner cut-outs of the board need special adaption to the connector selected. As a secondary standardization a BURNDY connector has been shoosen, and the specific board dimension are given in the tables.

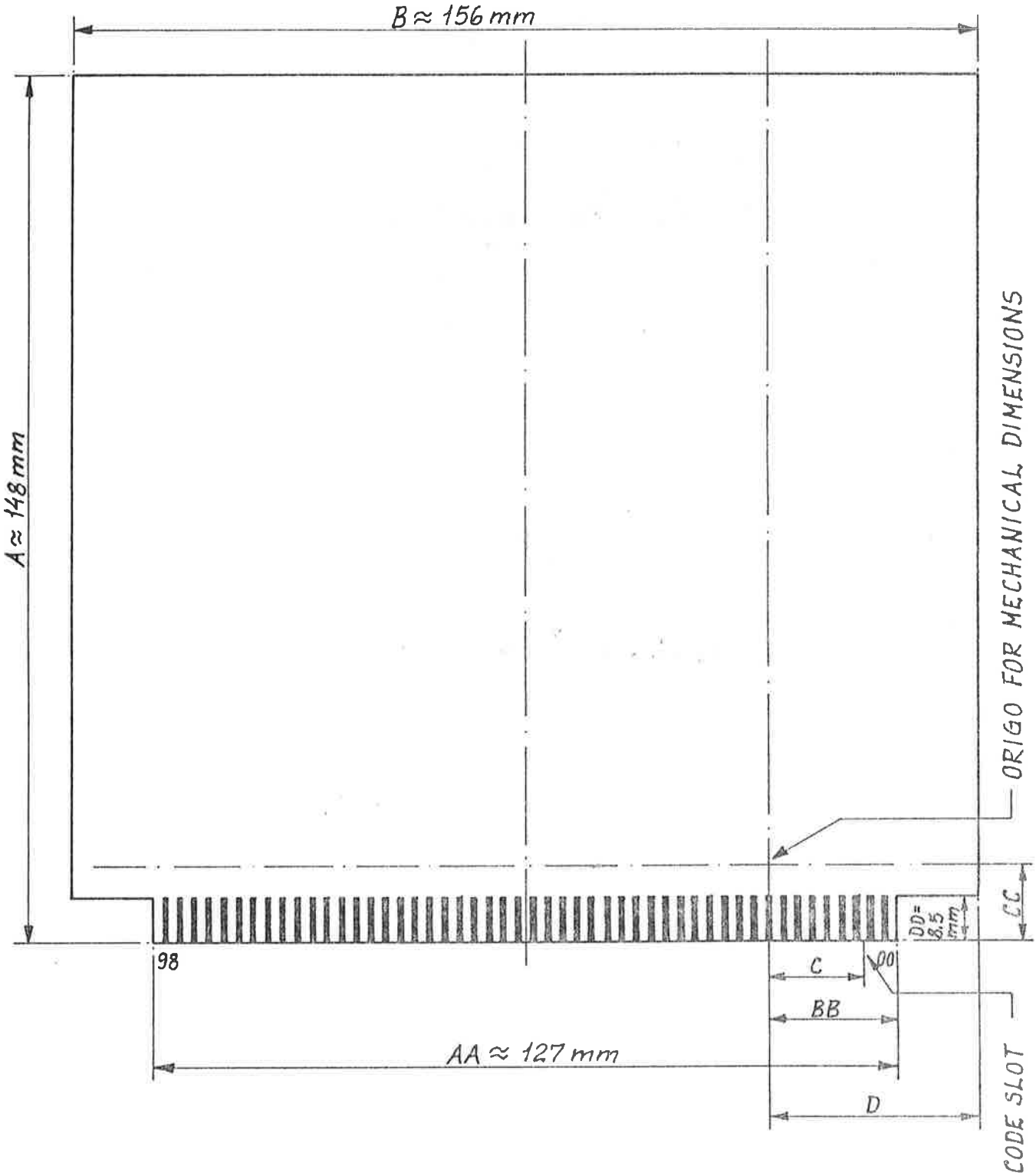

B ≈ 156 mm
A ≈ 148 mm
ORIGO FOR MECHANICAL DIMENSIONS
CC
DD= 8.5 mm
98
C
00
BB
AA ≈ 127 mm
D
CODE SLOT

Fig. 12

A = 148.2 ± 0.3mm

B = 156.2 ± 0.2mm

C = 16.51 ± 0.1mm (to centerline of code slot)

D = 36.19 ± 0.1mm

Contact finger width: 50 mil (1.27 ± 0.1mm)

Distance between fingers: 50 mil (1.27 ± 0.1mm)

Board thickness: nom. 1.6mm, 1.5 - 1.8mm incl. finishes to 3mm from edge.

9.3.2 Connector Standards

Specific to modules for use with connector: BURNDY PCBD 50 M10 GE00.

AA = 127.32 ± 0.15mm

BB = 21.76 ± 0.1mm

CC = 13.6 ± 0.2mm

DD = 8.5 ± 0.2mm

Code slot depth: 8.5 ± 0.5mm

Code slot width: 1.0 ± 0.1mm

9.3.3 Mounting Standards

Heigths of finished mounted modules is given in figure 13.

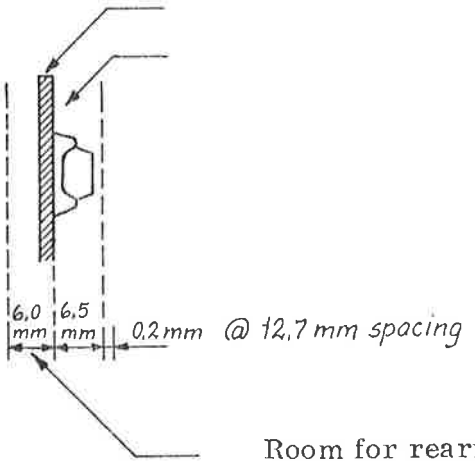


Fig. 13.

Modules with larger components will require two slots in the I/O rack.

		Terminal no.
ADDRESS BIT	15	52
	16	53
	17	54
OUTIDENT		6
INIDENT		7
OUTGRANT		8
INGRANT		9
IOXE		11
INPUT		15
MPX ADDRESS		19
CONNECT		23
INTERRUPT LEVEL 10		27
INTERRUPT LEVEL 11		31
INTERRUPT LEVEL 12		35
INTERRUPT LEVEL 13		39
INTERRUPT LEVEL 15		43
DMA REQUEST		47
DMA DATA READY		51
MASTER CLEAR		55
DEVICE CONNECTIONS		56 - 95
+5V		0, 1, 98, 99
GROUND		2, 3, 96, 97
BFQ1	19,2 khz	4
BFQ2	307,2 khz	5

10 SIGNAL DISTRIBUTION WITHIN ONE CARD RACK

		Terminal no.
DATA BIT	0	10
" "	1	12
" "	2	13
" "	3	14
" "	4	16
" "	5	17
" "	6	18
" "	7	20
" "	8	21
" "	9	22
" "	10	24
" "	11	25
" "	12	26
" "	13	28
" "	14	29
" "	15	30

ADDRESS BIT	0	32
	1	33
	2	34
	3	36
	4	37
	5	38
	6	40
	7	41
	8	42
	9	44
	10	45
	11	46
	12	48
	13	49
	14	50

11 FORMAT OF STATUS AND CONTROLWORD

The format of status and controlword may be assigned by the designer of each device controller. The following standard is used by ND for its own device control cards (when applicable) and is recommended for customer use.

11.1 Status Word

BIT		
	0	Ready for transfer, interrupt enabled
	1	Error interrupt enabled
	2	Device active
	3	Device ready for transfer
	4	Inclusive OR of errors
	5	Error indicator
	6	" "
	7	" "
	8	" "
	9	Selected unit
	10	" "
	11	Operational mode of device
	12	" " " "
	13	" " " "
	14	" " " "
	15	" " " "

11.2 Control Word

BIT		
	0	Enable interrupt on device ready for transfer
	1	Enable interrupt on errors
	2	Activate device
	3	Test mode
	4	Device clear
	5	Address bit 16
	6	Address bit 17
	7	Not assigned
	8	" "
	9	Unit select
	10	" "
	11	Device operation
	12	" "
	13	" "
	14	" "
	15	" "

NORSK DATA A.S.
Lørenvn 57 - Postboks 163, Økern
OSLO 1

COMMENT AND EVALUATION SHEET

NORD-10 Input/Output System ND-06.004.01

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM: _____

_____

_____

– we want bits of the future

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