

NORD-50
General Description
and
Module Description

NORSK DATA A.S



NORD-50

General Description and Module Description

Notes

Original Printing

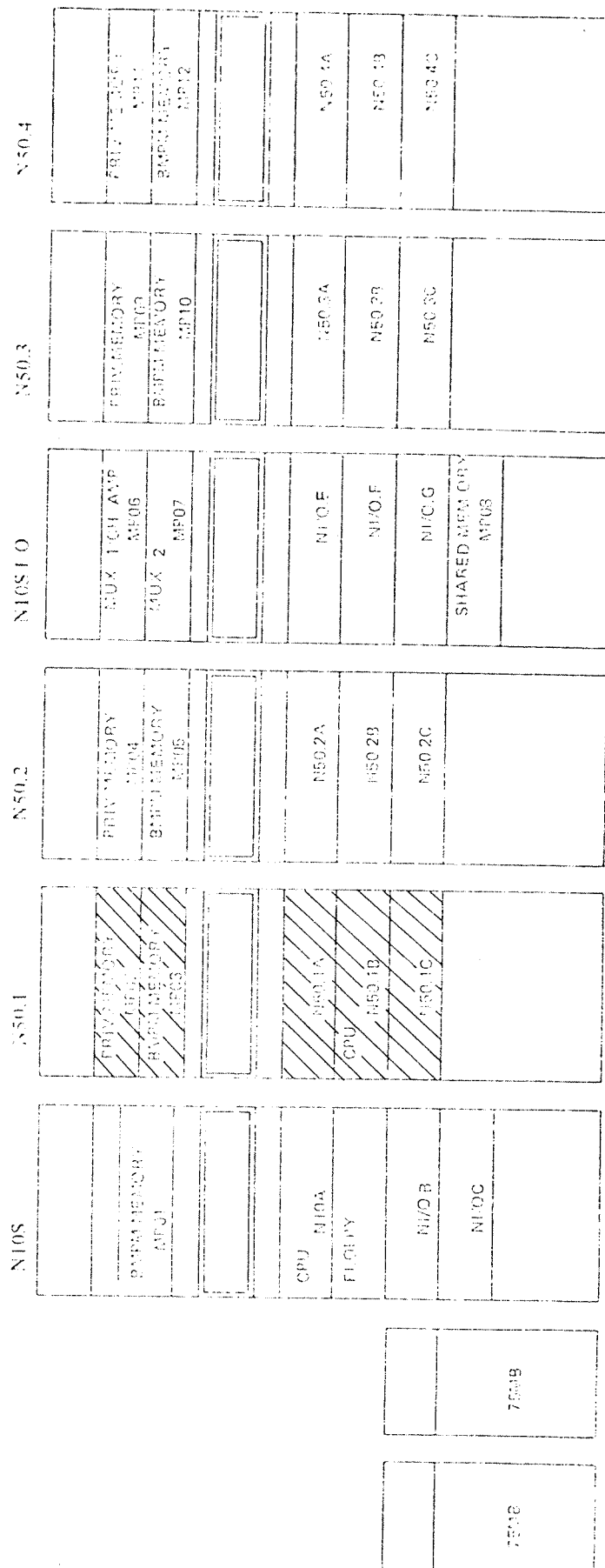
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SYSTEM CONFIGURATION F16



1

INTRODUCTION

NORD 50 is a 32 bit special purpose computer designed to be a slave processor to the general purpose NORD 10/S Computer. The maximum address space is 1024 K word (32 bits) or 4M bytes.

This memory may either be:-

- Private Memory

High speed static memory accessible only from the NORD 50.

NORD 10/S may deposit/examine instructions or data in this private memory via the NORD 10/S input/output system.

- Multiport Memory

Shared memory accessible from various sources as NORD 10/S, DMA devices and other NORD 50's via separate ports in the multiport memory system.

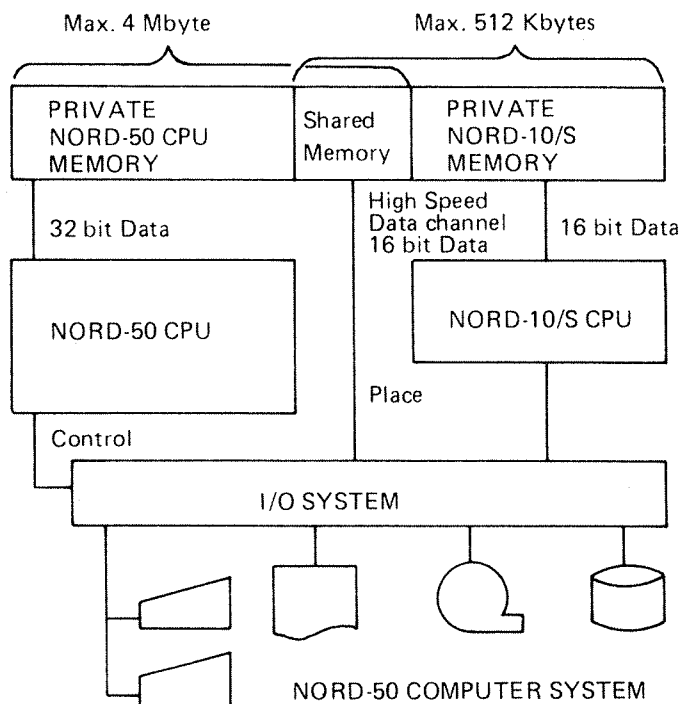


Fig. 2.1 to be inserted.

1.1 *WORD FORMAT*

In NORD 50 there is a 3 data word format:

- INTEGER WORD : 31 bits plus 1 sign bit, negative integer are represented in two complement notation.
- SINGLE PRECISION FLOATING WORD : 9 bits exponent
23 bits mantissa (fraction with hidden '1' bit).
2 bits for sign of exponent and mantissa.
- DOUBLE PRECISION FLOATING WORD : 9 bit exponent
55 bits mantissa (fraction with hidden '1' bit).
2 bits for sign of exponent and mantissa.

A double precision floating word will occupy two consecutive memory locations or two registers in the register block.

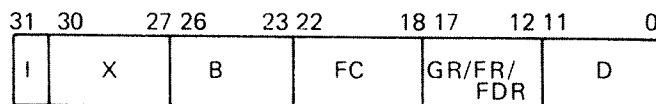
1.2 INSTRUCTION FORMATS

The instructions in the NORD-50 are always one word long. The instructions are divided into three groups:

- Memory Reference Instructions
- Inter-Register Instructions
- Argument Instructions

MEMORY REFERENCE INSTRUCTION WORD

The single precision memory reference instructions affect one memory word and one register, double precision two memory words and two registers. The memory addressing may be direct or indirect. Up to 16 levels of indirect addressing may be used. The instruction word format:

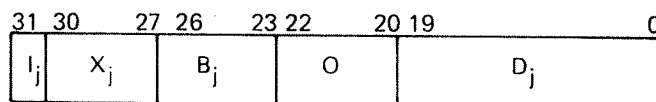


where

- I — Indirect addressing flag
- X — Index register - 1 of 16
- B — Base register - 1 of 16
- FC — Function code - 1 of 32 instructions
- GR — General register number
- FR — Single precision, floating register number
- FDR — Double precision, floating register number
- D — Displacement $0 \leq D < 4096$

MEMORY ADDRESSING

All memory reference instructions calculate an effective memory address, Ea_i (Effective address). When indirect memory addressing is specified, the indirect address word is used. The indirect address is modified by index and/or base register.



Indirect address Word - $I AW_j$ at level j .

- I_j — Indirect addressing flag at level j
- X_j — Index register for $I AW_j$
- B_j — Base register for $I AW_j$
- D_j — Displacement for $I AW_j$ $0 \leq D < 1048576$

INTER-REGISTER INSTRUCTIONS

The Inter-Register Instructions affect the central registers. The instructions specify two operand registers - source register A and source register B, together with a result register - the destination register.

The Instruction format:

31	30	27	26	23	22	19	18	12	11	6	5	0
	RFC	RSC		O		DR/DF/DFD		SRA/SRAD		SRB		

where

RFC/RSC	—	Inter-Register Instruction and subfunction code SHIFT, ARITHMETIC, TEST and SKIP, LOGICAL OPERATIONS, MISCELLANEOUS OPERATIONS
DR	—	Destination Register
DF	—	Destination Floating Register
DFD	—	Destination Double Precision Floating Register
SRA	—	Source Register A
SRAD	—	Double Precision Source Register A
SRB	—	Source Register B
SRBD	—	Double Precision Source Register B

ARGUMENT INSTRUCTIONS

The argument instructions have a 16 bit positive number as part of the argument instruction. The other operand is in the Register Block. During execution of the argument instruction, the the argument is extended to a 32 bit number with the 16 most significant bits equal to zero.

The instruction format:

31	30	29	28	23	22	18	17	16	15	0
1	AFC	DR		O	ASF	Argument				

AFC/ASF	—	Argument function and subfunction code - DIRECT LOGICAL/ARITHMETICAL operations, DIRECT TEST and DIRECT SKIP
DR	—	Destination Register

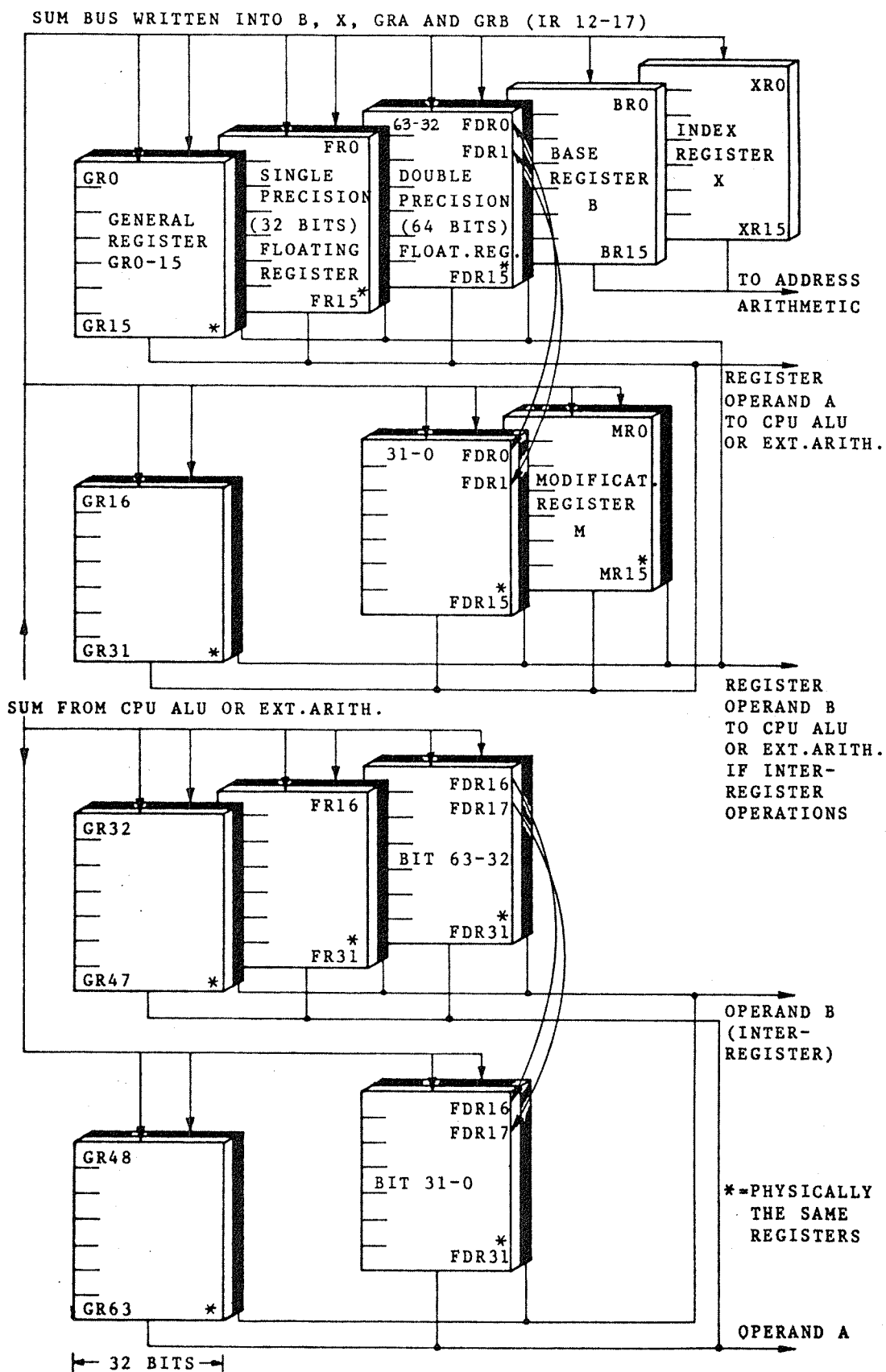
1.3 REGISTER BLOCK

The NORD 50 CPU has 64 general word registers (GRO-GR63) 32 bit wide; where

- 32 may be single precision floating registers
- 32 may be double precision floating registers (64 bits)
- 16 may be base registers (GRO-15)*
- 16 may be index registers (GRO-15)*
- 16 may be modification registers (GR16-31)

* These registers are also input to the hardware address-arithmetic and active while executing a memory reference instruction.

To reduce access-time for 2-operand instructions the register block is duplicated with identical constant, register block A and register block B.



Two auxiliary registers are used. The OR - the Overflow Register - holds the upper 32 bits of the product of a multiplication. The RR - the Remainder Register - is used to hold the remainder after a division.

1.4 *NORD 50 ORGANISATION*

The NORD 50 is built up of 3 19" racks, named A,B and C. The NORD 50 CPU occupies the B rack, and the A and C rack contains the external arithmetic.

For instructions not executed in the CPU rack, the CPU does:

- Present a A and a B operand of either 32 or 64 bits.
- Write the achieved result of 32 or 64 bits back to the CPU destination register.

The A rack contains:

- Arithmetic for MULTIPLY and DIVIDE, INTEGER and FLOATING.

The B rack contains:

- The register block
- The address arithmetic
- Memory interface. Data address and control logic
- NORD 10S interface. Data and control logic

The C rack contains:

- Arithmetic for floating add, subtract, convert integer to floating, convert floating to integer, shift and bit operations.
- NORD 10S communication logic.

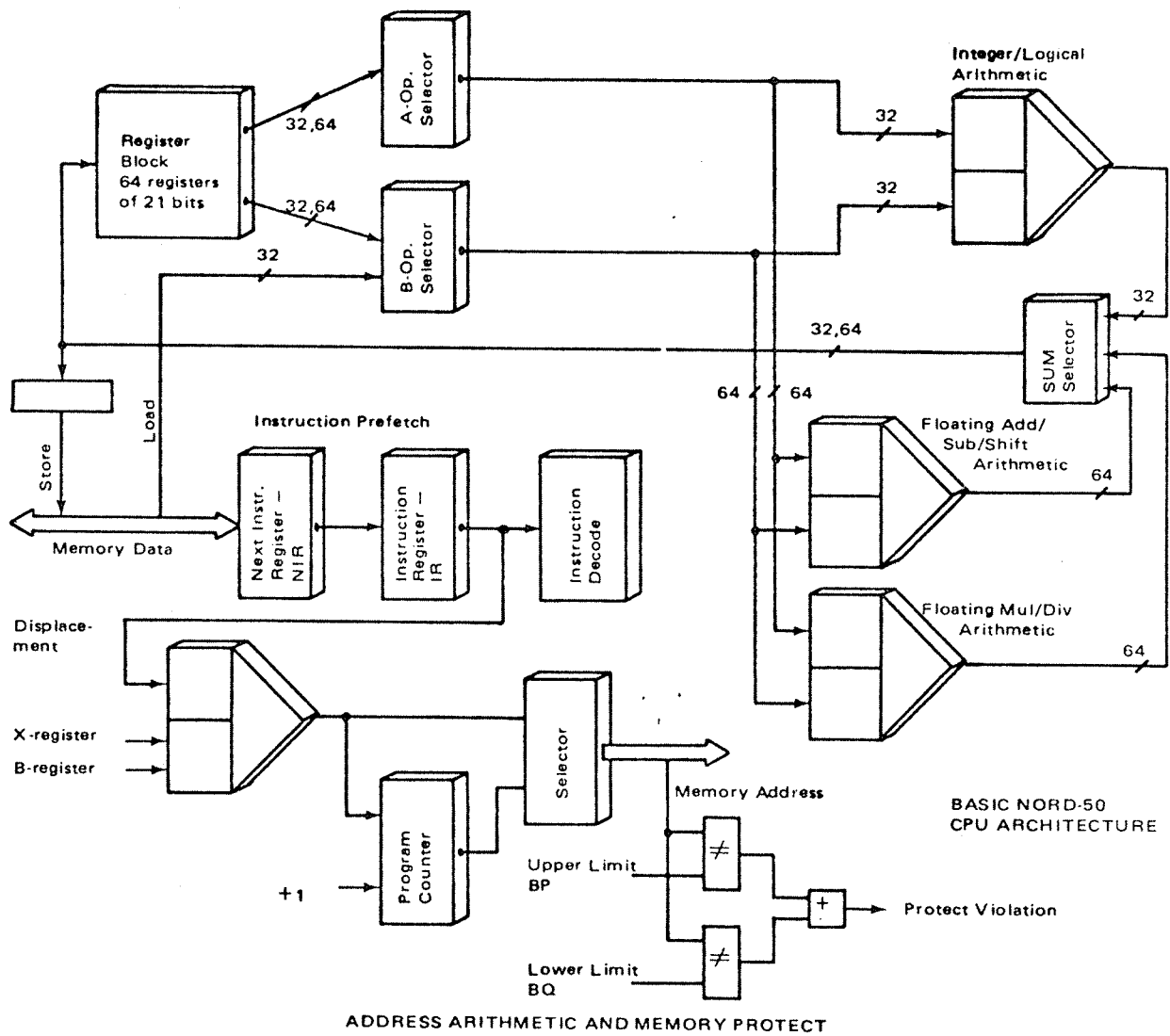
1.5 *INSTRUCTION EXECUTION*

The NORD 50 CPU employs instruction look ahead. While execution of current instruction takes place, the next is requested from memory and clocked into the Next Instruction Register - NI - prior to termination of the current instruction.

While executing a memory reference instruction, the memory address is calculated in parallel with the next instruction fetch.

While executing an inter register or argument instruction the instruction is decoded and executed in parallel with the fetch of the next instruction.

Upon completion, the next instruction residing in the NI register is transferred to the Instruction Register - IR for execution.



1.6 *NORD 10/S CONTROL OF NORD 50*

NORD 50 is equipped with no input/output system and no input/output instruction is available.

The sequence of loading and starting a NORD 50 programme is taken care of by NORD 10/S.

The NORD 50 is connected to the input/output system in NORD 10/S via two modules in the I/O rack, one for address and one for data.

32 bits data is exchanged between the computers by means of 2 IOX instructions, each transferring 16 bits of data (NORD 10/S A register)

Data may be:

- NORD 50 programme start address (SA)
- NORD 50 address violation limit registers (BP, BQ)
- NORD 50 stop or break conditions (MODUS)

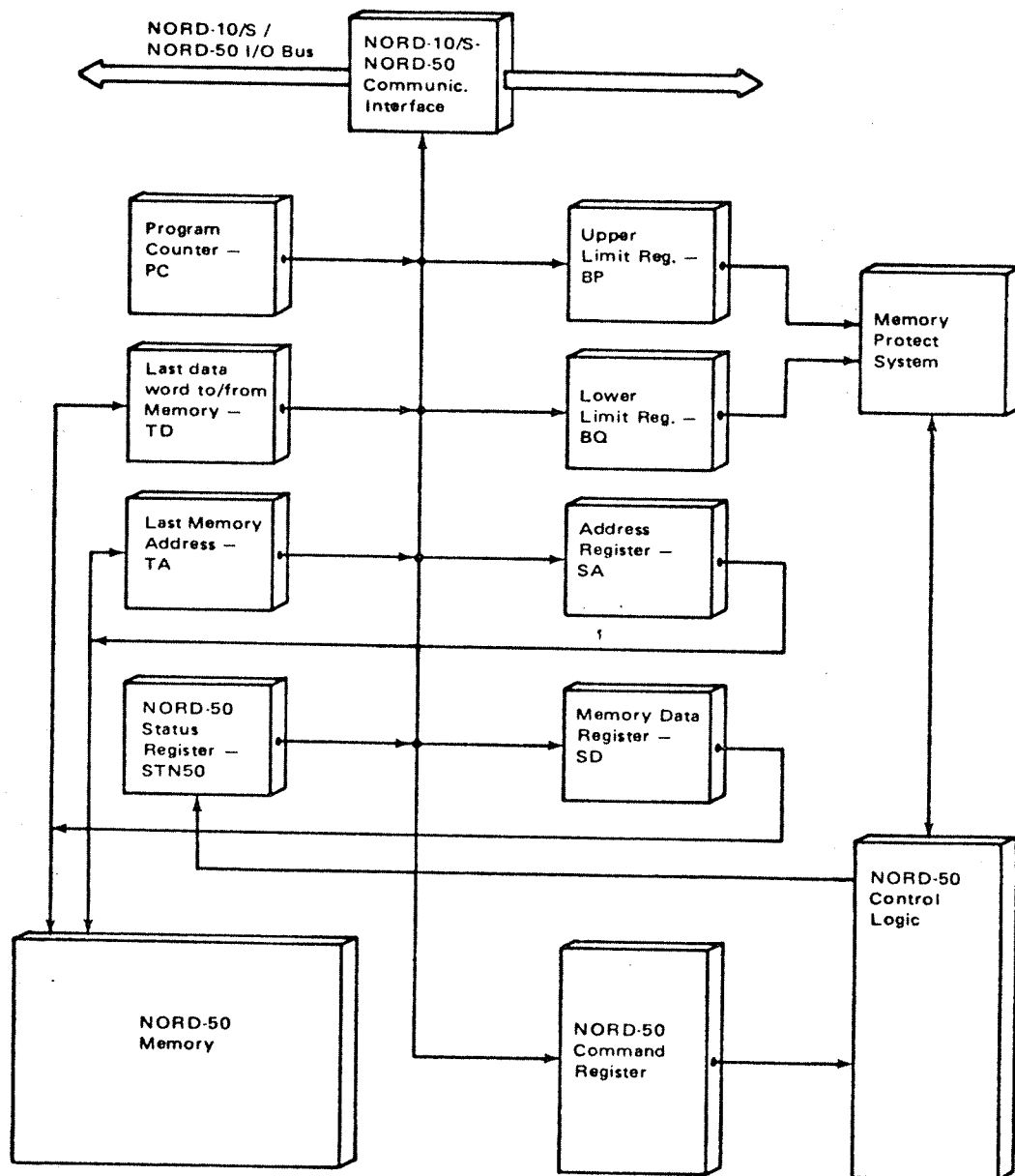
NORD 50 may then be started by a special IOX instruction in NORD 10/S. NORD 10/S can continue its tasks until it becomes interrupted by NORD 50 by either:

- NORD 50 execute on stop instruction
- or
- An error condition occurred

The communication lines are then used to check the STOP-condition.

NORD 10/S may EXAMINE/DEPOSIT in NORD 50 memory via the input/output system.

Running NORD 50 in SIMULATE-mode the memory may be simulated by supplying data and instructions via the NORD 10/S.



NORD-10/S / NORD-50 COMMUNICATION

1.7 *NORD 50 MEMORY CONNECTIONS*

NORD 50 is connected to memory shared by various sources as NORD 10/S, NORD 10/S DMA and another NORD 50, by separate ports in a multiport memory system

A 32 bits NORD 50 channel is obtained by accessing two banks simultaneously from one NORD 50. The addresses and request are the same in both banks as the address cable is common. Two data cables will each supply half of the 32 bits word. As NORD 50 receives a double set of ready signals, which may be out of phase, the signals are latched waiting for the slowest response.

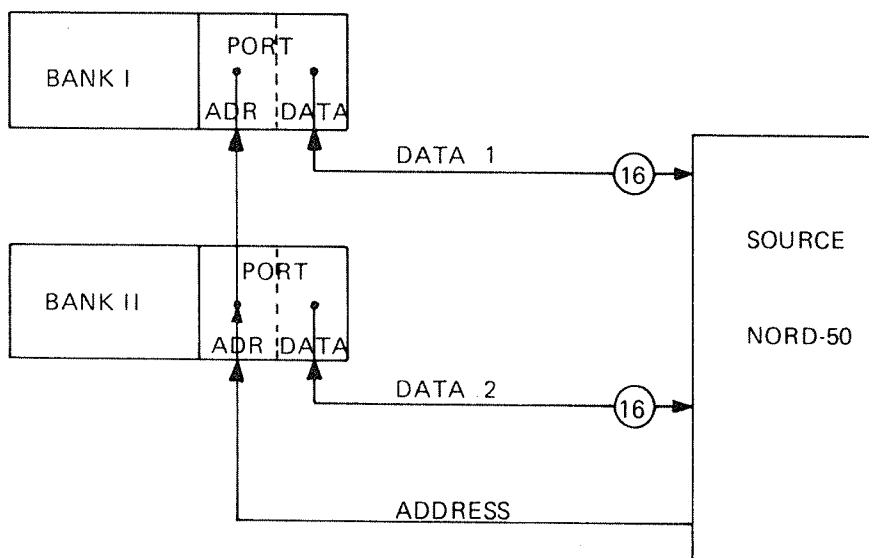
For a 32 bits channel as NORD 50 to communicate with a 16 bits channel as NORD 10/S and DMA, a special bank selection technique is necessary for the 16 bits channel. (Also referred to as interleave).

A DMA transfer will normally access consecutive location in one memory bank and NORD 50 will have trouble reading then out as a 32 bits word (Same for NORD 10/S). To overcome this the address cable of the DMA channel is interleaved or rotational shifted one place to the right.

Source address bit 0 will after the shifting be the most significant address bit and determine the bank selection.

The effect is that all even addresses will seem to lie between 0 and 1024K (one bank) while all odd addresses will appear as lying between 1024K and 2048K (another bank).

NORD 50 will access these two banks via two ports in parallel as both banks see identical NORD 50 address. 32 bits will then be access in parallel. 16 bits from each of the banks.



Two 16 Bit Banks Accessed as One 32 Bit Bank

NOTE THEN:

An even NORD 10/S or DMA address (address bit 0 = 0) will access NORD 50 bits 31-16, while an odd address (address bit 0 = 1) will access NORD 50 bits 15-0.

The concept may be illustrated in the following example.

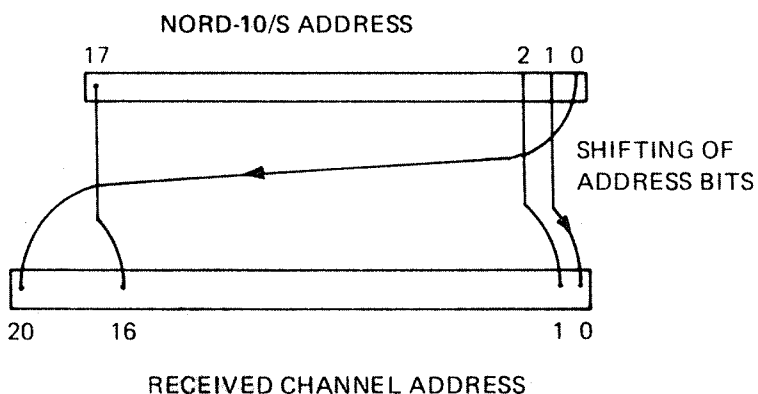
Example

Figure 1.11: Shifting of Address Bits

Address bit number 20 is used to select a bank.

Assuming NORD 10/S is storing 4 words in memory in consecutive locations (as seen from NORD 10/S) the lowest bit on the issued address will toggle and alternating banks will be selected. If the issued addresses are 0, 1, 2 and 3, the received addresses would be:

Received Address	Word No.:
0 0 0 0 0 0 0	1
4 0 0 0 0 0 0	2
0 0 0 0 0 0 1	3
4 0 0 0 0 0 1	4

etc.

The following illustration will show how the four words will be stored.

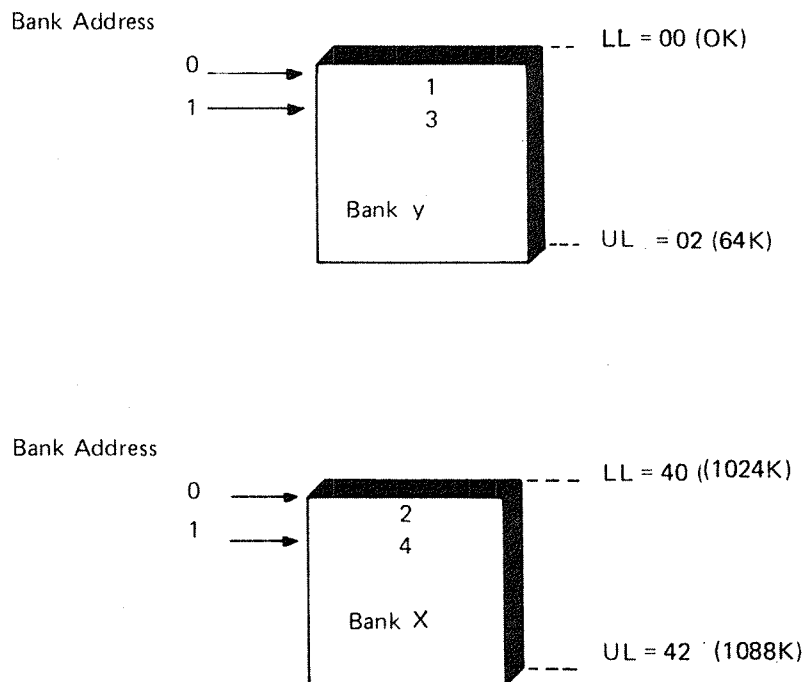


Figure 1.12: The Bank as seen from NORD 10/S

When NORD 50 reads those 4 NORD 10/S words, it regards the same two banks as one bank with double word length. The 4 16 bit words will then be read as two 32 bit words.

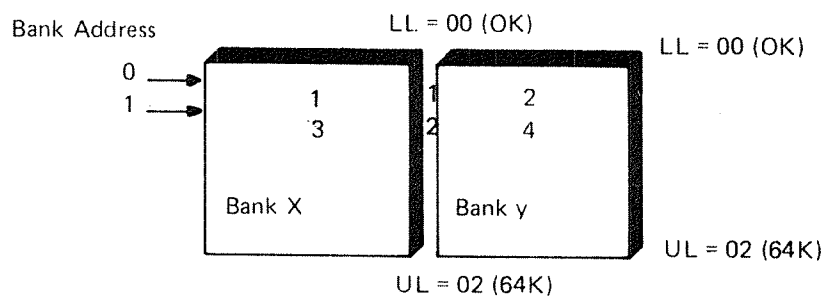


Figure 1.13: The Banks as seen from NORD 50

2 NORD 50 MULTIPLY/DIVIDE UNIT (A-RACK) GENERAL

The A-rack can be looked upon as a special processor being controlled by the NORD 50 CPU.

The processor is activated when:

- The CPU fetch a floating or integer, multiply or divide instruction for execution.
and
- The operands are latched in the CPU and presented on the A and B operand lines to the A-rack.

For a floating double memory reference instruction this implies that two memory references each reading a 32 bits operand have to take place before the processor is activated.

While the processor is active the CPU waits until a READY signal is received indicating that the SUM-bus to CPU contains an achieved result.

The ready signal triggers a CPU - WRITE-cycle, writing the result back to the register, specified in the destination field of the Instruction Register.

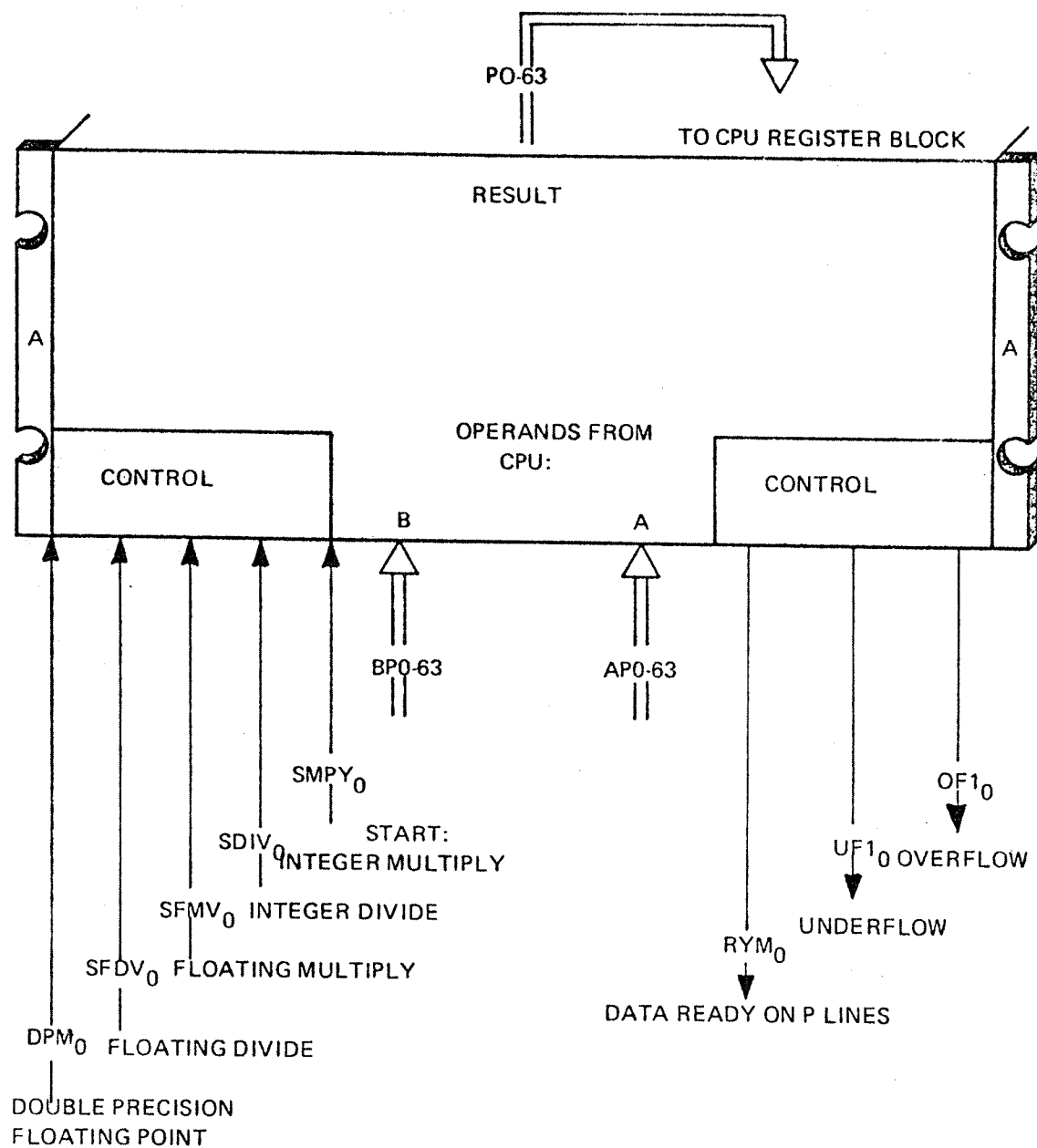
The 64 bits result of a floating double instruction is written back to the register block in parallel.

An integer product of 32 bits is written back to the specified register and in parallel the 32 overflow bits is written into the overflow register.

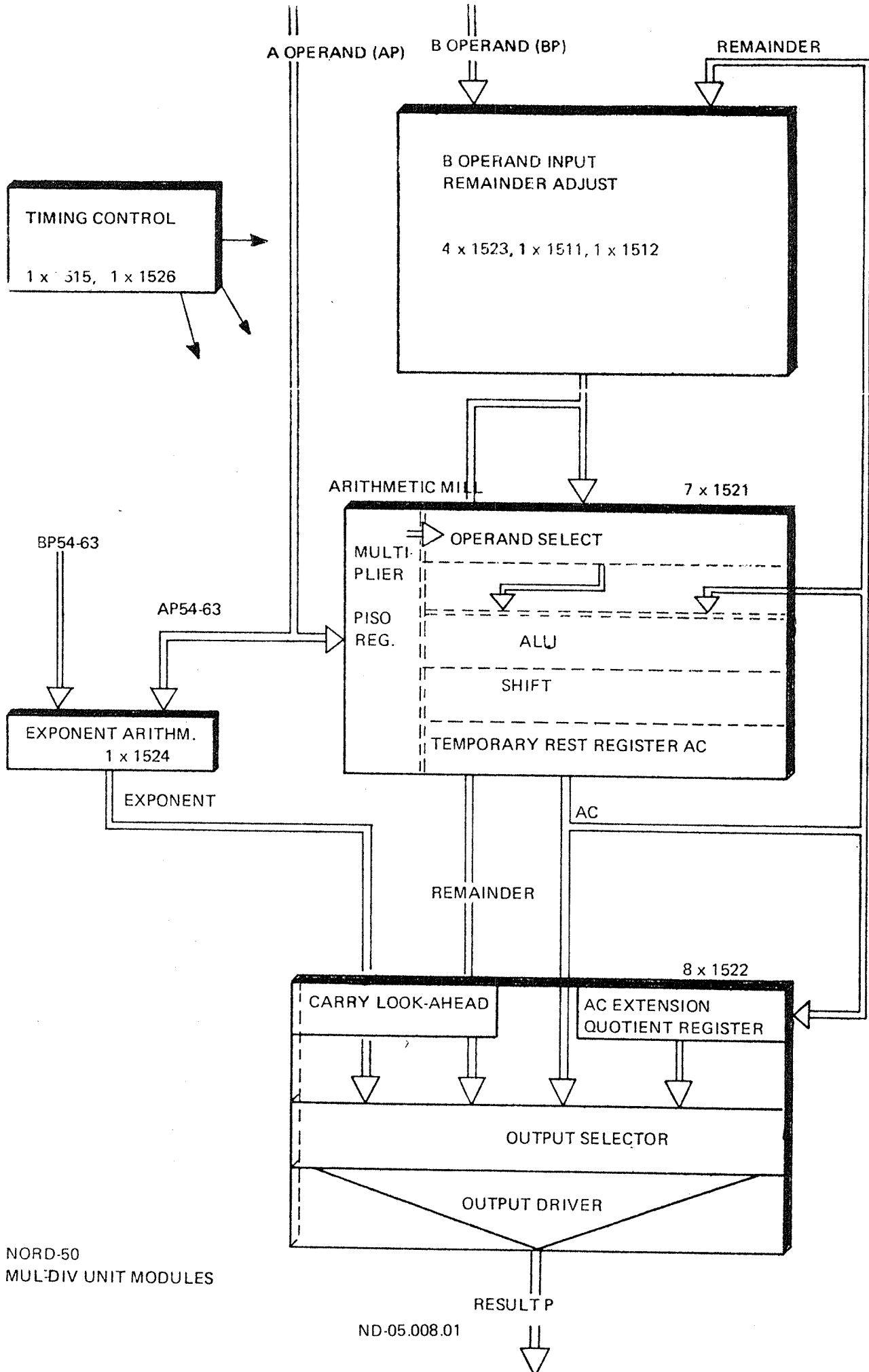
A quotient of 32 bits, the result of an integer division, is written back to the specified register and in parallel the 32 bits remainder is written into the remainder register.

RACK: A NORD-50 MUL/DIV UNIT**Position:**

1	1521.1	MUL-DIV ARITHMETIC
2	1522.1	OUTPUT SELECTOR
3	1521.2	MUL-DIV ARITHMETIC
4	1522.2	OUTPUT SELECTOR
5	1523.4	B-INPUT
6	1521.3	MUL-DIV ARITHMETIC
7	1522.3	OUTPUT SELECTOR
8	1521.4	MUL-DIV ARITHMETIC
9	1522.4	OUTPUT SELECTOR
10	1523.2	B-INPUT
11	1511	SHIFT MATRIX A
12	1512	SHIFT MATRIX B
13	1525	MUL-DIV TIMING
14	1526	MUL-DIV CONTROL
15	1521.5	MUL-DIV ARITHMETIC
16	1522.5	OUTPUT SELECTOR
17	1523.3	B-INPUT
18	1521.6	MUL-DIV ARITHMETIC
19	1522.6	OUTPUT SELECTOR
20	1521.7	MUL-DIV ARITHMETIC
21	1522.7	OUTPUT SELECTOR
22	1523.1	B-INPUT
23	1524	EXPONENT ARITHMETIC
24	1522.8	OUTPUT SELECTOR
25		
26		
27		
28		
29		
30		
31		
32		



NORD-50 MUL-DIV UNIT CONTROL AND DATA FLOW



2.2 MODULE DESCRIPTION

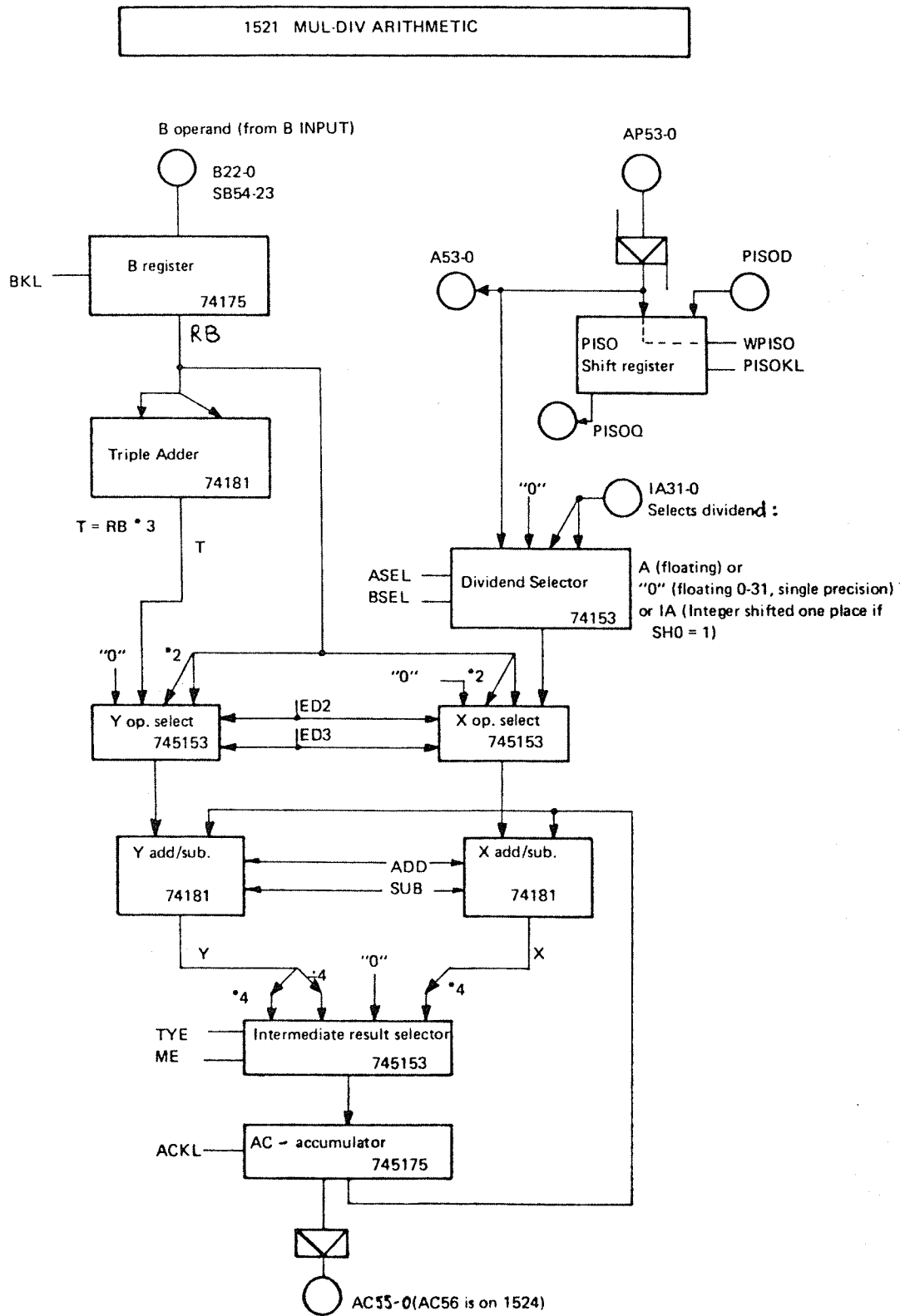
1521 - MUL-DIV ARITHMETIC -

POSITION:

A1 = 1521.1
 A3 = 1521.2
 A6 = 1521.3
 A8 = 1521.4
 A15 = 1521.5
 A18 = 1521.6
 A20 = 1521.7

This PCB Contains:

- B-operand latch (RB) [9D, 11D]
Contains divisor during divide and multiplicand during multiply.
- B-operand triple adder [6,7D-13,17D]
output three times the B-register.
- Y-ALU [5,6C-18,19C]
Adds temporary result register AC with selected multiple of B-operand during multiply and subtract during divide.
- X-ALU [8,9C-18,19B]
Subtract AC-register from selected multiple of B-operand during integer and floating divide. (one multiple less than A-ALU) .
- Y-ALU B-operand select [1D-19D]
- X-ALU B-operand select [11C-16B]
- X-ALU/Y-ALU select/shift unit [1B-16C]
- Temporary result register AC [4B, 19A]
- Integer-floating multiplier
parallel input serial output (PISO) Register [11A]



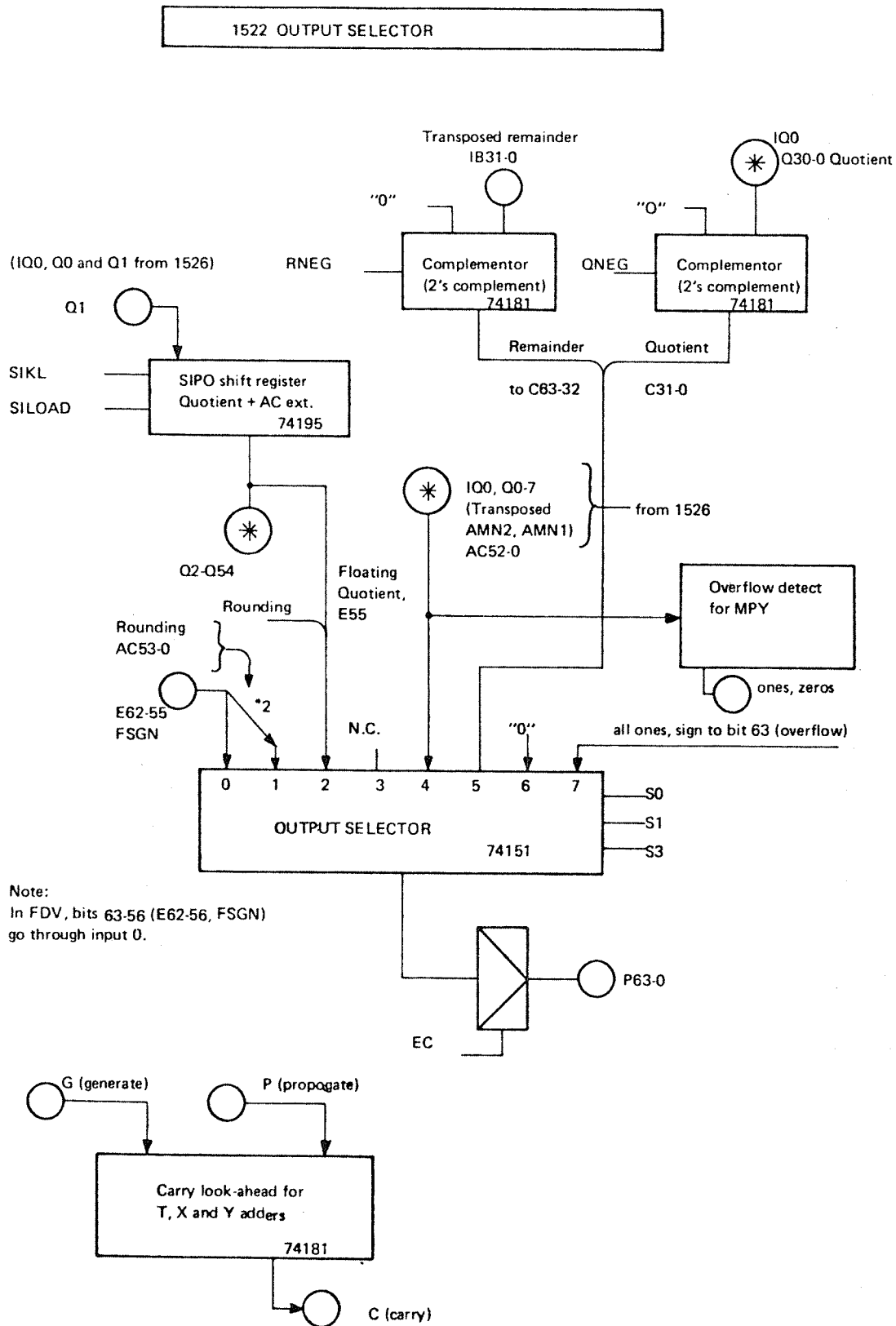
1522 - OUTPUT SELECTOR -

POSITION

A2 = 1522.1
 A4 = 1522.2
 A7 = 1522.3
 A9 = 1522.4
 A16 = 1522.5
 A19 = 1522.6
 A22 = 1522.7
 A24 = 1522.8

This PCB Contains:

- Selected result driver to CPU [5A,18B]
- Result selector [26-16C] (8-1 selector selecting:)
 1. Floating, exponent (1522.8)/Product (1522.7-1)
 2. Normalized floating product (1522.7-1)
 3. Floating exponent (1522.8)/Quotient (1522.1-7)
 4. Integer multiply : Overflow (1522.8-1522.5)/Product (1522.4-1)
 5. Integer divide : Remainder (1522.8-1522.5)/Quotient (1522.4-1)
 6. Zero (Floating underflow)
 7. One (Floating overflow or integer divide on zero)
- AC-extension register during integer multiply (1522.1)
and
Quotient register during floating and integer divide [4B,14B]
- Carry look-ahead for T, X and Y - adder on 1521 board [2A, 18A]
- Integer divide ALU [6/7B - 11/12B] That:
 1. Complement Quotient (1522.4-1)
 2. Complement Remainder (1522.8-5)
- Overflow detect for integer multiply (1522.8-5) [9A,12A]



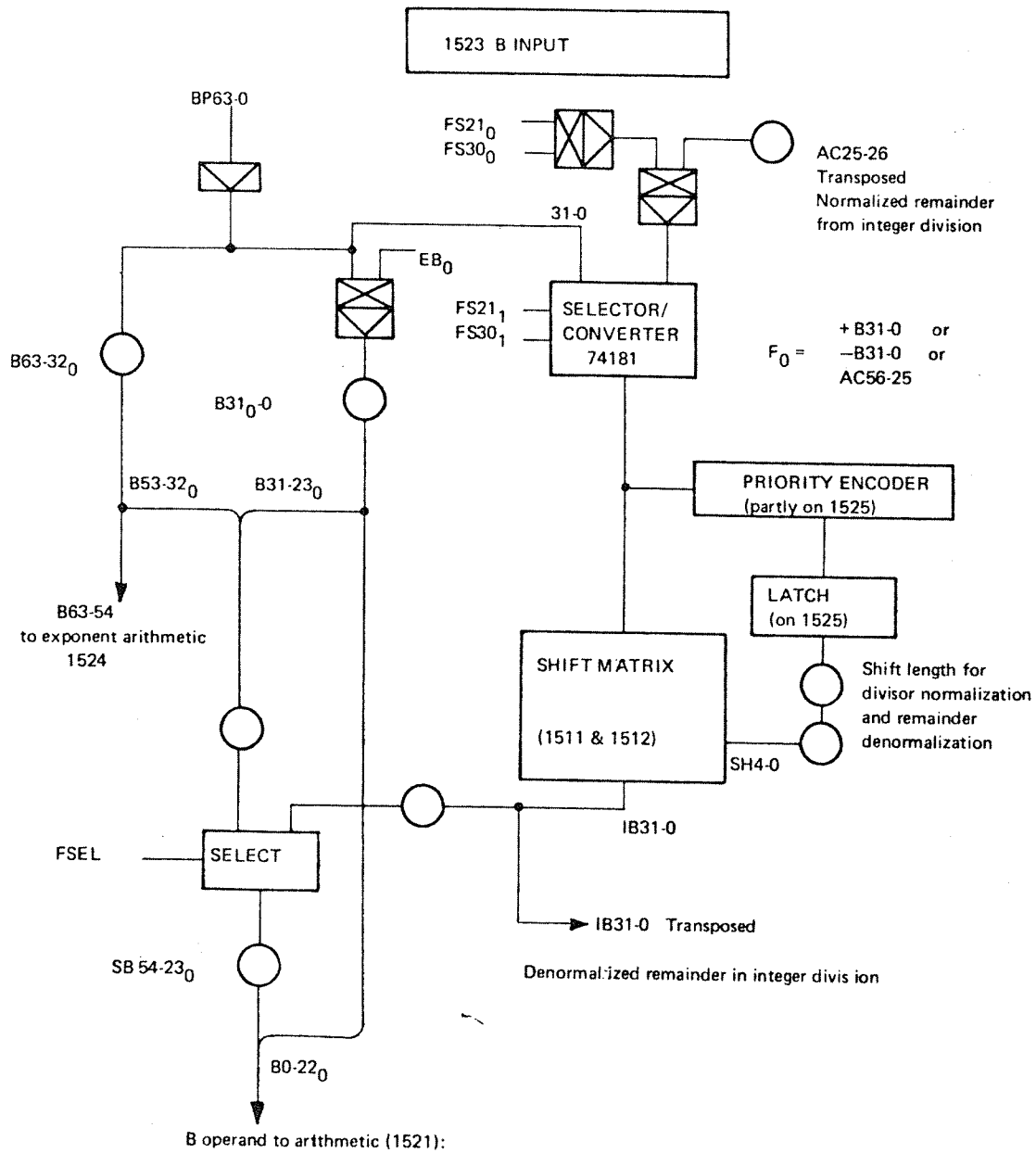
1523 - B-INPUT -

POSITION

A5 = 1523.4
 A10 = 1523.2
 A17 = 1523.3
 A22 = 1523.1

This PCB Contains:

- CPU B-operand receiver/buffer [12A,8A,6B]
- Floating double unshifted B-operand B0-B22 enable [8C, 10B]
- Floating mantissa or integer B-operand select → SB-bus [16A,18A]
- Arithmetic/ Logic unit [2A,2B] That:
 1. Select the B operand direct through → F
during integer, floating multiply and floating divide
 2. Select the B-operand and invert it if negative → F
during integer divide
 3. Select the remainder (AC 56-25) → F
during integer divide
- Priority encoder [10C] to find the most significant "1" bit position during integer divide. The divisor (B-operand) is shifted until the most significant divisor bit becomes 1. in the shift matrix.
- Zero divisor detect logic (Null) [10C]

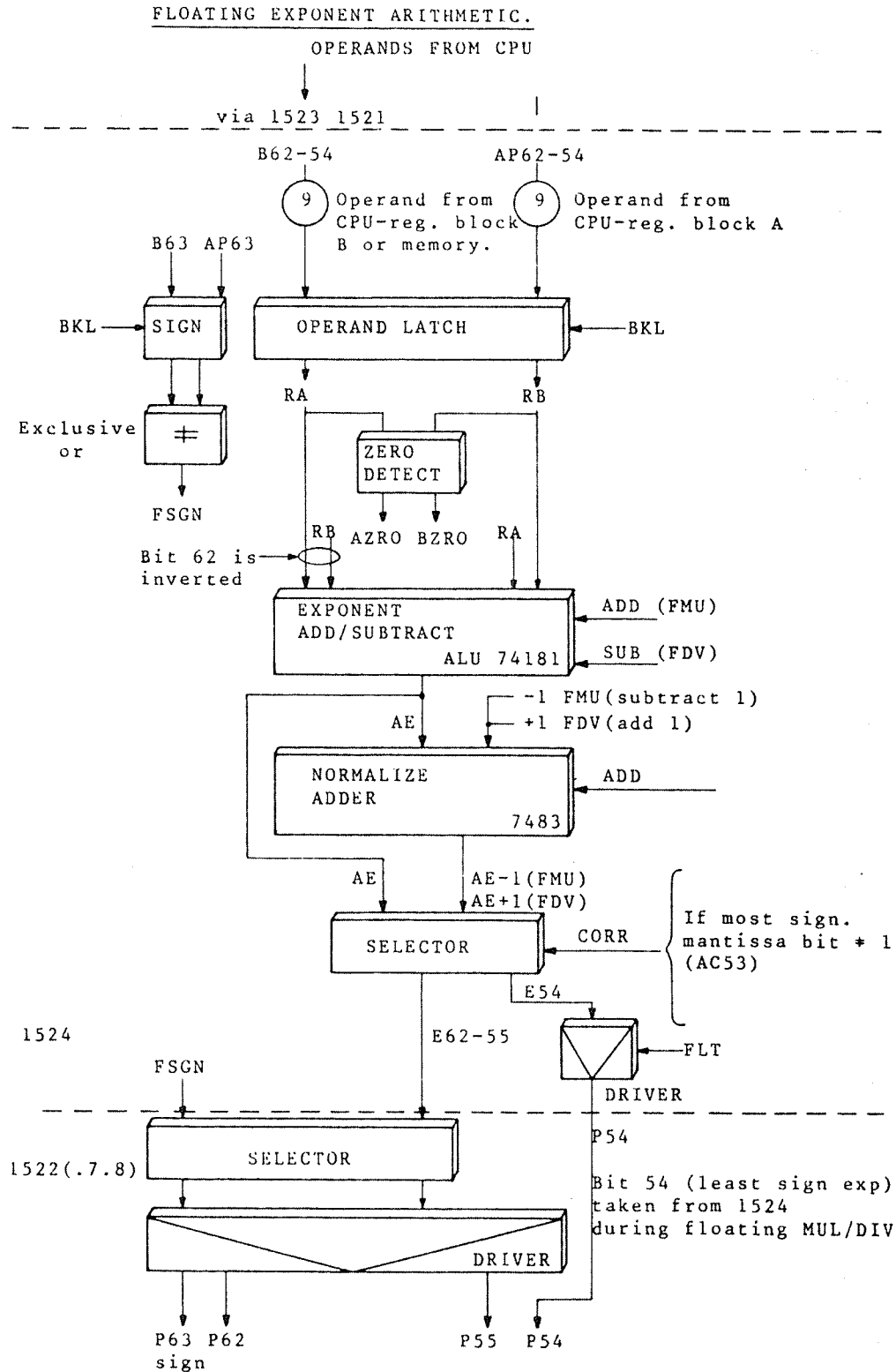


MPY	Signed two's complement B operand SB54-23
DIV	Unsigned value of B operand in SB54-23
FMU, FDV	Mantissa in SB54-32 (SB54 = 1)
Double Precision	Mantissa in SB54-23, B22-0 (SB54 = 1)
Unused B and SB bits must be zero	
EB	Enable BP31-0 to B31 during floating double

1524 - EXPONENT ARITHMETIC - POSITION A23

This PCB Contains:

- A and B-operand exponent register (bit 62-54) [2A-8A]
- Exponent equal zero detect logic [6D,4D]
- Exponent add/subtract ALU [2-3B/10-11B]
Adds during floating multiply, subtracts during floating divide
- Exponent normalize adder [2C-10C]
Exponent added with 1 if mantissa is shifted 1 location right (divide)
exponent subtracted with 1 if mantissa is shifted 1 location left (multiply)
- Selector selecting the corrected or the not corrected exponent to the output selector board (1522.8) [2D-8C]
- Circuits generating the floating point result sign [14C,16C]
- Underflow/overflow detect circuits [8C,8D,16,10D]
- Output selector control (SO-2) [14D]



1525 - MUL-DIV TIMING - POSITION A13

This PCB Contains:

- Or of start signals received from CPU [17A,17D]
- Hold latch for operation [17C]
- Cycle-counter (C0,C1,C2 and C3) [5B]
- Timing circuits [3C,3B]
- Iteration counters [10C,10D]
- Shift length decoder/latch for integer divide [12B/12C,12A]
- Integer multiply overflow detect (INOFL) [15B,15C,15D]

1526 - MUL-DIV CONTROL

POSITION A 14

This PCB Contains:

- Y-Adder operand select during multiply (ED2,ED3) [19B,13D,13C]
- AC - extension register (SIPO) serial input logic during integer multiply (Y0,Y1 → Q0,Q1) [11A,10B,7B,4B,6A]
- Integer/ floating divide quotient estimate (ED2,ED3) [13C,13B]
- Integer/ floating divide quotient generate (two serial input bit to SIPO-register) [10B,7B,4B,6A]
- ALU on 1521 board add/subtract control [3A]
- Floating rounding circuits not force a "1" detect circuits:
Floating divide: (SIQ0,SIQ32) [10D,4C,8A]
Floating multiply: (SFPC,SFPD) [10C,11A,8A]
- Driver for control-signals to CPU [3A]

3 NORD 50 - CPU - B - RACK

FUNCTION	ON PCB
NORD 50 registers*	1502
NORD 50 remainder and overflow registers*	1502
NORD 50 address arithmetic*	1503,1501
NORD 50 memory address drivers*	1501
NORD 50 memory data drivers/receivers*	1501
NORD 50 memory control signals drivers/receivers	1519/1500
NORD 10/S communications registers*	1501
NORD 10/S IOX-address decoding	1504

* = 4 bits per module

RACK: B NORD-50 CPU**Position:**

1	1501.1	ADDRESS ARITHMETIC
2	1502.1	REGISTERS
3	1503.1	ARITHMETIC BUFFER
4	1501.2	ADDRESS ARITHMETIC
5	1502.2	REGISTERS
6	1503.2	ARITHMETIC BUFFER
7	1501.3	ADDRESS ARITHMETIC
8	1502.3	REGISTERS
9	1503.3	ARITHMETIC BUFFER
10	1501.4	ADDRESS ARITHMETIC
11	1502.4	REGISTERS
12	1503.4	ARITHMETIC BUFFER
13	1501.5	ADDRESS ARITHMETIC
14	1502.5	REGISTERS
15	1503.5	ARITHMETIC BUFFER
16	1501.6	ADDRESS ARITHMETIC
17	1502.6	REGISTERS
18	1503.6	ARITHMETIC BUFFER
19	1501.7	ADDRESS ARITHMETIC
20	1502.7	REGISTERS
21	1503.7	ARITHMETIC BUFFER
22	1501.8	ADDRESS ARITHMETIC
23	1502.8	REGISTERS
24	1503.8	ARITHMETIC BUFFER
25	1504	NORD-50 CONTROLLER
26	1505	REGISTER ADDRESS
27	1510	INSTRUCTION CONTROL
28	1508	CHIP SELECTION
29	1507	ARITHMETIC CONTROL
30	1506	CYCLE COUNTER
31	1519	TIMING CONTROL
32	1500	NORD-50 I/O CONTROL

3.2 *MODULE DESCRIPTION*

1501 - ADDRESS ARITHMETIC

This PCB Contains:

- Memory address driver (MA) [19D,17D]
- Memory data driver/receiver [9A,11A/9B,11B]
- Part of address-arithmetic [18/19A]
- NORD 10/S writeable communication registers SA [5D], SD[7D], BP[1D] and BQ[3D]
- NORD 10/S readable communication registers SA [5D], TA[6C], TD[8C] and PC (Programme-Counter) [15C]
- Comparators comparing the NORD 50 memory address against the address violation limit registers [BQ,BP]
- NORD 50 memory data parity generate logic[15A,15B]
- Instruction Register IR[17B]
 Next Instruction Register NI[13B]
 Displayment Register D [19B]
- Address arithmetic and CPU ALU carry look-ahead [7A]

1502 - REGISTERS

This PCB Contains:

- 4 bits of the 64 A-Block registers [17C-14D]
- 4 bits of the 64 B-Block registers [9C-6D]
- Integer product overflow - register [8A]
- Integer divide remainder - register [10A]
- A-operand selector/latch [10B,8B/6B]
- B-operand selector/latch [4D,4C/15B]
- CPU integer ALU [18/19A]
- ALU output equal zero detect circuits [19D]
- Drivers for A-operand to external arithmetic A-rack [6A]/C-rack [4A]
- Drivers for B-operand to external arithmetic A-rack [14A]/C-rack[12A]
- External arithmetic result receiver [17B]

1503 - ARITHMETIC BUFFER

This PCB Contains:

- Index - registers XO-15 [12A]
- Base registers BO-15 [14A]
- Address arithmetic X,B adder/latch [13,14B/10C]
- Latch/driver for 4 of the 32 most significant A-operand bits to external arithmetic A-rack [6A/10A] and C-rack [6A/8A]
- Latch/driver for 4 of the 32 most significant B-operand bits to external arithmetic A-rack [6B/10B] and C-rack [6B/8B]
- External arithmetic result receiver [16C]

1504 - NORD 50 CONTROLLER - POSITION B25

This PCB Contains

- Byte parity generate logic [8A]
- Parity check circuits during memory read (Parity error : 1 → SB7)
- Parity error latch used to light failing byte number in operators panel (PEBO - PEB3)
- Address violation detect logic (ABP BQ)
- NORD 10/S IOX instruction address decode logic [18A]
- Select signals, selecting the source to the memory address bus (MA)
 1. SA - Register(MAE2)
 2. CA calculated address (CA) (MAE5)
 3. Programme-counter (PC)
- Memory Data-Bus (MD) enable signal (WR1)
- Receivers for external arithmetic - ready, overflow and underflow signals

1505 - REGISTER ADDRESS - POSITION B 26

This PCB Contains:

- Register block A chip select (ACS1-4) (1 chip contains 16 registers)
- Register block B chip select (BCS1-4)
- Register Block A register select (RAA 0-3)
- Register block B register select (RAB 0-3)
- Index register select (XA 0-3)
- Base register select (BA 0-3)
- Register Zero detect logic
 - (Register block A = ZROA)
 - (Register block B = ZROB)
- Driver for instruction register bit 0-5 and 23-30 (IRX 0-5, IRX 23-30) to external arithmetic C-rack
- Single/double floating operation detect logic (DPM,DPA)
- A-operand select signal (ABE 1)

1510 - INSTRUCTION CONTROL - POSITION B27

This PCB Contains:

- Instruction decode logic, decoding.
 1. External operations (EXOP)
 2. Single precision floating instructions (SGL)
- A and B register block write signal (ABW1)
- X and B register (GRO-15) write signal (XBW)
- Memory write signal generation (WRD)
- Instruction and displacement - Register clock signals (IRS1,IRS1B,DS1)
- Instruction hangup detect logic (CNT 15)
- TA and TD-registers clock signals (TAS1,TDS1)
- Next-instruction register strobe (NIS)
- Programme counter increment (PCCOO)
- B-operand select signal (RGE1)

1508 - CHIP SELECT - POSITION B28

This PCB Contains:

- Decoding logic and drivers for external arithmetic start signals (SFAD-SDIV)
- Enabling signals for the data buses to the external arithmetic (FADE,MPYE)
- Enabling signals for destination - registers (IR Dest-Field → Reg. ADR) (DRE1,DRE2)
- Enabling signals for source - register A and B (SRAE,SRBE)
- Instruction executed in external arithmetic detect logic (EXT)
- Latch signals for A and B-operands (STRA,STRB)

1507 - ARITHMETIC CONTROL - POSITION B29

This PCB Contains:

- CPU integer arithmetic ALU function select bit generation (FSO-3)
- Logic for carry input to least significant CPU ALU (CYSO)
- Inter-register carry flip-flop (CFF)
- External arithmetic result bus bit 63-32 enable (SEB)
- ALU A-operand select signal (FRE)

1506 - CYCLE COUNTER - POSITION B30

This PCB Contains:

- Main states flip-flops (DCCO-DCC2)
- Next cycle decision logic (input to the DCCO-DCC2 flip-flops)
- Logic checking if jump or skip conditions fulfilled (JEFF)
- Test condition decode logic (TC1, TC2)
- Last cycle of instruction detect logic (ENDIN)
- Programme counter → memory address bus (MA) select for next-instruction fetch (PCE2)
- Parallel load of programme-counter signal (MAS 3)

1519 - TIMING CONTROL - POSITION B31

This PCB Contains:

- Cycle decode logic (DC0-DC7)
- Cycle read phase flip/flop (REGR)
- Cycle write phase flip/flop (REGW)
- Main cycles read/write-phase decode logic (DCRO-DCR3/DCWO-DCW3)
- Memory address ready/data ready receive circuits (AR, RAR/DR, RDR)
- Simulated address ready/data ready generate circuits (ARS, DRS)
- Request signal generate/drive logic (RQ/RQM)
- Operand latch-strobe (SP) (Change from cycle read → write phase)
- Write pulse to registers (WP) (Cycle terminate)
- Completion signal to NORD 10/S generate/drive logic DEVC/LDEV

1500 - N-50 I/O CONTROL - POSITION B32

This PCB Contains:

- Memory address decoding (AO-15) = 4K banks
- Memory address → operations panel driver (DO-15, WO-15)
- Select signal from OPR switch 9 and 10 (SW9,10) selecting:
 1. Instruction fetch address (DCO + 4)
 2. Memory operand address (DCO + 4)₀
- Parity error drive circuits driving:
 1. Byte No. (WLO-3)
 2. What memory reference (WL4-6)
 3. Parity error detect signal (WL7)
- Receivers for address ready/data ready signal from memory (AR1,AR2/DR1,DR2)
- Logic waiting for the last address ready/data ready from multiport memory (ARL/DRL)

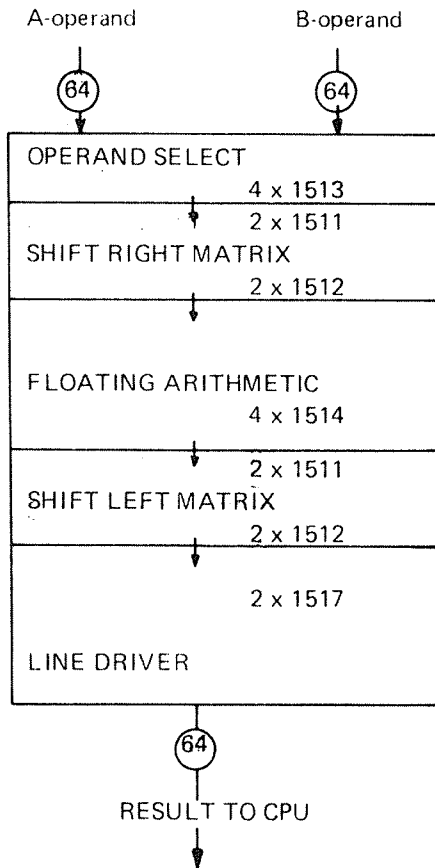
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NORD 50 C-RACK GENERAL

In the C-rack, as part of the external arithmetic, the following instructions are executed:

Mnemonic:	Memory Ref. Instr.	Inter. Register Instr.	Means:	No. of operand bits:
FAD	X		Floating Add $F + (EA)$	32
FADD	X		Floating DP Add $FD + (Ea, Ea + 1)$	64
RAF		X	Floating Reg. Add	32
RAFD		X	Floating DP Reg. Add	64
FSB	X		Floating Subtract $F - Ea$	32
FSBD	X		Floating DP Subtract $FD - (Ea, Ea + 1)$	64
FIX		X	Convert floating to Integer	32/32
FIXD		X	Convert DP floating to Integer	64/32
FIR		X	Convert floating to Rounded Integer	32/32
FIRD		X	Convert DP floating to Rounded Integer	64/32
FLO		X	Convert Integer to Floating	32/32
FLOD		X	Convert Integer to DP Floating	32/64
		X	Shift a 32 or 64 bit operand up to 63 places to the right or left with arithmetic, logical or rotational shift	32 or 64
BST		X	Bit set	32
BCL		X	Bit clear	32
BCM		X	Bit complement	32
BSZ		X	Bit skip on zero	32
BSO		X	Bit skip on one	32

As the table indicates, four of the instructions are memory reference instructions (one operand from memory and one from a register) and the rest are inter-register instructions (both operands, if two, are taken from the register block).



DATA FLOW

The C-rack consists of this main card set:

OPERAND SELECT 4 x 1513

Four 1513 cards select the operand to the internal bus.

SHIFT RIGHT MATRIX

Two 1511 cards shift the operand 0, 8, 16, 24, 32, 40, 48 or 56 places. The shift can be rotational or arithmetic.

Two 1512 cards shift the operand 0, 1, 2, 3, 4, 5, 6 or 7 places.

FLOATING ARITHMETIC 4 x 1514

The floating mantissas are added or subtracted on these cards. (Exponent arithmetic on card 1515.)

Shift operands go directly through. For bit instructions, the specified bit should now be in 0 and is manipulated and checked on card 1516.

SHIFT LEFT MATRIX

As right shift matrix but shifted left.

LINE DRIVER

Drives result on tri-state lines to CPU.

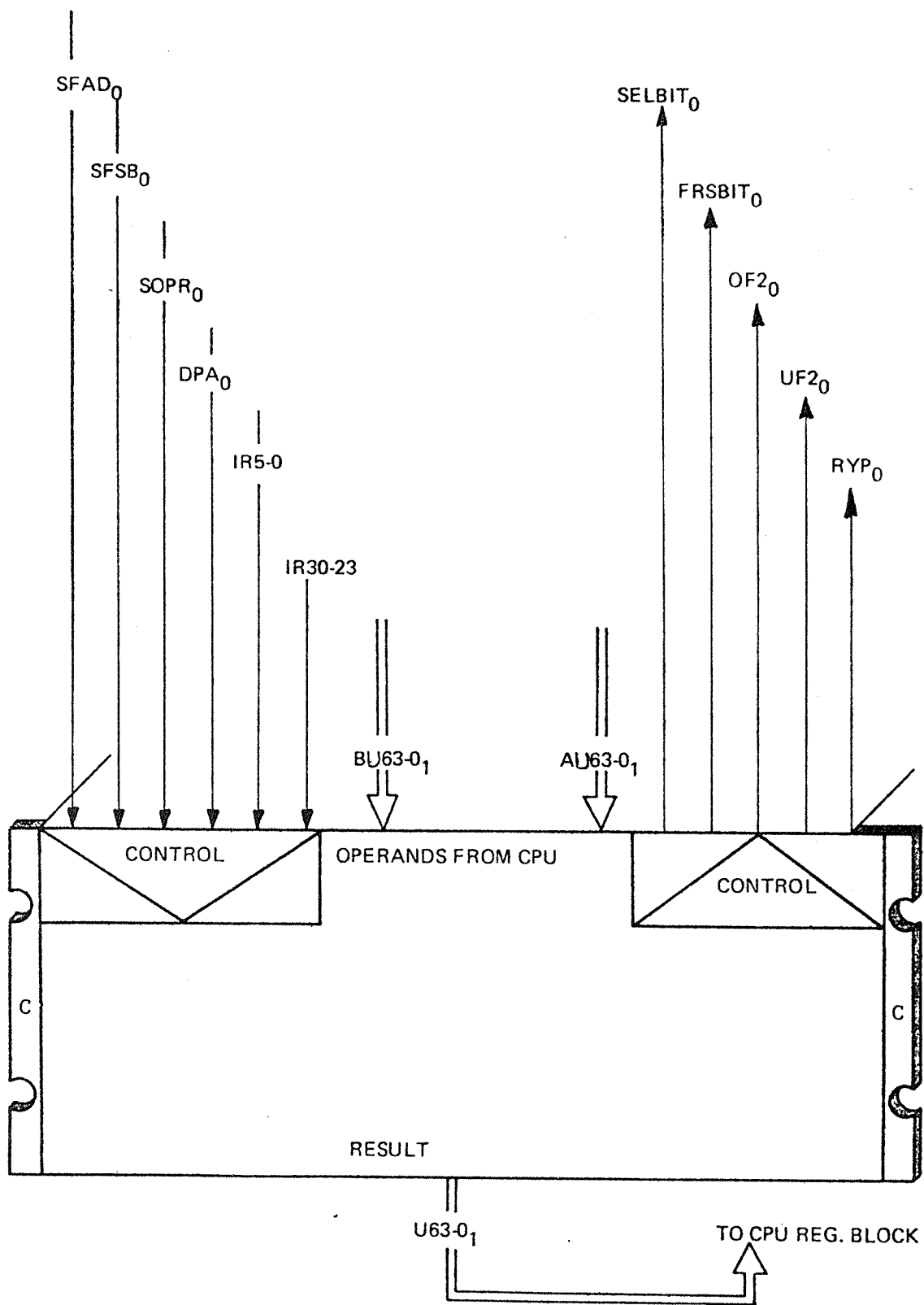
TIME USED:

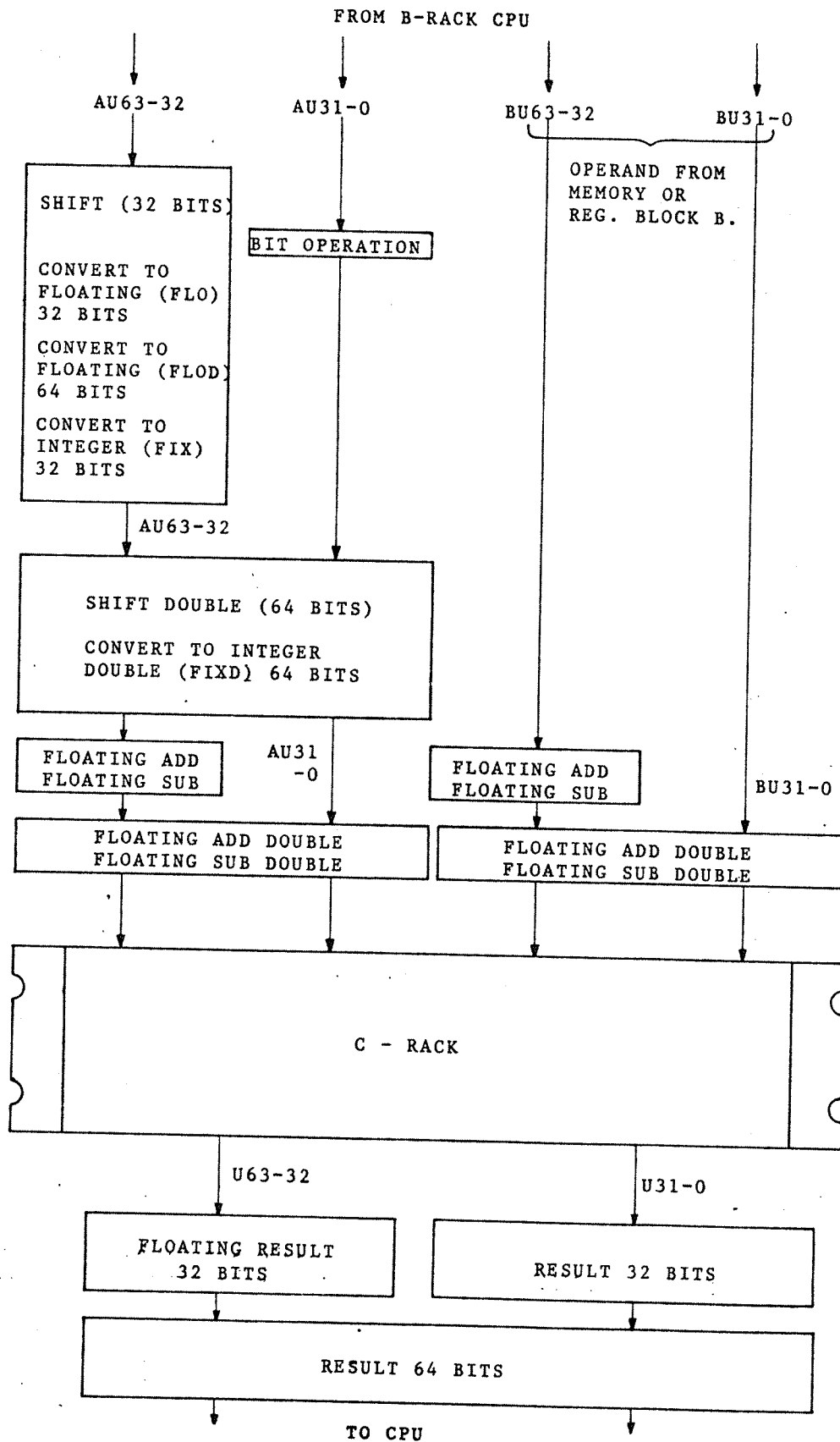
All instructions executed in the C-rack take the same amount of time. The time from the operands are presented until the result is on the result bus to the CPU is approximately 400 ns.

The operands passing through the C-rack are never latched, so the time used is given by adding the integrated circuit delays together.

The OR of all start signals to the C-rack triggers a one shot on the FLOATING CONTROL 1516 card. This one shot is set to approximately 400 ns equal the time the operands need passing through the logic and the result is ready on the data lines to CPU.

NORD-50 EXTERNAL ARITHMETIC C-RACK – CPU CONTROL AND DATA FLOW



C - RACK DATA FLOW

RACK: C NORD-50 ARIT**Position:**

1		
2	1513.1	DATA SELECTOR
3	1513.2	DATA SELECTOR
4	1513.3	DATA SELECTOR
5	1511.1	SHIFT MATRIX A
6	1511.2	SHIFT MATRIX A
7	1512.1	SHIFT MATRIX B
8	1512.2	SHIFT MATRIX B
9	1514.1	FLOATING ARITHMETIC
10	1514.2	FLOATING ARITHMETIC
11	1514.3	FLOATING ARITHMETIC
12	1514.4	FLOATING ARITHMETIC
13	1511.3	SHIFT MATRIX A
14	1511.4	SHIFT MATRIX A
15	1512.3	SHIFT MATRIX B
16	1512.4	SHIFT MATRIX B
17	1517.1	DATA BUFFER
18	1517.2	DATA BUFFER
19	1515	SHIFT CONTROL
20	1516	FLOATING CONTROL
21	1513.4	DATA SELECTOR
22		
23		
24	1523.1	DATA & ADDRESS BUS SELECTOR
25	1531	DEVICE REGISTERS
26	1532.2	DATA & ADDRESS BUS SELECTOR
27		
28		
29		
30		
31		
32		

4.2 *MODULE DESCRIPTION*

DATA SELECTOR - 1513 -

POSITION

C2 = 1513.1
 C3 = 1513.2
 C4 = 1513.3
 C21 = 1513.4

This PCB Contains:

- Two selectors selecting
 - A: The A or B-operand to the internal UB bus (to the shift-right matrix).
 - B. During floating add/sub select:
 - 1. The mantissa with the greatest exponent to the UA-bus (UA 54-0)
 - 2. The greatest exponent to the UA-bus (UA 62-54) (1513.4)
- Circuits for disabling the smallest exponent.
- Circuits for inserting the "hidden" 1-bit in the mantissa if the exponent $\neq 0$. (1514.4)

SHIFT MATRIX - 1511 -

POSITION

C5 Shift Right
 C6 Shift Right
 C13 Shift Left
 C14 Shift Left

This PCB Contains:

- Selectors for shifting the operand 0,8,16,24,32,40,48 or 56 places. (32 bits pr. module)
- Circuits for doing ROTATIONAL shift ($UB \rightarrow \beta$)
- Circuits for doing ARITHMETIC shift ($1 \rightarrow \beta$)

SHIFT MATRIX - 1512 -

POSITION

C7 Shift Right
 C8 Shift Right
 C13 Shift Left
 C14 Shift Left

This PCB Contains:

- Selectors for shifting the operand 0,1,2,3,4,5,6 or 7 places.
- Circuits for disabling the output of the shift matrix "O" output when true

FLOATING ARITHMETIC - 1514 -

POSITION

C9 = 1514.1
 C10 = 1514.2
 C11 = 1514.3
 C12 = 1514.4

This PCB Contains:

- ALU for adding/subtracting the mantissa of the greatest exponent (UA) and the shifted mantissa (N)
- Circuits for inverting if negative result out of ALU, (subtract) and to get proper rounding during floating operations.
- Priority encoders looking for the most significant "1" bit in the result mantissa
 - GS = Group (8 bits group)
 - SL = Bit position within the group.
- Carry look-ahead circuits for the ALU.
- Integer overflow detect circuits (OFL).

SHIFT CONTROL - 1515 - POSITION: C19

This PCB Contains:

- Shift-count to shift-right matrix (RSH 0-5) from either
 1. Instruction Register bit 0-5 during shift or bit instructions
 2. Exponent comparison ALU (2A-8A) (Active during Floating ADD/SUB and Floating to Integer instructions)(FIX)
- Operand to internal A bus or B-bus select logic (ATA,ATB)
- Priority encoder looking for the most significant "1" during normalising (Floating SUB) or Integer to Floating (FLO) instruction
- Exponent arithmetic (XP54-62) generating proper exponent during floating ADD/SUB and FLO instructions
- Selector selecting result bit UD 54-62 from shift left matrix (C54-62) or exponent arithmetic
- Shift count to shift-left matrix (LSH 0-5) from either
 1. IR bit 0-5
 - or
 2. Priority encoder (SLZ 0-5)

FLOATING CONTROL - 1516 - POSITION: C20

This PCB Contains:

- One shot determining when data is ready on the SUM bus to CPU (ready signal = RYP) (Set to 400ns)
- Logic decoding CPU Instruction register bit (23-29) active during: shift, bit and convert instructions.
- Driver for the following signals to CPU
 - RYP = Data ready
 - SELBIT = Selected bit during BIT-SKIP instructions
 - FRSBIT = Floating sign bit or floating ZERO (Floating register compare instructions)
 - OF2 = Overflow (floating, floating to integer)
 - UF2 = Underflow (floating)
 - U63 = Sign Bit
- Rounding Logic
 - ADD 02)
 - ADD 01)-Double precision floating
 - ADD 00)
 - ADD 30)
 - PIOFL)-Single precision floating
 - ADD 32)

DATA BUFFER - 1517 - POSITION:

C17 = BIT 0-31
C18 = BIT 32-62

This PCB Contains:

- Buffers for driving the result back to CPU

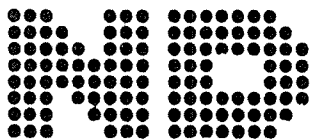
DATA-BUS SELECTOR - 1532.I - POSITION C24

DEVICE REGISTERS - 1531 - POSITION C25

ADDRESS-BUS SELECTOR - 1532.II - POSITION C26

These PCB's Contain:

- The NORD 10/S / NORD 50 Communication Logic
1532.I
- 16 bits differential line driver/receivers NORD 50/NORD 10/S
1531
- NORD 50 modus-register (MO-15)
- NORD 50 status-register (SBO-10)
1532.II
- Receivers for NORD 10/S IOX address bit 0,1 and 5 (IOA0,IOA1,IOA5)
- Receiver for NORD 10/S:
Start signal to NORD 50 (DEVS)
Stop signal to NORD 50 (X STOP)
Signal to start decoding of IOX bit 0,1 and 5 for NORD 10/S / NORD 50
communication register decoding (STROBE)



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COMMENT AND EVALUATION SHEET

NORD-50
General Description and Module Description

ND-05.008.01

January, 1979.

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM

– we make bits for the future

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