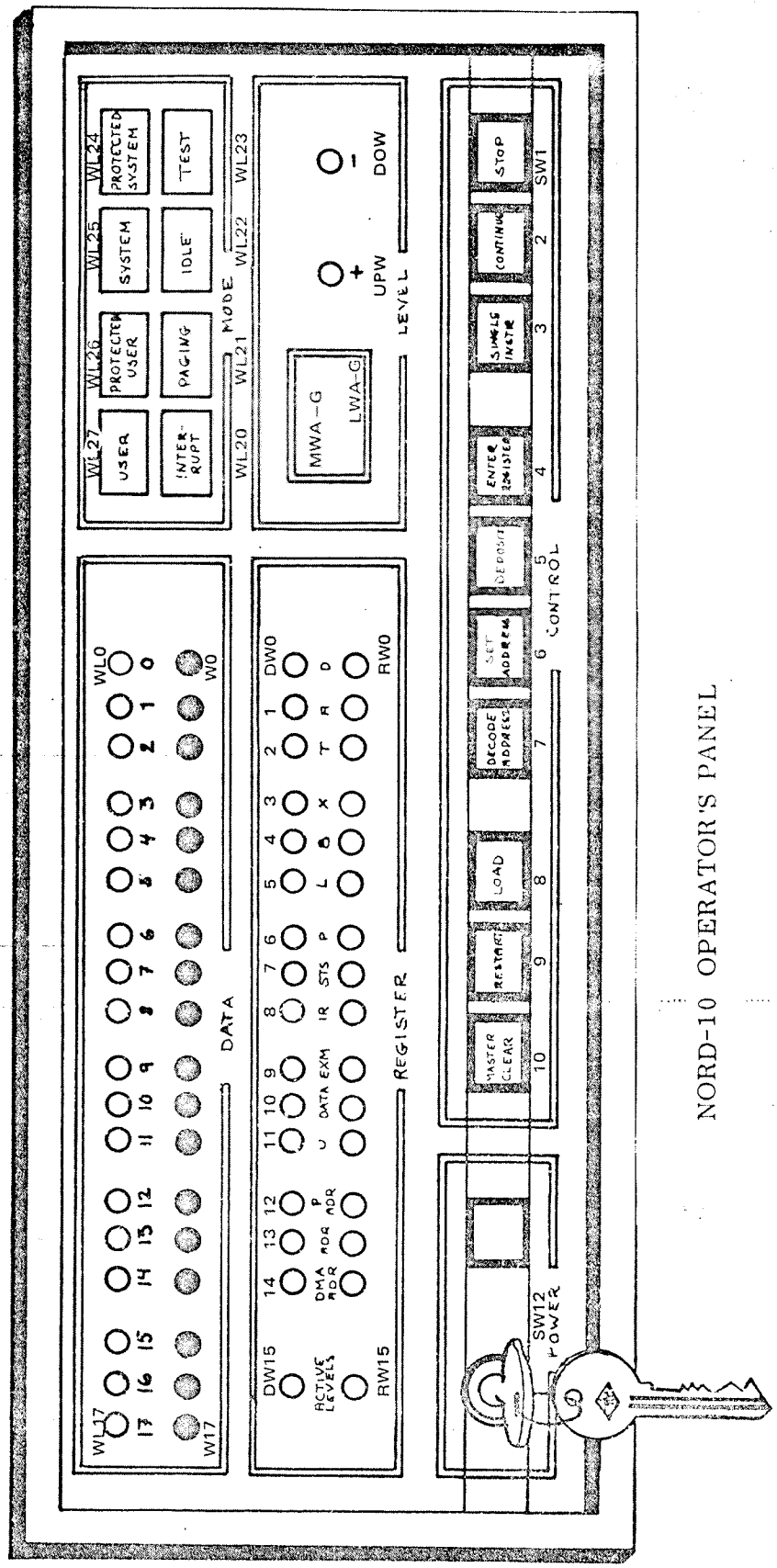
NORD-10
TEH

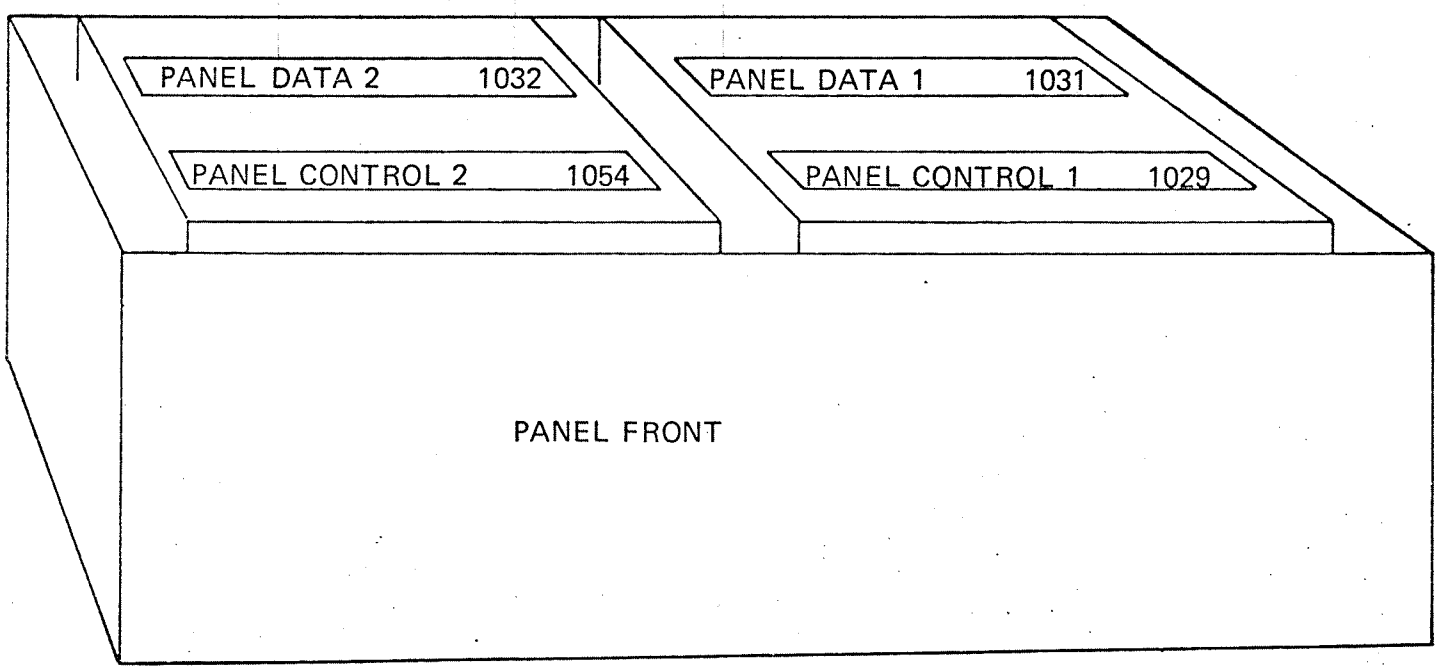
Operator's Panel
Hardware Description

A/S NORSK DATA-ELEKTRONIKK

NORD-10
Operator's Panel
Hardware Description



NORD-10 OPERATOR'S PANEL



PANEL CARD ASSEMBLY LAYOUT

OPERATORS PANEL

GENERAL

This document contains a short description of the functions of the four control cards in Operators Panel. PANEL CONTROL 1 1029 and 2 1054 and PANEL DATA 1 1031 and 2 1032, and the PANEL DRIVER 1033 located in the CPU card rack. POS A17.

A block diagram of these modules are shown in Figure 1.

MAIN DESCRIPTION

The connection (Data Transfer) between the Operators Panel and the CPU is via the 16 bit PANEL BUS(PB). This bus uses 16 time slices for one complete cycle of data transfers. The information on the bus for each time slice is shown in Table 1. The timing control of the bus is located at the PANEL CONTROL 1 (PC1) card, and consists of a 4 Mhz oscillator and a four-bit counter. The oscillator pulses (OSC) and a counter clear signal (CC) is transferred to the PANEL DRIVER (PDR), which has its own four-bit counter running synchronously with the counter on PC1. (Synchronized by CC.)

The PANEL DRIVER module 1033 has two additional "registers" which has no connection to the functioning of the panel. That is DECODED PIL (A0-15) and the Automatic Load Descriptor (ALD, CO-15). These are read by the microprogram with TRA9 or TRA10 respectively.

The OPERATORS PANEL is controlled both by the operator and the CPU microprogram. Control information is exchanged by using the TRA0 instruction to read panel status information and the TRR instruction to execute panel control functions.

When the CPU is in STOP-mode the panel status is read repeatedly (Frequency determined by micro program loop). In RUN-mode the micro-program servicing the panel is entered only every time the CPU receives a panel interrupt signal transferred via PB-bus as bit 12 on timing cycle 3, 7, 11, and 15, every 2,5 ms.

The main program is not interrupted if one of the following buttons is pushed: ACTIVE LEVELS, DMA ADR, PADR, U, DATA, IR. This is called a NOOP condition): No operation wanted by microprocessor.

Note that pushing ENTER REGISTER when a CPU-register is <u>not</u> selected is also a no-operation.

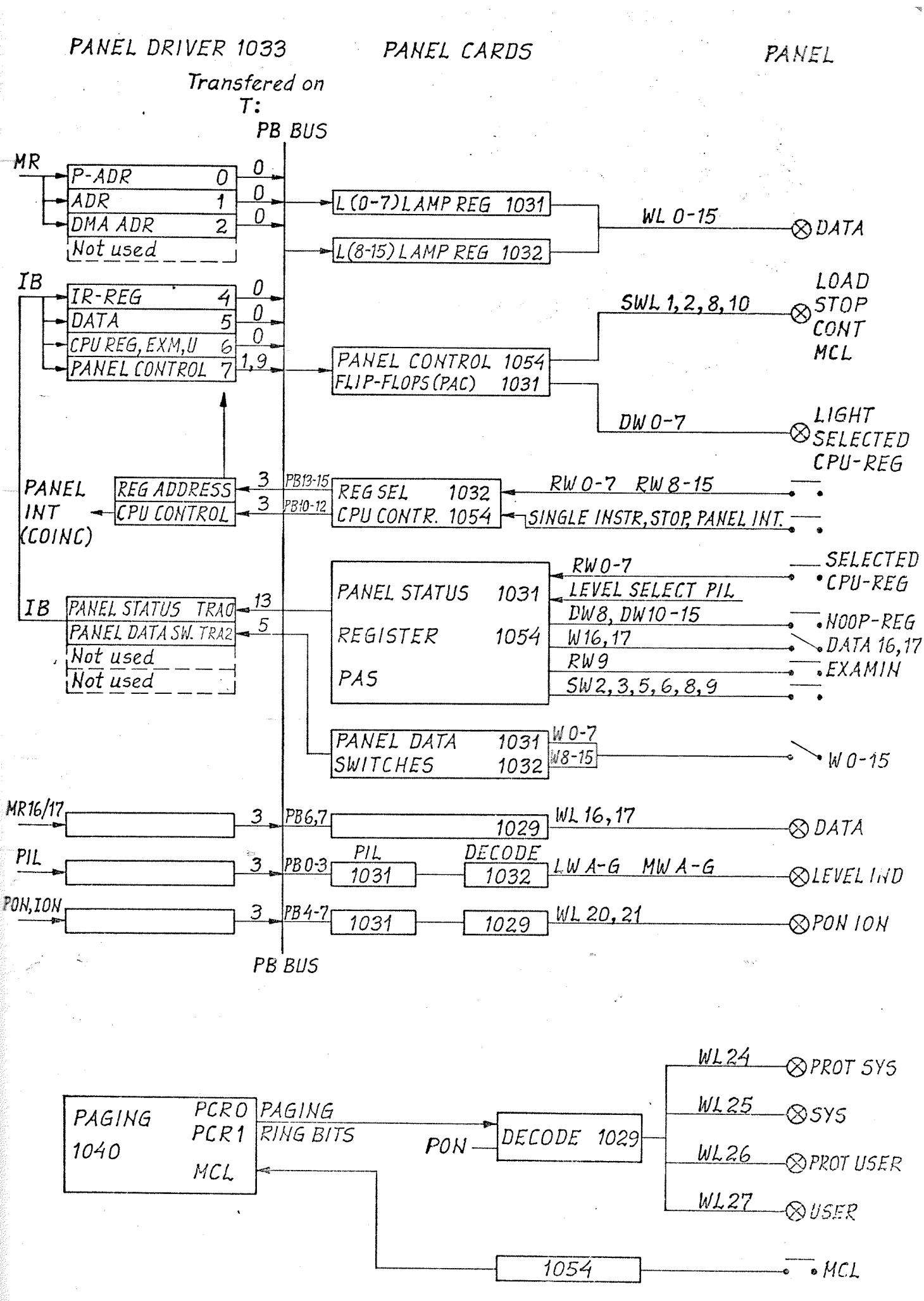


Figure 1 NORD-10 OPERATORS PANEL

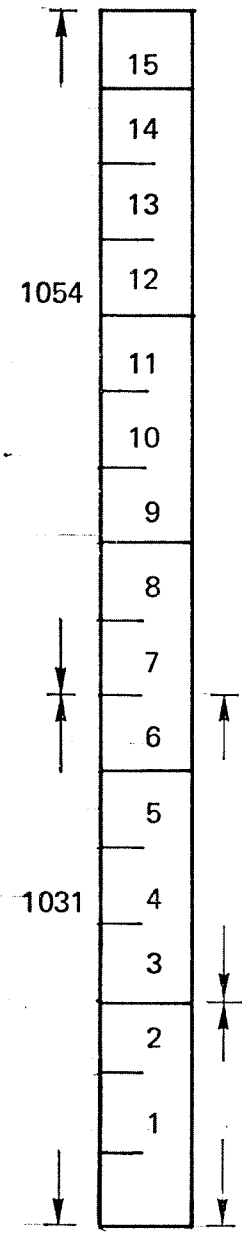
	PANEL DRIVER	PANEL CARDS
0	Selected register	→ L (General buffer)
1	Panel control	→ Control flip-flops
2	As 0	
3	PIL, PON, ION, MR16/17 Reg. adr. and CPU-control	→ Bufferregister ← Register selection and SINGL. INSTR. STOP and PANEL INTER-RUPT.
4	As 0	
5	Panel data reg.	← Panel data switches
6	As 0	
7	As 3	
8	As 0	
9	Panel control	→ Control flip-flops
10	As 0	
11	As 3	
12	As 0	
13	Panel status reg.	← Panel status reg.
14	As 0	
15	As 3	

Table 1 — Panel Bus Transfer Timing

Debugging Hint:

When the CPU-register selector-switches STS, D, P, B, L, A, T, X are functioning properly the microprogram is responding correctly, reading panel status and setting panel control. To check transfer of status-register from panel to Panel Data Register via PB-bus use CC (the best oscilloscope triggering signal for all check of PB, 1029 term 91 - Panel Data Reg 1) and look at time slice T13. Refer to Figure 2. For further check of transfer to CPU H-register via IB use TRA0 for triggering. For check of panel control work transfer via IB TRA0 may also be used for triggering, but look at the first TRR0 following TRA0. Note that the echo of the level code is not used by the panel. Instead the level code is sampled into a 4-bit buffer register from PB when panel status is enabled to PB in time slice T13. See Panel Data 1 (1031/8B).

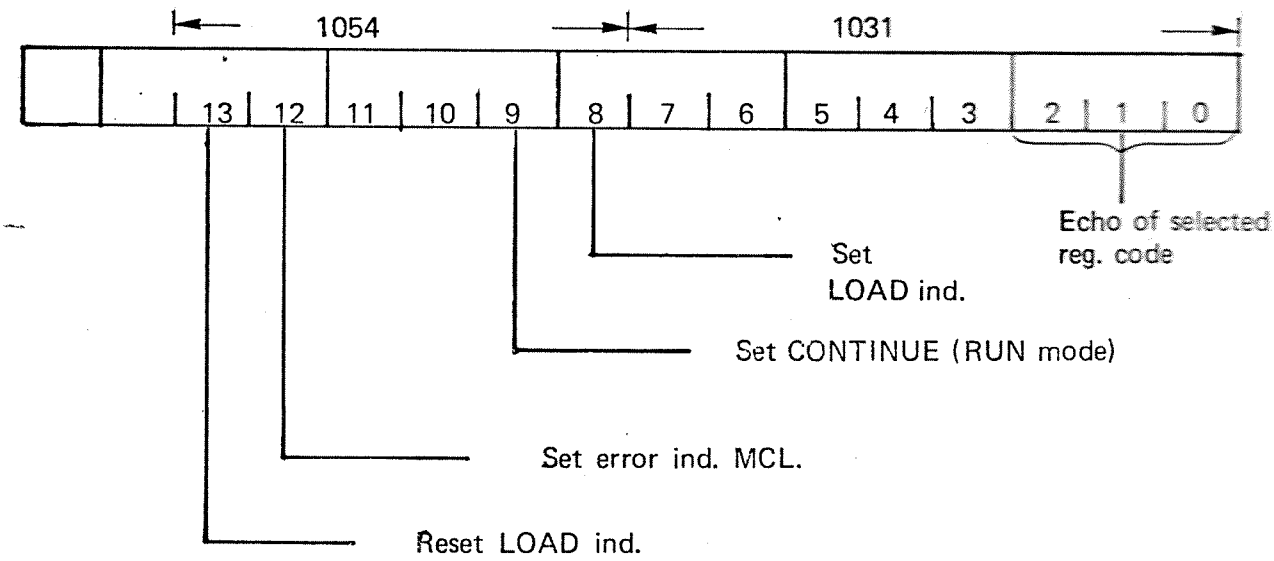
PAS – PANEL STATUS REGISTER



15	W17	- Switch register bit 17.
14	W16	- Switch register bit 16.
13	NOOP	- No operation. The content of Lamp Register(LMP) is not changed by microprogram.
12	SET ADR	- Set by pushing "SET ADDRESS" button, reset after first TRA PAS or "ENTER REGISTER" buttons.
11	DEP	- Set by "DEPOSIT", reset after first TRA PAS.
10	REST	- Set by "RESTART" buttons, reset after first TRA PAS.
9	SI+CONT	- Set by "SINGLE INSTRUCTIONS" or "CONTINUE", reset after first TRA PAS.
8	LOAD	- Set by "LOAD" button, AUTO LOAD or REMOTE LOAD function, reset after first TRA PAS.
7	EXAM	- Set by pushing "EXAM" select button.
6		
5		
4	LEVEL	- Code of selected level for register display.
3		
2		
1	REG	- Code of selected register for register display (STS, D, P, B, L, A, T, X).

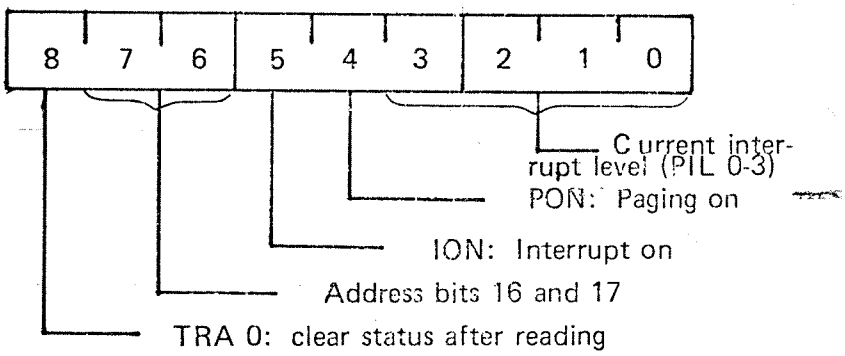
After reading panel status, the microprogram returns the panel control word using the TRR0 instruction (Transferred via PB on T1/T9).

PAC – OPERATORS PANEL CONTROL REGISTER



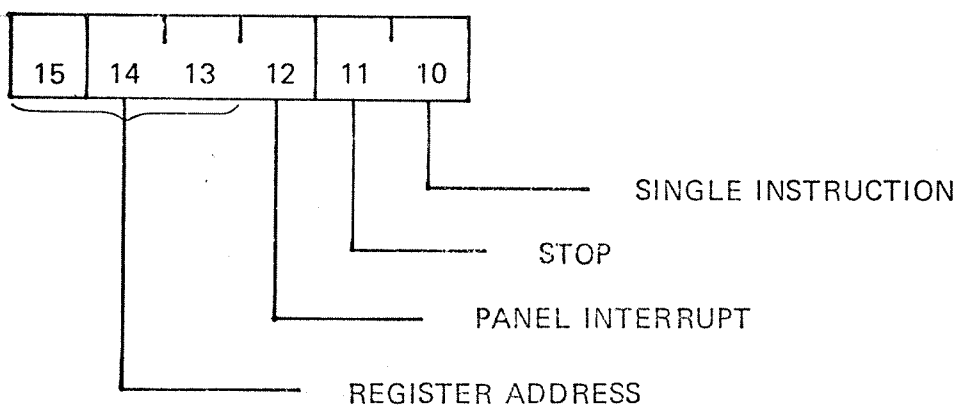
SIGNALS TO PANEL VIA PB BUS

Enabled on the PB bus with PLE signal in T3, T7, T11 and T15.



CONTROL SIGNALS FROM PANEL VIA PB BUS TO PANEL-DRIVER

Enabled on the PB bus with CE signal in T3, T7, T11 and T15.



Register	Operation Register Switch	Code	CPU Reg.	Reg. Addr. (RA (15A 1033) (Internal Trans. Code)	Panel Interrupt
D	0	1 ↑	X	6	X
A	1	5 Register	X	6	X
T	2	6 Code	X	6	X
X	3	7 1031	X	6	X
B	4	3 Output	X	6	X
L	5	4 12A	X	6	X
P	6	2	X	6	X
STS	7	0 ↓	X	6	X
IR	8	4 ↑		4	NO
EXM	9	7 Register		6	X
DATA	10	5 Code		5	NO
U	11	6 RC		6	NO
P.ADR	12	0 1032		0	NO
ADR	13	1 Output		1	NO
DMA ADR	14	2 14B		2	NO
ACTIVE LEVEL	15	3 ↓		No signif-icance	

NO = NOOP

Reg. Address:	Reg.:	Set By:
0	P. ADR	MDRY. FETCH
1	ADR	MDRY. $FETCH_0$ $DMAGRANT_0$
2	DMA.ADR.	MDRY. DMAGRANT
4	IR	MDRY. FETCH.
5	DATA	MDRY. $FETCH_0$ $DMAGRANT_0$
6	LMP	TRR2
7	PAC	TRR0

LMP code = 6 = U, EXM, STS, P, L, B, X, T, A, D.

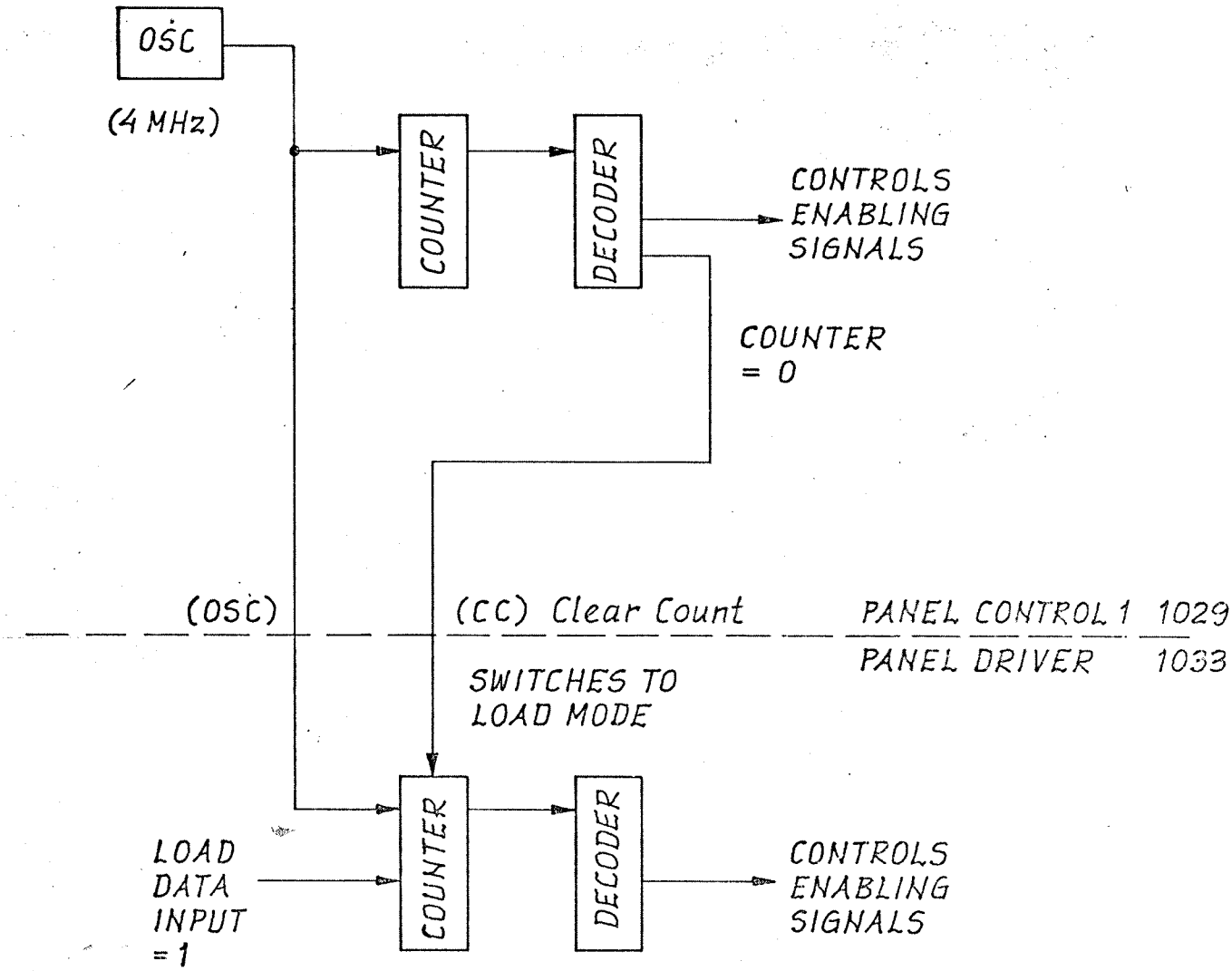
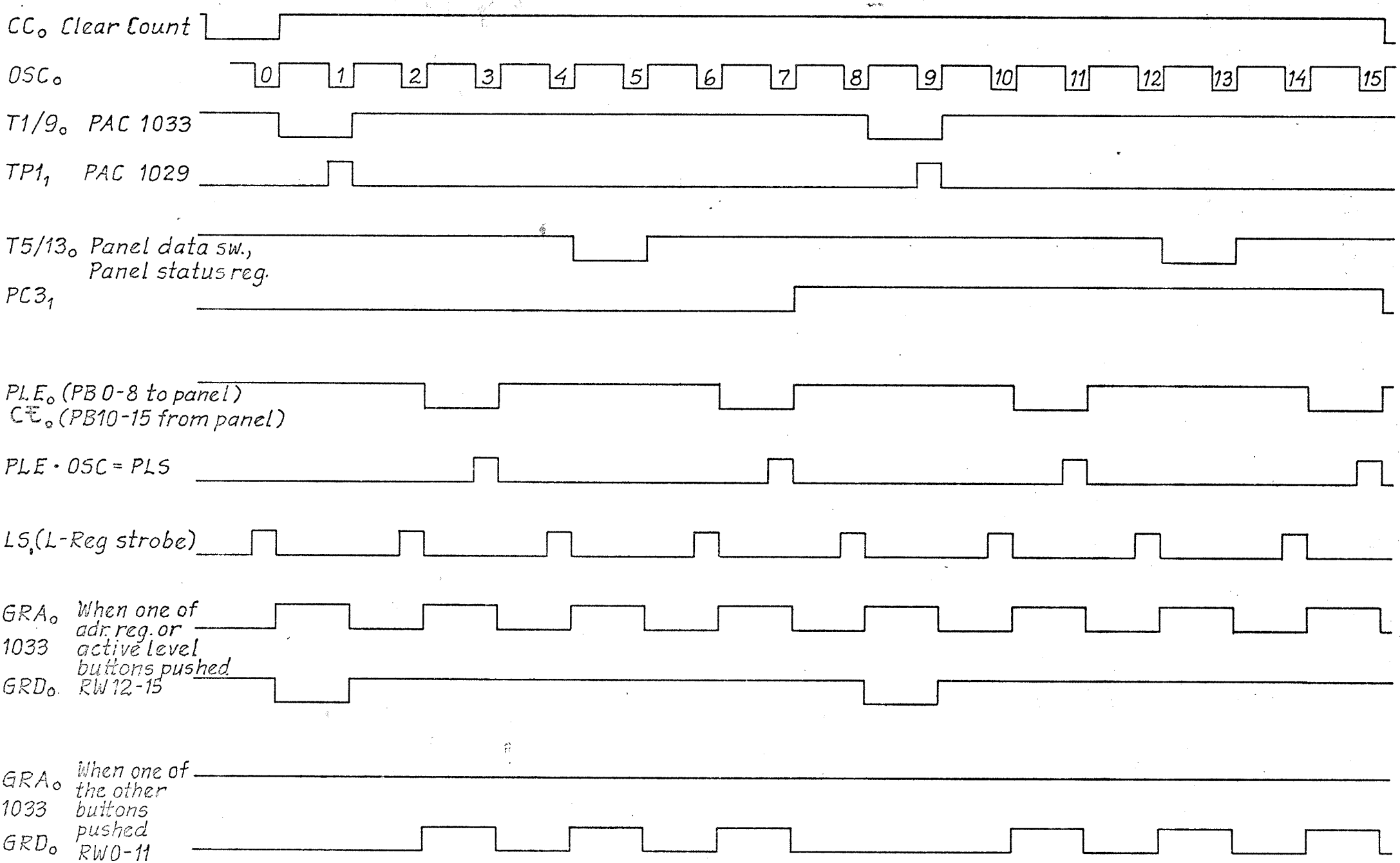


Figure 2 PANEL TIME PULSES GENERATION

PANEL TIMING



SIGNAL DEFINITION LIST

SIGNAL DEFINITION LIST

ADREN	1032	Enables light in bits 16 and 17 of lamp register in case of display of address and no address decoding.
CARRY	1031	UP (COUNTER = 15) DOWN (COUNTER = 0), which stops level select counter and enables current level defined by PIL.
CC	1029	Clear Counter. Transferred to Panel Driver 1033 and used to synchronize counters in panel and Panel Driver. CC = $TCO_0 1_0 2_0 3_0$
CE	1029	Control Enable, i.e. enable control signals to PB in T3, T7, T11 and T15 for transfer to Panel Driver (for bits 9 to 15 only).
CPUR	1054	CPU-register selected by panel switches, i.e. one of the registers D, A, T, X, B, L, P, STS.
CSB	1032	Strobe pulse to monostable "stretching" circuits. Occurs on TP1, TP5, TP9, and TP13 if ACTIVE LEVELS are selected. In the case of DECODE ADDRESS for the pulse above and TP3, TP7, TP11, and TP15.
DDx	1031	Digital Display signals in two digit binary coded decimal code. For source see PLE.
DECODE	1054	On/Off flip-flop complemented by Decode Address switch. DECODE signal is on when button is lighted.
DOW	P.S.	Signals from –button in LEVEL field.
DWxx	1031/32	Lamp signals to selected register indicator lamp (T, A, D, etc.).

Signal Definition List, continued

EXAM	1054	Panel status bit 7. EXAM = $CPUR_0 \cdot EXM_1$.
EXM	1032	Control flip-flop which is set to one by pushing EXM select switch and reset by pushing IR or any select switch to the left of EXM.
IDLE	1032	Decoding of PIL = 0, which drives IDLE indicator light.
ION	1031	Interrupt system on, same as corresponding CPU signal, transferred via PB5.
LCx	1032	Level Code (=PIL) or memory address block number defined by memory address bits 12 to 15. Used as input to active level decoding or decoded address.
LE	1032	If LE is true the content of the L (LMP) register (set by TRR2) controls the lamps in the DATA field of the panel. If LE is not true the lamps are controlled by the LC-decoder.
LS	1029	Strobe pulse to L register which transfers the content of LMP from Panel Driver 1033 via PB.
LWA	1029	Control signal which lights the A-segment of the lease significant display digit.
MCL	1054	Master Clear signal generated as a low level pushing MASTER CLEAR button.
MWA	1029	Control signal which lights the A-segment of the most significant display digit.
NOOP	1054	No Operation wanted by micro-processor in STOP mode. Transferred to CPU as panel interrupts when CPU is running. NOOP is true when any of the registers ACTIVE LEVELS, DMA, ADR, ADR, PDR, U, DATA, or IR is selected.

Signal Definition List, continued

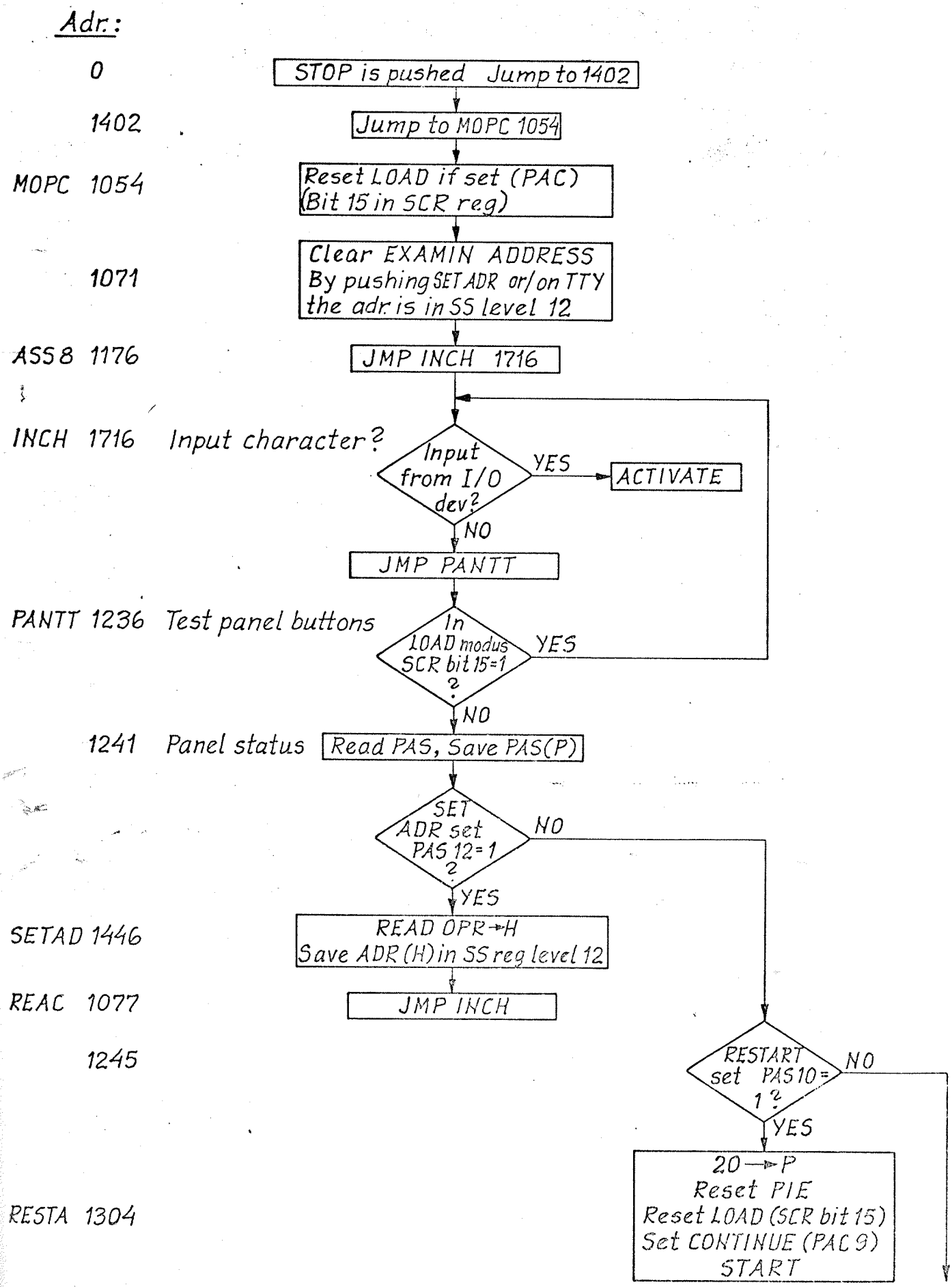
OSC	1029	Panel clock pulses, also transferred to Panel Driver (1033). Frequency: 4MHz (250ns).
PBxx	All	Wired OR data bus between panel cards and Panel Driver (1033). Two-way multiplexed communication.
PCRx	Paging Reg. 1040	Ring bits in CPU paging control.
PLE	1029	Enables PL (=PIL) as level code to the micro-processor as bits 3 to 6 in the panel status word. PLE becomes true if level counter is 15 and the + button is pushed or if level counter is 0 and the – button is pushed.
PLS	1029	Strobes PB bus into PL flip-flops and PON/ION flip-flops.
PON	1031	PAGING ON mode in CPU, same as corresponding signal in CPU, transferred via PB4.
RO/7	1031	True when any of the register select buttons 0-7 are pushed (D, A, T, X, B, L, P, STS).
R8/15	1032	True when any of the register select buttons are pushed (IR, EXM, DATA, U, PADR, ADR, DMA-ADR, ACTIVE LEVELS).
PLx	1031	Equal to PIL in CPU. Transferred from CPU via 1033 and PB.
RWxx	P.S.	Signals from register select switches.
STEP	1029	Single pulse generated by pushing + or – button in the level field of the panel.

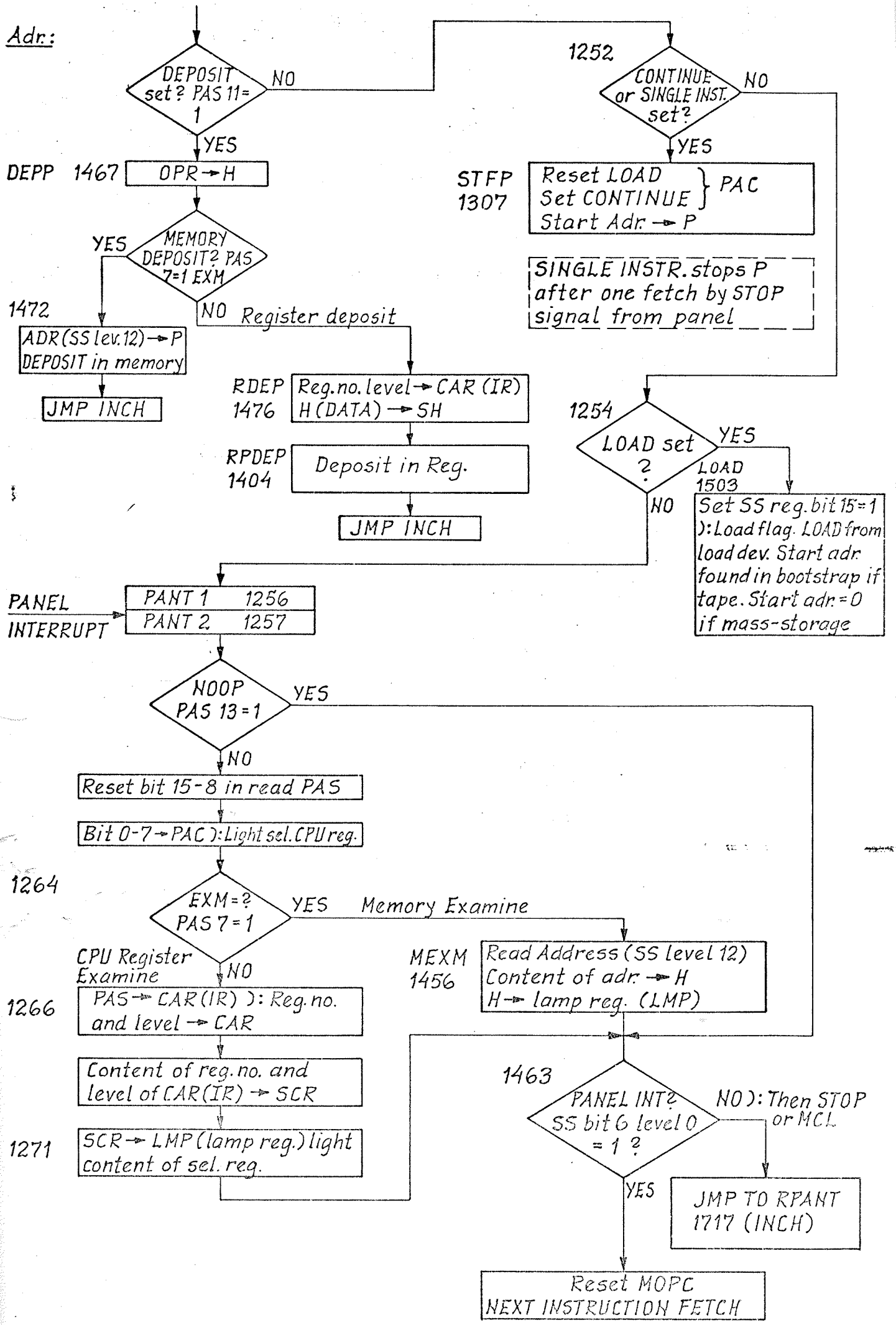
Signal Definition List, continued

SSTOP	1033	Stop signal from CPU (WAIT instruction when interrupt is off or FETCH and SINGLE INSTRUCTION).
SWxx	P.S.	Signals from panel control switches (push buttons).
TCx	1029	Time Counter flip-flops 4-bit binary counter.
TEST		Not used. Connected to GND.
TPx	1029	Corresponding T-signals gated with OSC.
Tx	1029	Decoded Time Counter states.
UP	1029	Control flip-flop set to one by pushing + button in level field. Set to zero by pushing −, $UP_0 = DOWN_1$.
UPW	P.S.	Signal from + button in level field.
Wxx	P.S.	Signals from panel data switches.
WLxx	1031/32	Signals to panel data indicator lights. See also LE.

THE MICROPROGRAM AND THE PANEL

THE MICROPROGRAM AND THE PANEL




Adr:
DEPOSIT set? PAS 11=1
NO
YES
1252
CONTINUE or SINGLE INST. set?
NO
YES
DEPP 1467
OPR → H
STFP 1307
Reset LOAD
Set CONTINUE
Start Adr. → P
PAC
SINGLE INSTR. stops P after one fetch by STOP signal from panel
YES
MEMORY DEPOSIT? PAS 7=1 EXM
1472
ADR (SS lev. 12) → P
DEPOSIT in memory
JMP INCH
NO Register deposit
RDEP 1476
Reg.no. level → CAR (IR)
H (DATA) → SH
RPDEP 1404
Deposit in Reg.
JMP INCH
1254
LOAD set ?
YES
LOAD 1503
Set SS reg. bit 15=1): Load flag. LOAD from load dev. Start adr found in bootstrap if tape. Start adr = 0 if mass-storage
NO
PANEL INTERRUPT
PANT 1 1256
PANT 2 1257
NOOP PAS 13=1
YES
NO
Reset bit 15-8 in read PAS
Bit 0-7 → PAC): Light sel. CPU reg.
1264
EXM=? PAS 7=1
YES
Memory Examine
CPU Register Examine
NO
MEXM 1456
Read Address (SS level 12)
Content of adr. → H
H → lamp reg. (LMP)
1266
PAS → CAR (IR)): Reg.no. and level → CAR
Content of reg.no. and level of CAR (IR) → SCR
1271
SCR → LMP (lamp reg.) light content of sel. reg.
1463
PANEL INT? SS bit 6 level 0 = 1 ?
NO): Then STOP or MCL
YES
JMP TO RPANT 1717 (INCH)
Reset MOPC
NEXT INSTRUCTION FETCH

PANEL INTERRUPT

The Entry Point Generator is by hardware set to address 1000. If a panel interrupt occurs:

The CPU is not in STOP mode): in CONTINUE and one of the following buttons have been pushed:

EXM or one of the CPU reg.: STS,P, L, B, X, T, A or D.

The Panel Interrupt signal is transferred to CPU every 2,5 ms (OSC 1054) on one of the following panel timing pulses:

T3, 5, 7, 11, or 15 [PB12 → COINC (1033), COINC → OPINT (1058) OPINT → CARD MICROADDRESSING 1075]

1000/JMP TO PANINC 1226

PANINC 1266/

Set MOPC (Flip-flop preventing internal interrupts and force the CPU to use reg. set on level 0.

↓

Read PANEL STATUS REG (PAS) → P
The interrupt signal is reset by TRA TRO (TRAPAS 1054)

↓

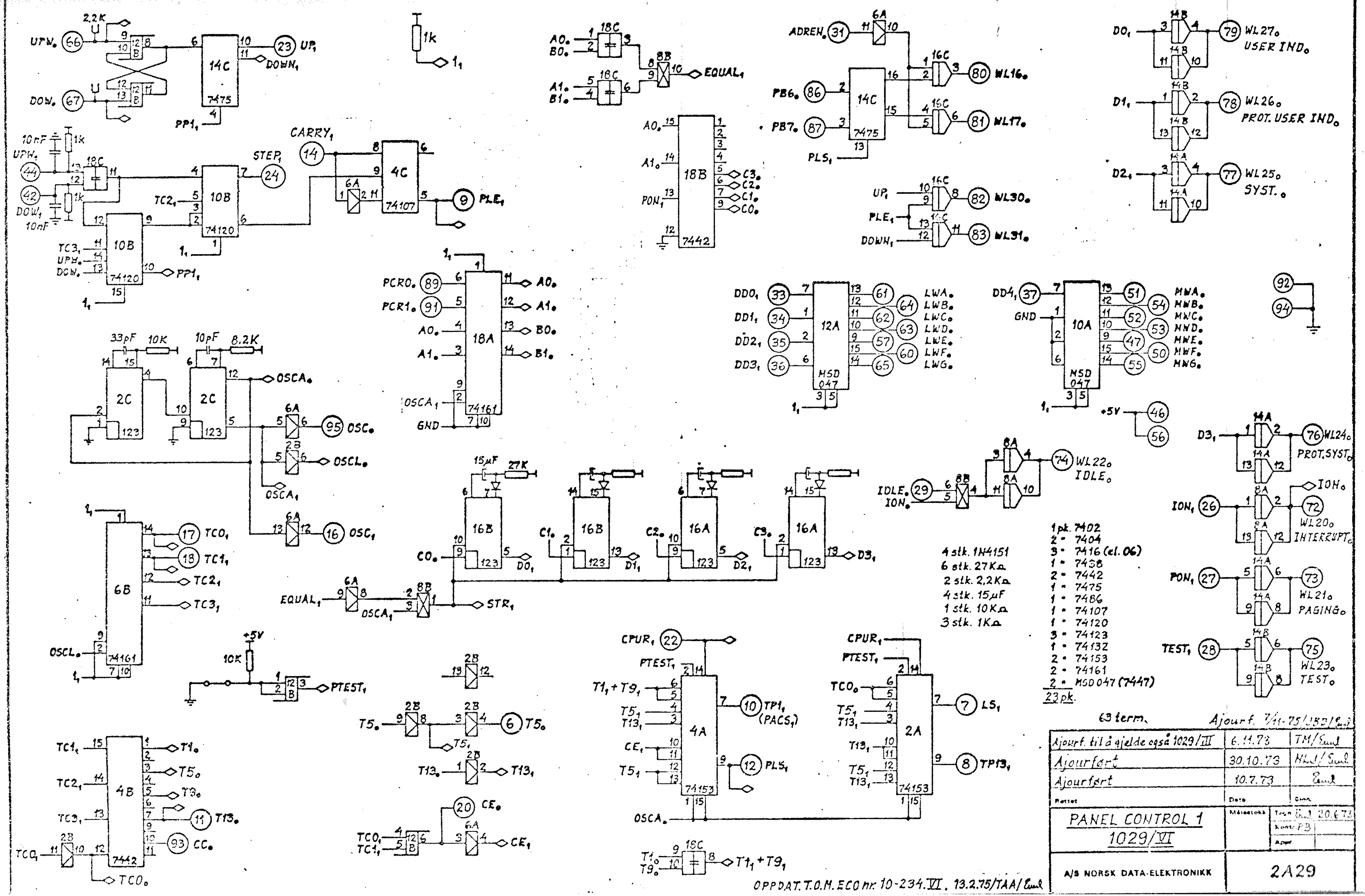
Set bit 6 (Panel interrupt flag) (SS level 0)

↓

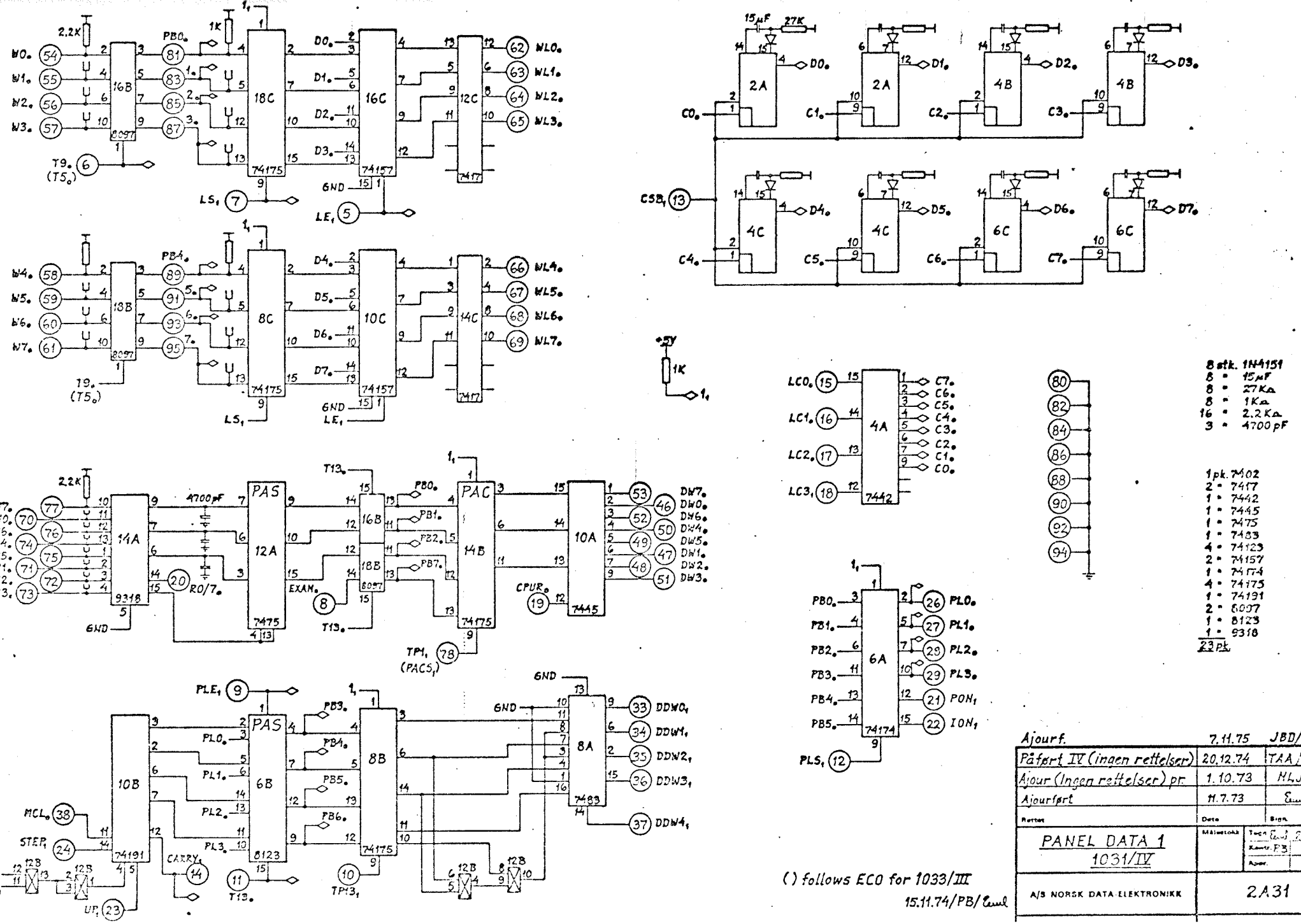
JMP TO PANT2 1257

↓

DRAWINGS

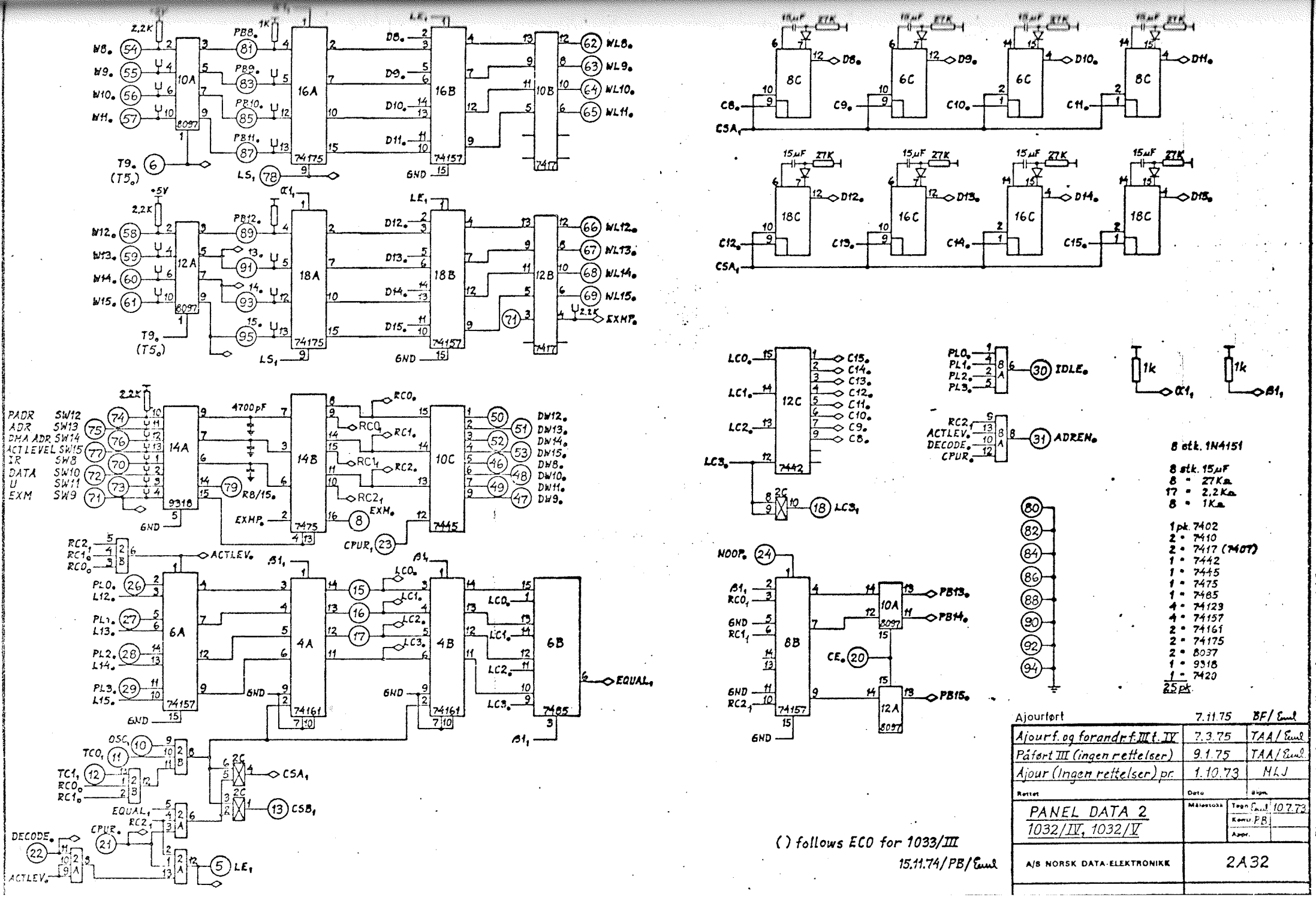


PANEL CONTROL 1
1029/VI
A/S NORSK DATA-ELEKTRONIKK
2A29
Ajourf. til å gjelde også 1029/III 6.11.73 TM/
Ajourført 30.10.73
Ajourført 10.7.73
Rettet
Dato
Målestokk
Tegn. 20.6.73
Kontr. PB
Appr.
Ajourf. 7/11-75
OPPDAT. T.O.M. ECO nr. 10-234.VI, 13.2.75/TAA/
63 term.
4 stk. 1N4151
6 stk. 27KΩ
2 stk. 2,2KΩ
4 stk. 15μF
1 stk. 10KΩ
3 stk. 1KΩ
1 pk. 7402
2 • 7404
3 • 7416 (el. 06)
1 • 7438
2 • 7442
1 • 7475
1 • 7486
1 • 74107
1 • 74120
3 • 74123
1 • 74132
2 • 74153
2 • 74161
2 • MSD 047 (7447)
23 pk.



() follows ECO for 1033/III
15.11.74/PB/Emil

Ajourf.	7.11.75	JBD/Emil
Påført IV (ingen rettelser)	20.12.74	TAA/Emil
Ajour (Ingen rettelser) pr.	1.10.73	HLJ
Ajourført	11.7.73	Emil
Rettet	Dato	Sign.
PANEL DATA 1 1031/IV	Målestokk	Tegn Emil 28.6.73 Kontr. PB Godkj.
A/S NORSK DATA ELEKTRONIKK		2A31



8 stk. 1N4151

8 stk. 15µF
8 • 27Kø
17 • 2,2Kø
8 • 1Kø

1 pk. 7402
2 • 7410
2 • 7417 (7407)
1 • 7442
1 • 7445
1 • 7475
1 • 7485
4 • 74123
4 • 74157
2 • 74161
2 • 74175
2 • 8037
1 • 9318
1 • 7420
25 pk

( ) follows ECO for 1033/III
15.11.74/PB/Eml

Ajourført	7.11.75	BF/Eml
Ajourf. og forandr.f.III t. IV	7.3.75	TAA/Eml
Påført III (ingen rettelser)	9.1.75	TAA/Eml
Ajour (Ingen rettelser) pr.	1.10.73	MLJ
Rettet	Dato	Sign.

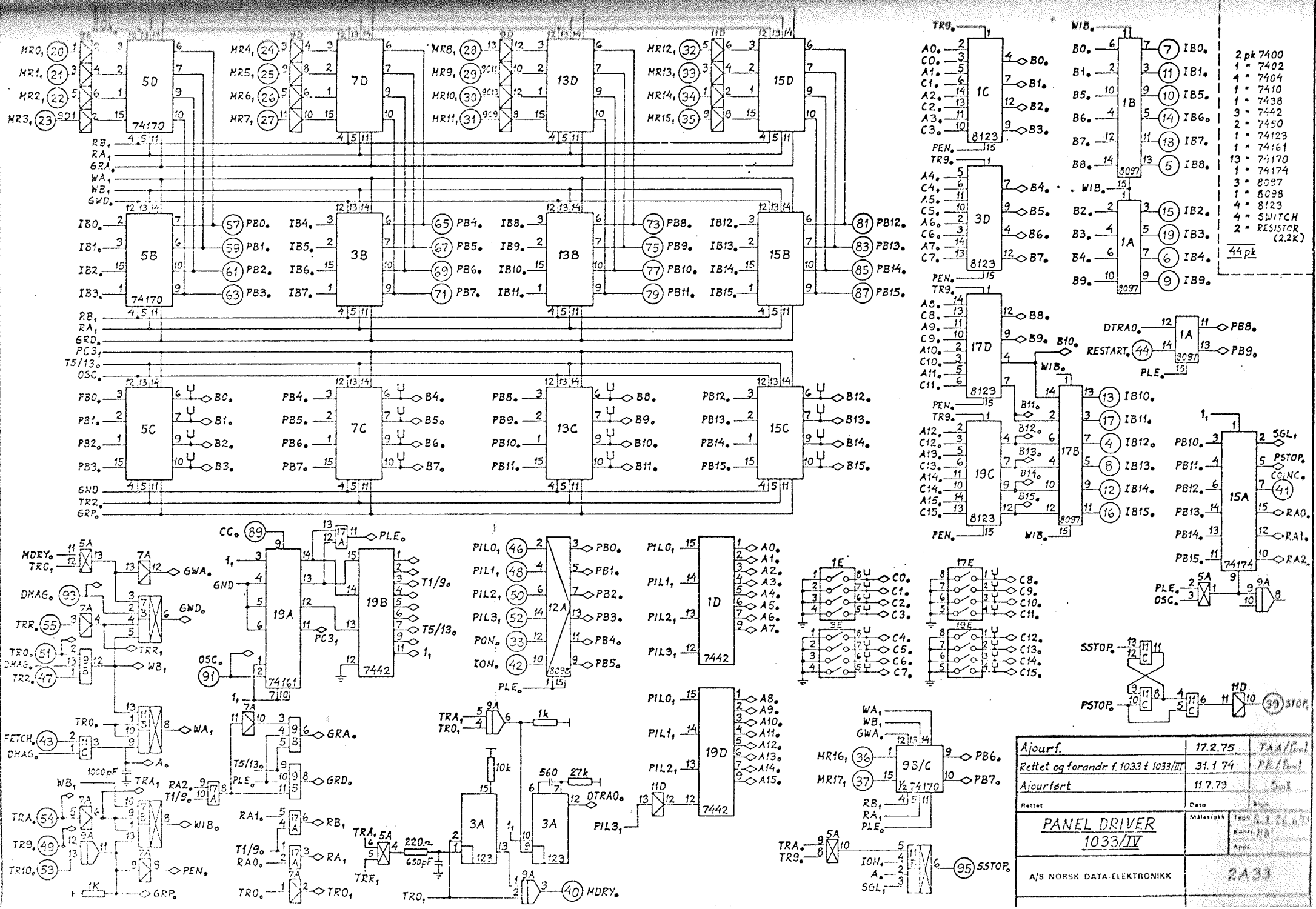
PANEL DATA 2
1032/IV, 1032/V

Målestokk | Tegn. Eml 10.7.73 | Kontr. PB | Appr.

A/S NORSK DATA-ELEKTRONIKK

2A32

Påført 1032/IV (ingen rettelser) 9.12.75/TAA/Eml



Ajourf.	17.2.75	TAA/Emil
Rettet og forandr. f. 1033 t. 1033/III	31.1.74	PB/Emil
Ajourført	11.7.73	Emil
Rettet	Dato	Sign

PANEL DRIVER
1033/IV

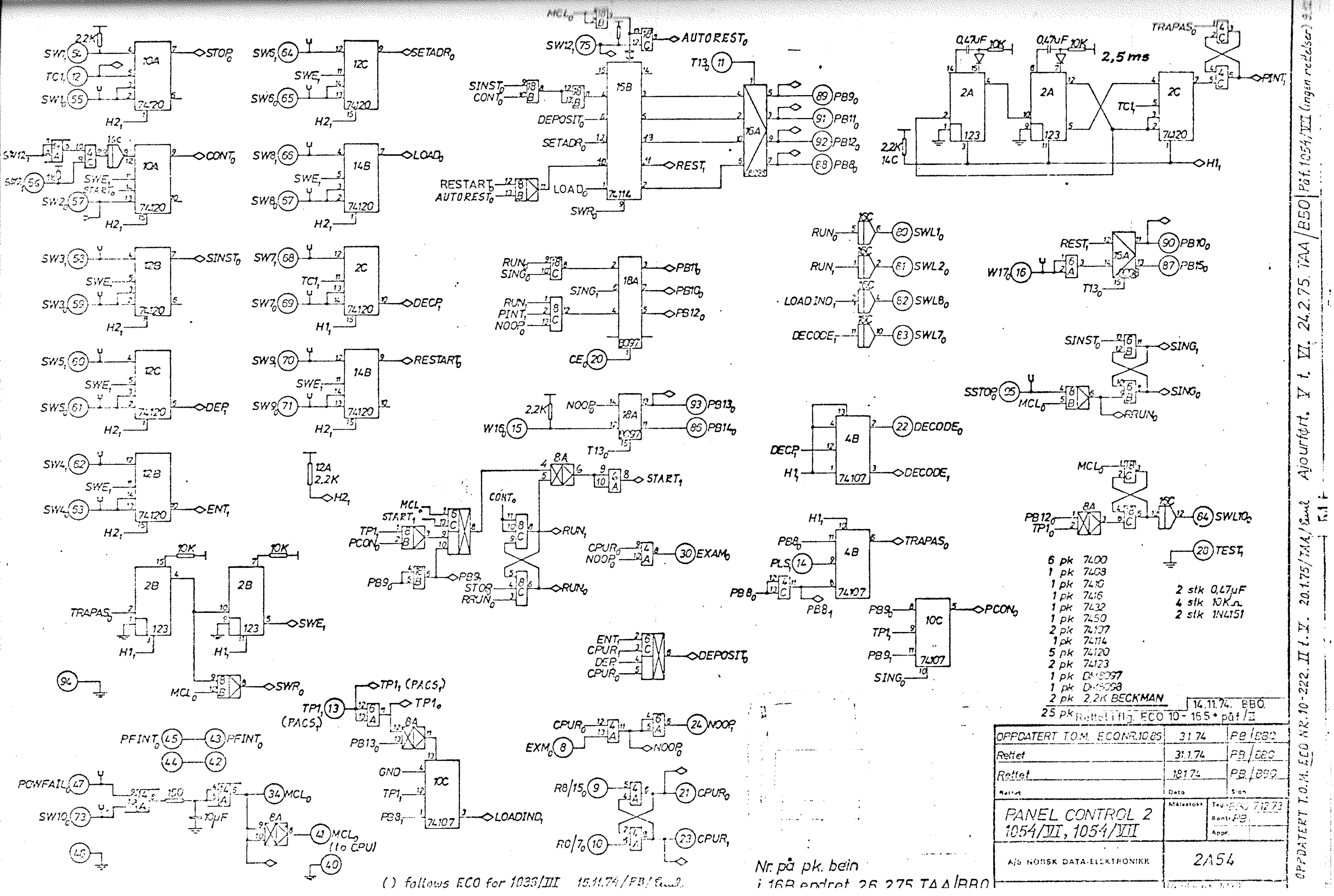
Målestokk

Tegn. Emil 26.6.72
Kontr. PB
Appr.

A/S NORSK DATA-ELEKTRONIKK

2A33

OPPDATERT T.O.M. ECO NR 10-215. III HI IX. 17.1.75/TAA/Emil



OPPDATERT T.O.M. ECONR.10.85	3.1.74	PB/BBO
Rettet	31.1.74	PB/BBO
Rettet	18.1.74	PB/BBO

PANEL CONTROL 2
1054/VI, 1054/VII

A/S NORSK DATA-ELEKTRONIKK — 2A54

– we want bits of the future

A/S NORSK DATA-ELEKTRONIKK LØRENVEIEN 57 OSLO 5 NORWAY PHONE: 21 73 71 TELEX: 18284