NORSK DATA A.S

C O N T E N T S N D - 5 0 0

NORSK DATA A.S

COMPUTER CONFIGURATION **ND-500**

S/N	PROJECT NO.	ISSUED BY	DATO	CUSTOMER

POWER SUPPLIES

	PRODUCER	TYPE	VOLTAGE	SERIAL NO.	REMARKS
CPU-RACK L	E M I	ESP 27I/2	+5V		
" " R	E M I	ESP 27I/2	+5V		
MEMORY	E M I	ESP 27I/2	+5V		
MEMORY STB	TORE SEEM	S 6005	+5V/+I2V		
OTHER CONTR.PANL	E M I	EMP 325			
POWER PANEL					

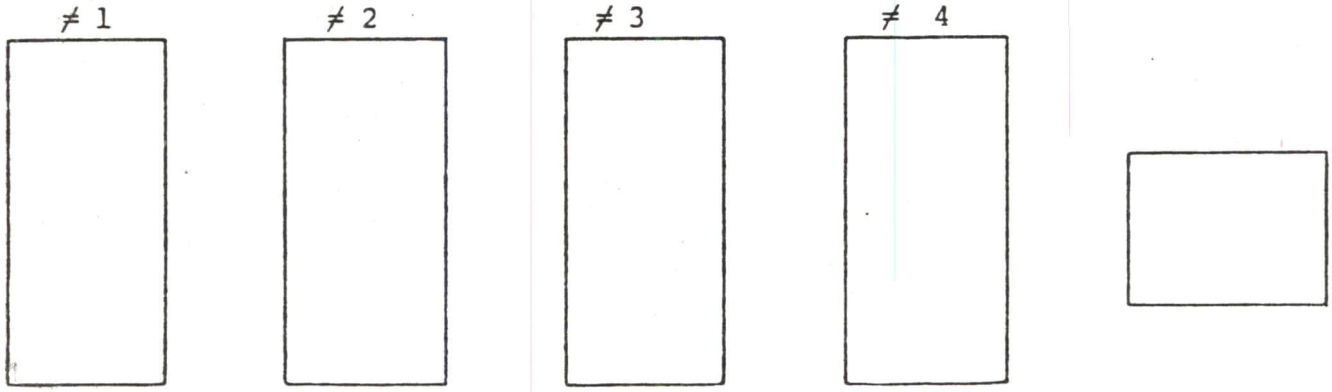
MEMORY

	CACHE-MEM.		BIG MPM	
MEM.MAN			BANK X	BANK Y
CACHE YES				
SIZE/BIT AT				
TYPE				
MODUL SIZE				
ECC				

CABINET

CABINET TYPE			
NUMBER OF CARD RACKS			
NUMBER OF FREE N-500 SLOTS			
NUMBER OF FREE MPM - SLOTS			
NUMBER OF MPM-PORTS IN USE			
ND 500 OP. PANEL	YES		
	YES / NO		
		POWER DISTRIBUTION 322763	
PLUG PANEL			

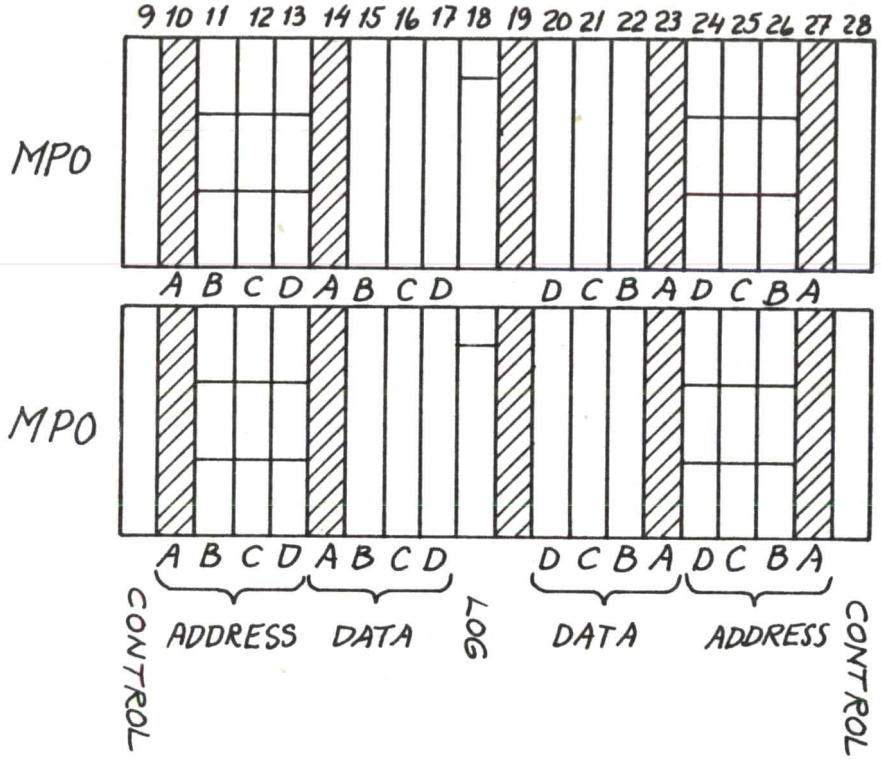
MODULE LOCATION



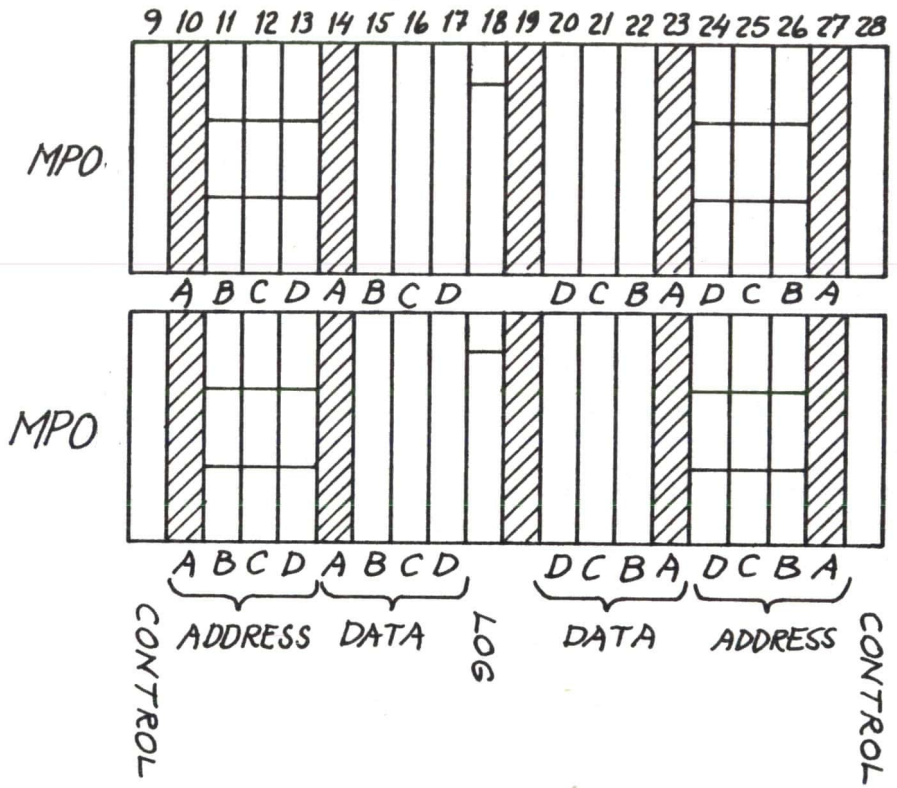
SLOT NO	N-500 CARD ASSEMBLY		
	CARD NAME	PRINT NO	ECO LEVEL
1	CACHE INB 3	5007.4	
2	CACHE INB 2	5007.3	
3	CACHE INB 1	5007.2	
4	CACHE INB 0	5007.1	
5	CACHE CONTROL INSTB.	5017	
6	CACHE DATB 3	5007.4	
7	CACHE DATB 2	5007.3	
8	CACHE DATB 1	5007.2	
9	CACHE DATB 0	5007.1	
10	CACHE CONTROL DAT.B.	5017	
11	MEM. MAN. INSTR. (ADDR.DRIVER)	5005 (5013)	
12	MEM. MAN. DATA (ADDR.DRIVER)	5005 (5013)	
13	CONTROL II	5015	
14	PREFETCH	5018	
15	CONTROL I	5012	
16	TRAP	5019	
17	CONTROL STORE	5020	
18	SEQUENCER	5004	
19	CPU-SLICE	5001.4	
20	CPU-SLICE	5001.3	
21	CPU-SLICE	5001.2	
22	CPU-SLICE	5001.1	
23	ARITH. 1	5008	
24	ARITH. 2	5009	
25	ARITH. 3	5011	
26	ARITH. 4	5014	
27	SPARE		

BMPM SWITCH SETTING

BMPM in N100 Cabinet



BMPM in N500 Cabinet

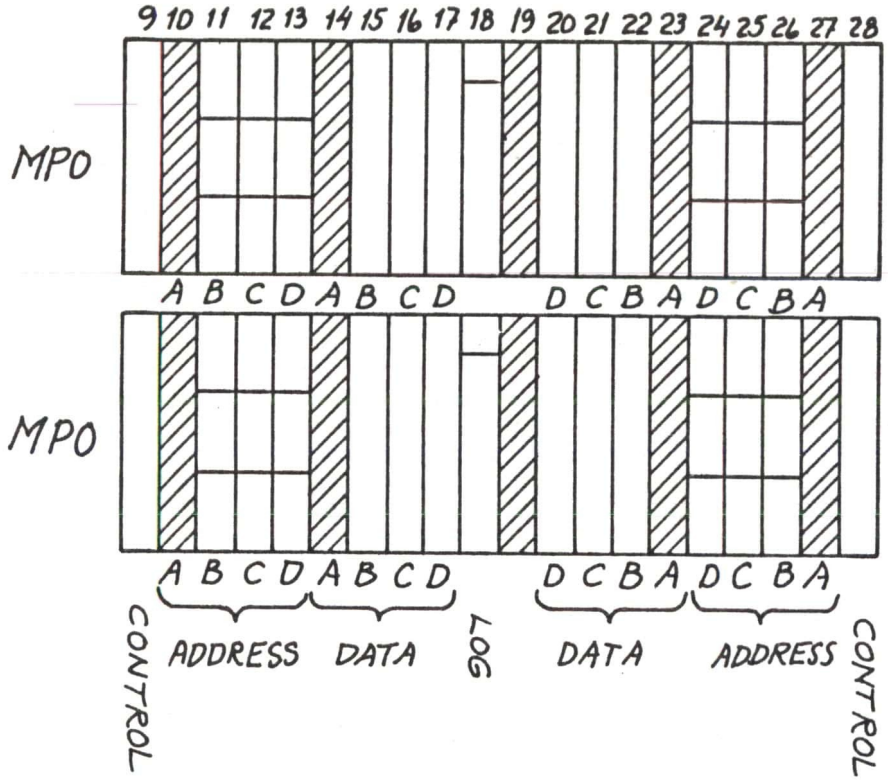


CHANNEL	A	NOT IN USE
— " —	B	N 100
— " —	C	N 500 INSTR.
— " —	D	N 500 DATA

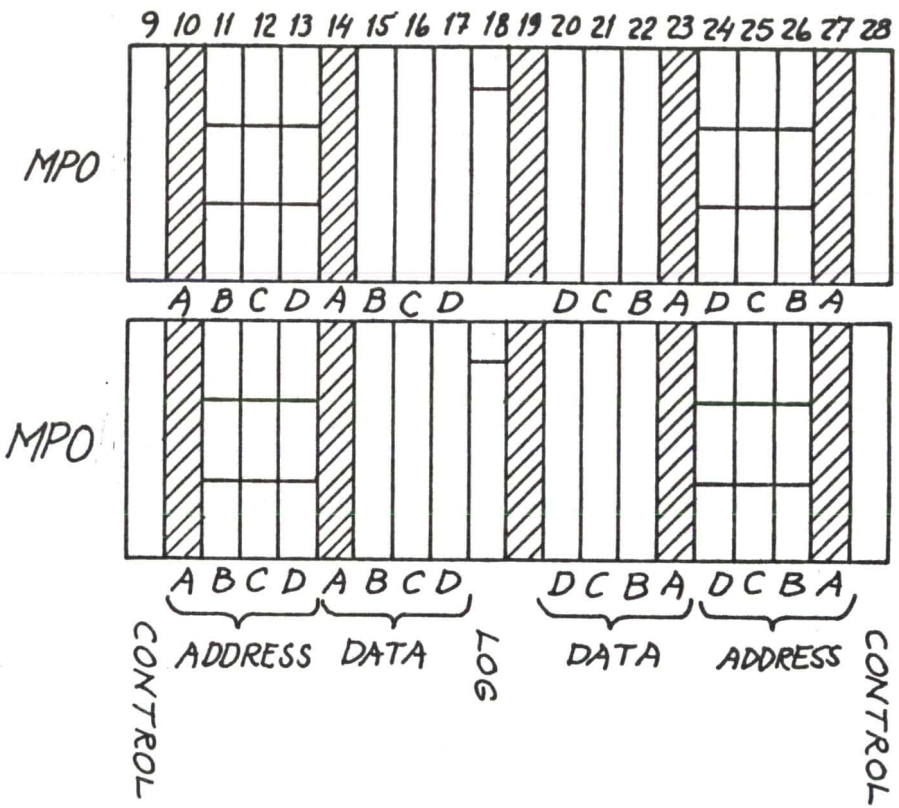
Multiport Racks seen from back side of cabinet.

BMPM SWITCH SETTING

BMPM IN MULTIPORT CABINET FRONT SIDE

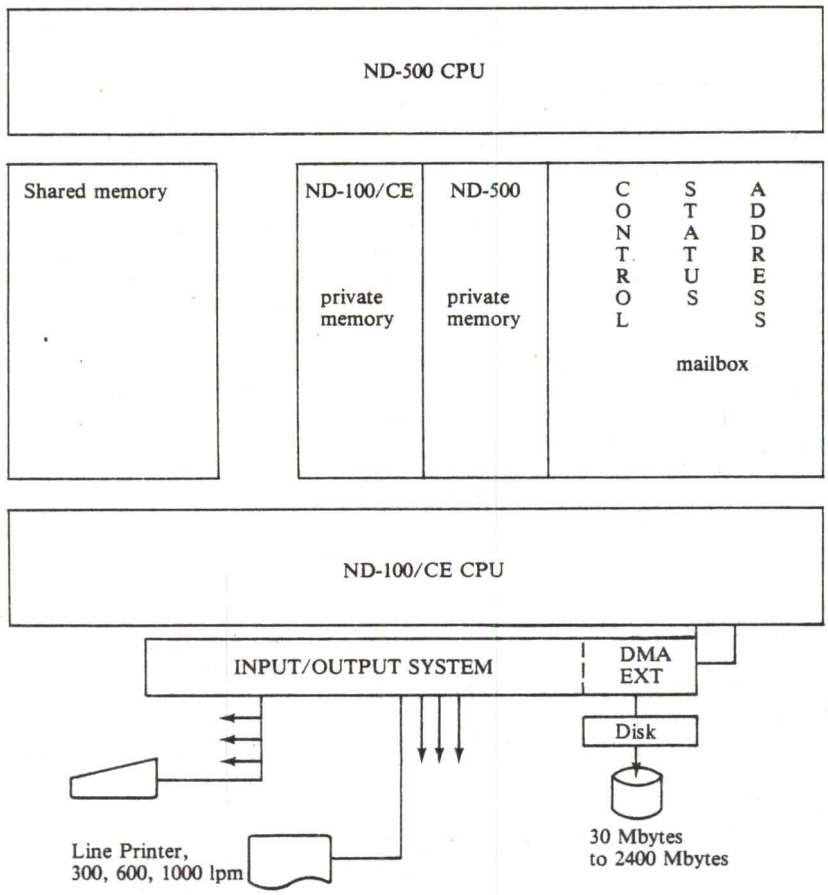


BMPM IN MULTIPORT CABINET BACK SIDE



CHANNEL	A	NOT IN USE
— " —	B	N 100
— " —	C	N 500 INSTR.
— " —	D	N 500 DATA

COMPUTER SYSTEMS



BASIC ND-500 COMPUTER SYSTEM

ND 060 ND-500 Central Processing Unit

INTRODUCTION

The ND-500 is the new top-of-the-line computer system offered by NORSK DATA.

The 32 bit architechture accommodates very large program sizes. The ND-500 has an advanced high-capacity CACHE memory, efficient instruction repertoire, prefetching of data and instructions and high-speed floating point hardware, resulting in a powerful, compact computer module that uses the latest technology available.

The dual computer system consists of an ND-500 CPU, executing large timeconsuming user programs, integrated with an ND-100/CE minicomputer which runs the multimode, multi-user SINTRAN III/VSE-500 Operating System, and performs all input/output handling, jobscheduling and resource-allocations, leaving the ND-500 CPU free to run the user programs with a minimum of system overhead.

Up to 30 users can access the system in Real-Time, Time-Sharing and Batch mode, and share up to 32 Mbytes of fast MOS memory and 2300 Mbytes of disk storage, and a variety of other peripherals.

FEATURES

- High Execution Speed.
  The basic time of 200 ns executes the majority of the ND-500's machine instructions, provididng a formidable processing power. Several ND-500 processors, with 32/64 bit floating point multiply/divide hardware, can act as a multiprocessor system supervised by an ND-100/CE.

- Advanced Instruction Repertoire.
  Instructions are byte-oriented and tailored for high level program execution efficiency, such as FORTRAN «DO-loop», COBOL string-handling and decimal arithmetic instructions.

- Accuracy.
  The hardware arithmetic provides 32 bit single precision floating point operations with 23 bit mantissa and 9 bit exponent, for double precision 64 bit operations the values are 55 and 9 bit respectively.

- Large Program Size.
  The 32 bit, byte oriented addressing mode permits execution of programs with up to 4 giga bytes logical address space and another 4 gigabytes of data.

- Multiprogramming Capabilities.
  Through the use of an efficient virtual memory management system, the ND-500 CPU can be shared by many user programs. Context switching routines are implemented in the microcode.

- CACHE Memory employs a prefetch mechanism from main memory. Each access to memory will be up to 16 bytes wide thus eliminating the usual memory bandwidth bottleneck. There are two independent but identical CACHE systems, one for instructions and one for data. The CACHE can be partitioned and each partition can be used either as CACHE memory or as a high speed local memory.

- Multiport Memory.
  The main memory is of the multiport type, allowing sharing and direct access for ND-500, ND-100/CE and DMA transfer devices such as disk memories and high performance communication links (HDLC). Maximum memory size is 32 Mbytes of physical memory.

- Writable Control Store (WCS).
  In addition to the fixed instructions of the repertoire, a writeable control store allows future addition of new instructions.

- Operating system is SINTRAN III/VSE-500.
  The ND-100/CE CPU of the ND-500 processing system will run the operating system and handle the input/output system, file system, supervisor functions and job scheduling for the ND-500 CPU, leaving it free to run user jobs.

PRODUCT DESCRIPTION

Configurations

The Basic ND-500 Computer System is an integration of the ND-100/CE CPU and its associated I/O devices and interfaces, a ND-500 CPU, and a Multiport Memory System.

All memory is shared between the ND-500, the ND-100/CE and I/O devices to allow for easy access and control by all components in the system. The SINTRAN III/VSE Operating System including the ND-500 MONITOR resides in the ND-100/CE's private memory for increased protection and simultaneous access.

The CACHE memory of the ND-500 can contain 32 Kbytes, 64 Kbytes or 128 Kbytes, evenly divided for instructions and data.

The **Multiport Memory System** can be established with two or four-bank memory racks, using 1, 2 or 4 racks together providing space for maximum 32 Mbytes. pending on the number of memory banks used, a 2 to 8 ways interleaved memory access increases the throughput of the memory system.

The Multiport Memory System provides several independent dataways to the memory, where the ND-500 uses two ports, the ND-100/CE uses one port and the remaining port(s) is (are) used for direct transfer of data (DMA) for disks and magnetic tapes.

The physical memory can range from 512 Kbytes of high-speed MOS memory with Error Checking and Correction (ECC), up to 32 Mbytes with the necessary memory racks installed.

Disk Storage ranges from 30 Mbytes to 288 Mbytes removable disk packs to a total of 2300 Mbytes, and a variety of peripherals, magnetic tapes and floppy diskettes can be attached.

This basic system can then be further expanded by additional ND-500 CPU's for increased computational c city.

THE ND-500 CPU

Registers

The ND-500 CPU has a set of special purpose and general purpose registers accessible by the programmer as well as a «scratch-pad» register file accessible by the microprogram only.

The user accessible registers are as follows:

P-register (program counter) 32 bits
holds the logical address

L-register (link register) 32 bits
used for subroutine returns and linking

B-register (base register) 32 bits
used for local addressing

R-register (record-base register) 32 bits
also used for addressing of records (refer to section on addressing modes)

The R1, R2, R3 and R4 General Purpose Registers are 32 bit registers used for index registers while addressing or as general purpose registers for data manipulations.

The D1, D2, D3 and D4 Accumulators are 64 bit registers used for floating point arithmetic.

The registers are addressed by the microprogram as eight 32 bit registers A1, A2, A3, A4, E1, E2, E3, E4.

ST	Status register (64 bits)
OTE	Own Trap Enable register (64 bits)
CTE	Child Trap Enable
MTE	Mother Trap Enable
TEMM	Trap Enable Modification Mask
TOS	«Top-Of-Stack» register (32 bits)
LL	Low Limit trap (32 bits)
HL	High Limit trap (32 bits)
THA	Trap Handler Address register (32 bits)

Control Store

This memory unit contains the microcode for execution of the machine level instructions. The control-store word is exceptionally wide and wraps the majority of instructions into one microcycle only.

The standard instruction set, as well as special routines for memory management context switching and communication with the ND-100/CE supervisor, are implemented in approximately 72 Kbytes.

Prefetch Processor

This processor handles the pre-decoding and assembling of machine level instructions in the pipeline, as well as initiations of data fetch cycles for memory reference instructions.

The prefetch processor will always keep the instruction and data pipelines full to ensure minimum idle time for the microprocessor hence maximum execution speed.

Arithmetic Logic Unit (ALU)

The Arithmetic Logic Unit is the heart of the microprocessor and will do specified operations on the data of specified registers.

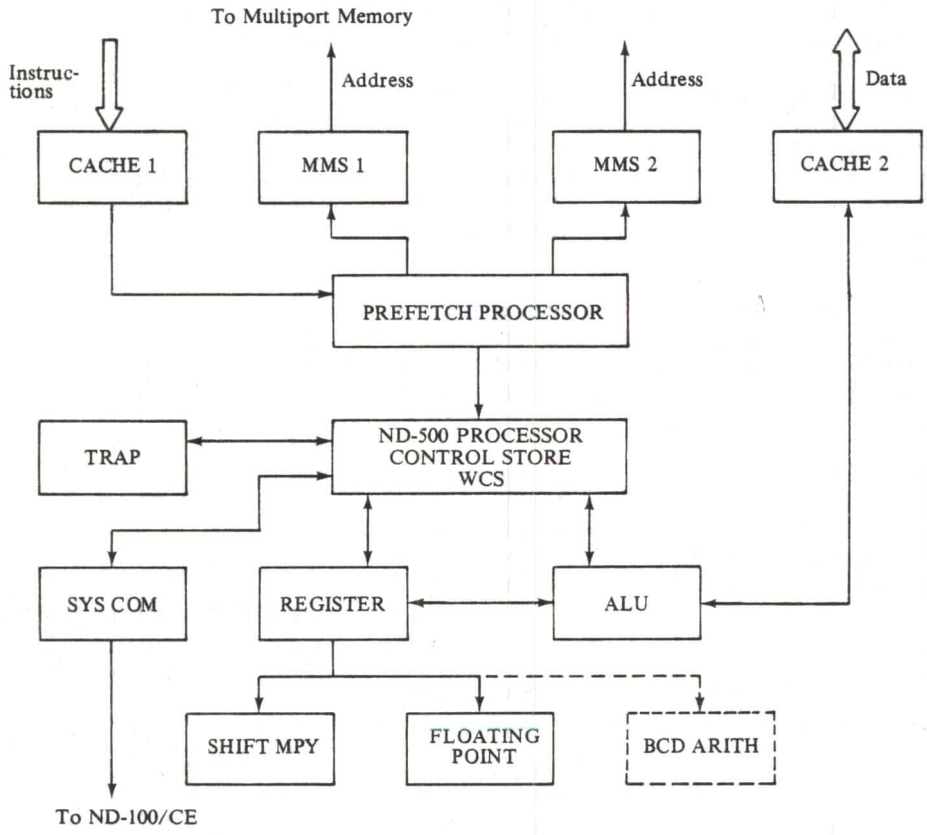
Floating Point Hardware

This is a set of specialized hardware controlled by the microprocessor in the ND-500. This unit will perform all floating point arithmetic as well as Integer Multiply, Shift and Divide, at hardware speeds.

This hardware contains accumulators for temporary storage of results and can be used effectively for combined operations, such as multiplication of many elements etc.

Trap System

There is a set of conditions that can be specified in the Trap Register where the program in the ND-500 can be forced to branch to certain places in memory. These traps are conditions such as: overflow on arithmetic, underflow, page fault in memory management, trap on branch (trace), always trap (to single step and trace a program) and others. There are a total of 33 traps that can be specified for program control at run-time.



ND-500 CPU BLOCK

ND-100/CE — ND-500 Communication

All or part of the memory can be shared between the ND-500 CPU, the ND-100/CE CPU and the associated I/O devices. This allows for easy access and control by all components of the system.

The communication between the ND-100/CE and the ND-500 is set up as a mailbox and DMA transfer system. The mailbox contains 3 registers:

- Control register:
  For ND-100/CE to give ND-500 a command.

- Status register:
  For ND-500 to give ND-100/CE a command.

- Address register:
  A pointer to where in the ND-100/CE memory chains of instruction or data will be found, or where the ND-500 can store extended status information.

The status information returned to ND-100/CE reports that a job is finished, the reason for ND-500 termination and type of possible ND-500 malfunctions.

The ND-500 microprogram initiates and controls the DMA access channel to ND-100/CE memory. The communication channel is also used extensively for diagnostic and test program information. The ND-100/CE is used as a diagnostic vehicle for the ND-500.

Memory Management System (MMS)

There are two separate but identical Memory Management Systems in the ND-500, one for instructions and one for data.

The MMS maps the 32 bit logical byte address into a 25 bit physical byte address used when addressing main memory. The system acts as a protect mechanism for sections of memory that can be read-only, system data etc.

The 4 gigabyte address space is divided into 32 segments, with a paging substructure for dynamic allocation of physical memory. Memory protection is performed on the segment level. The Memory Management System also extends the logical address range to 2^{40} bytes, by allowing each process (or user) to access a maximum of 256 domains, each of 4 gigabytes.

To convert the logical address to physical address, a multi-level table look-up procedure is used. In order to speed up this procedure, a copy of the most recently used address conversions are kept in a separate buffer memory.

The access to CACHE memory for data or instructions and the access to the address translation buffer are done simultaneously. If the CACHE does not contain the desired address conversion, the multiple table look-up procedure is performed by the ND-500 microprogram.

CACHE

The CACHE memory consist of two identical systems, one for instructions, and one for data.

The CACHE word can be 32, 64 or 128 data bits wide and is 4 Kwords deep. In addition to the bits of the data word, certain control bits in each word are used by the CACHE system to identify the information stored.

The width of the CACHE word is equal to the width of the channel to main memory.

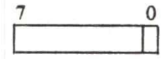
The CACHE is addressed by the logical address from the CPU and is byte addressable.

The maximum CACHE size is 64 Kbytes for instructions and 64 Kbytes for data, giving a total of 128 Kbytes.

DATA FORMATS

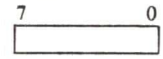
The basic unit for addressing is one byte of 8 bits. The data formats are bit, byte, half word, word, single precision floating point and double precision floating point.

Bit



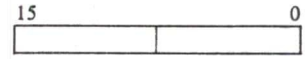
The least significant bit in a byte may be accessed by bit instructions. Bit arrays may be accessed using post incrementing or descriptor addressing.

Byte



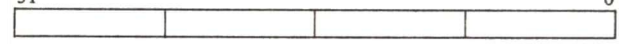
A byte is 8 bits and can be used as an unsigned number with the range 0 to 2^8-1 or as a two's complement number with the range -2^7 to 2^7-1.

Half Word



A half word is 2 bytes or 16 bits and can be used as an unsigned number with the range 0 to 2^{16}-1 or as a two's complement number with the range -2^{15} to 2^{15}-1.

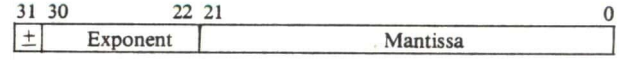
Word



A word is 32 bits or 4 bytes and can be used as an unsigned number with the range 0 to 2^{32}-1 or as a two's complement number with the range -2^{31} to 2^{31}-1.

Single Precision Floating Point

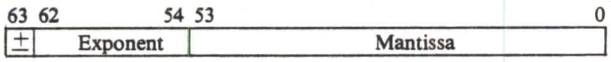
A floating point number is represented by a mantissa of 22 + 1* bits, an exponent of 9 bits with the bias 400_8 and a sign bit.



The range is 10^{-76} to 10^{76}. Zero is represented as all bits zero. The accuracy is approximately 7 digits.

Double Precision Floating Point

A double precision floating point number is represented by a mantissa of 54+1* bits, an exponent of 9 bits with the bias 400_8 and a sign bit.

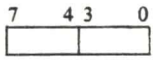


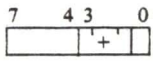
The range is 10^{-76} to 10^{76}. Zero is represented as all bits zero. The accuracy is approximately 16 digits.

* The extra bit in the mantissa is the most significant bit and is set to one unless all bits in the exponent are zero. The bit is used in the arithmetic and is removed in the result.

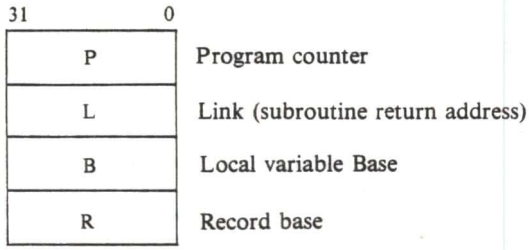
Packed Decimal

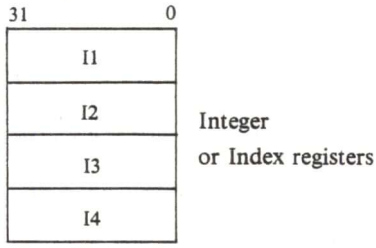
Two BCD-digits per byte, sign in lowest half of rightmost byte, from 1 to 16 bytes (31 digit plus sign) in length.



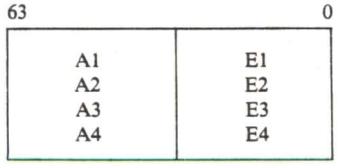


ND-500 REGISTER BLOCK

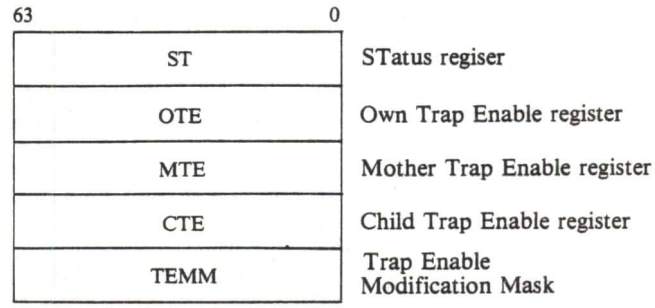


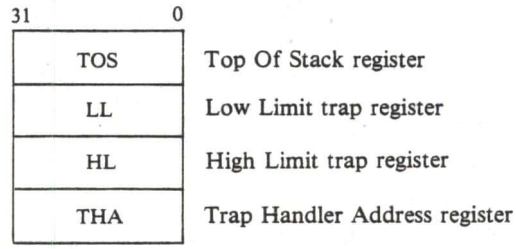


The In accumulators are namned BIn, BYn, Hn, and Wn when used for BIt, BYte, Halfword, or Word operations. (n = 1, 2, 3, 4).



The An accumulators are named Fn when used as single precision floating point registers. The (An, En) double registers are named Dn when used as double precision floating point registers.





INSTRUCTIONS

The ND-500 instruction repertoire is highly symmetric in the sense that all addressing modes may be used with all instructions and that all instruction exists for all the data types it is useful for operating on. The instruction repertoire is designed for easy construction of high level language compilers which produce reliable and compact code. Even though the ND-500 is a 32 bit computer, it will use more compact code than most 16 bit computers.

The instruction repertoire includes all types of arithmetic on 8, 16 and 32 bit binary data, single- and double-precision floating point, packed decimal (BCD) as well as conditional and unconditional branching, shift and bit handling, and a variety of powerful string manipulation on byte arrays and other data types.

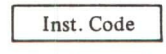
The ND-500 has a full set of register operations together with a large number of memory-to-memory instructions. The register instructions are useful for calculating very complex expressions and for the calculation of values which will be used for addressing. Memory-to-memory instructions give the possibility of direct execution in one instruction of frequently occuring high level statements as

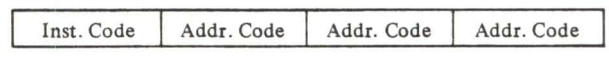
A = A + B	(ADD2)
C = D*F	(MUL3)

Special instructions are implemented for high level constructions such as DO-loops, subroutine call and array index checking (LOOP, CALL and LIND), and for library use the square root, integer exponentiation and polynomial evaluation.

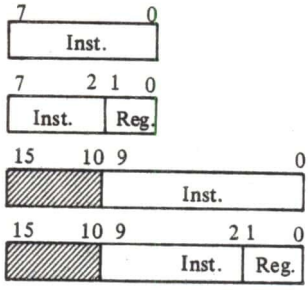
Instruction Formats

An instruction consists of one instruction code and a variable number of address codes.





An instruction code can be one or two bytes, and can have a two bit register specification.



Short instruction codes are used for the operations most frequently generated by the computers.

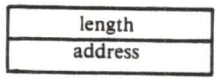
The type of operands handled by the instruction (bit, byte, half word, word, floating or doubling precision floating) is specified in the instruction code.

Address Codes

The branch instructions have P-relative addressing with a displacement one, two or four bytes. All other instructions may have several general operands that are specified by using one of the 29 different address codes.

Address codes may be preceded by a one byte address code prefix specifying descriptor addressing or alternative domain addressing. The size of the address codes most frequently generated by the compilers are one byte only.

Descriptor addressing is a powerful way of accessing strings or arrays of data.



ND-500 descriptor format

The index in the string or array in descriptor addressing is in the register specified in the descriptor address code prefix.

Alternative addressing is used in the memory management system for example for accessing the user addressing domain from the Operating System.

In post indexing and descriptor addressing, the type of data operated upon is used in the hardware address arithmetic multiplying the index by the size of the data elements. The logical index of a structure may therefore be used directly in the index register and no calculations are necessary in the program for taking the data type into account.

Physical Specifications

High performance Schottky TTL logic technology is used throughout the ND-500 CPU. Low power STTL is used where possible to reduce power consumption.

Power dissipation:

ND-500 CPU	Approximately 1.3 kW
Cooling system	Forced air

Power requirements:

ND 3500	220 VAC ± 10 %, 50 Hz ± 2 Hz
ND 2500	110 VAC ± 10 %, 60 Hz ± 2 Hz
Operating temperature ..	+ 10° C to + 35° C

CABINETS IN THE NORD-500 COMPUTER-SYSTEMS

11 MODULE CABINETS:

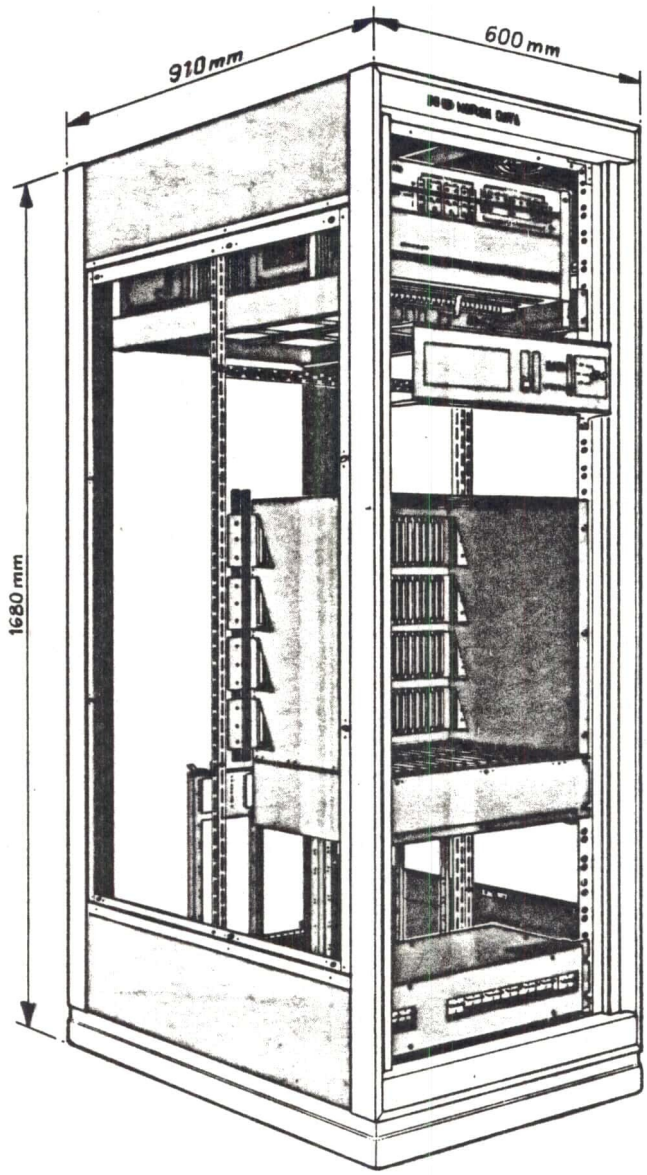
(11 X 5 1/4'' MODULES IN FRONT)

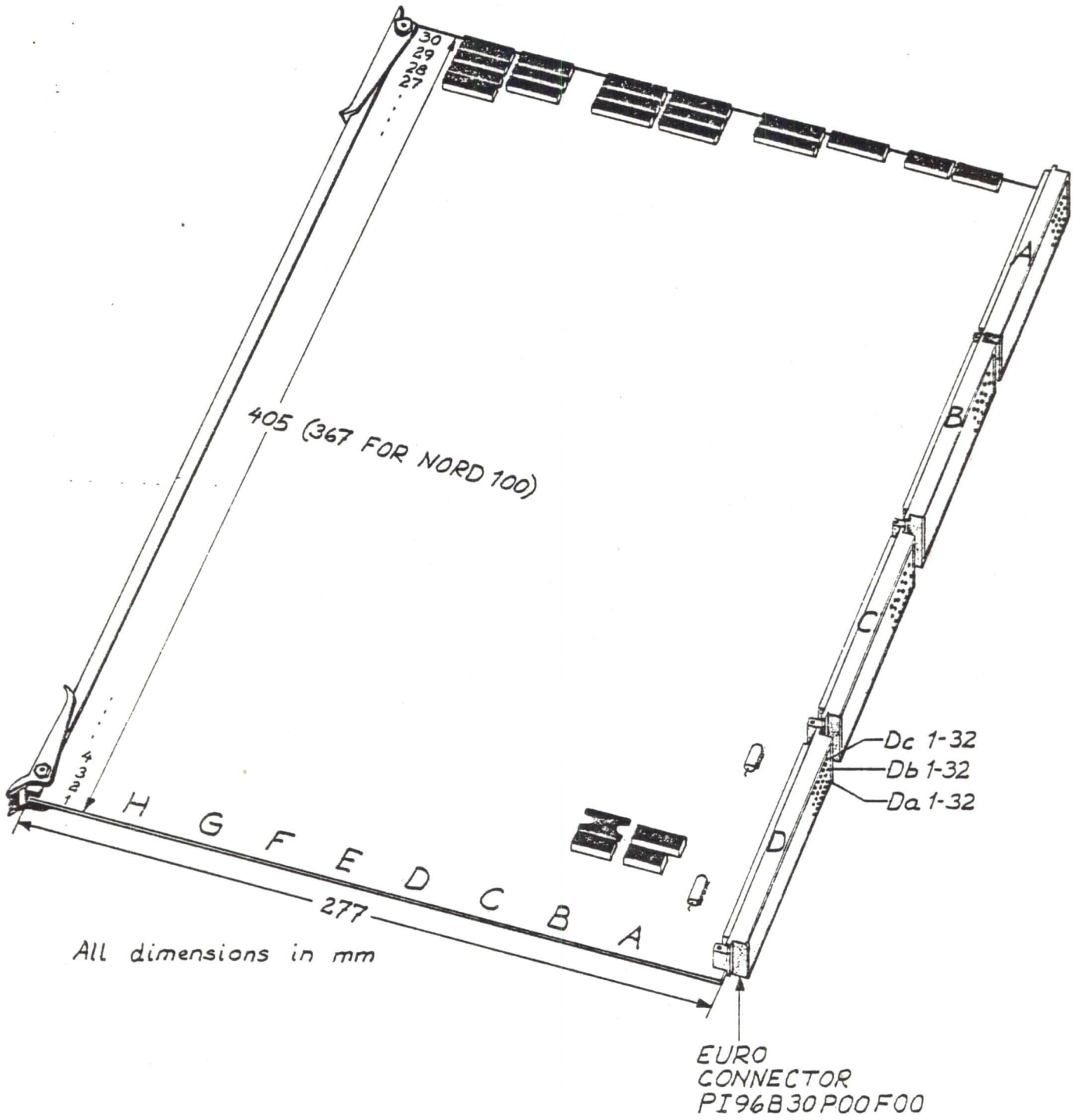
NORD-500 SYSTEMS:

- **POWER SUPPLY OF 2 X 150 (5V)**
  AND
  STANDBY POWER IF MULTIPORT
  IN THE SAME CABINET
- **AC DISTRIBUTION POWER PANEL**
- **1 NORD-500 CARD-CRATE**
- **1 PLUG-PANEL (ACCESSIBLE FROM REAR)**
- **MAX 1 M BYTES OF NORD-10/S MULTIPORT**
  2 RACKS WITH PLUG-PANEL INCLUDED
  (ACCESSIBLE FROM REAR)

NORD-500 MEMORY SYSTEMS:

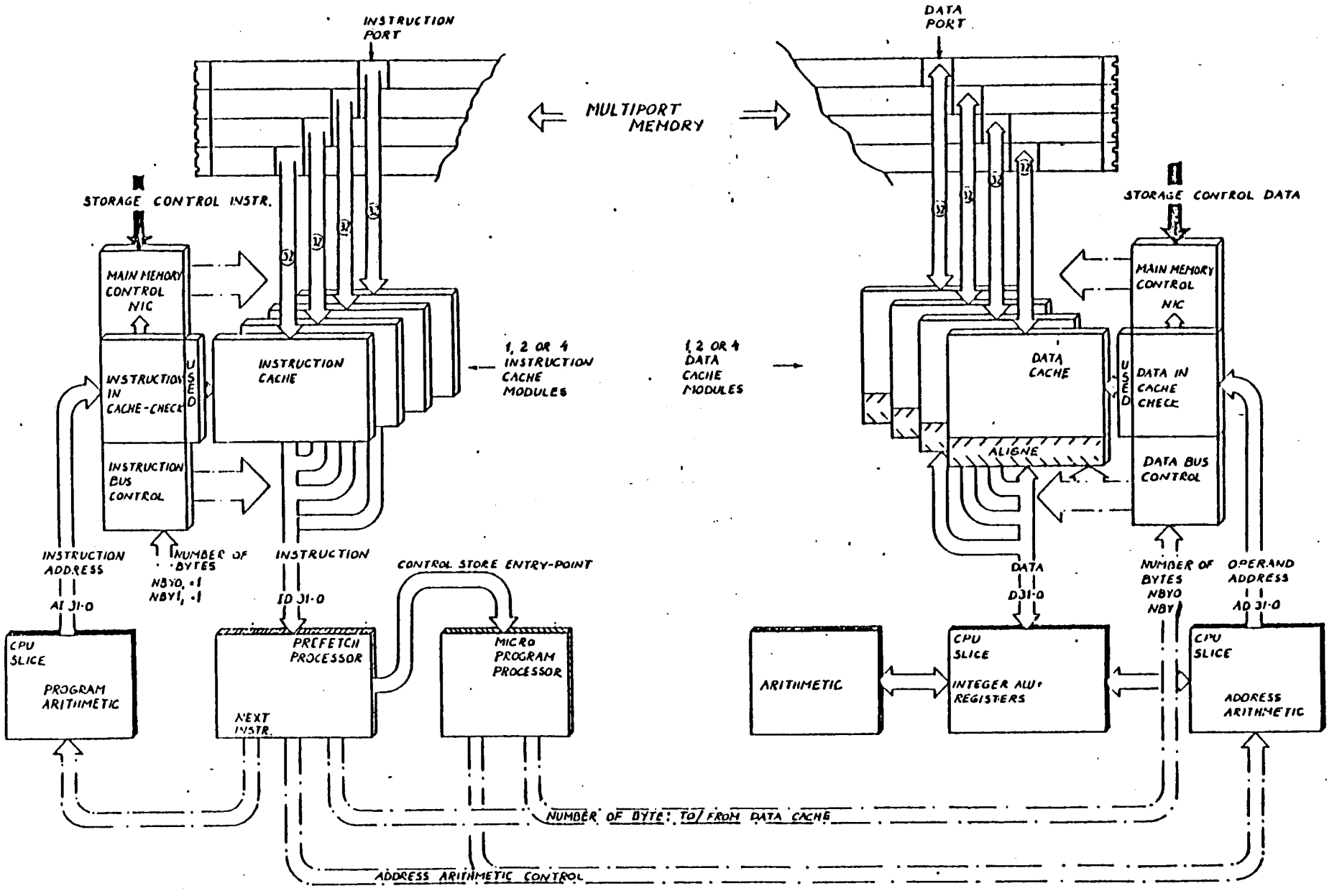
- **POWER SUPPLY OF 1 X 150 A (5V)**
  2 X STANDBY POWER EACH OF
  20A (5V), 4A (12V)
- **AC DISTRIBUTION POWER PANEL**
- **MAX 2 M BYTES OF NORD-10/S MULTIPORT**
  4 RACKS WITH PLUG-PANEL INCLUDED
  (ACCESSIBLE FROM REAR)


910 mm
600 mm
1680 mm

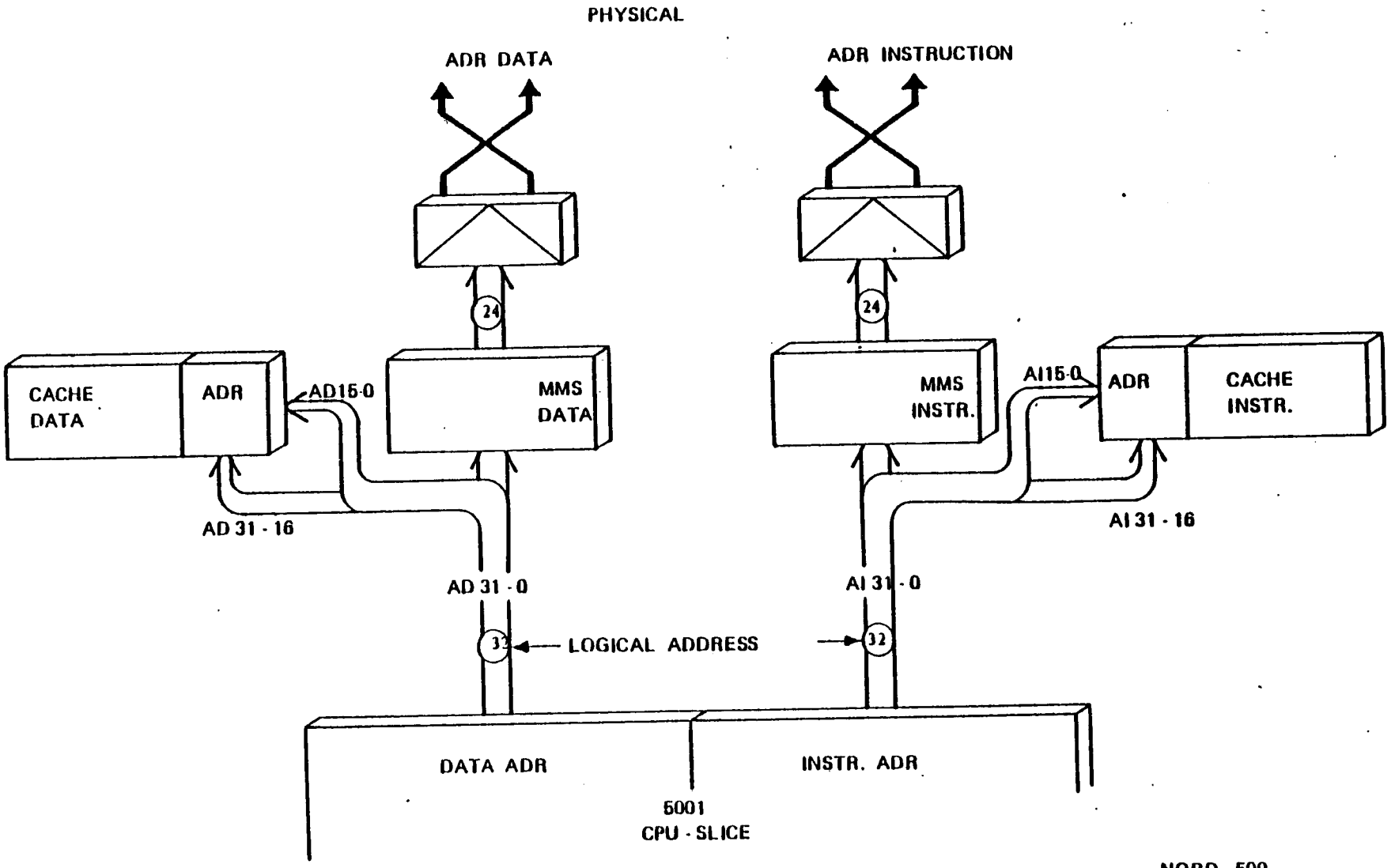


NORD 500 MODULE

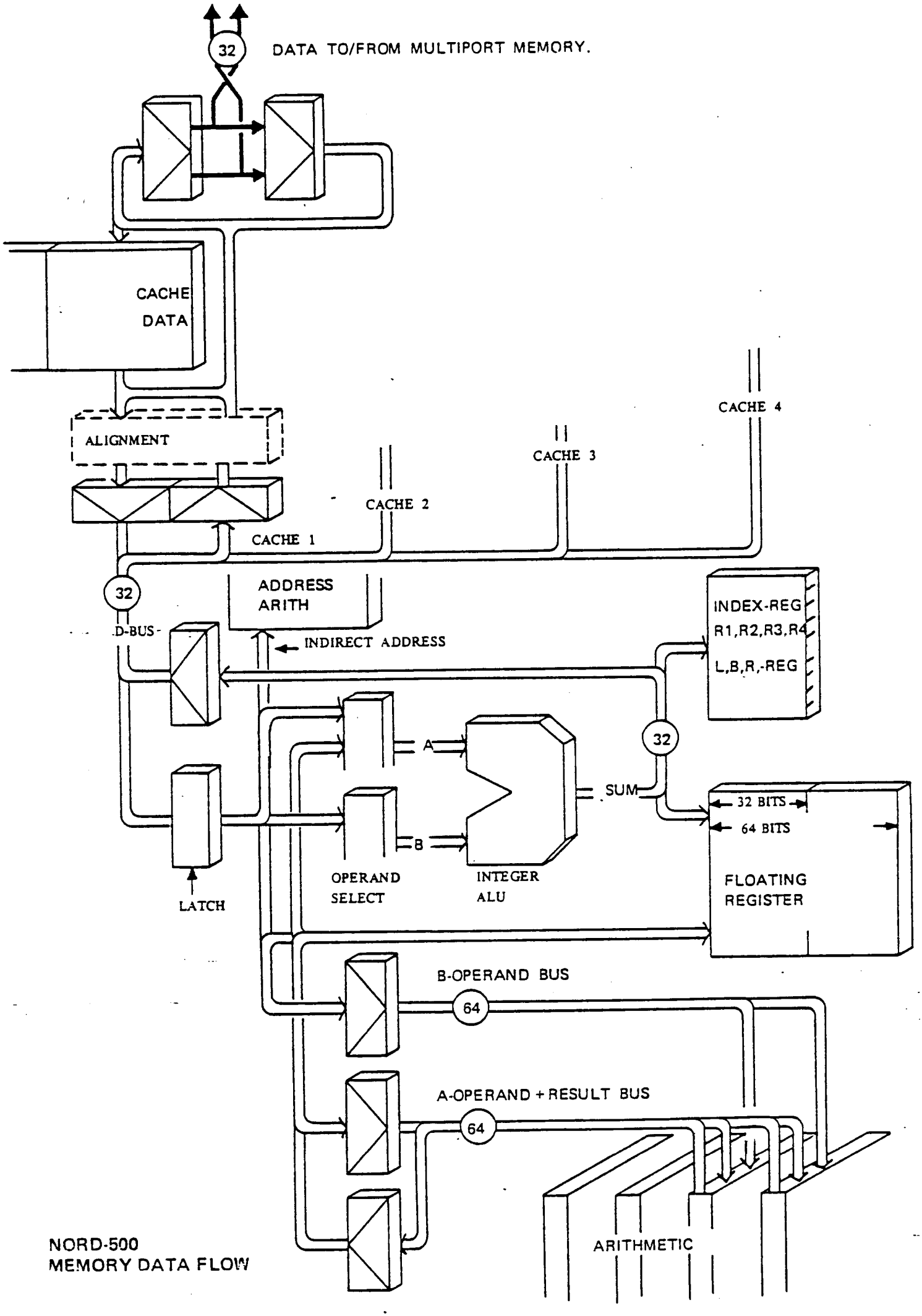
NORD-500 MAIN COMPONENTS, ADDRESS, DATA AND INSTRUCTION FLOW



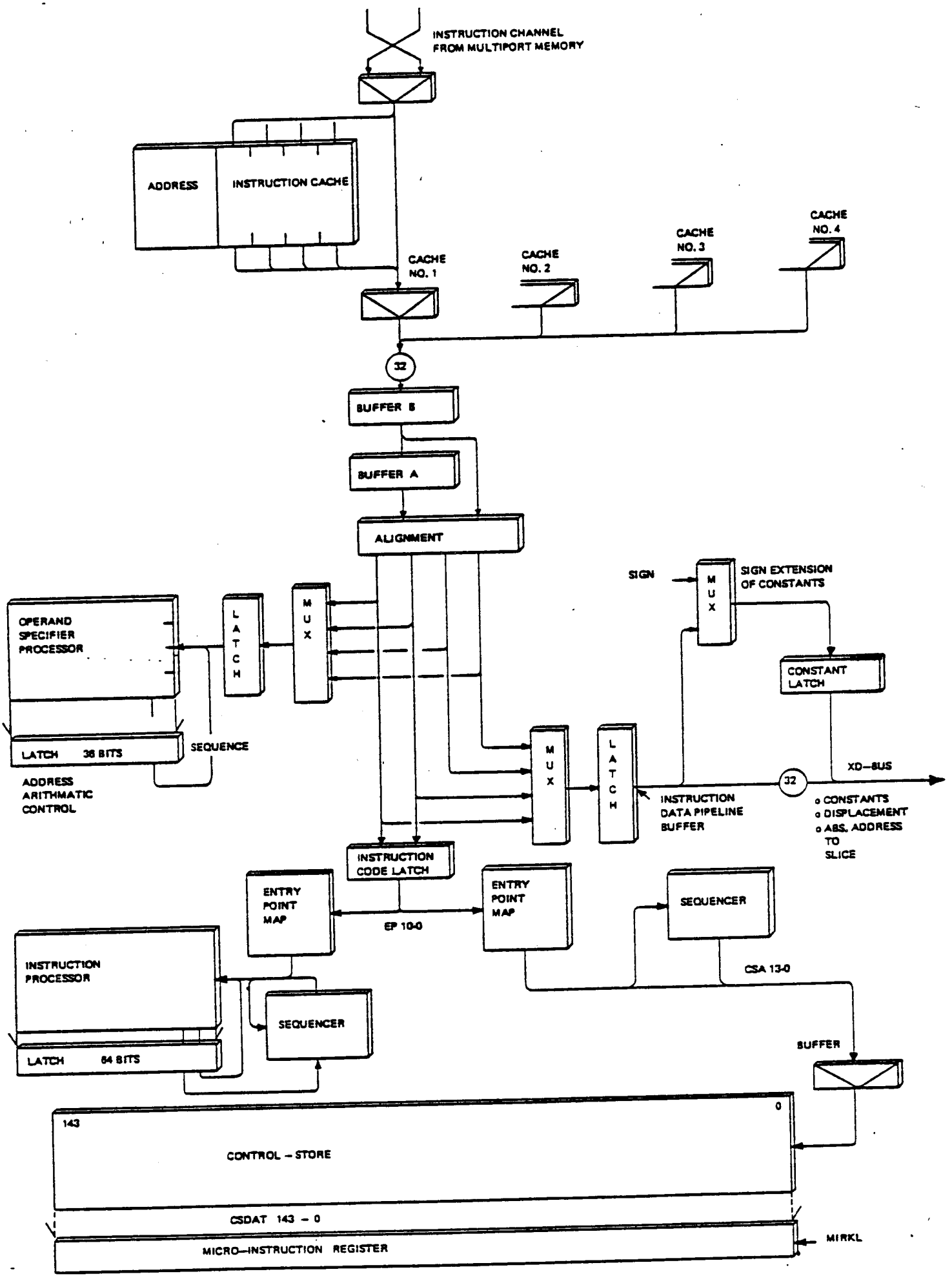
NORD-500
STORAGE CONTROL



NORD - 500
ADDRESSING

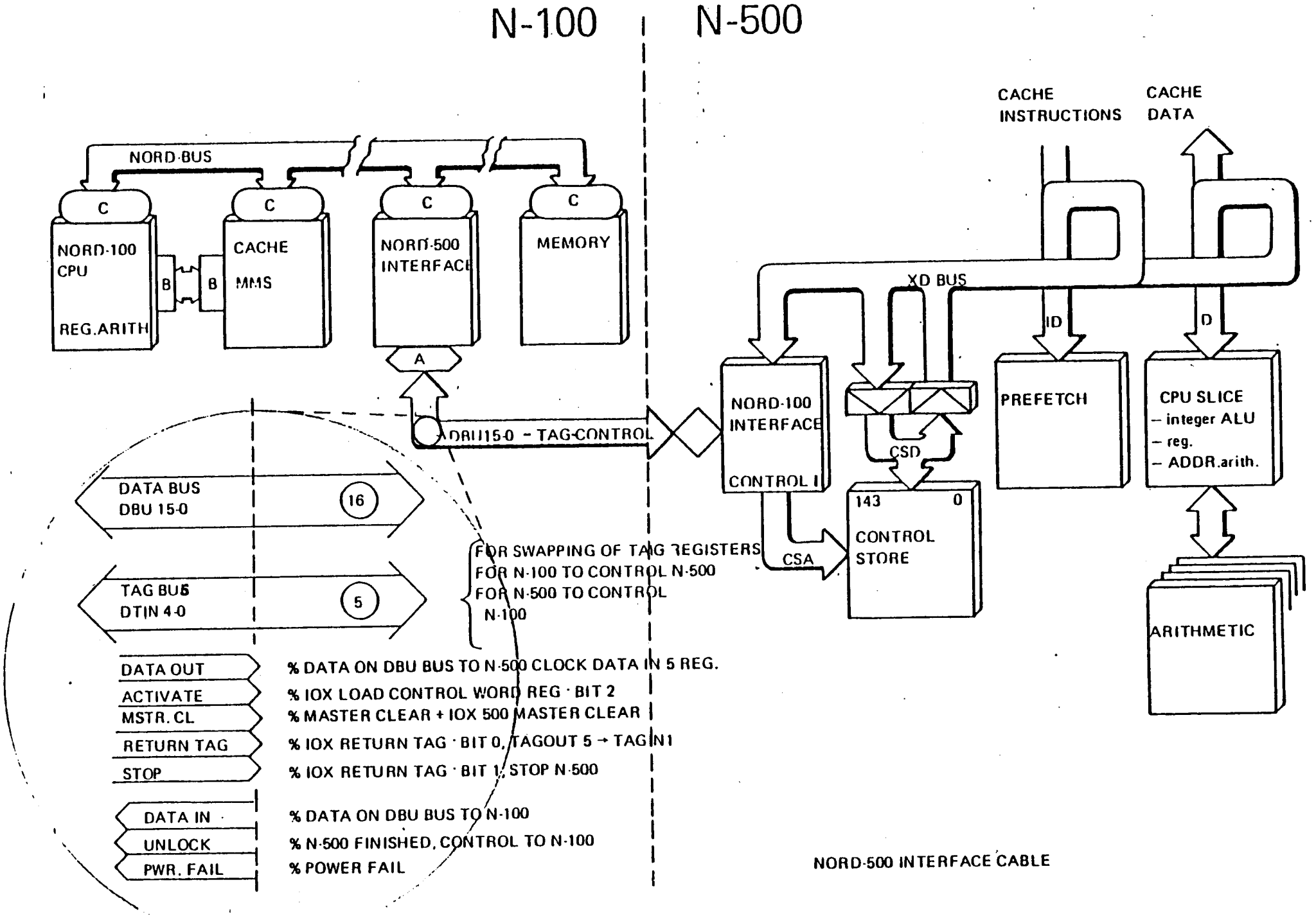


NORD-500
MEMORY DATA FLOW



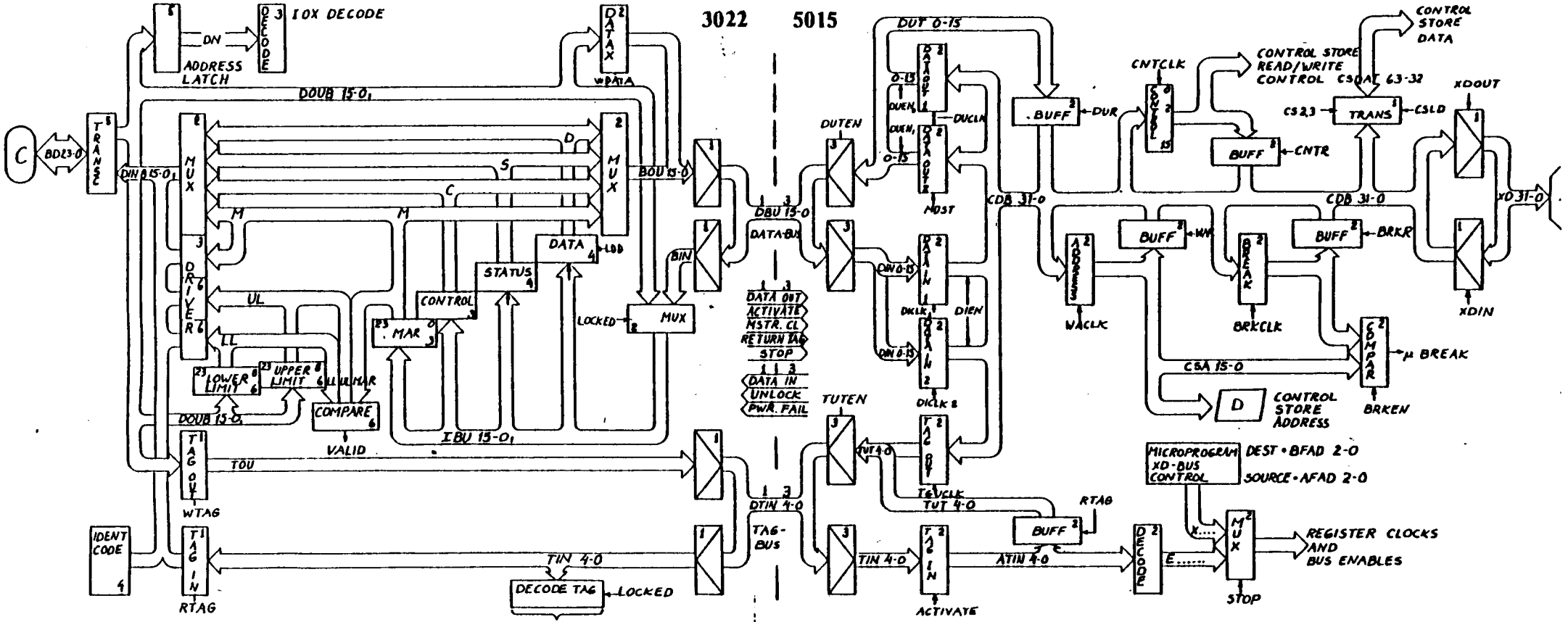
NORD 500 INSTRUCTION PROCESSING

NORD-100/NORD-500 COMMUNICATION



NORD-500 INTERFACE CABLE

N-100 N-500
3022 5015



REGISTER CONTROL BY N500

The CONTROL register bits have the following interpretation:

Bit No.

0	Enable interrupt from NORD-500
1	Not used
2	Activate NORD-500, mailbox to NORD-500 (LOCKED)
3	Test mode
4	NORD-500 programmed clear
5	Disable TAG-IN decoding when locked
6	DMA error
7	Command chaining
8-14	NORD-500 operation
15	Not used

The STATUS register can always be read by NORD-500 and the bits are defined as follows:

Bit No.

0	Interrupt enabled
1	Not used
2	NORD-500 bu
3	NORD-500 flag
4	Error
5	Interface locked
6	DMA error

TAG-OUT Register (data from NORD-500) (Writeable)

Bits 0-2 gives 8 code values. The code values are:

0	Read memory address register
1	Write memory address register
2	Read status register
3	Write status register
4	Read control register
5	Reset activate
6	Read data register (and NORD-100 memory)
7	Write data register (and then into NORD-100 memory)

IOX INSTRUCTIONS/LOCKED/TEST/DECODING:

IOX Inst	Locked Not Test	Locked Test	Not Locked Not Test	Not Locked Test
60			Read MAR x 2	Read MAR x 2
61			Load MAR x 2	Load MAR x 2
62	Read STATUS	Read STATUS	Read STATUS	Read STATUS
63				Load STATUS
64		Read CONTROL		Read CONTROL
65			Load CONTROL	Load CONTROL
66	Master Clear		Master Clear	Read DATA
67	Terminate		Terminate	Load DATA
70	Read TAG-IN		Read T IN	Read UPPER-LIM*
71	Write TAG-OUT		Write OUT	Load UPPER-LIM*
72				Read LOWER-LIM*
73	Write DATAX		Write .AX	Load LOWER-LIM*
74			Set LOCKED	

THE TAG-IN REGISTER ON 5015 (I/O FROM NORD-100)

The TAG-IN register is used to control the communication from N100 when N500 is in STOP-mode.

Bits 0 - 3 give 16 code values. The codes are:

0	NOT USED	
1	DICLK1	Clock data-in-1 register
2	DICLK2	Clock data-in-2 register
3	DUCLK	Clock data-out register (both)
4	WACLK	Clock write-address register
5	BRKCLK	Clock break register
6	TGUCLK	Clock tag-out register
7	CNTCLK	Clock CSCNT register
8	DIEN	Enable data-in register to bus (CDB)
9	DUEN	Enable data-out register (least significant)
10	WAR	Read write-address register
11	BRKR	Read break register
12	CNTR	Read CSCNT register
13	RESBRK	Reset break
14	DUNL	Unlock
15	EDUTEN	Enable data line driver (from NORD-500)

Bit 4 — not used.

Bit 5 — used to return tag-in bits (0-4).

Control Store Control Register (CSCNT 16 bits Readable and Writeable):

0	CSLOAD	Control store load
1	CSREAD	Control store read
2-5	WE0-WE3	Control store group (0-3)
6	BRKEN	Break enable
7	STADREN	Start address enable
8	TSTPTY	Test control store parity check (NORD-500 passive)
9	TSTTGU	Returns tag-out instead of tag-in
10	CSPTY	Control store parity
11	AFIN	Prefetch address calc. not finished
12	PFIN	Prefetch instruction not finished
13	BALUM	Memory reference not finished
14	IOWAIT	I/O operation not finished
15	EXTWAIT	External arith. operation not finished

Bits 10-15 may only be read. They give microprogram stop conditions.

TAG-OUT Register (data from NORD-500) (Writeable)

Bit 3 means NORD-100 if it is 0 and not NORD-100 if it is 1.

Bits 4-6 are not used.

Bit 7 is the MOST bit. It enables the most significant part of the DATA-OUT register

CACHE AND MULTIPORT MEMORY SYSTEM

MAIN MEMORY CONTROL

Upon a request from the PREFETCH or MICROPROGRAM processor, the CACHE CONTROL module will check to see if the DATA is found in the READ SPEED-UP BUFFER or in the CACHE memory.

If the DATA is not in the SPEED-UP BUFFER or in the CACHE memory, the MAIN MEMORY CONTROL logic will request the MULTIPORT-MEMORY.

The MAIN MEMORY CONTROL LOGIC will read 4, 8, or 16 bytes from MAIN MEMORY dependent of the number of CACHE modus. The DATA read will be written into the READ SPEED-UP buffer and the WRITE SPEED-UP buffer. From the WRITE SPEED-UP buffer, the data is forwarded to the CACHE memory.

The data flow including parity check/generate is monitored by the MAIN MEMORY CONTROL LOGIC.

To ensure identical content of the CACHE and the MAIN MEMORY during a WRITE operation, the following steps take place:

1. The MAIN MEMORY control logic reads 32, 64 or 128 bits from the main memory.

2. The byte(s) to be written are merged with the MAIN MEMORY data.

3. The merged data is written to the MAIN MEMORY.

4. The merged data is written to the CACHE memory.

Steps 1 and 3 may be performed simultaneously if the data to be written is occupying the complete memory channel(s).

CACHE ADDRESSING

1 Cache Module: Cache Block Adr. →

BIT NO. →

Byte No. ↓

	31			0
0	0	1	2	3
1	4	5	6	7
2	10	11	12	13
3	14	15	16	17
4	20	21	22	23

← Cache No. 1 →

2 Cache Modules:

Cache Block Adr. →

	31			0	31			0
0	0	1	2	3	4	5	6	7
1	10	11	12	13	14	15	16	17
2	20	21	22	23	24	25	26	27

← Cache No. 1 → ← Cache No. 2 →

4 Cache Modules:

Cache Block Adr. →

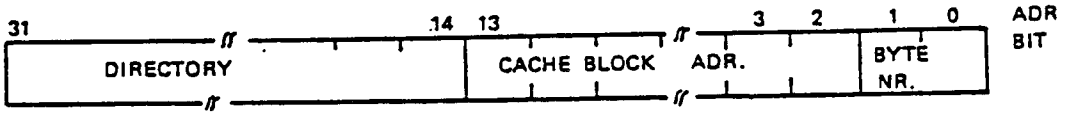
	31			0	31			0	31			0	31			
0	0	1	2	3	4	5	6	7	10	11	12	13	14	15	16	17
1	20	21	22	23	24	25	26	27	30	31	32	33	34	35	36	37

← Cache 1 → ← Cache 2 → ← Cache 3 → ← Cache 4 →

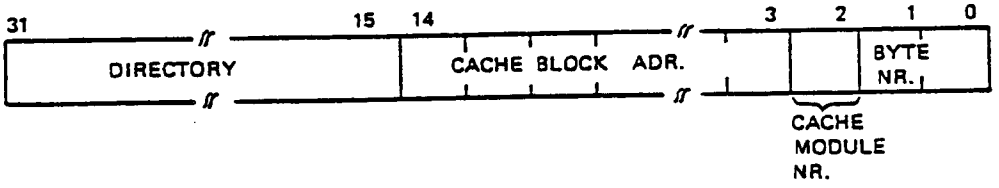
NB! 1 Cache Block = 1, 2 or 4 cache words

3 Addressing Formats

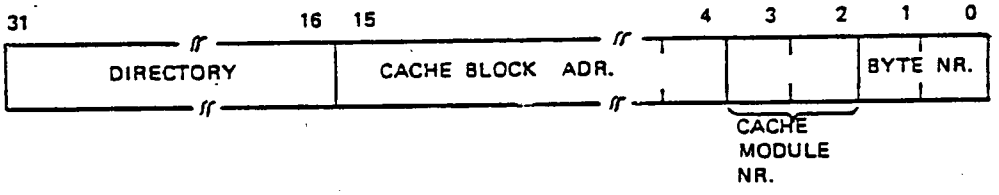
1 Cache Module:



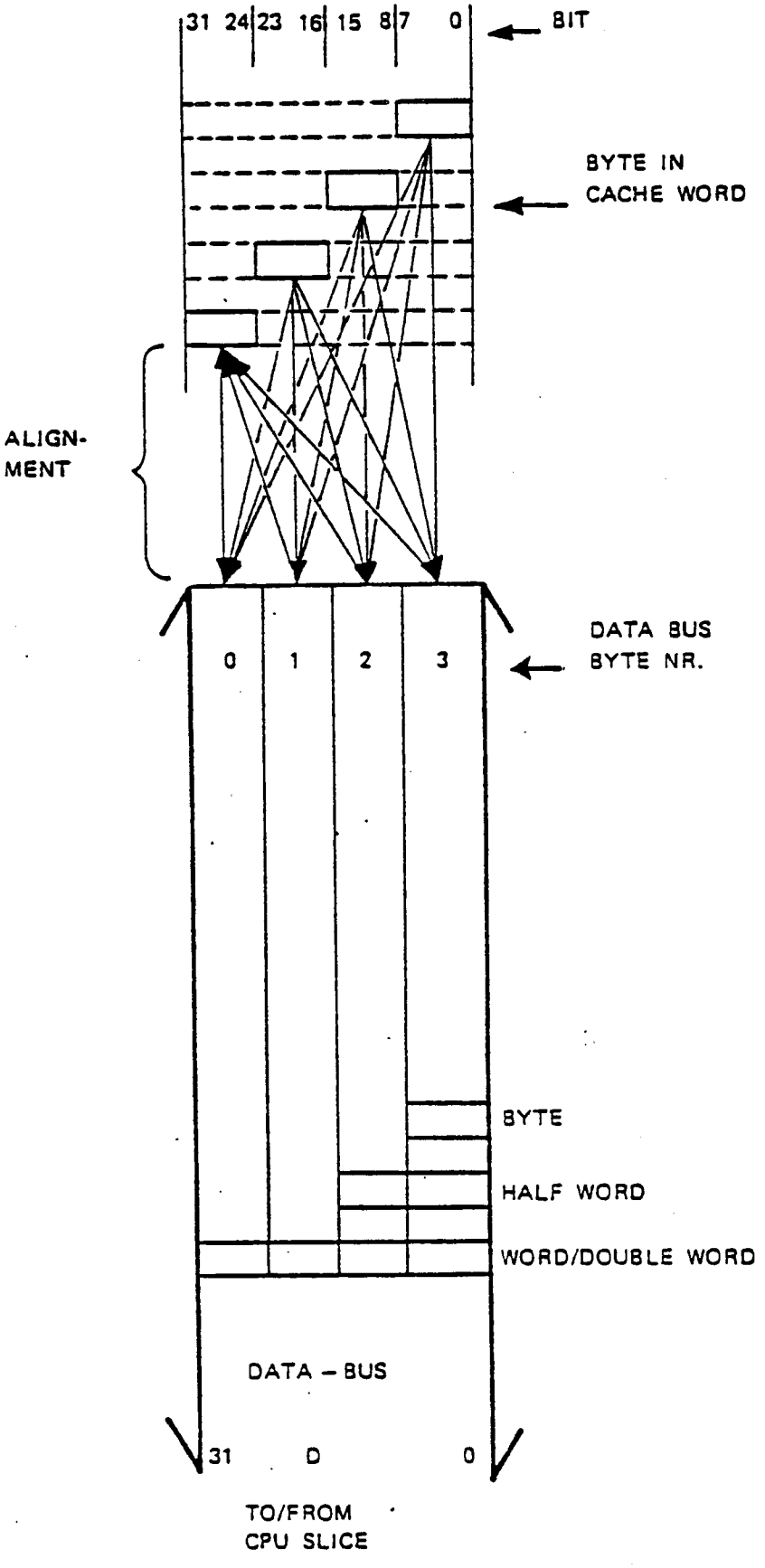
2 Cache Modules:



4 Cache Modules:



CACHE ALIGNING (Data Cache)



CACHE PARTITIONS

— Cache memory can be partitioned in 1, 2 or 4 partitions

— Each partition = 1KB per cache module

— Each partition = 1KB with one cache module
= 2KB with two cache modules
= 4KB with four cache modules

— One user can have 1, 2, 3 or 4 partitions

— Partitions in cache can be fixed to:
* the operating system
* common reentrant library

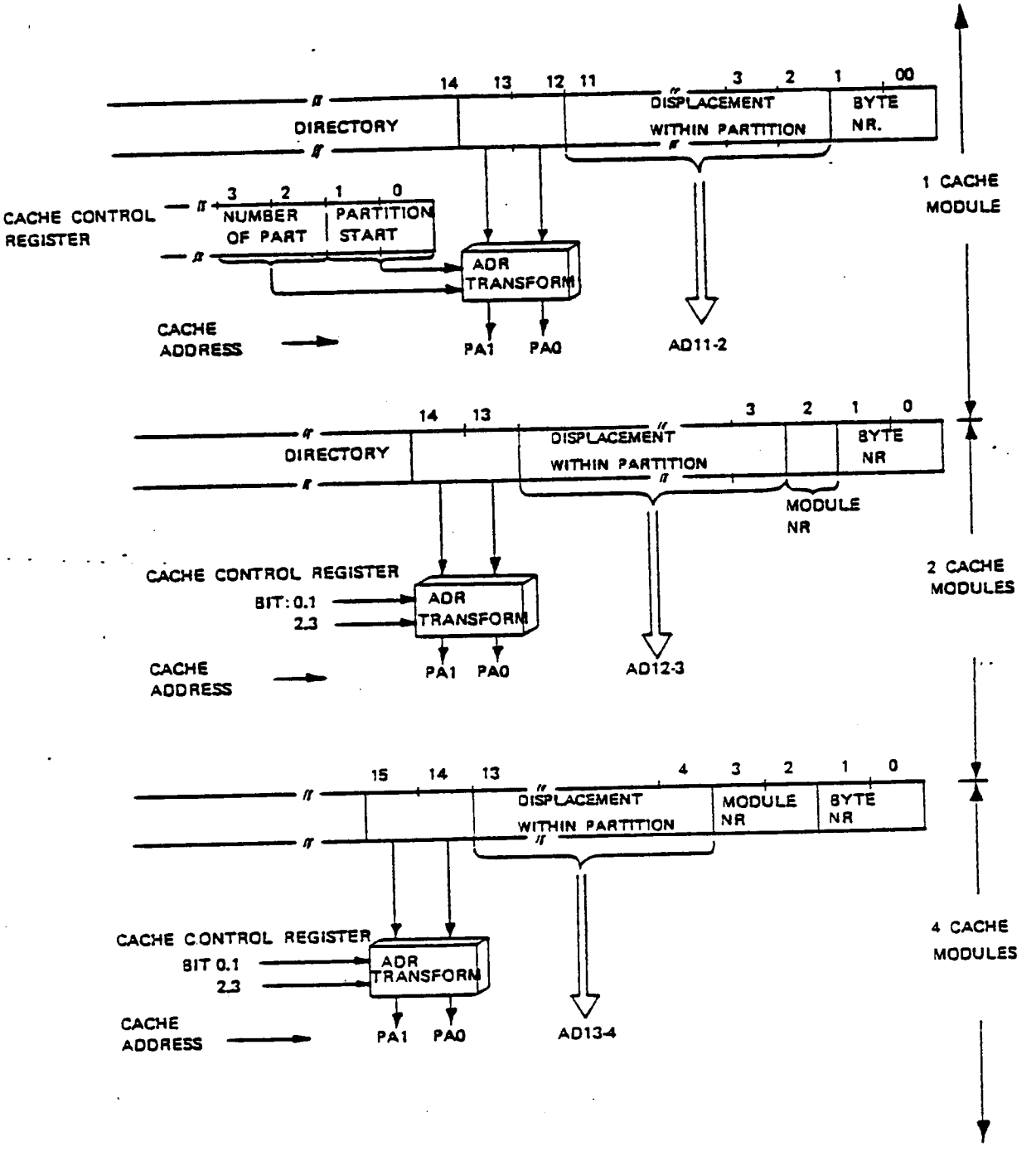
— Saves cache fill-up between context switch

— Partitions can be used by one user as fast private memory

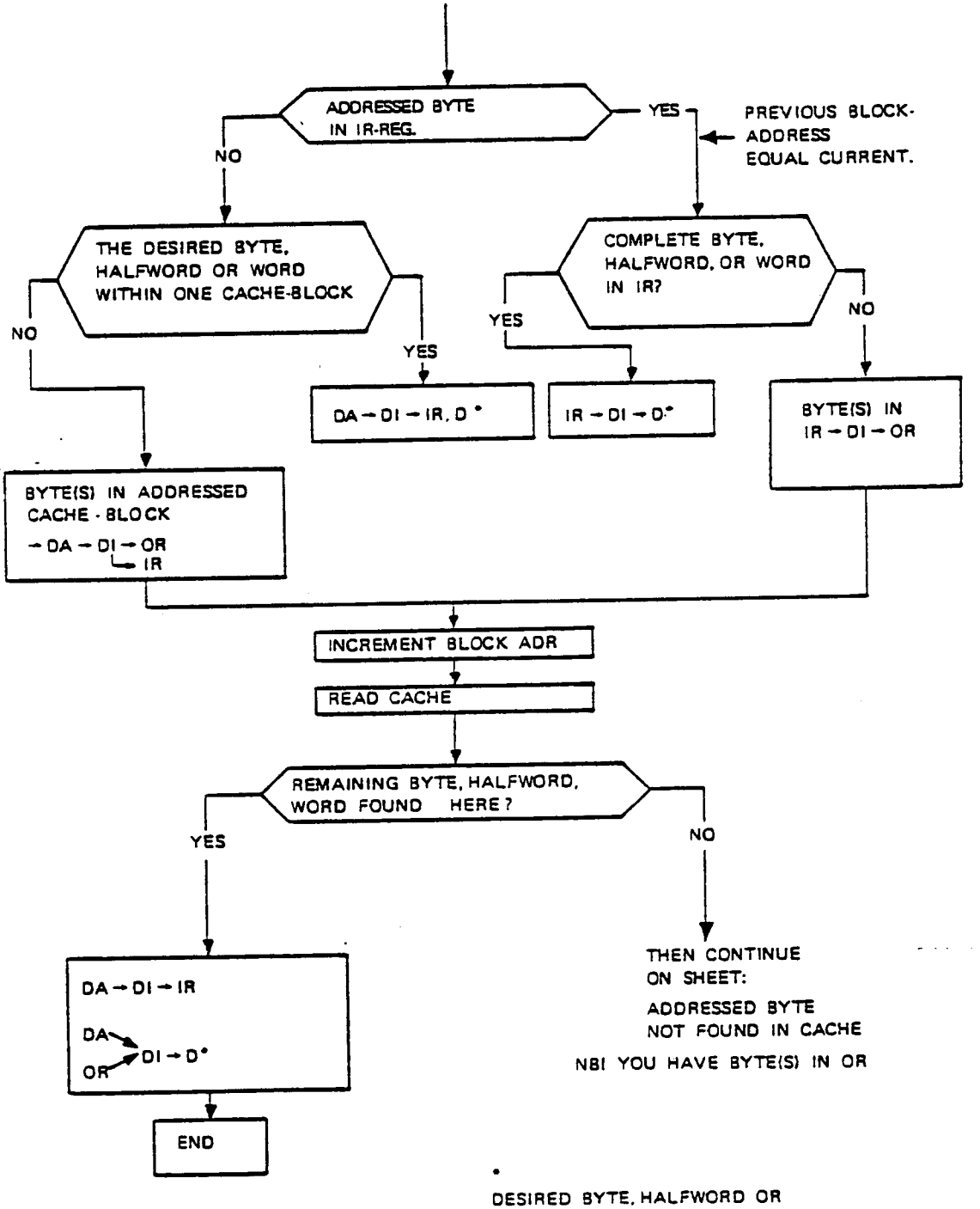
— Cache partitions administrated by the operating system

(partitions set up by micro code to registers in cache system)

CACHE PARTITION ADDRESSING

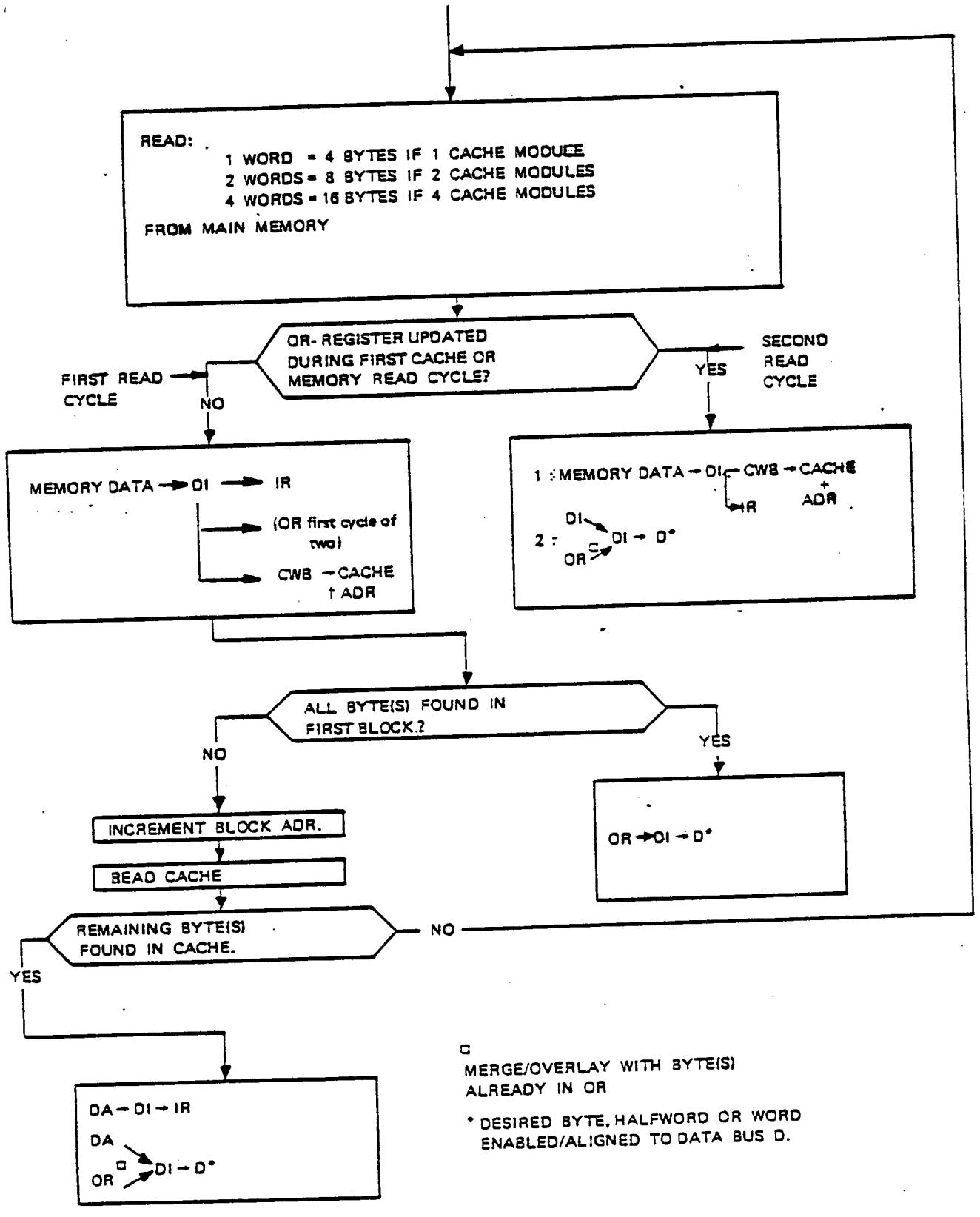


MEMORY READ ADDRESSED BYTE FOUND IN CACHE



* DESIRED BYTE, HALFWORD OR WORD ENABLED/ALIGNED TO DATA BUS D.

MEMORY READ ADDRESSED BYTE NOT FOUND IN CACHE



MAIN/CACHE MEMORY WRITE GENERAL:

— Write through algorithm as NORD-10/S-NORD-100. Cache data identical to main memory data

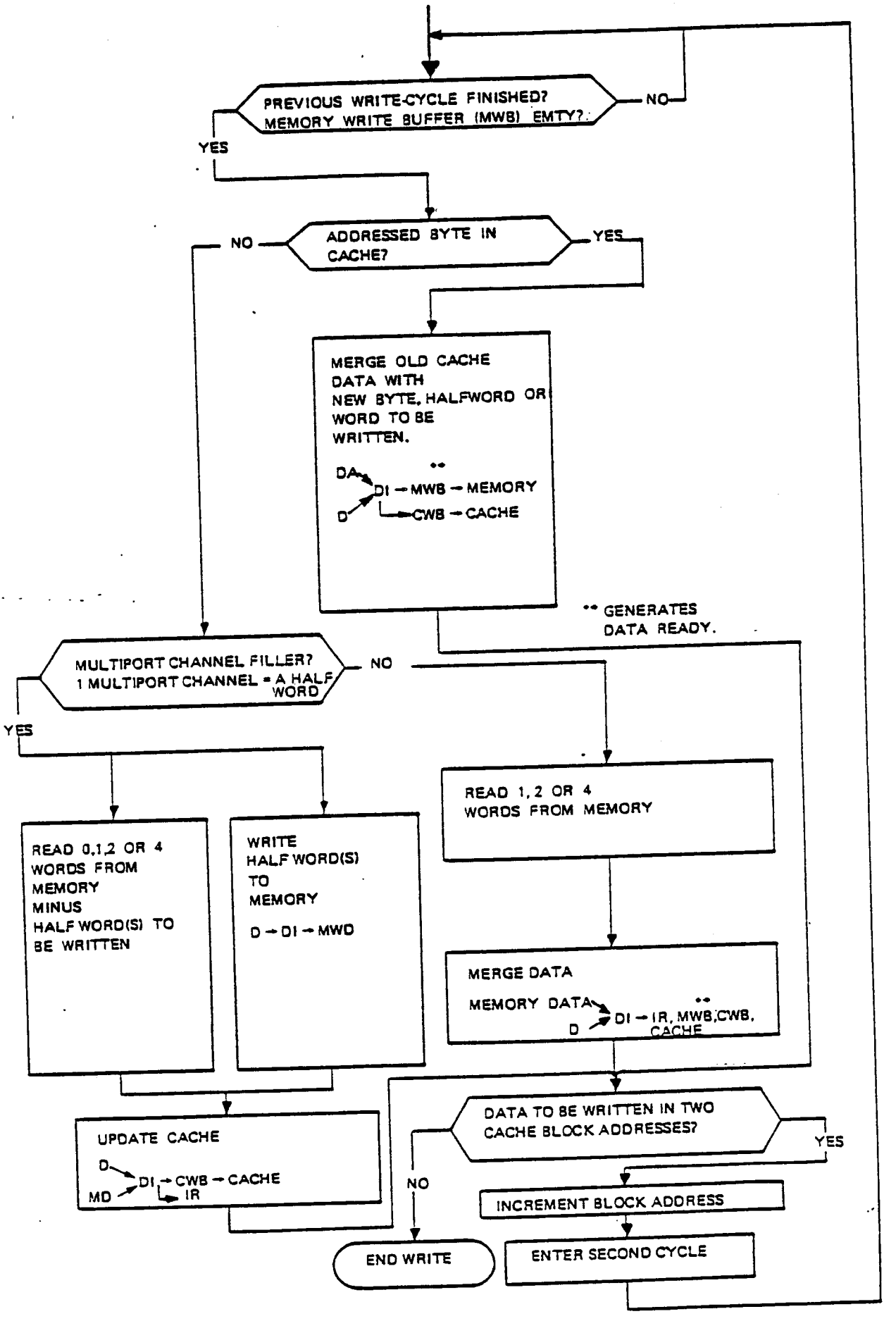
— Minimum main memory write = 1 multiport channel = 16 bits = 2 bytes = left or right half word

— Maximum main memory read = 8 multiport channels = 128 bits = 16 bytes (16 bytes of data and 16 bytes of instruction)

— When one cache module is installed, and one cache block (32 bits) is to be written:

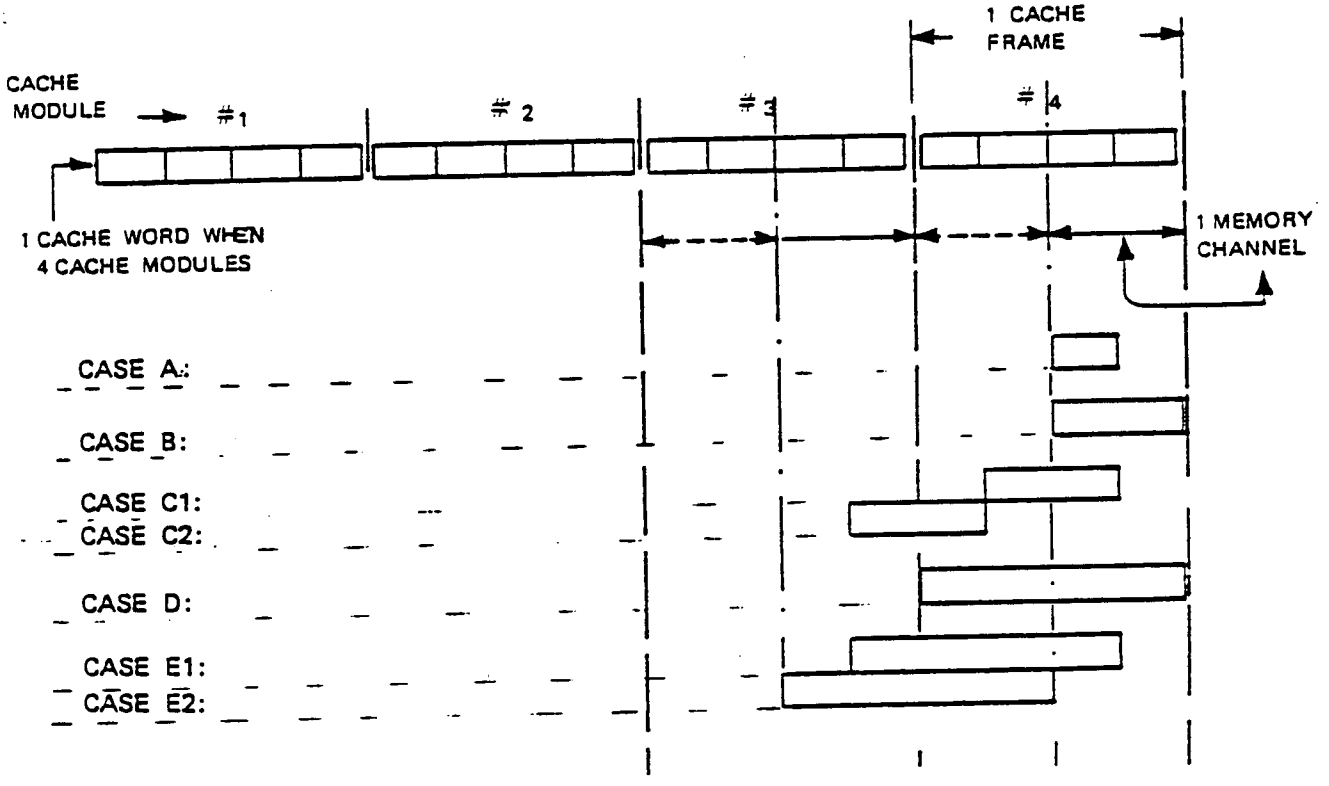
  Write main memory and update cache.
  (As N10/S and N100.)

MEMORY WRITE



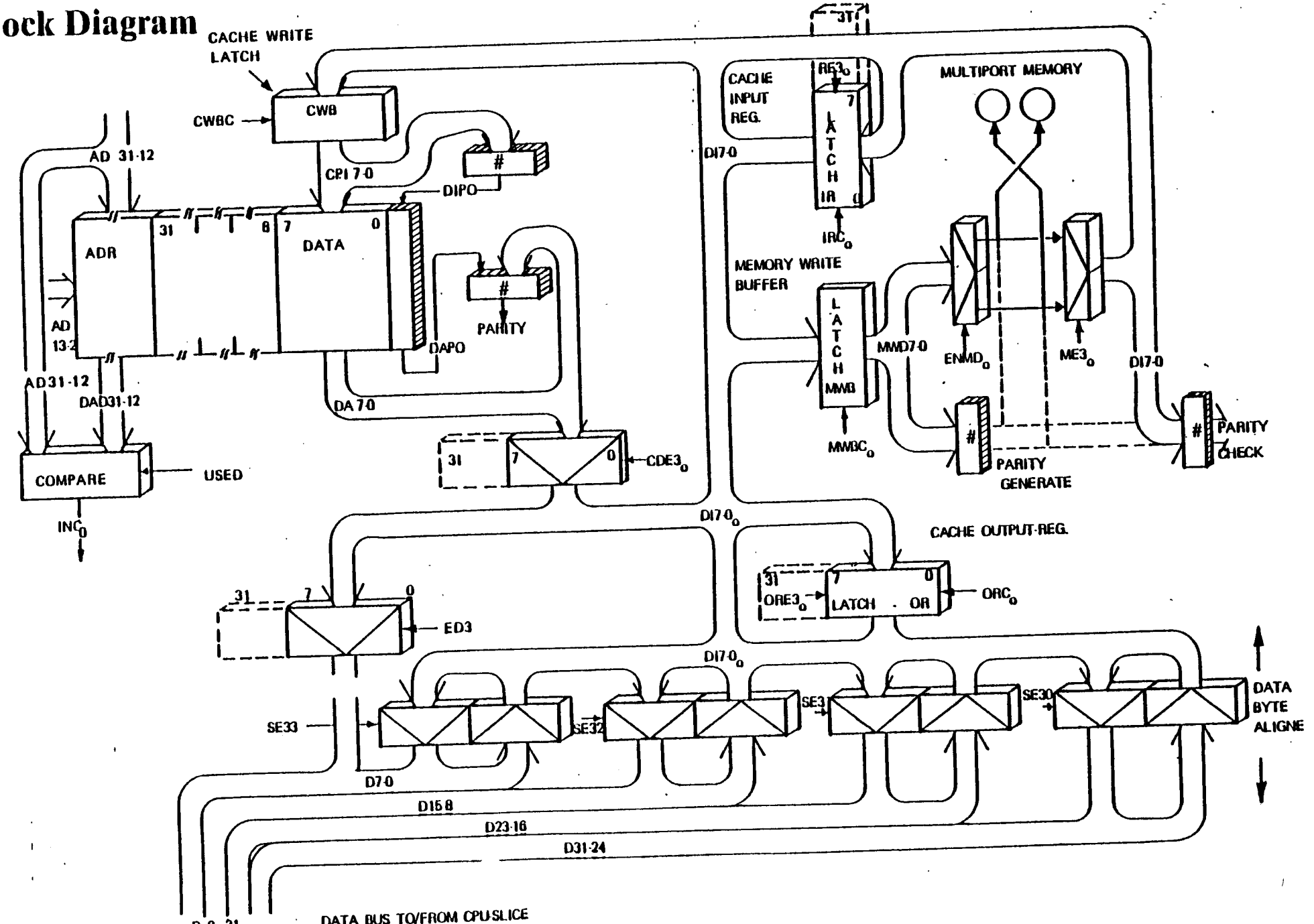
CACHE WRITE, continued.

Write and Data Not Found in Cache:



1 BYTE OF N-500 CACHE MEMORY

Block Diagram



EXTENDED DATA BUS - XD

NORD-100

The NORD-100 controls the XD bus when writing into the writable part of the control store.

Each control store address contains 144 bits and these bits are transferred from NORD-100 to the control store via the XD bus.

Sixteen bits are transferred from NORD-100 to the NORD-500 at a time.

The CONTROL STORE CONTROL register bits 2-5 (decoded as CS8-0) control which part of the control store word the 16 bits are written into. After 9 accesses a complete NORD-500 control store word is written.

Note that the control store group CS3 and CS2 handling bits 63-32 will not use the XD bus but will be routed directly to the control store via the internal bus on the NORD-100/500 communication module 5015 (CONTROL II).

The control store content may also be checked/read, by NORD-100, via the XD bus. This is controlled by bits 0 and 1 in the control store control register. Control store control register bit 0 equals 1 means: Control store load. While bit 1 equals 1 means: control store read.

NORD-500 XD BUS

The XD bus or the extended data bus is the main data highway for exchanging data and controlling information between the following NORD-500 modules:

- Memory Management
- Cache
- Control modules
- CPU slice

The XD bus is 32 bits wide and the data is exchanged via the A connector.

There are three sources that can control the data flow on the XD bus.

- The NORD-100
- The Prefetch Processor
- The Microprogram

THE PREFETCH PROCESSOR

The prefetch processor will use the XD bus for passing the extracted information from the instruction to the SLICE modules. The following information is extracted from the DATA part of the instruction:

— DISPLACEMENT BYTE(S)
— ABSOLUTE ADDRESS BYTES
— CONSTANTS BYTE(S)

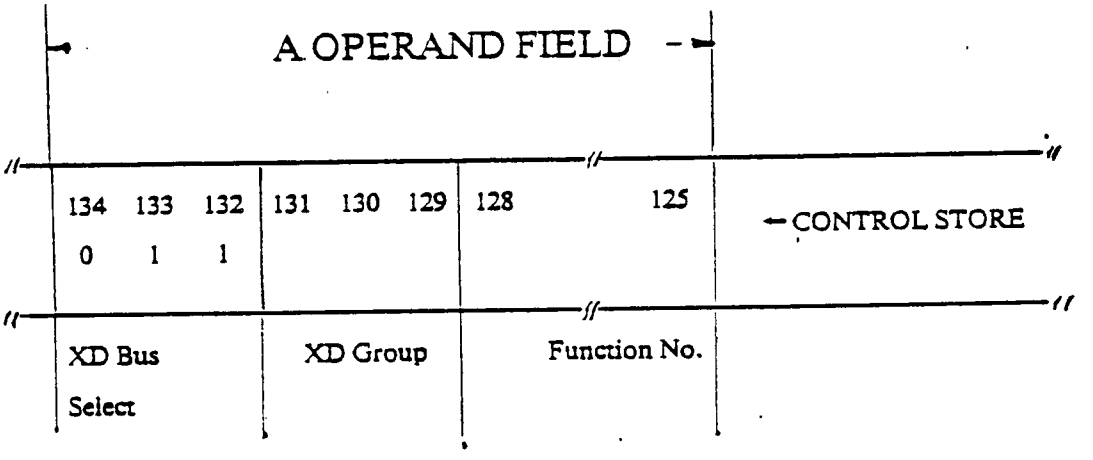
The displacement and the absolute address bytes will be routed to the address arithmetic on the SLICE. The constant bytes will be routed to the SLICE where the bytes will be passed on to the DATA bus and latch in the DATA latches.The DATA latches will then be selected as input to the INTEGER ALU or the FLOATING ARITHMETIC, depending on the constant type and the operation type.

XD BUS MICROPROGRAM CONTROL

The XD bus will be selected as operand when the control store bits 134 - 132 = 3. The modules connected to the XD bus, able to pass data onto the bus, are identified by the control store bits 131-129.

These bits are also referred to as the XD GROUP bits in the A operand field. Control store bits 128-125 (FUNCTION NO. bits) will select the operand register within the selected module. Note that XD GROUPS 1 and 2 have 3 modules. These modules will be separated by the function number.

XD BUS A OPERAND SELECT:



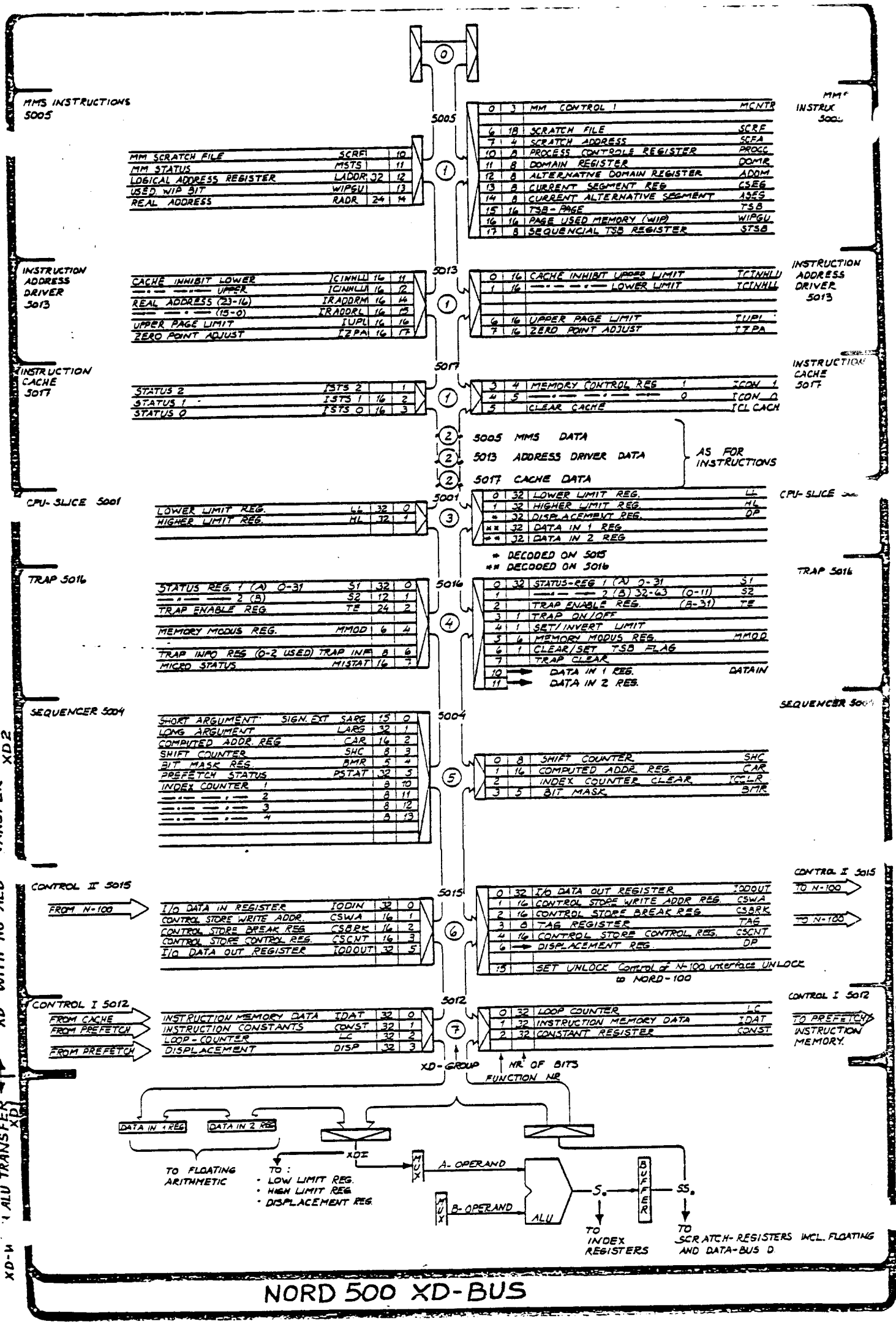
The destination module of the XD bus data is identified by the control store bit 112-110 (XD GROUP). The control store bits 109-106 equal the function number within the destination module.

If the DESTINATION SELECT field (bits 115-113) equals 6 the XD bus operand data will be routed through the INTEGER ALU as an A operand. Logical/arithmetical operations can then be performed with any selected B operand. The output of the ALU will be written into the selected destination XD group/ function.

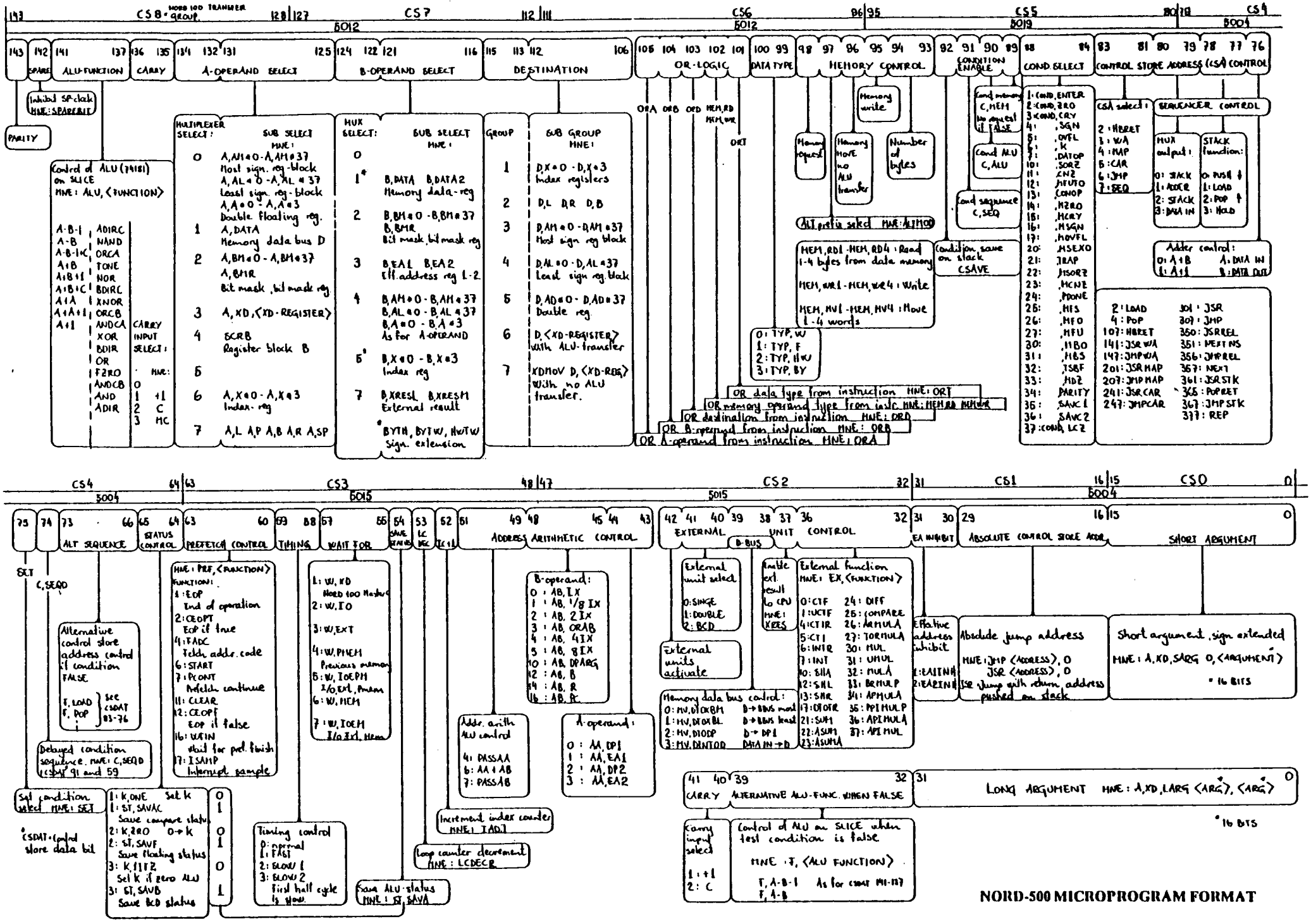
With the DESTINATION SELECT field equal to 7 the selected XD operand will be routed directly to the XD destination group function by bypassing the integer ALU.

The micro code mnemonic for this is: XDMOV % XD BUS MOVE.

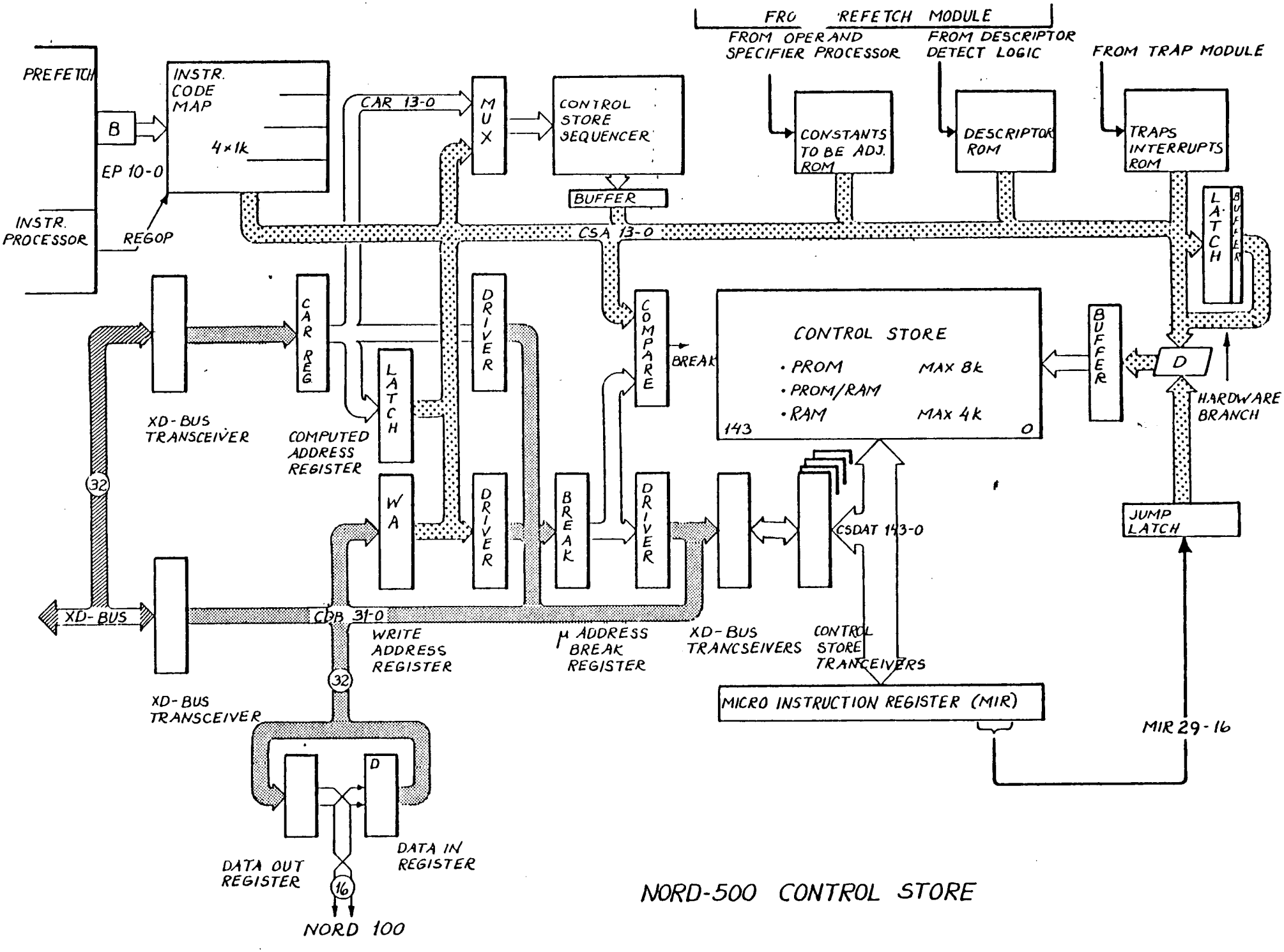
115	114	113	112	111	110	109	106	← Destination field of control store
			XD Group			XD Function		
1	1	0	XD1 = XD ALU TRANSFER					
1	1	1	XD2 = XD NO ALU TRANSFER					


MMS INSTRUCTIONS 5005
INSTRUCTION ADDRESS DRIVER 5013
INSTRUCTION CACHE 5017
CPU-SLICE 5001
TRAP 5016
SEQUENCER 5004
CONTROL II 5015
CONTROL I 5012
FROM N-100
FROM CACHE
FROM PREFETCH
FROM PREFETCH
MM SCRATCH FILE SCRF 10
MM STATUS MSTS 11
LOGICAL ADDRESS REGISTER LADDR 32 12
USED WIP BIT WIPGU 13
REAL ADDRESS RADR 24 14
CACHE INHIBIT LOWER ICINHLL 16 11
UPPER ICINHLU 16 12
REAL ADDRESS (23-16) IRADDRM 16 14
(15-0) IRADDRL 16 15
UPPER PAGE LIMIT IUPL 16 16
ZERO POINT ADJUST IZPA 16 17
STATUS 2 ISTS 2 1
STATUS 1 ISTS 1 16 2
STATUS 0 ISTS 0 16 3
LOWER LIMIT REG. LL 32 0
HIGHER LIMIT REG. HL 32 1
STATUS REG. 1 (A) 0-31 S1 32 0
2 (B) S2 12 1
TRAP ENABLE REG TE 24 2
MEMORY MODUS REG. MMOD 6 4
TRAP INFO REG (0-2 USED) TRAP INF 8 6
MICRO STATUS MISTAT 16 7
SHORT ARGUMENT SIGN. EXT SARG 15 0
LONG ARGUMENT LARG 32 1
COMPUTED ADDR. REG CAR 16 2
SHIFT COUNTER SHC 8 3
BIT MASK REG. BMR 5 4
PREFETCH STATUS PSTAT 32 5
INDEX COUNTER 1 8 10
2 8 11
3 8 12
4 8 13
I/O DATA IN REGISTER IODIN 32 0
CONTROL STORE WRITE ADDR. CSWA 16 1
CONTROL STORE BREAK REG CSBRK 16 2
CONTROL STORE CONTROL REG. CSCNT 16 3
I/O DATA OUT REGISTER IODOUT 32 5
INSTRUCTION MEMORY DATA IDAT 32 0
INSTRUCTION CONSTANTS CONST 32 1
LOOP-COUNTER LC 32 2
DISPLACEMENT DISP 32 3
5005
0 3 MM CONTROL 1 MCNTR
6 18 SCRATCH FILE SCRF
7 4 SCRATCH ADDRESS SCFA
10 8 PROCESS CONTROLE REGISTER PROCC
11 8 DOMAIN REGISTER DOMR
12 8 ALTERNATIVE DOMAIN REGISTER ADOM
13 8 CURRENT SEGMENT REG CSEG
14 8 CURRENT ALTERNATIVE SEGMENT ASES
15 16 TSB-PAGE TSB
16 16 PAGE USED MEMORY (WIP) WIPGU
17 8 SEQUENCIAL TSB REGISTER STSB
5013
0 16 CACHE INHIBIT UPPER LIMIT TCINHLU
1 16 LOWER LIMIT TCINHLL
6 16 UPPER PAGE LIMIT TUPL
7 16 ZERO POINT ADJUST TZPA
5017
3 4 MEMORY CONTROL REG 1 ICON 1
4 5 0 ICON 0
5 CLEAR CACHE ICL CACH
5005 MMS DATA
5013 ADDRESS DRIVER DATA
5017 CACHE DATA
AS FOR INSTRUCTIONS
5001
0 32 LOWER LIMIT REG. LL
1 32 HIGHER LIMIT REG. HL
* 32 DISPLACEMENT REG. DP
** 32 DATA IN 1 REG.
** 32 DATA IN 2 REG
* DECODED ON 5015
** DECODED ON 5016
5016
0 32 STATUS-REG 1 (A) 0-31 S1
1 2 (B) 32-43 (0-11) S2
2 TRAP ENABLE REG. (A-31) TE
3 1 TRAP ON/OFF
4 1 SET/INVERT LIMIT
5 6 MEMORY MODUS REG. MMOD
6 1 CLEAR/SET TSB FLAG
7 TRAP CLEAR
10 DATA IN 1 REG. DATAIN
11 DATA IN 2 RES.
5004
0 8 SHIFT COUNTER SHC
1 16 COMPUTED ADDR. REG. CAR
2 INDEX COUNTER CLEAR ICCLR
3 5 BIT MASK BMR
5015
0 32 I/O DATA OUT REGISTER IODOUT
1 16 CONTROL STORE WRITE ADDR REG. CSWA
2 16 CONTROL STORE BREAK REG CSBRK
3 8 TAG REGISTER TAG
4 16 CONTROL STORE CONTROL REG. CSCNT
6 DISPLACEMENT REG. DP
15 SET UNLOCK Control of N-100 interface UNLOCK to NORD-100
5012
0 32 LOOP COUNTER LC
1 32 INSTRUCTION MEMORY DATA IDAT
2 32 CONSTANT REGISTER CONST
CONTROL I 5015
TO N-100
TO N-100
CONTROL I 5012
TO PREFETCH INSTRUCTION MEMORY
XD-GROUP
NR OF BITS
FUNCTION NR
DATA IN 1 REG
DATA IN 2 REG
XDI
TO FLOATING ARITHMETIC
TO :
• LOW LIMIT REG.
• HIGH LIMIT REG.
• DISPLACEMENT REG.
MUX
A-OPERAND
B-OPERAND
ALU
S
SS
BUFFER
TO INDEX REGISTERS
TO SCRATCH-REGISTERS INCL. FLOATING AND DATA-BUS D
XD WITH NO ALU TRANSFER XD2
ALU TRANSFER XD
NORD 500 XD-BUS

CONTROL MODULES



NORD-500 MICROPROGRAM FORMAT



NORD-500 CONTROL STORE

CPU SLICE 5001 (8 BITS PER MODULE)

- 4 index registers I1 - I4

- 32 duplicated scratch registers out of which:
  * 4 floating registers (32 bits) A1 - A4
  * 4 floating registers (64 bits) D1 - D4 = (A1 - A4) + (E1 - E4)
  * 1 THA, trap handler address register
  * 1 TOS, top of stack register

- Memory operand registers: B and R

- Subroutine return register: L

- Address arithmetic
  * index register scaling
    (with post indexing and descriptor addressing)
  * sign extension of the displacement

- Program arithmetic
  * Program counter (PC)
  * Next program counter (NPC)
  * Instruction look ahead counter (ILC)

- Lower limit/upper limit address registers

- Address comparators against lower/upper limit

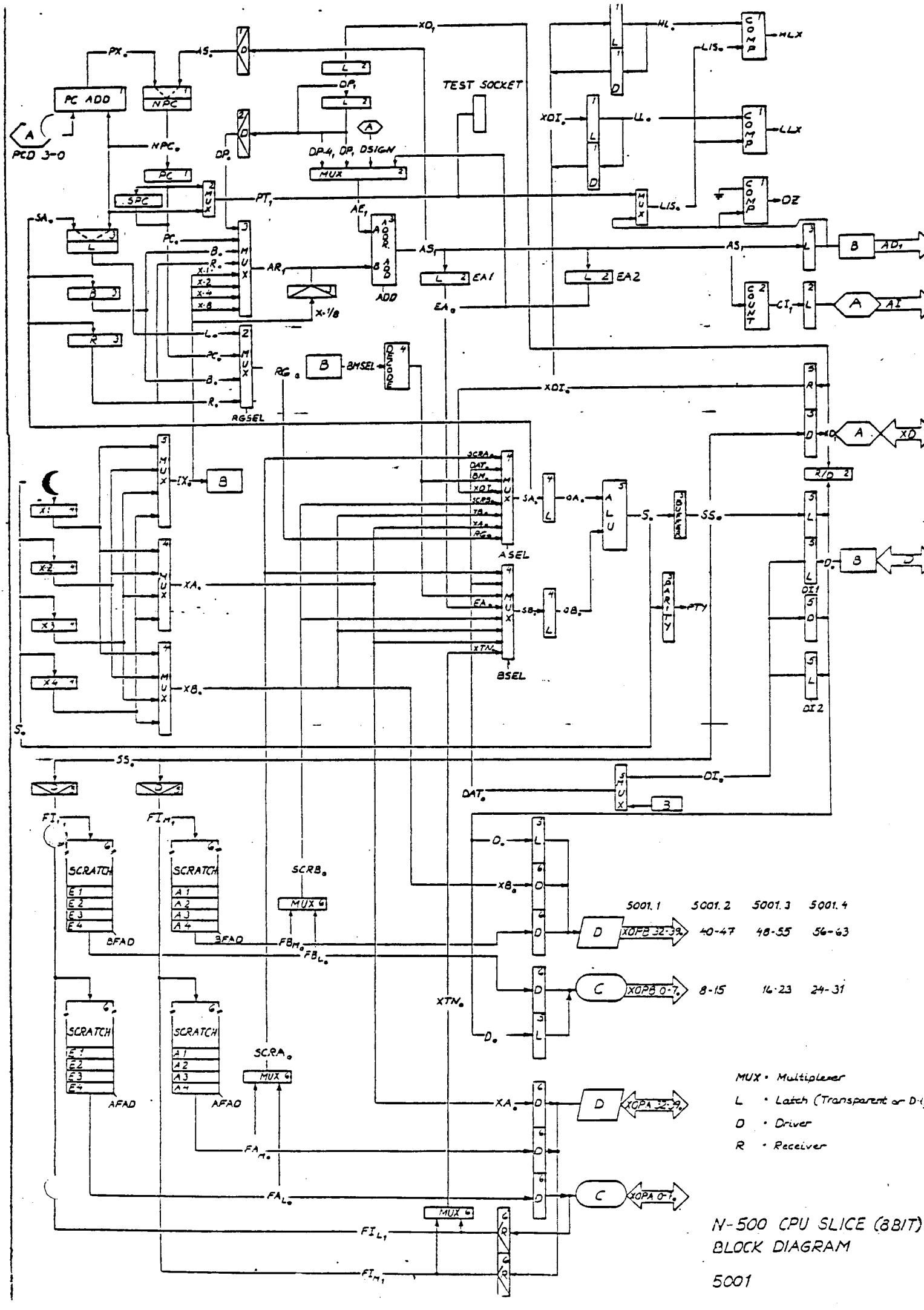
- Address zero comparator

- Integer ALU

- Data bus (D) transceivers/latches

- Extended data bus (XD) transceivers

- Floating arithmetic data bus transceivers/latches



N-500 CPU SLICE (8BIT)
BLOCK DIAGRAM

5001

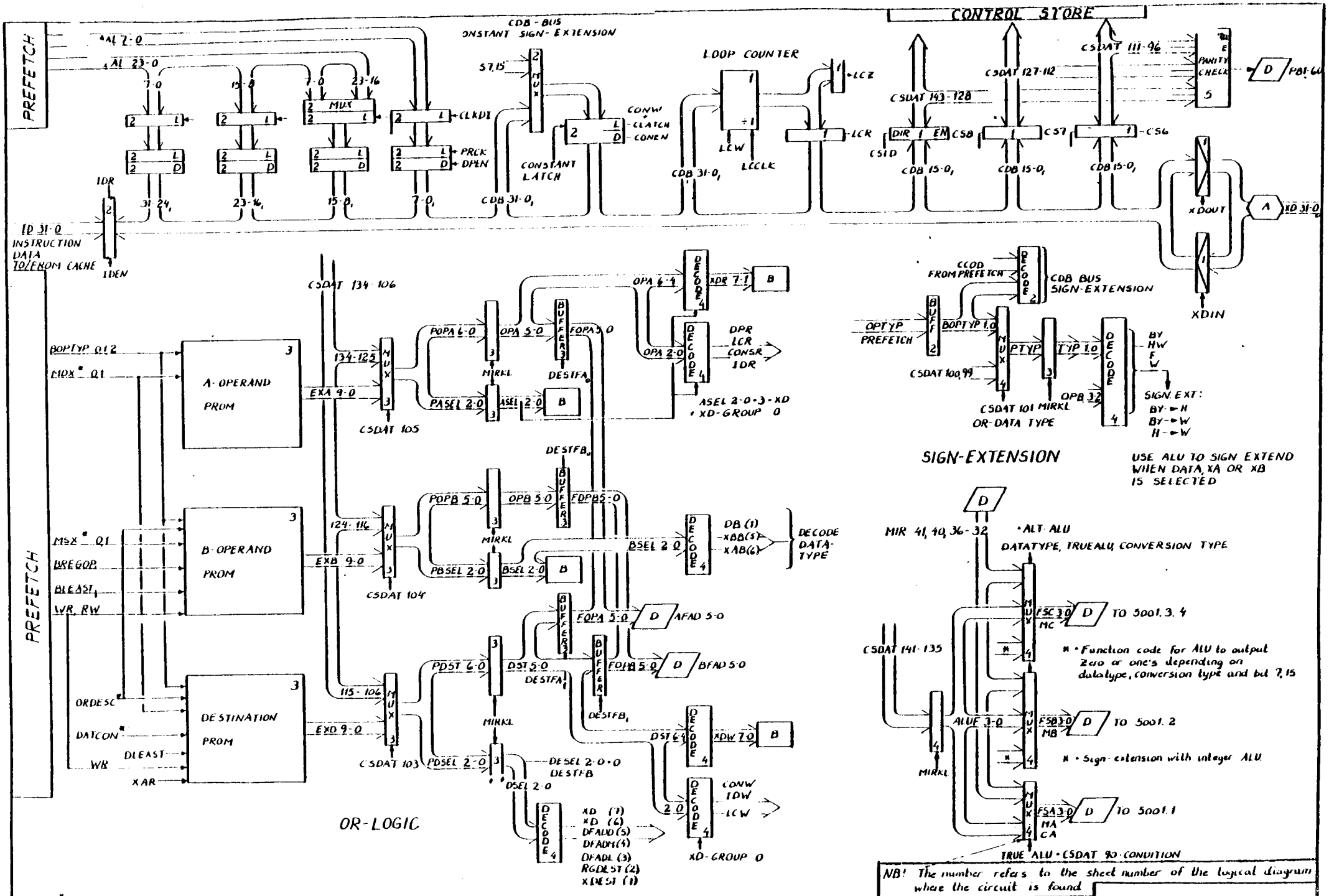
CONTROL I 5012

* Transceivers for control store bit 143 - 96
* XD bus transceivers
* Instruction data bus (ID) transceivers
* Prefetch extensions:
  2 pipeline registers for
  - Constants
  - Absolute addresses or
  - Displacements

Logic to sign extend instruction constants
Constant latch
* Loop counter
* OR logic (register maps)
  - A operand PROM
  - B operand PROM
  - Destination PROM

} PROM address from prefetch processor given by:
—index reg. no.
—data operand type and
—memory operand instruction

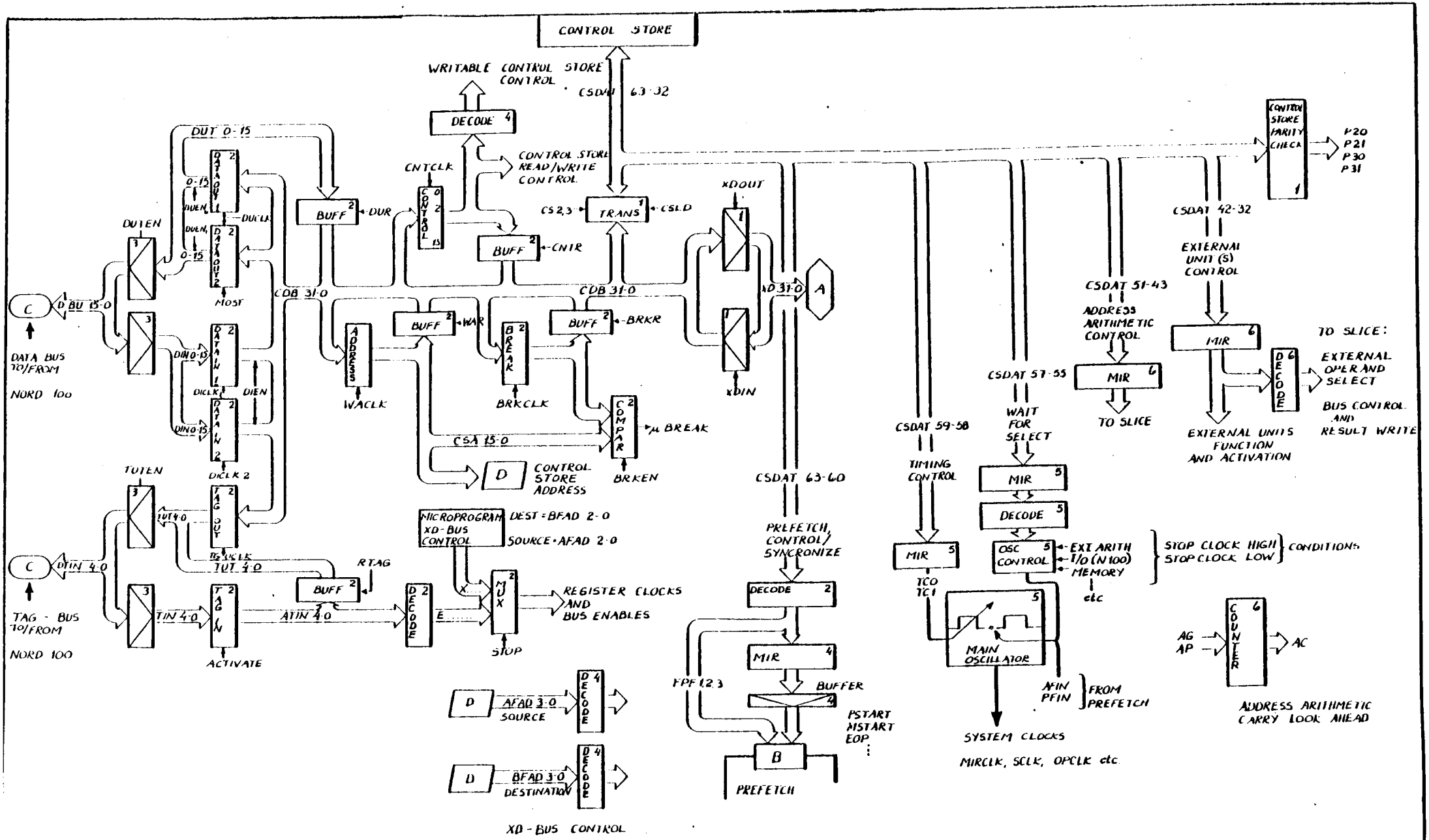
* A/B operand and destination select logic
* XD group decode logic
* ALU function control
  - Including logic to sign extend data with the integer ALU


PREFETCH
CONTROL STORE
CDB - BUS
ONSTANT SIGN- EXTENSION
LOOP COUNTER
CSDAT 111-96
CSDAT 127-112
CSDAT 143-128
CONSTANT LATCH
CDB 31-0,
CDB 15-0,
LCZ
LCR
LCCLK
LCW
CLKDI
PRCK
OPEN
CONW
CLATCH
CONEN
IDR
ID 31-0
INSTRUCTION DATA TO/FROM CACHE
IDEN
XDOUT
XDIN
CCOD FROM PREFETCH
CDB BUS SIGN-EXTENSION
OPTYP PREFETCH
BOPTYP 1-0
PTYP
TYP 1-0
CSDAT 100,99
CSDAT 101 MIRKL OR-DATA TYPE
OPB 3-2
SIGN EXT: BY-►H BY-►W H-►W
SIGN-EXTENSION
USE ALU TO SIGN EXTEND WHEN DATA, XA OR XB IS SELECTED
CSDAT 134-106
CSDAT 105
CSDAT 104
CSDAT 103
A-OPERAND PROM
B-OPERAND PROM
DESTINATION PROM
BOPTYP 0,1,2
MDX* 0,1
MSX* 0,1
BREGOP
BLEAST
WR, RW
ORDESC
DATCON*
DLEAST
WR
XAR
EXA 9-0
EXB 9-0
EXD 9-0
OPA 6-4
OPA 2-0
OPA 5-0
POPA 6-0
PASEL 2-0
ASEL 2-0
MIRKL
DESTFA0
DESTFB0
DESTFA1
DESTFB1
DPR
LCR
CONSR
IDR
ASEL 2-0=3=XD
XD-GROUP 0
OPB 5-0
POPB 5-0
PBSEL 2-0
BSEL 2-0
DB (1)
XBB(5)
XAB(6)
DECODE DATA-TYPE
FOPA 5-0
FOPB 5-0
AFAD 5-0
BFAD 5-0
DST 5-0
PDST 6-0
PDSEL 2-0
DESEL 2-0=0
DESTFB
DSEL 2-0
XDW 7-0
CONW
IDW
LCW
XD (7)
XD (6)
DFADD(5)
DFADM(4)
DFADL (3)
RGDEST (2)
XDEST (1)
OR-LOGIC
MIR 41, 40, 36-32
*ALT ALU
DATATYPE, TRUEALU CONVERSION TYPE
FSC 3-0
MC
FSB 3-0
MB
FSA 3-0
MA
CA
TO 5001.3.4
TO 5001.2
TO 5001.1
ALUF 3-0
CSDAT 141-135
* Function code for ALU to output Zero or one's depending on datatype, conversion type and bit 7,15
* Sign-extension with integer ALU
TRUE ALU - CSDAT 90 CONDITION
NB! The number refers to the sheet number of the logical diagram where the circuit is found
ALU-FUNCTION
FROM PREFETCH VIA VENCER (5004)
MIR GISTER
OPERAND/DESTINATION/ DECODE
5012 CONTROL I

CONTROL II 5015

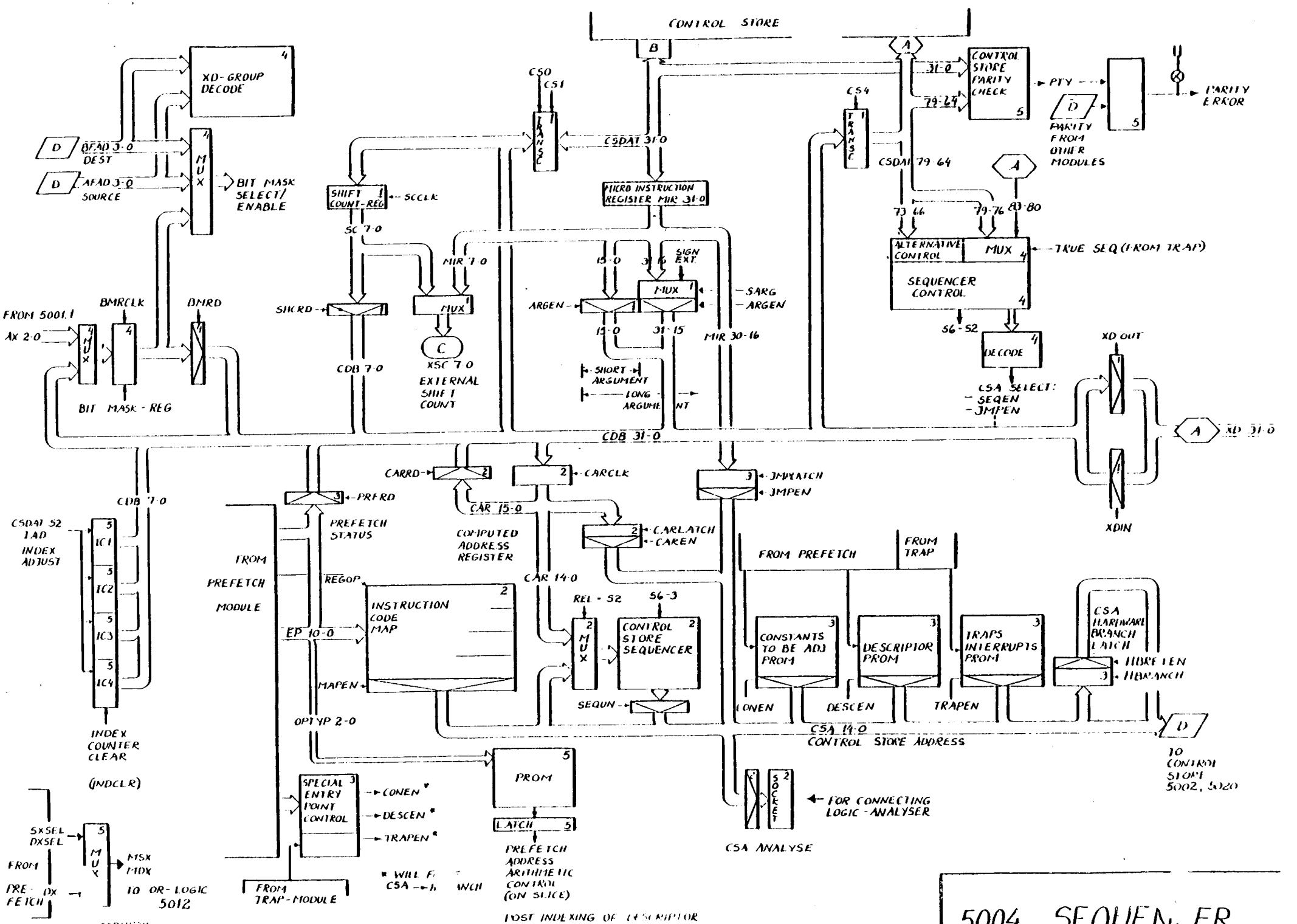
* Transceivers for control store bit 63 - 32
* XD bus transceivers
* NORD-100 communication logic including:
  - Data out register
  - Data in register
  - Tag in register
  - Tag out register
  - Control store write addr. reg.
  - Micro addr. break reg.
  - Control store control reg.
  - Drivers/receivers for data bus/tag bus + control signals

* Prefetch processor control logic
* Main oscillator
  - Including external units (I/O, Floating and Memory) Syncronize logic
* Address arithmetic control
  - Also address arithmetic carry look ahead
* Floating arithmetic control
  - Function bits + request
  - Floating data bus control
* XD group/function decode logic
* Result/destination clock generate


CONTROL STORE
WRITABLE CONTROL STORE CONTROL
CSDAT 63-32
DECODE 4
CONTROL STORE READ/WRITE CONTROL
CONTROL STORE PARITY CHECK
P20
P21
P30
P31
CNTCLK
CONTROL 15
TRANS 1
CSLD
CS2,3
BUFF 2
CNTR
DUR
DUT 0-15
DUEN
DUCLK
DATA OUT 2
MOST
DUTEN
DATA BUS TO/FROM NORD 100
C
DBU 15-0
DATA IN 2
DIN 0-15
DICLK
DICLK 2
DIEN
CDB 31-0
ADDRESS
WACLK
BUFF 2
WAR
BREAK 2
BRKCLK
BUFF 2
BRKR
COMPAR 2
μBREAK
BRKEN
CSA 15-0
D
CONTROL STORE ADDRESS
XDOUT
XDIN
1
XD 31-0
A
CSDAT 42-32
EXTERNAL UNIT (S) CONTROL
CSDAT 51-43
ADDRESS ARITHMETIC CONTROL
MIR 6
TO SLICE
MIR 6
DECODE 6
TO SLICE:
EXTERNAL OPERAND SELECT
BUS CONTROL AND RESULT WRITE
EXTERNAL UNITS FUNCTION AND ACTIVATION
CSDAT 59-58
TIMING CONTROL
MIR 5
TCO
TC1
CSDAT 57-55
WAIT FOR SELECT
MIR 5
DECODE 5
OSC CONTROL 5
EXT ARITH
I/O (N 100)
MEMORY
etc
STOP CLOCK HIGH
STOP CLOCK LOW
CONDITIONS
MAIN OSCILLATOR
AFIN
PFIN
FROM PREFETCH
SYSTEM CLOCKS
MIRCLK, SCLK, OPCLK etc
TUTEN
TUT 4-0
TUCLK
TUT 4-0
TAG BUS TO/FROM NORD 100
C
TIN 4-0
TAG IN 2
TAG OUT 2
ACTIVATE
TIN 4-0
BUFF 2
RTAG
DECODE 2
E
MICROPROGRAM XD-BUS CONTROL
DEST = BFAD 2-0
SOURCE = AFAD 2-0
X
MUX 2
REGISTER CLOCKS AND BUS ENABLES
STOP
D
AFAD 3-0
SOURCE
DECODE 4
D
BFAD 3-0
DESTINATION
DECODE 4
XD-BUS CONTROL
CSDAT 63-60
PREFETCH, CONTROL/ SYNCRONIZE
DECODE 2
MIR 4
BUFFER 4
PSTART
MSTART
EOP
FPF 1,2,3
B
PREFETCH
AG
AP
COUNTER 6
AC
ADDRESS ARITHMETIC CARRY LOOK AHEAD

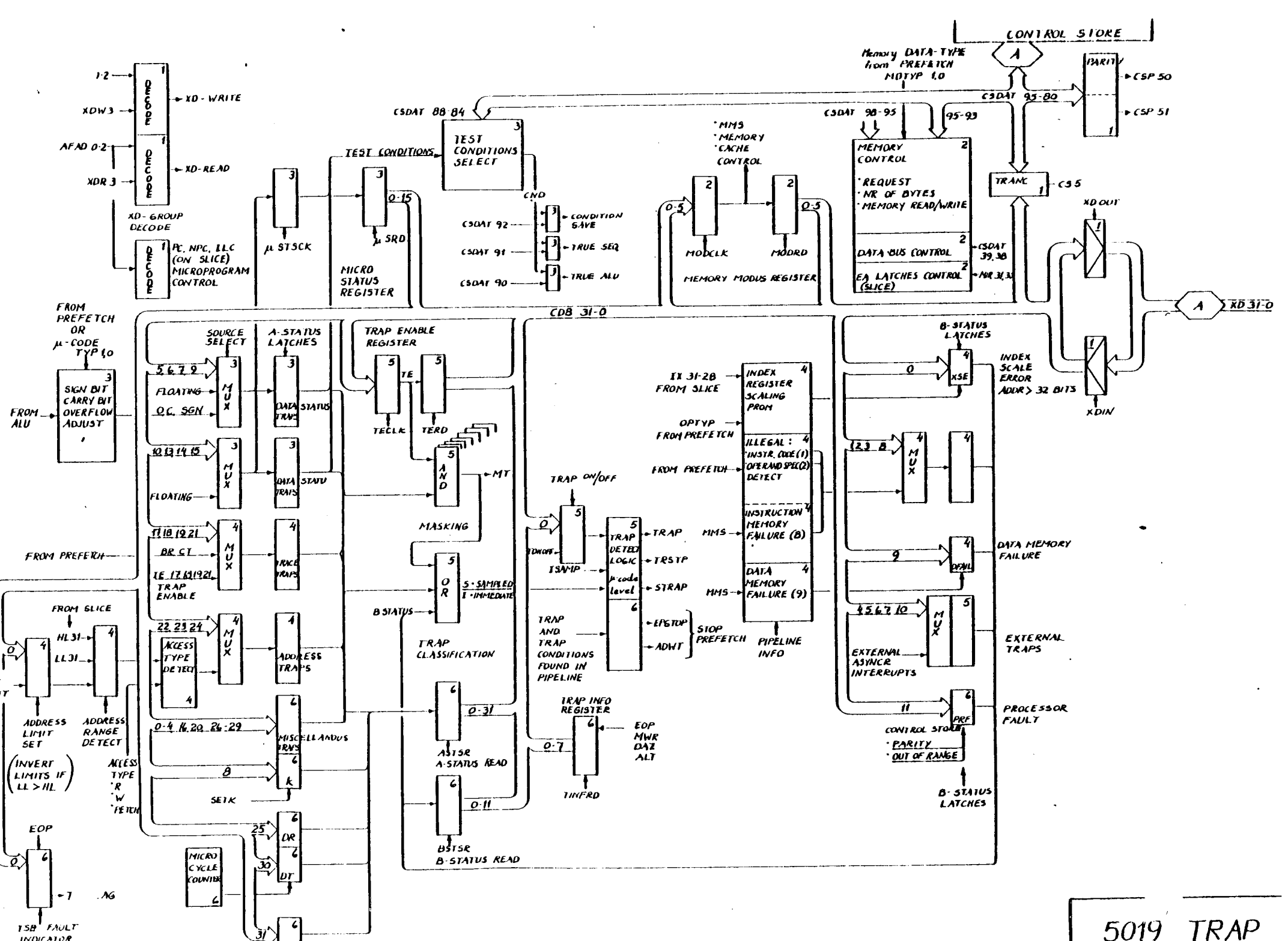
SEQUENCER 5004

* Transceivers for control store bit 79 - 64 and 31 - 0
* XD bus transceivers
* Microprogram addressing including:
  Control store address bus with these sources:
  - Instruction OPCODE MAP
    First micro instruction address
  - Sequencer (74S482)
    Next sequencial micro instruction address
  - Jump address (CSDAT 29 - 16)
  - Computed address register
    Micro instruction subroutine return address jump
  - PROMS giving special entry points for:
    * Descriptor addressing
    * Constant operand with mismatch in data type
    * Traps/interrupts
* XD group/function decode logic
* Bit mask register (5 bits)
* Control logic to bit mask decoder on CPU slice
* Short/long arguments registers (CSDAT 15-0 and 30 - 0)
* External shift count select
  Shift count register (SC7-0) or MIR7-0 = CSDAT 7-0.
* Index counters (4 x 8 bits)


CONTROL STORE
XD-GROUP DECODE
DFAD 3-0 DEST
AFAD 3-0 SOURCE
MUX
BIT MASK SELECT/ ENABLE
CS0
CS1
CS4
CSDAT 31-0
CONTROL STORE PARITY CHECK
PTY
PARITY ERROR
PARITY FROM OTHER MODULES
CSDAT 79 64
SHIFT COUNT-REG
SCCLK
SC 7-0
MICRO INSTRUCTION REGISTER MIR 31-0
MIR 7-0
SHCRD
MUX
C
XSC 7-0
EXTERNAL SHIFT COUNT
SIGN EXT
ARGEN
SARG
ARGEN
SHORT ARGUMENT
LONG ARGUMENT
MIR 30-16
ALTERNATIVE CONTROL
SEQUENCER CONTROL
TRUE SEQ (FROM TRAP)
56-52
DECODE
CSA SELECT:
- SEQEN
- JMPEN
XD OUT
XDIN
XD 31-0
FROM 5001.1
AX 2-0
BMRCLK
BMRD
BIT MASK-REG
CDB 31-0
CDB 7-0
CARRD
CARCLK
JMPLATCH
JMPEN
PREFRD
PREFETCH STATUS
CAR 15-0
COMPUTED ADDRESS REGISTER
CARLATCH
CAREN
CSDAT 52
IAD
INDEX ADJUST
IC1
IC2
IC3
IC4
INDEX COUNTER CLEAR
(INDCLR)
FROM PREFETCH MODULE
REGOP
EP 10-0
MAPEN
INSTRUCTION CODE MAP
CAR 14-0
REL-52
56-3
MUX
CONTROL STORE SEQUENCER
SEQUN
OPTYP 2-0
FROM PREFETCH
FROM TRAP
CONSTANTS TO BE ADJ PROM
DESCRIPTOR PROM
TRAPS INTERRUPTS PROM
CSA HARDWARE BRANCH LATCH
HBRPTEN
HBRANCH
CONEN
DESCEN
TRAPEN
CSA 14-0
CONTROL STORE ADDRESS
TO CONTROL STORE 5002, 5020
SPECIAL ENTRY POINT CONTROL
PROM
LATCH
PREFETCH ADDRESS ARITHMETIC CONTROL (ON SLICE)
SOCKET
FOR CONNECTING LOGIC-ANALYSER
CSA ANALYSE
SXSEL
DXSEL
FROM PRE-FETCH
MSX
MDX
10 OR-LOGIC 5012
FROM TRAP-MODULE
* WILL F... CSA ...H
...OST INDEXING OF ...SCRIPTOR
5004 SEQUENCER

TRAP 5019

* Transceivers for control store bit 95-80
* XD bus transceivers
* Trap system including
  - Trap enable register
  - Masking of trap/enable/status bits
  - Stopping of prefetch processor when traps
* Status register of 48 bits
* Logic for detecting carry, sign, zero and overflow according to the data type
* Micro status registers of 15 bits
* Memory control logic
  - Memory request
  - Memory read/write } to cache control
  - Number of bytes
  - Memory data ready } from cache control
* Test conditions
  - Sequencer control (seq./alt. seq. inst.)
  - Prefetch control when IF instr.
  - ALT-ALU control
* Micro cycle counter
  - Instruction SOLO turns of trap system for 256 micro cycles.
* XD group/function decode logic


CONTROL STORE
Memory DATA-TYPE from PREFETCH MDTYP 1,0
CSDAT 95-80
CSP 50
CSP 51
CSDAT 98-95
95-93
CSDAT 88-84
TEST CONDITIONS
TEST CONDITIONS SELECT
COND
CSDAT 92
CSDAT 91
CSDAT 90
CONDITION SAVE
TRUE SEQ
TRUE ALU
µ ST5CK
µ SRD
MICRO STATUS REGISTER
MMS
MEMORY
CACHE CONTROL
MODCLK
MODRD
MEMORY MODUS REGISTER
MEMORY CONTROL
REQUEST
NR OF BYTES
MEMORY READ/WRITE
DATA BUS CONTROL
EA LATCHES CONTROL (SLICE)
CSDAT 39,38
NR 31,30
TRANC
CS 5
XD OUT
XDIN
XD 31-0
CD8 31-0
XD-WRITE
XD-READ
XD-GROUP DECODE
PC, NPC, LLC (ON SLICE) MICROPROGRAM CONTROL
FROM PREFETCH OR µ-CODE TYP 1,0
FROM ALU
SIGN BIT CARRY BIT OVERFLOW ADJUST
SOURCE SELECT
A-STATUS LATCHES
FLOATING
O.C. SGN
DATA TRAPS
STATUS
TRAP ENABLE REGISTER
TECLK
TERD
MASKING
MT
B STATUS
TRAP CLASSIFICATION
S-SAMPLED I-IMMEDIATE
FROM PREFETCH
TRAP ENABLE
ADDRESS TRAPS
PRICE TRAPS
ACCESS TYPE DETECT
FROM SLICE
SET LIMIT
ADDRESS LIMIT SET
ADDRESS RANGE DETECT
(INVERT LIMITS IF LL > HL)
ACCESS TYPE R W FETCH
MISCELLANOUS TRAPS
SETK
EOP
TSB FAULT INDICATOR
MICRO CYCLE COUNTER
DR
DT
ASTSR A-STATUS READ
BSTSR B-STATUS READ
TRAP ON/OFF
TRAP AND TRAP CONDITIONS FOUND IN PIPELINE
TRAP DETECT LOGIC
µ code level
TRAP
TRSTP
STRAP
EPSTOP
ADWT
STOP PREFETCH
TRAP INFO REGISTER
EOP MWR DAZ ALT
TINFRD
IX 31-28 FROM SLICE
INDEX REGISTER SCALING PROM
OPTYP FROM PREFETCH
ILLEGAL : INSTR. CODE (1) OPERAND SPEC (2) DETECT
INSTRUCTION MEMORY FAILURE (8)
DATA MEMORY FAILURE (9)
MMS
PIPELINE INFO
B-STATUS LATCHES
XSE
INDEX SCALE ERROR ADDR > 32 BITS
DPAIL
DATA MEMORY FAILURE
EXTERNAL ASYNCR INTERRUPTS
EXTERNAL TRAPS
PRF
PROCESSOR FAULT
CONTROL STORE PARITY OUT OF RANGE
B-STATUS LATCHES

5019 TRAP

FLOATING POINT UNIT

COMBINATORIAL FLOATING POINT PROCESSOR AS AN INTEGRAL PART OF THE COMPUTER

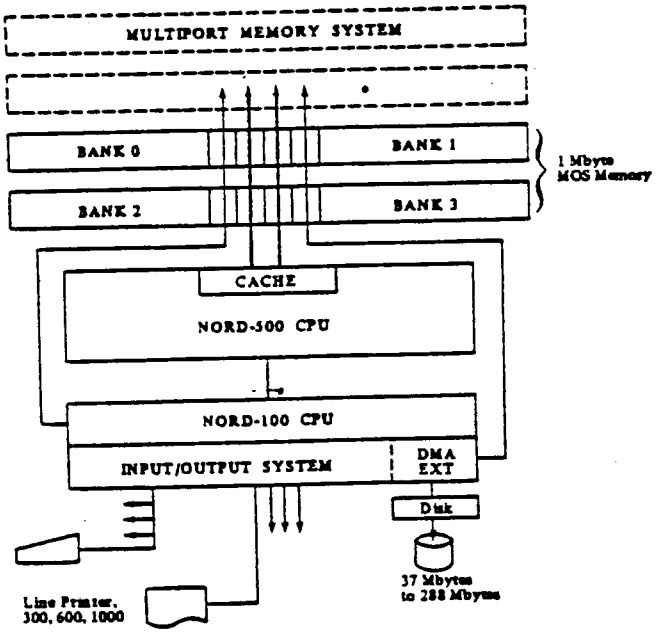
Tor Undheim
Norsk Data A.S
Jerikoveien 20
Lindeberg gård, Oslo 10
Norway

INTRODUCTION

The NORD-500 is a dual computer system consisting of a NORD-500 CPU, a NORD-100 CPU and a multiport memory. The NORD-500 CPU executes large time-consuming user programs. The NORD-100 minicomputer acts as a system supervisor for the NORD-500. The NORD-100 runs the multi-mode, multi-user SINTRAN III/VS operating system and performs all input/output handling, job scheduling and resource allocations. The NORD-100 leaves the NORD-500 CPU free to run user programs with a minimum of system overhead.

Up to 64 users can access the system in Real-Time, Time-Sharing and Batch mode, and share up to 32 Mbytes of fast MOS memory and 2300 Mbytes of disk storage, and a variety of other peripherals.

The basic time of 200 ns executes the majority of the NORD-500's machine instructions. Several NORD-500 processors, with hardware array logic for 32/64 bit floating point multiply/divide, can act as a multiprocessor system supervised by a NORD-100.



Basic NORD-500 Computer System

DATA FORMATS IN NORD-500

The basic unit for addressing is one byte of 8 bits. The data formats are bit, byte, half word, word, single precission floating point and double precision floating point.

Bit

The least significant bit in a byte may be accessed by bit instructions. Bit arrays may be accessed using post indexing or descriptor addressing.

Byte

A byte is 8 bits and can be used as an unsigned number with the range 0 to $2^8 - 1$, or as twos complement number signed with the range -2^7 to $2^7 - 1$.

Half Word

A half word is 2 bytes or 16 bits and can be used as an unsigned number with the range 0 to $2^{16} - 1$, or as a twos complement number signed with the range -2^{15} to $2^{15} - 1$.

Word

A word is 32 bits or 4 bytes and can be used as an unsigned number with the range 0 to $2^{32} - 1$, or as a twos complement number with the range -2^{31} to $2^{31} - 1$.

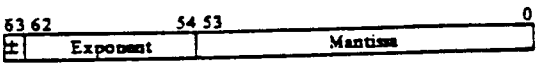
Single Precision Floating Point

A floating point number is represented by a mantissa of 22 + 1* bits, an exponent of 9 bits with the bias 400_8, and a sign bit.

The range is 10^{-76} to 10^{76}. Zero is represented as all exponent bits zero. The accuracy is approximately 7 digits.

Double Precision Floating Point

A double precision floating point number is represented by a mantissa of 54 + 1* bits, an exponent of 9 bits with the bias 400_8 and a sign bit.



The range is 10^{-76} to 10^{76}. Zero is represented as all exponent bits zero. The accuracy is approximately 16 decimal digits.

• For both single and double floating point number there is always one hidden bit in the mantissa. This is called the implicit bit. The implicit bit is always assumed to be one, unless all bits in the exponent are zero. This bit is used in the arithmetic and removed from the result, thereby giving one more bit (+1) of precision.

THE FLOATING POINT UNIT

The Floating Point Unit (FPU) is made mainly to handle floating point numbers, but some instructions to handle integers are also implemented in this unit. The instruction list below indicates those instructions that can handle both integers and floating point numbers, or only integers.

The FPU is asynchronous to the rest of the CPU.

The CPU may either wait for the result or go back and read the result later. It may ever let the FPU take care of the result and use it in further calculations.

Each instruction is microprogrammed in the CPU.

INSTRUCTIONS

The FPU has the following one cycle (micro) instructions:

One Operand Instructions:

Convert integer (W, HW, BY) to floating
Unsigned convert to floating (W)
Convert floating to integer with rounding
Convert floating to integer with truncation
Integer part with rounding
Integer part with truncation
Shift arithmetic (W, HW, BY)
Shift logical (W, HW, BY)
Shift rotational (W, HW, BY)

Two Operand Instructions:

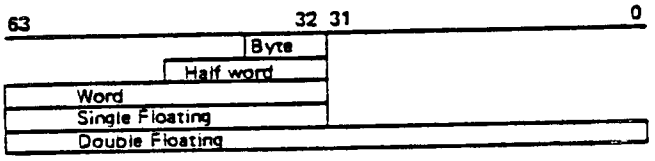
Add two operands [(A + B) → CPU]
Add one operand to accumulated result [(SA + B) → CPU]
Add one operand to accumulated result, save new result
[(SA + B) → SA]
Subtract second operand from first [(A − B) → CPU]
Compare A and B (only SIGN and ZERO flags valid)
Multiply A with table value for 1/B, save result
[(A · 1/B) → SA]
Multiply two operands (W, HW, BY, F, FD)
[(A · B) → CPU]
Unsigned multiply (W) [(A · B) → CPU]
Multiply two operands and save result [(A · B) → SA]
Multiply B and 1/B and save result
[(B · 1/B) → SP, $\overline{SP}$]
Multiply saved A and saved P, save result
[(SA · SP) → SA]
Multiply saved P and inverted P, save result
[(SP · $\overline{SP}$) → SP, $\overline{SP}$]
Multiply saved A and inverted P, save result
[(SA · $\overline{SP}$) → SA]
Multiply saved A and inverted P, result to CPU
[(SA · $\overline{SP}$) → CPU]

Some of these one cycle instructions have no "meaning" alone, but are used to form complete instructions like Divide and Polynomial.

COMMUNCIATION WITH THE CPU

Two 64 bit data busses are used to transmit data from the register block to the FPU. One of them is used to return the result.

The location of the different data types on the 64 b. busses is shown in the figure below.



In addition, there are 15 control signals, 7 status signals and 2 signals for timing.

The control signals are:

5 for instruction
2 for data type (byte, half word, word + floating)
2 for unit (single or double floating + combinations for further extensions)
6 for shift count

The status signals are:

Overflow
Underflow
Divide by zero
Sign of result
Zero as reusit
Inexact result (not used)
Invalid operation (not used)

Timing signals are:

START execution of an instruction in the FPU
DATA READY to indicate that the calculation is finished and the result may be transferred to the register block.

PHYSICAL DIMENSIONS

The whole NORD-500, including the optional 64 K byte instruction cache memory and 64 K byte data cache memory, consists of 26 printed circuit boards. Each board is approximately 16 inches high and 11 inches deep; and all of them are mounted on the same rack. Each board has four EURO connectors, and interconne ns are done by wire wrapped back panels.

The four layer PC boards have the same layout on inner layers (Power, Ground, etc.) and through plated holes. Only the outer layer traffic is different.

IC Count

The FPU is located on 4 different PC boards. The total number of IC's is 579. Those that are most often used are listed below:

34 pcs 8 x 8 Multiplier, 40 pins
113 pcs 1 K x 4 bit PROM, 18 pins
99 pcs 4 bit shifters, 16 pins
35 pcs 8 bit latches, 20 pins
91 pcs Data Selectors/Multiplexers with 2, 4 or 8 inputs
63 pcs 4 bit ALUs of different types
16 pcs 4 bit Comparators

The rest are Gates, Line drivers, PROMs, PALs and Priority Encoders.

INSTRUCTION REPERTOIRE

The instructions handled by the FPU are: (only floating point format if data type not mentioned)

Compare
Test against zero
Add
Subtract
Multiply (overflow) BY, HW, W, F, FD
Divide (remainder) BY, HW, W, F, FD
Unsigned multiply W
Unsigned divide W
Increment
Decrement
Shift (logical, arithmetic, rotational) BY, HW, W
A to the I'th power
I to the J'th power BY, HW, W
Square root
Polynomial ($C_0 + C_1 X + C_2 X^2 + ...$)
Floating remainder
Integer part
Integer part with rounding
Multiply and Add ($R(n) \cdot X + Y \rightarrow R(n)$)
Sum of products ($X \cdot Y + R(n) \rightarrow R(n)$)
Data type conversion
Data type conversion with rounding

INSTRUCTION EXECUTION TIMES

Instruction execution times for some of the instructions with operands in registers are:

Compare, Shift — 260 nsec.
Add, Subtract, Convert — 400 nsec.
Multiply — 480 nsec.
Integer Multiply — 580 nsec.
Divide, Single floating — 1.3 usec.
Divide, double floating — 2.1 usec.
Divide, integer — 3.3 usec.

DATA FLOW

The data flow during the execution of an instruction in the FPU is more easily understood by combining the following text with the figure in Appendix A.

Data and Instruction are latched at the end of a 60 nsec. START pulse. For one operand instructions, only the B operand is latched. For two operand instructions, both A and B operands are latched at the end of START, except if the specified A operand is already saved in the FPU from the previous instruction. Some specific instructions also latch the A operand into SP for later use.

The magnitude of the operands are compared in dedicated logic. This is used to gate the smallest operand to the Right Shifter in Add and Subtract instructions, and also to give Sign and Zero flags in Compare instructions.

Exponent arithmetic takes care of the exponent during floating point instructions. A normalized exponent is used as reference in Convert instructions and in Integer Part. Latches are used to save the exponent during a Divide sequence.

Two sets of Data Selectors are used to select operands. The smallest operand is selected for the route through the Right Shifter in Floating Add and Subtract instructions. Integer is selected if the data type is Byte, Half Word, Word (Multiply, Convert and Shift instructions).

All instructions, except where multiply is performed, use the data route through a Tristate Buffer for one operand and through a Right Shifter for the other (least) operand. In case of only one operand, this is gated through the Shifter. The shifter is composed of 3 levels of 4 input shift elements (25S10 or 74S350).

For all instructions, or part of the instructions where two operands have to be multiplied, the operands are used as input to a Multiplier Array. The Multiplier Array consists of 34 8 x 8 bit multipliers (67558 from MMI) and a lot of 1 K x 4 PROMs. The PROMs are used to add two columns and 5 rows to give a 4 i result. The first level is a reduction from the maximum 13 rows to maximum 6 rows. For the part with 6 rows, carry save adders of the type 74S283 are used for reduction to 5 rows. The remaining 5 rows are reduced to 2 by 1K x 4 PROMs. Output from this level is tristate and connected to the same ALU as used by all other instructions.

The ALU is used to add, subtract or invert. The operands may come from the Tristate Buffer/Right Shifter or from the Multiplier Array.

The output from the ALU is connected to a Priority Encoder and to a Left Shifter. If the result is a floating point number, then the Priority Encoder gives shift count to the shifter. Out comes the normalized unrounded floating point mantissa. If the result is an integer, the shift count is supported by the CPU as part of the instruction.

Rounding is performed in accordance with the IEEE proposed standard for Floating Point Arithmetic concerning addition, subtraction and convert instructions. In multiplications, some

information is lost due to the missing least significant part of the Multiplier. Divide is implemented by an inexact algorithm and is even worse than Multiply. At any rate, the same Rounding Adder is used for rounding of all floating point results.

The result is enabled to one of the 64 bit data busses between the CPU and the FPU, and may be clocked in the CPU and/or in the FPU, dependent on whether it is a final and/or an intermediate result.

WHY NONFLOATING OPERATIONS IN THE FPU?

The reason for implementing some nonfloating operations in the FPU is that most of the logic for implementing them is already there. Integer multiplication is done in the same multiplier array as the floating point mantissa. Integer divide is done by converting to floating point format first, do a floating point divide, and converting the floating result to integer. Shift instructions are easily handled by the Right and Left Shifters already there to shift the floating point mantissa.

DIVIDE

As mentioned, divide with integer operands is executed by:

Converting both operands to double precision floating point numbers
Do a double precision floating point divide
Convert the result to the specified type of integer (i.e., BY, HW, W)

When D is element in [0.5, 1> and is the dividend's mantissa and d is element in [0.5, 1> and is the divider's mantissa, the division D/d is executed by:

1. Multiply D and table value for 1/d, save result in A
2. Multiply d and table value for 1/d, save result in P
3. If single precision, go to 6.
4. Multiply saved A and two's complement of saved P, save result in A
5. Multiply saved P and two's complement of saved P, save result in P
6. Multiply saved A and two's complement of saved P, result to CPU.

Inexact Result

This method of dividing one number by another may give an inexact result.

If we call the correct result for Q we have

$$Q = D/d$$

We define a value R as the table value for 1/d and

$$P_1 = dR = 1 \pm e \qquad (e \text{ is a small value}) \qquad (1)$$

If we look at the divide steps, the double precision calculation gives us:

1. $Q_1 = DR = D/d\,(1 \pm e)$
2. $P_1 = dR = 1 \pm e,\ \overline{P_1} = 1 \mp e$
3. $Q_2 = Q_1 \cdot \overline{P_1} = D/d\,(1 - e^2)$
4. $P_2 = P_1 \cdot \overline{P_1} = 1 - e^2,\ \overline{P_2} = 1 + e^2$
5. $Q_3 = Q_2 \cdot \overline{P_2} = D/d\,(1 - e^4)$

From the calculation we can see that the calculated Q_3 is equal to the desired Q minus $Q \cdot e^4$. This is the ideal, but we also introduce some errors due to rounding.

Let us look at the e:

From (1) $P = dR = 1 \pm e$ we get

$$|e| = |dr - 1| \qquad (2)$$

We know that D is element in [0.5, 1> and d is element in [0.5, 1>

The value R we get from the table as "best guess" for 1/d can be defined as

$$R = 1/d_1$$

With an 8K lookup table, 13 bits are used to select R. The most significant bit in the mantissa is 1 unless the divider is zero, and is taken for granted in the lookup address. The table is calculated to give the best guess for the bits included in the address, which means it expects the first not included bit to be one and all others to be zero. This means that the maximum difference we can get between the divider d and the modified divider d_1 is in the range one unit of the first bit not included in the lookup address, or:

$$d_1 = d \pm 1 \cdot 2^{-13}$$

Worst case is $d = 0.5$, $R \sim 2\ [1.77774_8]$

This gives

$$|e| = |Rd_1 \pm R \cdot 2^{-15} - 1| \sim 2^{-14}$$

For d close to 1, R will also be close to 1 and

$$|e| \sim 2^{-15}$$

For double precision this gives us a maximum error in the result due to the method if Q is close to 2; that is

$$E_M = 2 \cdot (2^{-14}) = 2^{-53}$$

After that, the result is normalized, so that Q_{RES} is element in [0.5, 1> and

$$E_{RM} = 2^{-56}$$

Correcting Factor

If we look more closely to d and d_1 on the figure:

d_1 = .1XXXXXXXXXXXXX100 .....
and

d = .1XXXXXXXXXXXXXYYY .....

where all bits denoted X are used as addresses to the 1/d table.

The maximum difference between d and d_1 is

.000000000000001

From (2) we get

$|\varepsilon| = |dR - 1|$
$|\varepsilon| = |d/d_1 - 1|$

If we denote the difference between d and d_1 as

$\delta = |d_1 - d|$
or
$d = d_1 \pm \delta$

we get

$|\varepsilon| = |d_1/d_1 \pm \delta/d_1 - 1|$

or

$|\varepsilon| = |\delta/d_1|$

This formula is a good tool when inspecting the systematic error due to the method. What it shows is that the error in the final result decreases fast when d moves away from the "worst case" values. The bad thing about this error is that it is always in the same direction and therefore compensation has been introduced.

Rounding Errors

Contrary to the biased error due to the method, the rounding error is neutral. If we compare the magnitude, we find that the maximum rounding error in single precision is 16 times the maximum error due to the method. In double precision, the maximum rounding error is 5 times the maximum error due to the method. The rounding error in double precision may be 2 times the value of the least significant bit in the final result.

Integer divide uses the same divide sequence as double precision floating divide. However, there are no rounding errors in the two first multiplications and the maximum rounding error in the final floating result is in the range one time the value of the least significant bit.

It is very important that the final floating result is not less than the correct one in an integer divide sequence. As an example, two divided by one could give a result that in double floating format is one unit of the least significant mantissa bit less than two, and would give one as result when converted to integer. This is prevented by adding a small fraction to the final floating result.

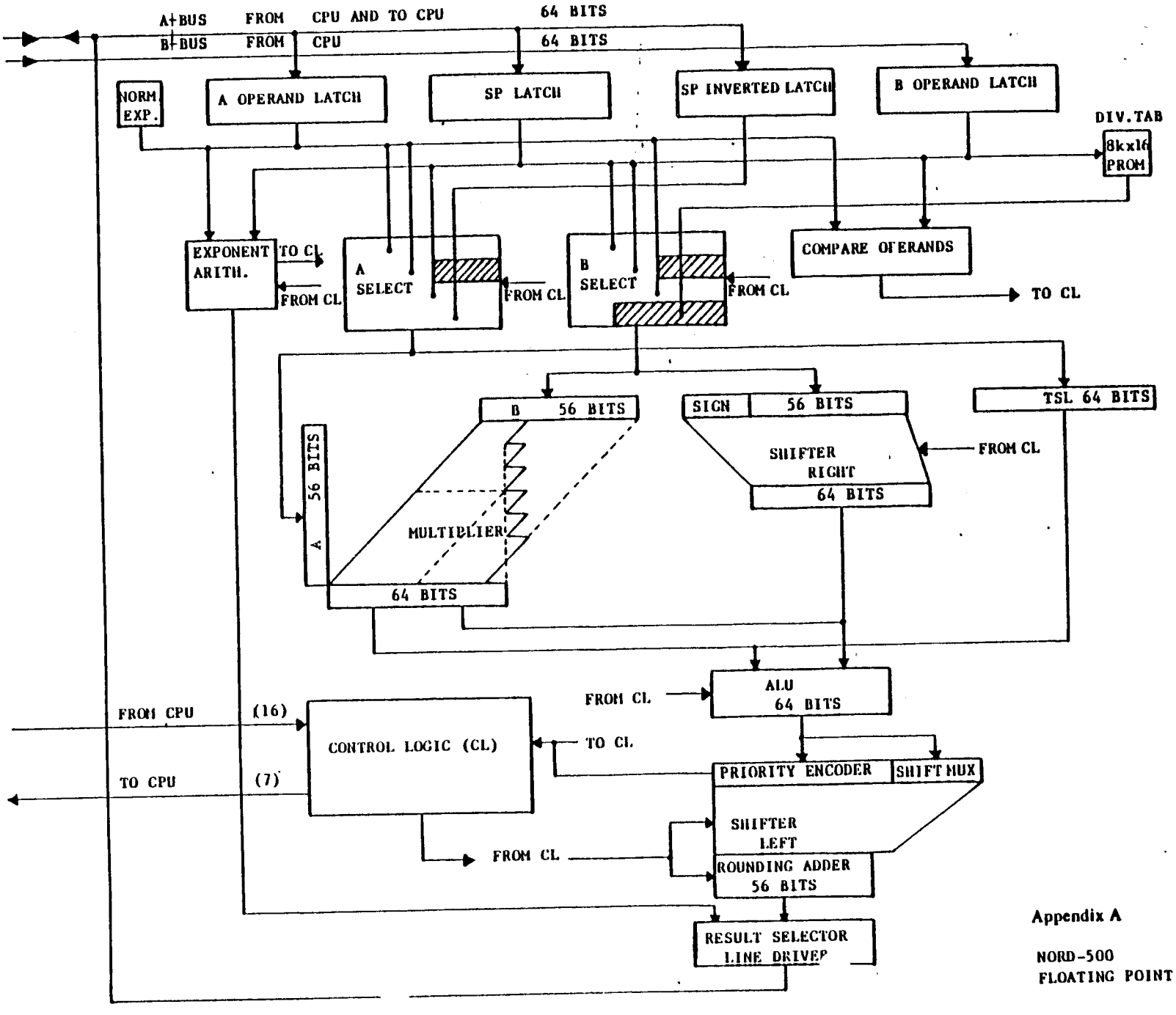
MULTIPLY

The multiply array has a missing part in the least significant end. This missing part gives a biased error in the result. The maximum value of this error is $5 \cdot 2^{-6}$ times the least significant bit in the result.

CONCLUSION

The Floating Point Unit in the NORD-500 computer is designed as a combinatorial unit. The formats of the floating point numbers are not the same as proposed in the IEEE proposal for standard, but that is for historical reasons.

Multiply and divide has reduced accuracy to achieve reduction in hardware cost and complexity. Correcting factors are used to compensate for the biased error this reduction in hardware would normally give.



Appendix A

NORD-500
FLOATING POINT UNIT

3. A short list of registers, IOX instructions etc.

The interface between the ND-100 and the ND-500 consists of 2 interface cards; the 3022 card on the ND-100, and the 5015 card on the ND-500. These cards contain several registers, which are listed below.

3.1. The CONTROL word register on 3022.

Bit:	Meaning:
0	Enable interrupt from ND-500
1	Not used
2	Activate ND-500 operation (and lock the communication)
3	Test mode
4	ND-500 programmed clear
5	Disable TAG-IN decoding when locked
6	DMA error
7	Command chaining
8-14	ND-500 operation
15	Not used

3.2. The STATUS register on 3022.

Bit:	Meaning:
0	Interrupt enabled
1	Not used
2	ND-500 busy
3	ND-500 finished
4	Error
5	Interface locked
6	DMA error
7	ND-500 power fault (set by micro program). The stop bit is set
8	ND-500 power is/has been off
9	ND-500 micro clock has stopped
10-14	ND-500 stop reason
15	CONTROL register bit 15

3.3. The memory address register (MAR) on 3022.

This is a 24 bit register, pointing to the ND-100 memory. It is used in DMA transfers. It must be loaded from the 16-bit A-register in two operations. The most significant part is loaded first. It must also be read in two operations. The least significant part will be read first. When it is read, the upper half of the leftmost 16 bits of MAR (bits 24-31, not used) will be equal to the upper half of the rightmost 16 bits (bits 8-15).

3.4. The DATA register on 3022.

This is a 16 bit register. It acts as an intermediary between the ND-500 and the ND-100 memory in DMA transfers from ND-500 to ND-100. In DMA transfers from ND-100 to ND-500, the DATAX register is used as the intermediary register, but the DATA register is set, nonetheless.

3.5. The DATAX register on 3022.

This 16-bit register connects the bus DOUB with the bus BOU. It is also used in DMA transfers from ND-100 to ND-500. Do not confuse it with the DATA register.

3.6. The DATA-IN register on 5015.

This 32-bit register is either used as a whole, or as DATA-IN-1 (the lower 16 bits), and DATA-IN-2 (the uppermost 16 bits). When the other registers on the 5015 cards are loaded from ND-100, data goes via the DATA-IN register to the CDB bus. In DMA read (ND-100 memory read by ND-500), data will go to the DATA-IN register. The MOST bit selects the most or least significant part.

3.7. The DATA-OUT register on 5015.

This 32-bit register is either used as a whole, or as DATA-OUT-1 (the lower 16 bits), and DATA-OUT-2 (the uppermost 16 bits). When the other registers on 5015 are read from ND-100, data goes via DATA-OUT to ND-100. In DMA write (ND-500 to ND-100), data must be placed in DATA-OUT before the write. The MOST bit selects the most or least significant part.

3.8. The BREAK register on 5015.

This 16-bit register is used when the control store is loaded. Data to be loaded must be in the BREAK register. The BREAK register is connected to the least significant part of the CDB bus.

3.9. The write address register (WA) on 5015.

The 16-bit WA register is used to hold the control store address when loading and reading the control store. The WA register is connected to the least significant part of the CDB bus.

3.10. The lower and upper limit registers (LL, UL) on 3022.

These are 16-bit registers, and represent bits 8-23 of a DMA address. They are compared with bits 8-23 of the MAR register to ensure that ND-500 keeps within limits. For instance, if LL contains 1, and UL contains 3, the legal area for DMA transfers is 0400, 0401, ... , 01376, and 01377.

3.11. The control register (CSCNT) on 5015.

Bit:	Name:	Meaning:
0	CSLOAD	Control store load
1	CSREAD	Control store read
2-5	WE0,WE1,WE2,WE3	Control store group (0-8)
6	BRKEN	BREAK enable
7	STADREN	Start address enable
8	TSTPTY	Test control-store-parity-checking (ND-500 passive)
9	TSTTGU	Returns TAG-OUT instead of TAG-IN
10	CSPTY	Control store parity
11	AFIN	Prefetch addr. calc. not finished
12	PFIN	Prefetch instruction not finished
13	BALUM	Memory reference not finished
14-15		Not used

Bits 10-15 may only be read. They give micro program stop conditions.

3.12. The TAG-IN register on 5015 (I/O from ND-100).

The tag registers are additional control registers used to control the communication.
Bits 0-3 in the TAG-IN register on 5015 give 16 code values. Bit 4 is not used, and bit 5 (octal 040) is used to return TAG-IN bits (0-4). The codes are:

Bit:	Name:	Meaning:
0		Not used
1	DICLK1	Clock DATA-IN-1 register
2	DICLK2	Clock DATA-IN-2 register
3	DUCLK	Clock DATA-OUT register (both)
4	WACLK	Clock write-addr register
5	BRKCLK	Clock BREAK register
6	TGUCLK	Clock TAG-OUT register
7	CNTCLK	Clock CSCNT register
8	DIEN	Enable DATA-IN register to bus (CDB)
9	DUEN	Enable DATA-OUT register (least sign.)
10	WAR	Read write-addr register
11	BRKR	Read BREAK register
12	CNTR	Read CSCNT register
13	RESBRK	Reset break
14	DUNL	Unlock
15	EDUTEN	Enable data line driver (from ND-500)

3.13. The TAG-OUT register on 5015 (data from ND-500).

Bits 0-2 in the TAG-OUT register on 5015 give 8 code values.
Bit 3 means ND-100 if it is 0, and not ND-100 if it is 1.
Bits 4-6 are not used.
Bit 7 is the MOST bit. It enables the most significant part of the DATA-OUT register, and determines which part of the register to use when micro programmed. MOST also controls least/most significant part of the DATA-IN register. The codes are (for MOST=1, add 0200):

Bit: Meaning:

0 Read memory address register
1 Write memory address register
2 Read STATUS register
3 Write STATUS register
4 Read CONTROL register
5 Reset activate
6 Read DATA register (and ND-100 memory)
7 Write DATA register (and then into ND-100 memory)

3.14. IOX instructions.

The ND-500 communication can be locked or unlocked, in test mode or not in test mode. These states are set by IOX LCON (load CONTROL register). IOX instructions have different meanings, depending on the state. In the following list, the three columns display the MAC mnemonics of physical device numbers, the octal device numbers themselves, and their meaning.

Locked and not in test mode:

RSTA 062 Read STATUS register
MCLR 066 ND-500 Master Clear
TERM 067 Terminate
RTAG 070 Read TAG-IN
WTAG 071 Write TAG-OUT
WDAT 073 Write DATAX (NB not the DATA register)
SLOC 074 Set locked
CLKD 075 Clock DATA
UNLC 076 Release locked (unlock)
RETG 077 Return tag

Locked and in test mode:

RSTA 062 Read STATUS register
RCON 064 Read CONTROL register

A short list of registers, IOX instructions etc.

Unlocked and not in test mode:

RMAR 060 Read memory address register
LMAR 061 Load memory address register
RSTA 062 Read STATUS register
LCON 065 Load CONTROL register
MCLR 066 ND-500 Master Clear
TERM 067 Terminate
RTAG 070 Read TAG-IN
WTAG 071 Write TAG-OUT
WDAT 073 Write DATAX (NB not the DATA register)
SLOC 074 Set locked
UNLC 076 Release locked (unlock)
RETG 077 Return tag

Unlocked and in test mode:

RMAR 060 Read memory address register (do it twice)
LMAR 061 Load memory address register (do it twice)
RSTA 062 Read STATUS register
LSTA 063 Load STATUS register
RCON 064 Read CONTROL register
LCON 065 Load CONTROL register
MCLR 066 Read DATA register
TERM 067 Load DATA register
RTAG 070 Read upper limit register
WTAG 071 Load upper limit register
RLOW 072 Read lower limit register
WDAT 073 Load lower limit register

ND-100 bits 0-15 go to limit register bits 8-23.

3.15. Some widely used communication subroutines.

The routines that follow below are written in MAC (assembly) code.

3.15.1. Master clear, set stop bit, reset tag bits.

```
IOX   UNLC     % unlock
SAA   040
IOX   LCON
SAA   2
IOX   RETG     % set stop bit
IOX   MCLR
SAA   0
IOX   WTAG     % write TAG-OUT on 3022
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate
EXIT
```

3.15.2. Write tag from the A register.

```
IOX   WTAG     % write TAG-out on 3022
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate
EXIT
```

3.15.3. Write data to 5015 from the A register.

The following routine uses the most/least significant part of the DATA-IN register, depending on the value of n (DATA-IN-1 is the least significant part):

```
IOX   WDAT     % A register to DATAX
SAA   n        % n=1: clock DATA-IN-1.  n=2: clock DATA-IN-2
IOX   WTAG
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate
SAA   010      % enable DATA-IN to the CDB bus on 5015
IOX   WTAG
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate
EXIT
```

3.15.4. Read data from 5015 to the A register.

The following routine has 3 entry points. The first does not enable the DATA-OUT register (DUEN). The third does not clock the CDB bus to the DATA-OUT register.

```
ENTR1=*

SAA   3
IOX   WTAG     % clock CDB to DATA-OUT
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate
JMP   COMON

ENTR2=*

SAA   3
IOX   WTAG     % clock CDB to DATA-OUT
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate

ENTR3=*

SAA   011
IOX   WTAG     % enable DATA-OUT
SAA   044
IOX   LCON     % activate
IOX   UNLC
SAA   040
IOX   LCON     % reset activate

COMON=*

SAA   017
IOX   WTAG     % enable data line driver (DUT to DBU)
SAA   044
IOX   LCON     % activate
IOX   CLKD     % clock DATA on 3022
IOX   UNLC
SAA   050
IOX   LCON     % set test mode
SAA   0
IOX   MCLR     % read DATA (test mode)
STA   SAVE
SAA   040
IOX   LCON
SAA   0
IOX   WTAG     % reset tag bits
SAA   044
IOX   LCON
IOX   UNLC
SAA   040
```

```
IOX   LCCN     % reset activate
LDA   SAVE
EXIT
```

3.16. Subroutines to write and read the control store.

The control store address is supposed to be in the WA register. The part number is a number in the range 0-010. A control store word consists of 9 16-bit words, and the part number points to one of these 9 words. Part number 010 (8) points to the most significant part. Data to be written must be in the BREAK register. Data that is read will appear in DATA-OUT-1. The WA register is set by the sequence

```
LDA  ADDR; JPL  WRDAT; SAA  4; JPL WRTAG
```

3.16.1. Write a 16-bit word into the control store.

The A register contains the 16 bit data word. The T register contains a control word that is 1, 5, 011, 015, ... , 041 depending on the part number (0-010).

```
STA   SAVE
COPY  SL DA
STA   LINK
LDA   SAVE
JPL   WRDAT    % data to the CDB bus on 5015
SAA   5
JPL   WRTAG    % clock the BREAK register
COPY  ST DA
JPL   WRDAT    % control word to the CDB bus
SAA   7
JPL   WRTAG    % clock the CSCNT register
LDA   SAVE
JMP   I LINK
```

3.16.2. Read a 16-bit word from the control store.

The A register contains a control word that is 2, 6, 012, 016, ..., 042 depending on the part number (0-010).

```
STA   SAVE
COPY  SL DA
STA   LINK
LDA   SAVE
JPL   WRDAT    % control word to the CDB bus
SAA   7
JPL   WRTAG    % clock the CSCNT register
JPL   ENTR3    % read data, already in DATA-OUT
JMP   I LINK
```

3.17. Other registers used by the test programs.

3.17.1. The prefetch status register (PSTAT, 32-bit, read only).

Bits:	Name:	Meaning:
0-10	EP	Operation code.
		Bit 10 is 0: short operation code. Bits 8-9 are then both zero. Bits 0-7 contain 252 different operation codes, complemented, and not 256. The codes 1111111xx, where x is 1 or 0, do not exist for short codes. When the six most significant bits are one, it means long operation code.
		Bit 10 is 1: long operation code. Bits 0-9 contain 1024 different operation codes, complemented. A long operation code consists of 16 bits. The six most significant bits are 1, and, since EP is 11 bits long, 5 of them are discarded.
11-14	PCD	Program counter displacement.
		Gives the length (complemented) of the current instruction. 017 means 1 byte, 016 2 bytes, and so on.
15-16	VLB	Valid bytes. 3 means 4 bytes left in the instruction buffer, 2 means 3 bytes left, and so on.
17-19	OPTYP	Operand type.
		From 0 to 5: word, float, halfword, byte, bit, and double float.
20	REGOP	Register operand.
		1 if the address code (first byte of operand specifier) was 0320-0323, otherwise 0.
21	CONOP	Constant operand.
		1 for constant operands as, for instance, in argument instructions, otherwise 0.
22	DESC	Descriptor addressing.
		0 if legal, otherwise 1.
23	WR	Write operation.
		1 if write operation, otherwise 0.
24		Not used.

25 PFIRST First operand.

1 for the first operand, otherwise 0. Becomes 0 as soon as the first operand has been fetched. For a sequence of LDR instructions, for instance, it will be 1 all the time.

26-27 DX Descriptor register.

Used in descriptor adressing to give the number of the register to use. 3 means R1, 2 means R2, 1 means R3, and 0 means R4.

28-29 SXSEL Source register select.

Gives the number of the source register, when there is one. 3 means R1, and so on.

30-31 DXSEL Destination register select.

Gives the number of the destination register, when there is one. 3 means R1, and so on.

3.17.2. The (trap) status register S1.

This is a 32 bit register. Only bits 9-31 can give a trap. If one of bits 9-29 is to give a trap, the corresponding bit must be set in the trap enable (TE) register.

Bit:	Meaning:
0	Not used
1	Privileged instruction allowed
2	Part done
3	Instruction reference
4	Process switch disable
5	Zero
6	Carry
7	Sign
8	Flag
9	Overflow
10	Not used
11	Invalid operation
12	Divide by zero
13	Floating underflow
14	Floating overflow
15	BCD overflow
16	Illegal operand value
17	Single instruction trap
18	Branch trap
19	Call trap
20	Breakpoint instruction trap
21	Address trap fetch
22	Address trap read
23	Address trap write
24	Address zero access
25	Descriptor range
26	Illegal index
27	Stack overflow
28	Stack underflow
29	Programmed trap
30	Disable process switch timeout
31	Disable process switch error

If bits are going to be set in S1 by software, two mnemonics can be used. D,XST1 must be used to set the bits 17-19, 21-24, or 30-31. D,S1 must be used to set the other bits.

3.17.3. The (trap) status register S2.

This is a 12 bit register.

Bit:	Meaning:
0	Index scaling error
1	Illegal instruction code
2	Illegal operand specifier
3	Instruction sequence error
4	Not used
5	Activate from ND-100
6	Terminate from ND-100
7	Not used
8	Instruction failure (PV, MOR, CPE, MME, MSE, PGE)
9	Data failure
10	Power fail
11	Processor fault

3.17.4. The memory and cache registers.

The cache length is always 4K. The width may be 32, 64, or 128 bits. This corresponds to (byte) address ranges of 0-037777 0-077777, and 0-177777. If one cache module is present, the width is 32 bits. If 2, the width is 64 bits, and if 4 modules are present, the width is 128 bits.

The whole cache may be used (partitions 0-3). Two partitions may be used, 0-1, 1-2, or 2-3. Only one partition may be used, 0, 1, 2, or 3. The use of the cache is controlled by the data and instruction memory control registers. There are also status registers to display the status of the instruction and data cache.

3.17.4.1. Data memory status registers (DSTS0, DSTS1, DSTS2).

DSTS0

Bits:	Meaning:
0-1	Partition number
2-3	Number of partitions (0-3 means 1-4)
4	TSB-fault
5	Memory parity error
6	Cache parity error + illegal use of cache
7	Blocked. If this bit is 1, then bits 8-15 in DSTS0 and bits 12-15 in DSTS1 will be blocked (they will not change).
8	Cache parity error, cache module 0.
9	" " " " " 1.
10	" " " " " 2.
11	" " " " " 3.
12	Memory " " " " 0.
13	" " " " " 1.
14	" " " " " 2.
15	" " " " " 3.

DSTS1

Bits:	Meaning:
0	Memory parity error, byte 0 (bits 7- 0).
1	" " " " 1 (" 15- 8).
2	" " " " 2 (" 23-16).
3	" " " " 3 (" 31-24).
4	Cache " " " 0 (" 7- 0).
5	" " " " 1 (" 15- 8).
6	" " " " 2 (" 23-16).
7	" " " " 3 (" 31-24).
8-9	Cache module number (0-3).
10	Memory timeout.
11	Illegal partition setting.
12	Cache control parity error, byte 0.
13	" " " " " 1.
14	" " " " " 2.
15	Cache clear is active.

DSTS2

Bits:	Meaning:
0-7	Memory channel 0-7. If bit 10 in DSTS1 is 1, then some of the bits 0-7 will also be 1.

3.17.4.2. Data memory control registers (DCON0, DCON1).

DCON0

Bits:	Meaning:
0-1	Select (the first) partition number
2-3	Number of partitions (0-3 means 1-4)
4	Cache disable (must be zero)

DCON1

Bits:	Meaning:
0-1	Select cache module no. for bits 0-7 DSTS1.
2	HIC (hit in cache).
3	Clear block.
4	TSB trap enable.
5	Memory parity error trap enable.
6	Cache parity error trap enable.
7	Memory out of range trap enable.

3.17.4.3. Instruction memory status registers (ISTS0, ISTS1, ISTS2).

These registers have the same format as the data memory status registers.

3.17.4.4. Instruction memory control registers (ICON0, ICON1).

These registers have the same format as the data memory control registers.

3.17.5. Memory modus register (MMOD).

Bit:	Meaning:
0	Alternative address area (default).
1	Alternative address area selected by ALTMOD.
2	Lock until write (not used yet)
3	Data do not use cache
4	Instruction do not use cache
5	Instruction memory reference from micro code

3.17.6. Limit registers (HL,LL).

These higher and lower limit registers contain 32 bit logical addresses. They are constantly compared to logical program and data addresses, and may give trap condition if the proper address traps are enabled.

To get an address trap, the proper bit in TE must be set to 1. In addition, if the address of a memory reference (fetch, read or write) is called ADDR, trap depends on the value of D,SETLIM:

D,SETLIM is 0: LL<=ADDR.AND.ADDR<HL is true gives trap
D,SETLIM is 1: LL<=ADDR.OR.ADDR<HL is true gives trap

3.17.7. Memory management substitute registers.

ND-500 may be without memory management. Then there will be some additional registers:

DZPA and IZPA: Data and instruction memory zero point adjust registers. They are 14-bit registers and contain page numbers. A page has 2K bytes. These registers point to the physical page in the memory where the first page of the program itself is loaded.

DUPL and IUPL: Data and instruction memory upper page limit register. They are similar to DZPA and IZPA, and point to the program's last physical page in the memory.

DCINHLL, DCINHLU, ICINHLL, and ICINHLU: Data and instruction memory cache inhibit limit registers, lower and upper. They are similar to DZPA and IZPA, and inhibit write into the cache memory when the actual program's physical page number is in the range lower to upper (LL <= pageno <= LU).

DRADDRL, DRADDRM, IRADDRL, IRADDRM. Data and instruction memory least and most significant real (physical) address registers. DRADDRL and IRADDRL contain 16 bits, and DRADDRM and IRADDRM contain 8 bits. A real address is a 24-bit byte address (a real address has actually 25 bits, but the most significant bit is removed). The page number in DZPA/IZPA multiplied by 04000 is added to a program's logical data and instruction addresses, and the result goes to the real address registers. If errors occur, the real address registers are locked (that is, new real addresses will not be loaded into them before the clear-block bit in DCON1/ICON1 is set).

3.17.8. Memory management registers.

There are two sets of these registers, one for the data memory and one for the instruction memory.

A real address is a logical address translated by the memory management system. The translated address is then shifted one position to the right, thereby discarding bit 0. The real address is therefore a halfword address.

3.17.8.1. Scratch files (ISCRF,DSCRF).

These are two sets of 16 16-bit registers. Such a register is addressed by loading ISCFA or DSCFA with a number in the range 0-15. After each access, ISCFA or DSCFA is incremented by 1, modulo 16.

3.17.8.2. Status registers (IMSTS,DMSTS).

Bit:	Name:	Meaning:
0	PALT	0: ALT mode. Locked by TSB-fault.
1	SMM0	0: SEGEQ (same segm). Locked by TSB-fault. The segment register and bits 31-27 of the logical address are equal.
2	SMM1	0: SEGZ (zero segm). Locked by TSB fault. Bits 31-27 of the logical address are zero.
3	PUS	1: Real-addressed page is used.
4	WIP	1: Real-addressed page is written into.
5	USED	0: Used. Dynamic USED-status of the hashed part of TSB. Only valid if bit 13=0.
6	TSBF	1: TSB-fault (PCN=0: 0. PCN=1: 1 if bit 5=1 or not match).
7	NEWS	0: New segment (1 when DMSTS). Bits 31-27 of the logical address are not all zero, and they are not equal to bits 4-0 of the segment register.
8	MMTR	1: MM-trap (locked. Inclusive or of bits 6, compl(7), 9, 10,23).
9	ALTPV	1: ALT protect violation.
10	WRPV	1: Write protect violation.
11	PCN	1: Paging on.
12	TSBC	1: TSB clear is active (not completed).
13	FAS2A	1: Match not found in sequential TSB, if TSB fault. Sequential TSB is accessed only if TSBF = 1 and if FAS2 = 1 (in IPROCC/DPROCC) and if USED = 0 (in actual hashed TSB entry)
14	SPARE	Not defined.
15	SPARE	Not defined.
16	SP0	1: Parity error 0 (PROC0-2, DCM0-4).
17	SP1	1: Parity error 1 (DCM5-7, SEG0-4, AD19-26).
18	SP2	1: Parity error 2 (AD11-18).
19	SP3	1: Parity error 3 (BSG0-15). Page number + two dummy bits.

20	SP4	1: Parity error 4 (the three permit bits). See ICSEG/DCSEG, bits 5-7.
21	SPARE	0
22	SPARE	0
23	BUFFP	1: OR-ed parity error (0 if PON=0 or not used).
24	TEQ0	0: Match on PROC and DOM bit 0-4.
25	TEQ1	0: Match on SEGM (or bits 27-31) and DOM bit 5-7.
26	TEQ2	0: Match on log. addr. bits 11-18.
27	TEQ3	0: Match on log. addr. bits 19-26.
28	USED	0: used. Static USED-status of the hashed part of TSB.
29	SPARE	Not defined.
30	SPARE	Not defined.
31	SPARE	Not defined.

Locked bits are unlocked when the memory management is turned off, or when the TSB is written into.

3.17.8.3. Logical address (ILADDR,DLADDR).

These two 32-bit registers hold the instruction and data logical addresses.

3.17.8.4. WIP/PGU broadside (IWIPGU,DWIPGU).

A broadside is a 16-bit extract from a 16K bit buffer. There are two such buffers, one for WIP (written in page) and one for PGU (page used). The 16 bits represent one group of 16 pages. Each group is addressed by means of the 10 most significant bits of the real address. Bit 0 represents the page with the lowest page number of the 16, bit 15 represent the page with the highest page number. To read WIP or PGU, bit 9 in IMCNTR or DMCNTR has to be set. Then bit 7 in IPROCC or DPROCC selects either WIP or PGU. If 1, WIP is selected, and if 0, PGU. Default for this bit is 0.

3.17.8.5. Real address (IRADDR,DRADDR).

These two 24-bit registers hold the instruction and data real addresses. A real address is a logical address translated by the memory management system, and then divided by 2. The result is a halfword address.

3.17.8.6. Control registers (IMCNTR,DMCNTR).

Bit:	Meaning:
4	Clear ITSB or DTSB.
9	Start to read IWIPGU or DWIPGU.

3.17.8.7. Scratch file address (ISCFA,DSCFA).

Two 4-bit registers, each pointing to one of the 32 scratch file registers (16 in each set).

3.17.8.8. Process control registers (IPROCC,DPROCC).

Bit:	Name:	Meaning:
0	PROC0	Bit 0 of process number.
1	PROC1	Bit 1 of process number.
2	PROC2	Bit 2 of process number.
3	PGN	Paging on.
4	TSBD	Disable TSB. 1: writing into TSB, 0: reading.
5	HX8	Bit 8 of TSB address (TSB has two ident. parts).
6	FAS2	Enable use of sequential TSB (STSB).
7	SWIP	Select WIP-part of IWIPGU/DWIPGU (default 0).

3.17.8.9. Domain registers (IDOMR,DDOMR).

Two 8-bit registers, containing the main domain number (0-255). In the ND-500 Reference Manual, DOMR is called CED (Current Executing Domain).

3.17.8.10. Alternative domain registers (IADOM,DADOM).

Two 8-bit registers, containing the alternative domain number (0-255). In the ND-500 Reference Manual, ADOM is called CAD (Current Alternative Domain).

3.17.8.11. Current segment registers (ICSEG,DCSEG).

Two 8-bit registers, containing the current segment number in bits 0-4, and the protect status in bits 5-7.

Bit:	Meaning:
5	0: Shared segment status. 1: Not shared
6	0: Parameter access permitted. 1: Not permitted
7	0: Write permitted. 1: Not permitted

In the ND-500 Reference Manual, CSEG is called CES (Current Executing Segment).

3.17.8.12. Alternative segment registers (IASEG,DASEG).

Similar to current segment registers, but containing alternative segment number and status. In the ND-500 Reference Manual, ASEG is called CAS (Current Alternative Segment).

3.17.8.13. Translate speed-up buffer page (ITSB,DTSB).

Two buffers, each contains 1024 14-bit page addresses (the page part of a real address). One is for data and one for instruction memory. Each buffer has two parts. Bit 5 (HX8) of IPROCC/DPROCC selects which part to use. Each part is divided into two sections. The lower section is addressed by a hashing algorithm, and the upper is addressed sequentially.

The hashing algorithm computes an 8-bit index by EXCLUSIVE OR-ing four numbers A, B, C, D. In the following, if AD31-27 are all zero, SEG4-0 come from the segment register, bits 4-0. If AD31-27 are not all zero, SEG4-0 come from AD31-27 (the five most significant bits of the logical address).

A:	AD22	AD11	AD16	AD15	AD14	AD13	AD12	AD11
B:	AD20	AD21	SEG4	SEG3	SEG2	SEG1	SEG0	AD17
C:	AD23	AD14	AD20	AD19	AD18	PROC2	PROC1	PROC0
D:	AD15	AD16	DOM0	DOM1	DOM2	DOM3	DOM4	DOM5

3.17.8.14. Sequential TSB address register (ISTSB,DSTSB).

Two 8-bit registers. Top of sequential buffer. 0 means that the sequential buffer is empty, 0377 means that it is full (255 entries). ISTSB/DSTSB must be set and updated by software (micro program). Bit 5 (HX8) in IPROCC or DPROCC specifies which buffer part to use.

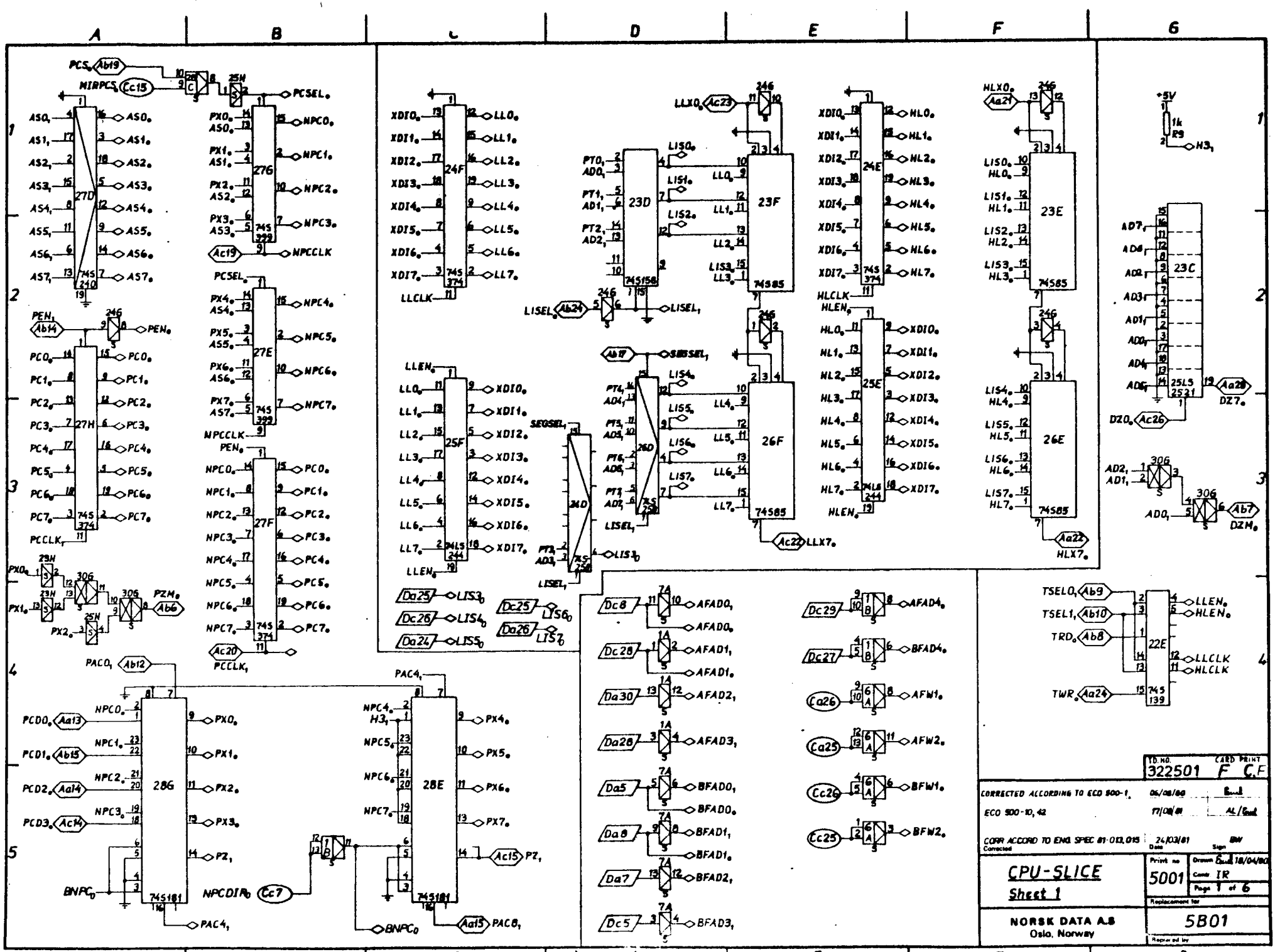
3.17.8.15. Index for hashed or sequential TSB (IHXA,DHXA).

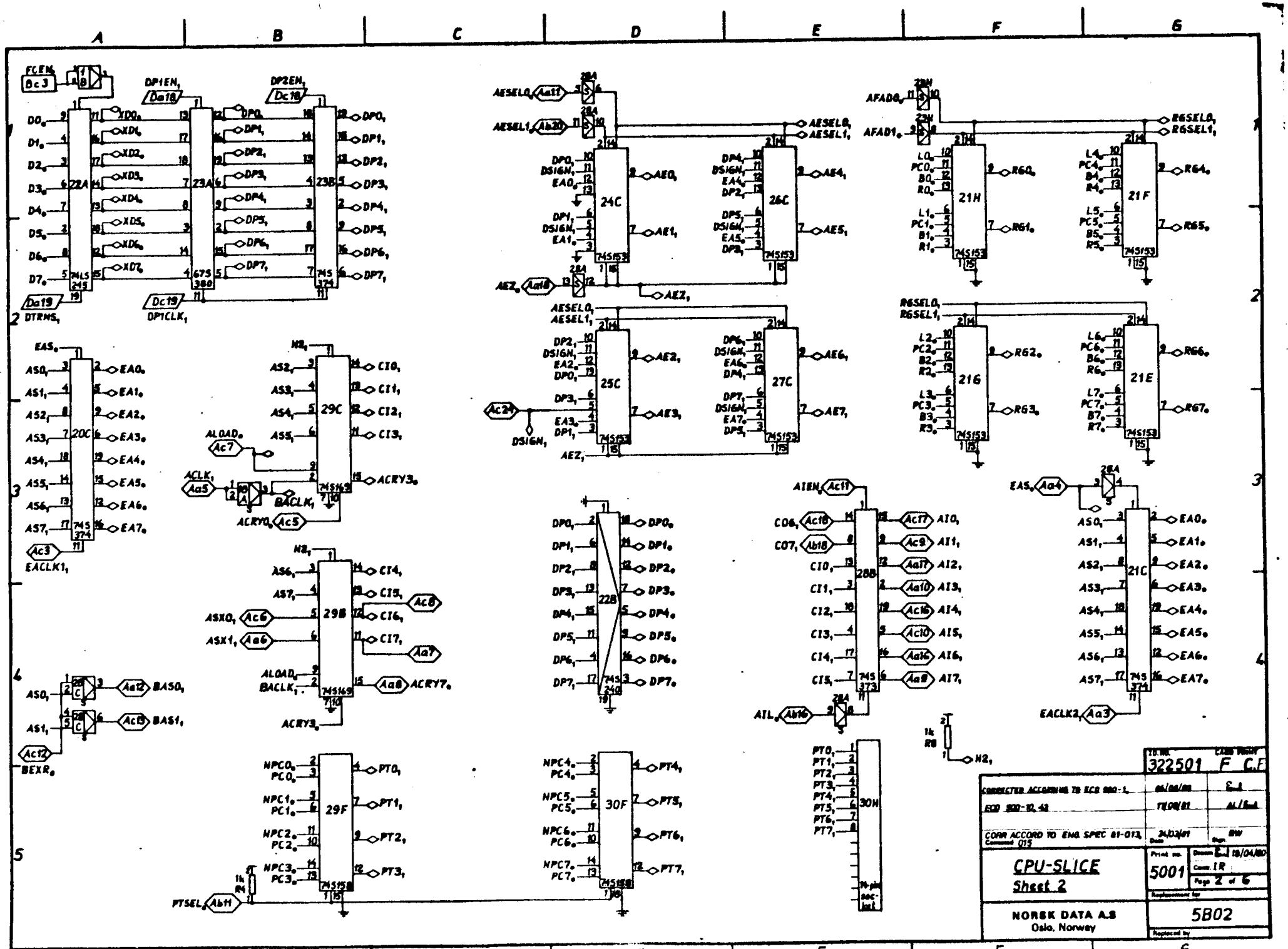
The 8-bit index may be read and checked. There is one index for instruction memory, and one for data. Either the computed index for the hashed part of TSB is read, or ISTSB/DSTSB. This depends upon the value of bit 13 (FAS2A) of the status register (IMSTS/DMSTS). If this bit is 1, ISTSB/DSTSB is read. If it is 0, the computed index for the hashed part is read.

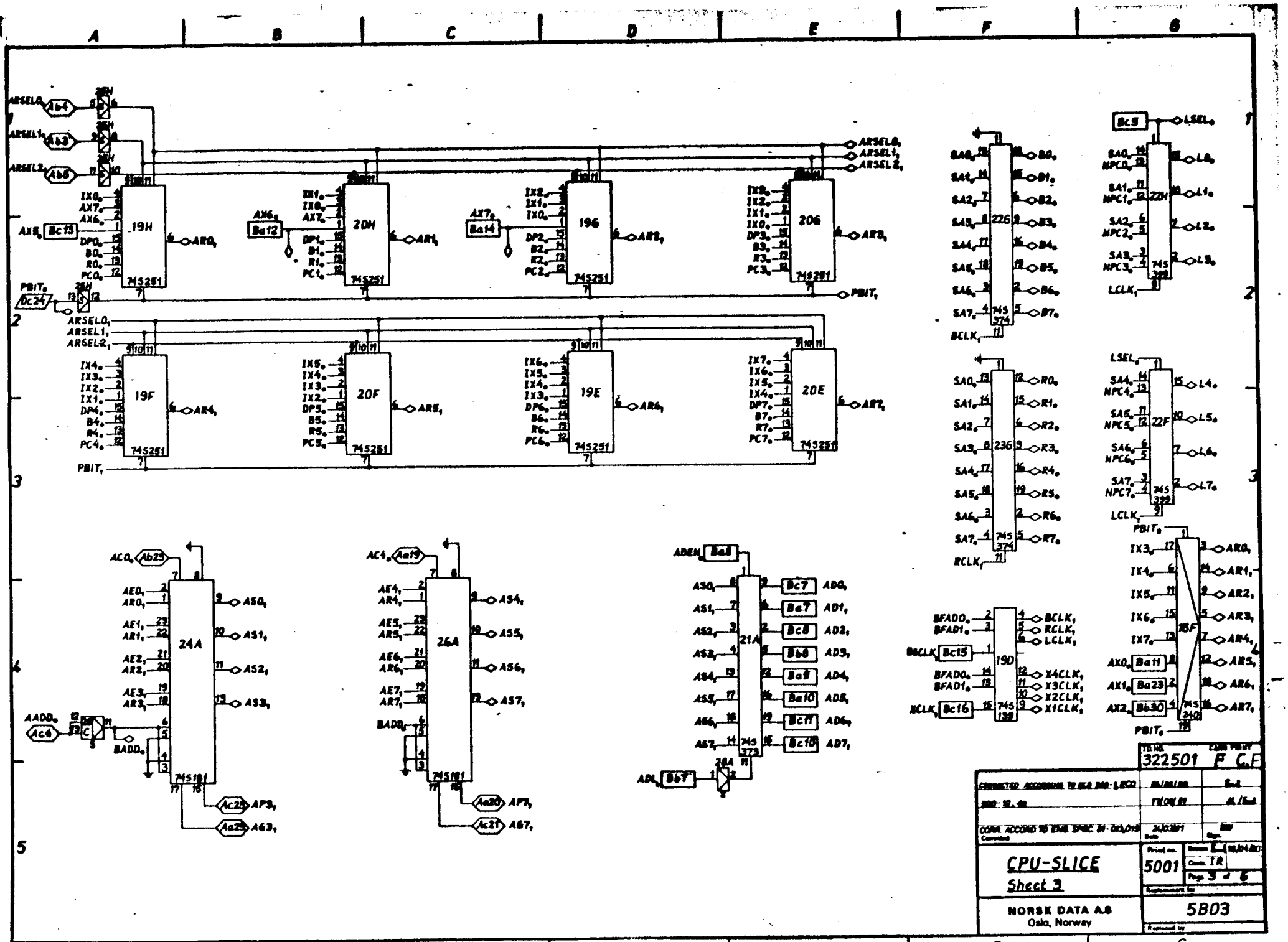
ND-500

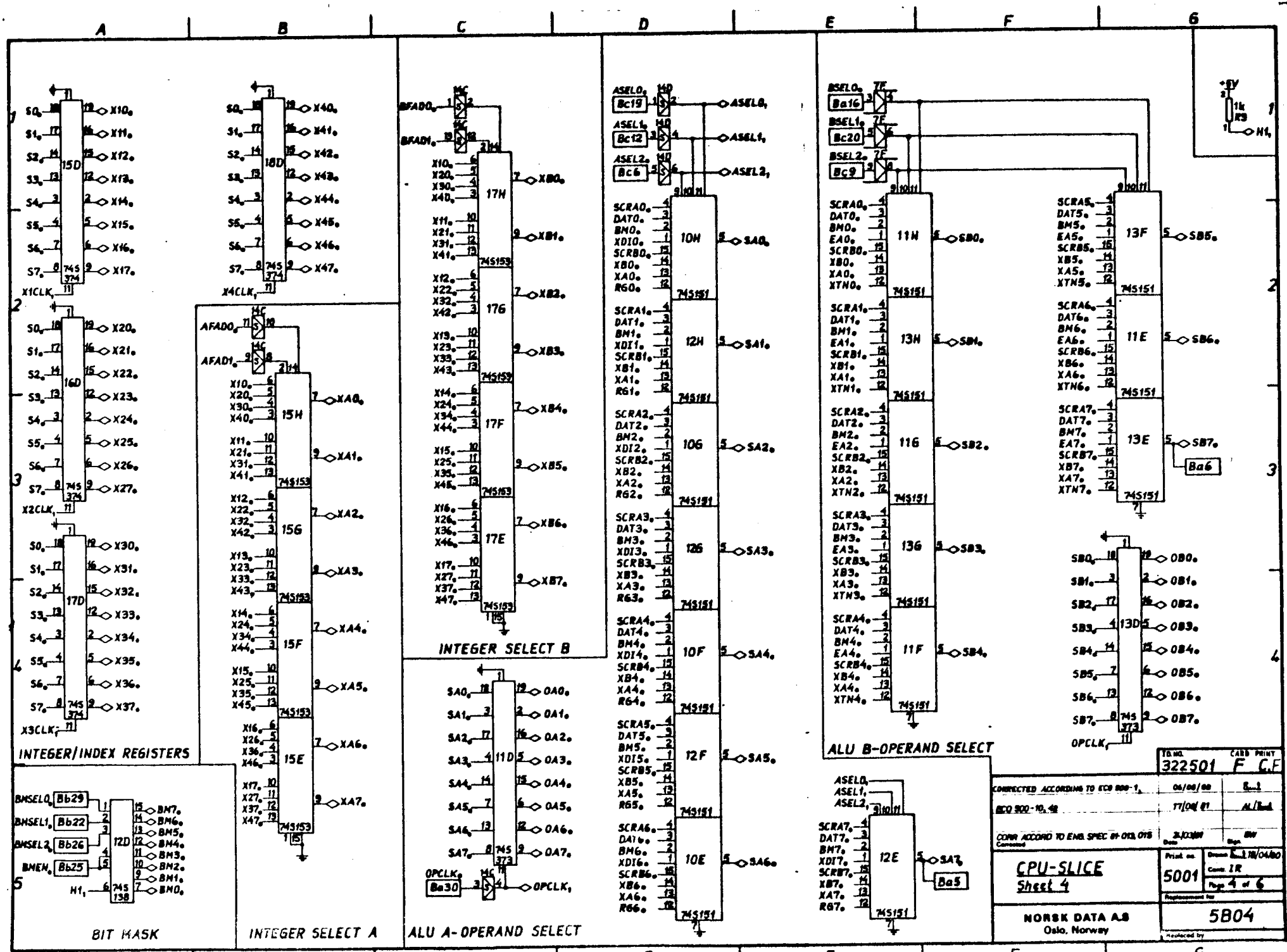
LOGIC DIAGRAMS

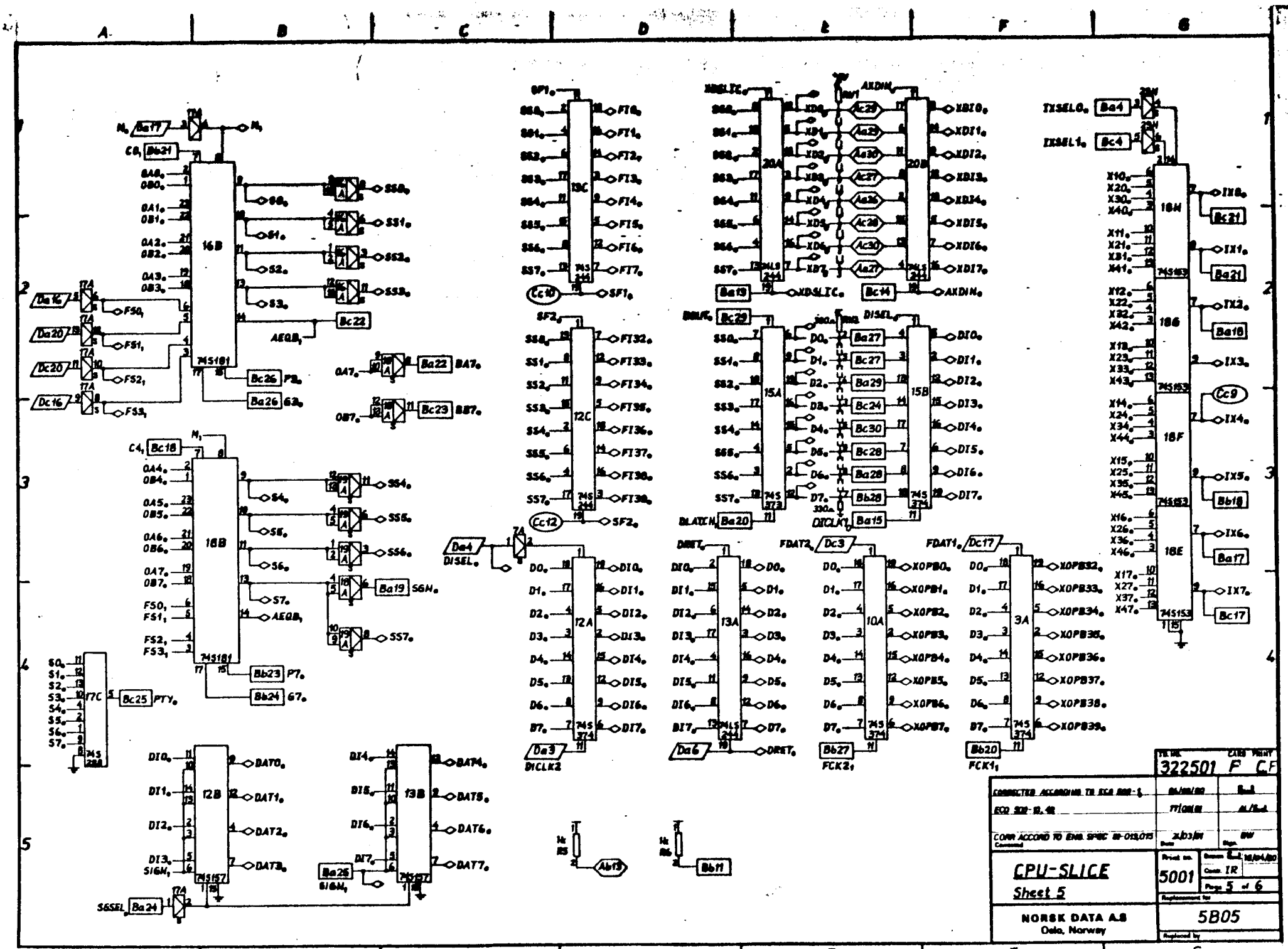
TABLE OF CONTENTS

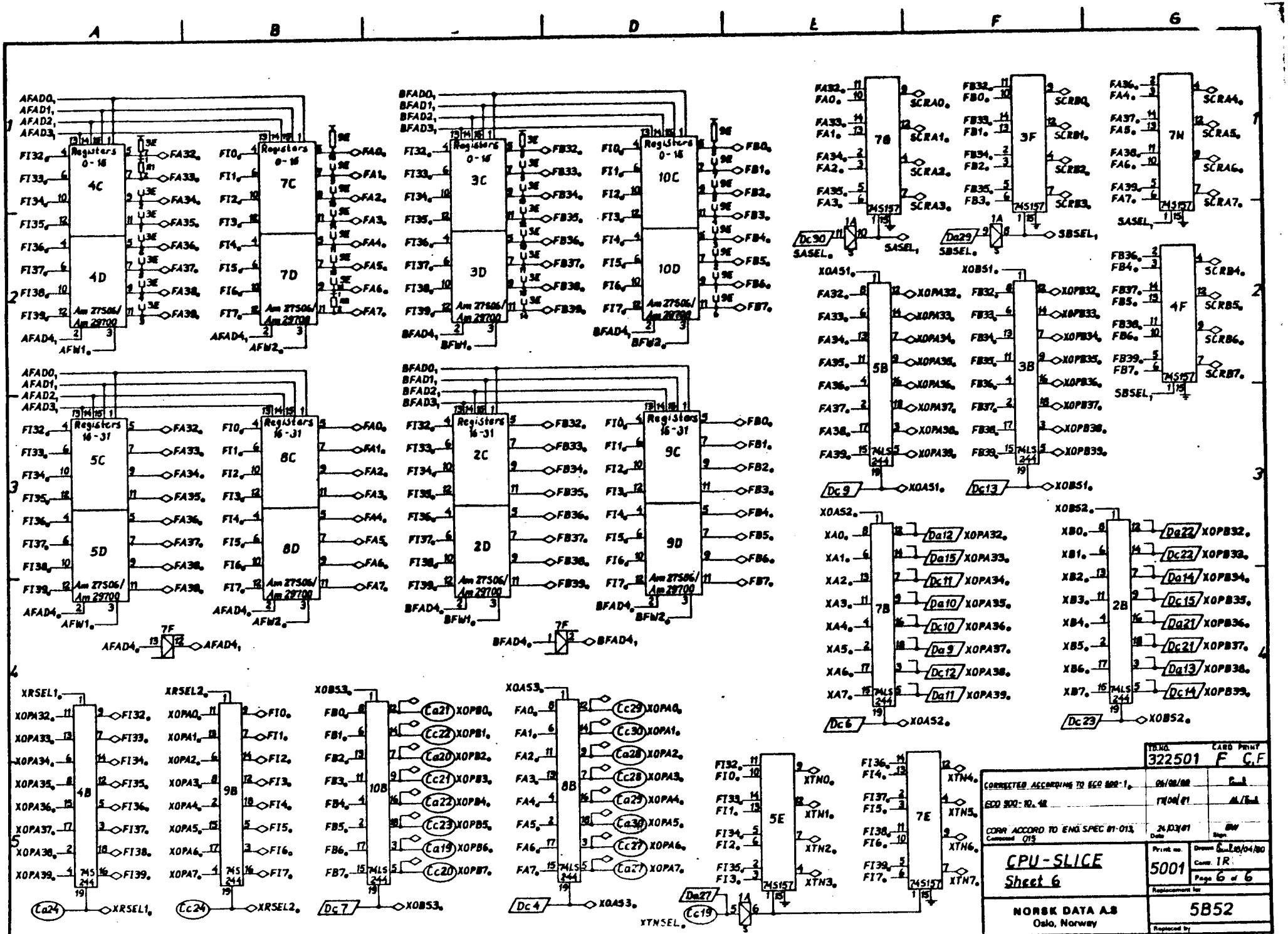

A
B
C
D
E
F
G
1
2
3
4
5
PCS
Ab19
MIRPCS
Cc15
25H
PCSEL
ASO
AS1
AS2
AS3
AS4
AS5
AS6
AS7
27D
745 240
PXO
PX1
PX2
PX3
276
745 399
NPCO
NPC1
NPC2
NPC3
Ac19
NPCCLK
PX4
PX5
PX6
PX7
27E
NPC4
NPC5
NPC6
NPC7
PEN
Ab14
246
PCO
PC1
PC2
PC3
PC4
PC5
PC6
PC7
27H
745 374
PCCLK
27F
Ac20
306
PZM
Ab6
PACO
Ab12
PAC4
NPCDIR
Cc7
BNPC
286
28E
745181
Aa13
Ab15
Aa14
Ac14
Aa15
PAC8
PZ
Ac15
XDIO
XDI1
XDI2
XDI3
XDI4
XDI5
XDI6
XDI7
24F
745 374
LLCLK
LLO
LL1
LL2
LL3
LL4
LL5
LL6
LL7
LLEN
25F
745 244
Da25
Da26
Da24
LIS3
LIS4
LIS5
LIS6
LIS7
SEGSEL
Ab17
24D
LISEL
PT0
PT1
PT2
PT3
PT4
PT5
PT6
PT7
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
23D
745158
LIS0
LIS1
LIS2
LLX0
Ac23
23F
74S85
Aa24
26D
LIS4
LIS5
LIS6
LIS7
26F
Ac22
LLX7
24E
HL0
HL1
HL2
HL3
HL4
HL5
HL6
HL7
HLCLK
HLEN
25E
745 244
HLX0
Aa21
23E
HLX7
Aa22
26E
+5V
1k
R9
H3
23C
25LS 2531
DZ0
Ac26
Aa28
DZ7
306
AD2
AD1
AD0
Ab7
DZM
TSEL0
Ab9
TSEL1
Ab10
TRD
Ab8
TWR
Aa24
22E
745 139
LLEN
HLEN
LLCLK
HLCLK
Dc8
Dc28
Da30
Da28
Da5
Da8
Da7
Dc5
AFADO
AFAD1
AFAD2
AFAD3
BFADO
BFAD1
BFAD2
BFAD3
Dc29
Dc27
Ca26
Ca25
Cc26
Cc25
AFAD4
BFAD4
AFW1
AFW2
BFW1
BFW2
TD.NO.
322501
CARD PRINT
F C.F
CORRECTED ACCORDING TO ECO 900-1, ECO 900-10, 42
05/08/80
17/08/81
AL/Emil
CORR ACCORD TO ENG SPEC 81-013,015
24/03/81
BW
CPU-SLICE
Sheet 1
Print no
5001
Drawn Emil 18/04/80
Conn TR
Page 1 of 6
Replacement for
NORSK DATA A.S
Oslo, Norway
5B01


A
B
C
D
E
F
G
1
2
3
4
5
FCEN
Bc3
DP1EN,
Da18
DP2EN,
Dc18
DO0
D1
D2
D3
D4
D5
D6
D7
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
DP0
DP1
DP2
DP3
DP4
DP5
DP6
DP7
22A
23A
23B
74LS 245
675 389
74S 374
Da19
DTRMS,
Dc19
DP1CLK,
AESEL0,
Aa11
AESEL1,
Ab20
AESEL0,
AESEL1,
24C
26C
AE0,
AE1,
AE4,
AE5,
AEZ,
Aa18
AEZ,
25C
27C
AE2,
AE3,
AE6,
AE7,
Ac24
DSIGN,
AFAD0,
AFAD1,
RGSEL0,
RGSEL1,
21H
21F
21G
21E
R60,
R61,
R64,
R65,
R62,
R63,
R66,
R67,
EA5,
Aa4
20C
EA0,
EA1,
EA2,
EA3,
EA4,
EA5,
EA6,
EA7,
Ac3
EACLK1,
M2,
29C
CI0,
CI1,
CI2,
CI3,
ACRY3,
ALOAD,
Ac7
ACLK,
Aa5
BACLK,
ACRY0,
Ac5
29B
CI4,
CI5,
CI6,
CI7,
ACRY7,
Ac6
Aa6
Aa7
Aa8
ASX0,
ASX1,
ALOAD,
BACLK,
ACRY3,
22B
DP0,
DP1,
DP2,
DP3,
DP4,
DP5,
DP6,
DP7,
AIEN,
Ac11
CO6,
Ac18
CO7,
Ab18
CI0,
CI1,
CI2,
CI3,
CI4,
CI5,
28B
AI0,
AI1,
AI2,
AI3,
AI4,
AI5,
AI6,
AI7,
Ac17
Ac9
Aa17
Aa10
Ac16
Ac10
Aa16
Aa9
AIL,
Ab16
21C
EACLK2,
Aa3
AS0,
AS1,
Ac12
BEXR,
Aa12
BAS0,
Ac13
BAS1,
PTSEL,
Ab11
1k
R4
29F
30F
30H
NPC0,
PC0,
NPC1,
PC1,
NPC2,
PC2,
NPC3,
PC3,
NPC4,
PC4,
NPC5,
PC5,
NPC6,
PC6,
NPC7,
PC7,
PT0,
PT1,
PT2,
PT3,
PT4,
PT5,
PT6,
PT7,
1k
R8
N2,
322501
F
C.F
CPU-SLICE
Sheet 2
5001
Page 2 of 6
NORSK DATA A.S
Oslo, Norway
5B02

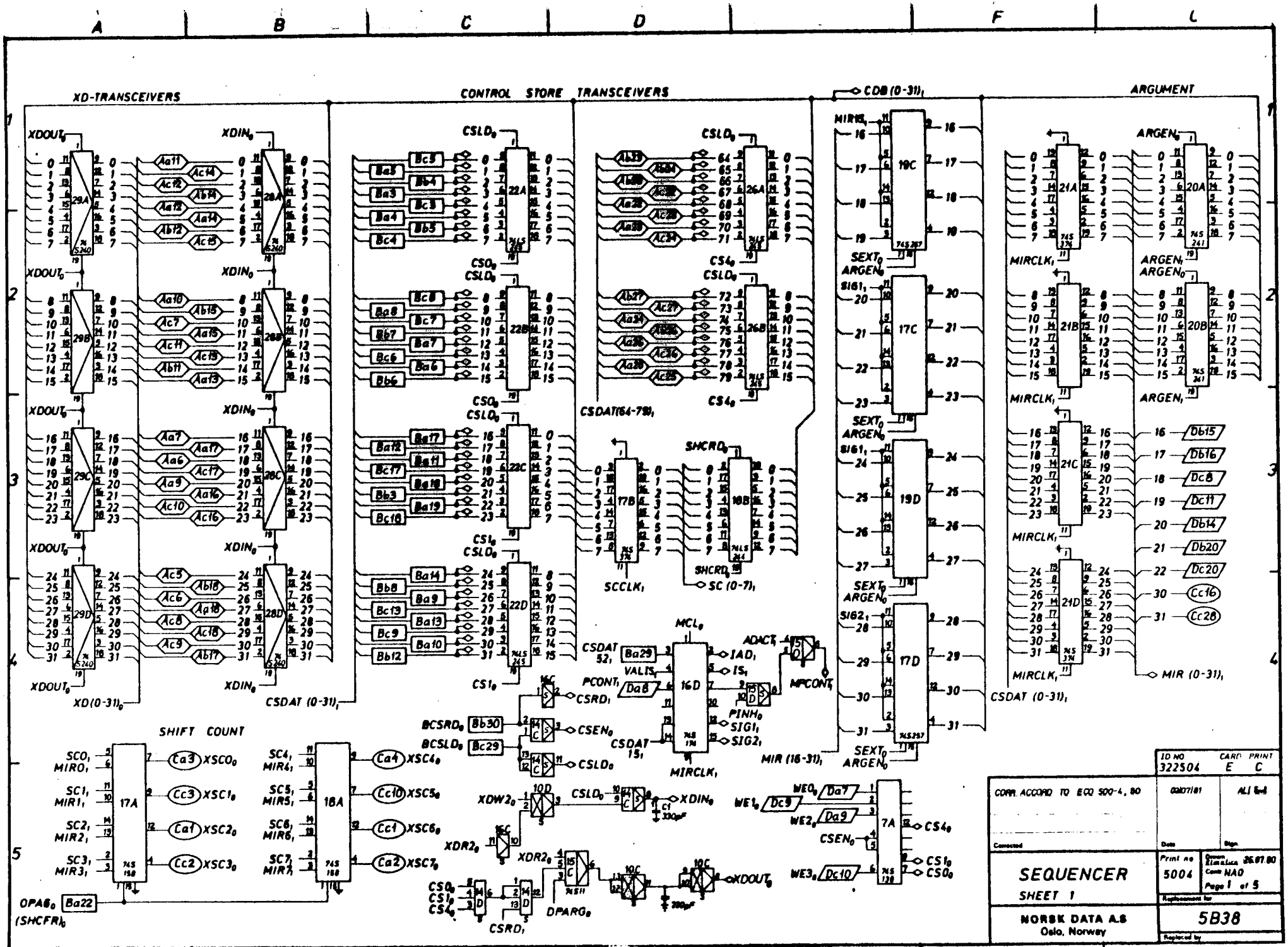

A
B
C
D
E
F
G
1
2
3
4
5
ARSEL0
ARSEL1
ARSEL2
Ab4
Ab3
Ab5
19H
20H
19G
20G
19F
20F
19E
20E
745251
AX5
AX6
AX7
Bc13
Ba12
Ba14
ARB0
ARB1
ARB2
ARB3
PBIT0
Bc24
PBIT1
IX0
IX1
IX2
IX3
IX4
IX5
IX6
IX7
DP0
DP1
DP2
DP3
DP4
DP5
DP6
DP7
B0
B1
B2
B3
B4
B5
B6
B7
R0
R1
R2
R3
R4
R5
R6
R7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
ARB4
ARB5
ARB6
ARB7
BCLK1
LCLK1
RCLK1
LSEL0
Bc9
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
NPC0
NPC1
NPC2
NPC3
NPC4
NPC5
NPC6
NPC7
L0
L1
L2
L3
L4
L5
L6
L7
226
22H
22F
236
374
399
ACC0
Ab25
AEC0
ARC0
AE1
AR1
AE2
AR2
AE3
AR3
24A
AS0
AS1
AS2
AS3
AADD0
Ac4
BADD0
745181
Ac25
Aa25
APS1
A63
AC4
Aa19
AE4
AR4
AE5
AR5
AE6
AR6
AE7
AR7
25A
AS4
AS5
AS6
AS7
Aa26
Ac27
APS
A67
ADEN
Ba8
AS0
AS1
AS2
AS3
AS4
AS5
AS6
AS7
21A
Bc7
Ba7
Bc8
Bb8
Ba9
Ba10
Bc11
Bc10
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
ABL
Bb7
BFADC
BFAD1
BBCLK
Bc15
BFAD0
BFAD1
BCLK1
Bc16
19D
X4CLK
X3CLK
X2CLK
X1CLK
PBIT0
IX3
IX4
IX5
IX6
IX7
AX0
AX1
AX2
Ba11
Ba23
Bb30
16F
ARB0
ARB1
ARB2
ARB3
ARB4
ARB5
ARB6
ARB7
322501
F C F
CPU-SLICE
Sheet 3
5001
NORSK DATA A.S
Oslo, Norway
5B03

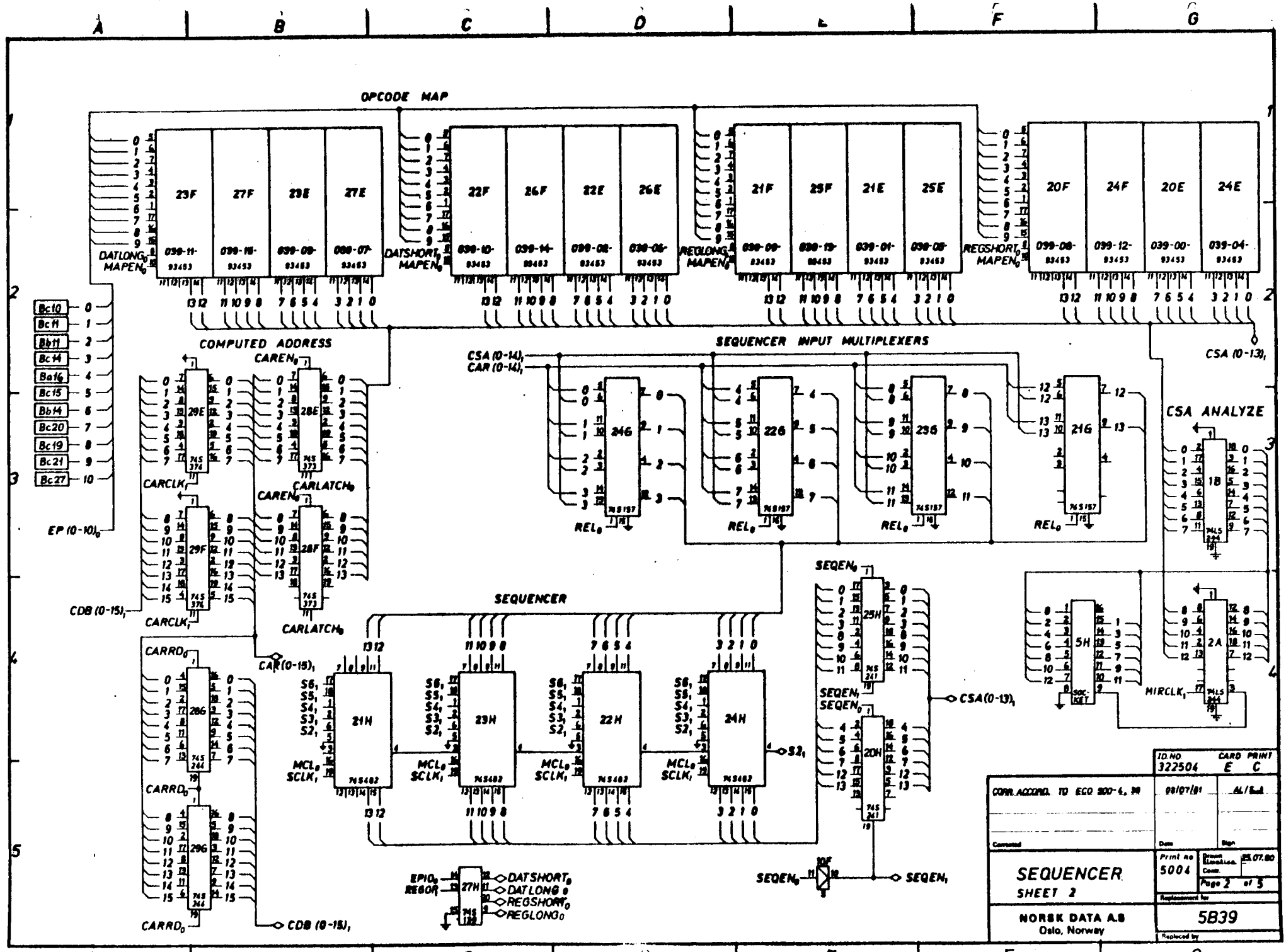

INTEGER/INDEX REGISTERS
INTEGER SELECT A
INTEGER SELECT B
ALU A-OPERAND SELECT
ALU B-OPERAND SELECT
BIT MASK
CPU-SLICE
Sheet 4
5001
NORSK DATA A.S
Oslo, Norway
5B04
322501 F C.E
Page 4 of 6

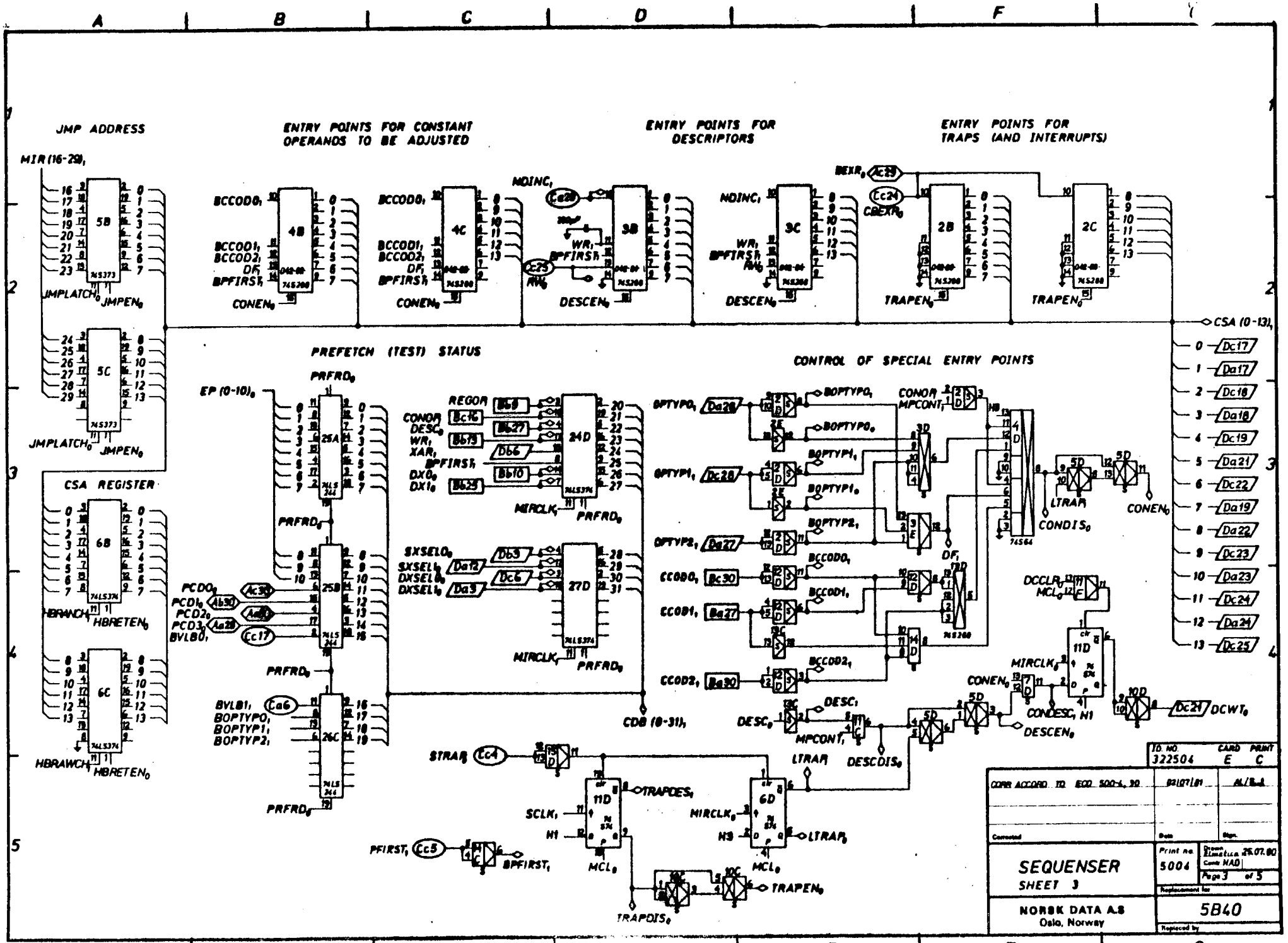

A
B
C
D
E
F
G
1
2
3
4
5
16B
745181
16A
745157
17A
17C
745288
12C
12A
12B
13C
13A
13B
15A
15B
745373
745244
20A
20B
10A
3A
18H
18G
18F
18E
745153
M1
M0
CB1
BA0
BB0
BA1
BB1
BA2
BB2
BA3
BB3
AEQB1
Ba17
Bb21
Ba16
Ba20
Dc20
Dc16
FS0
FS1
FS2
FS3
Bc22
Ba22
Bb23
Bb24
Bb26
Bc29
Ba26
Bb29
BA7
BB7
P8
P7
G8
G7
C4
Bc18
BA4
BB4
BA5
BB5
BA6
BB6
BA7
BB7
FS0
FS1
FS2
FS3
S4
S5
S6
S7
AEQB
S6M
S7
S0
S1
S2
S3
S4
S5
S6
S7
Bc25
PTY
DI0
DI1
DI2
DI3
SIGM
DAT0
DAT1
DAT2
DAT3
DI4
DI5
DI6
DI7
DAT4
DAT5
DAT6
DAT7
S6SEL
Ba24
Ba25
SIGM
SF1
SS0
SS1
SS2
SS3
SS4
SS5
SS6
SS7
Cc10
FT0
FT1
FT2
FT3
FT4
FT5
FT6
FT7
SF2
Cc12
FI32
FI33
FI34
FI35
FI36
FI37
FI38
FI39
Da4
DISEL
DO
D1
D2
D3
D4
D5
D6
D7
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
Da3
DICLK2
XBSLIC
AXDIN
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
Ac29
Aa29
Aa30
Ac27
Aa26
Ac28
Ac30
Aa27
XDI0
XDI1
XDI2
XDI3
XDI4
XDI5
XDI6
XDI7
XDSLIC
Ba19
Bc14
AXDIN
DBSLIC
Bc29
Ba27
Bc27
Ba29
Bc24
Bc30
Bc28
Ba28
Bb28
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
BLATCH
Ba20
DICLK1
Ba15
DRST
Da6
FDAT2
Dc3
FCK2
Bb27
FDAT1
Dc17
FCK1
Bb20
XOPB30
XOPB31
XOPB32
XOPB33
XOPB34
XOPB35
XOPB36
XOPB37
XOPB38
XOPB39
TXSEL0
TXSEL1
Ba4
Bc4
X10
X20
X30
X40
X11
X21
X31
X41
X12
X22
X32
X42
X13
X23
X33
X43
X14
X24
X34
X44
X15
X25
X35
X45
X16
X26
X36
X46
X17
X27
X37
X47
IX0
IX1
IX2
IX3
IX4
IX5
IX6
IX7
Bc21
Ba21
Ba18
Cc9
Bb18
Ba17
Bc17
1k R5
Ab13
1k R6
Bb11
322501
F
CPU-SLICE
Sheet 5
5001
Page 5 of 6
NORSK DATA A.S
Oslo, Norway
5B05

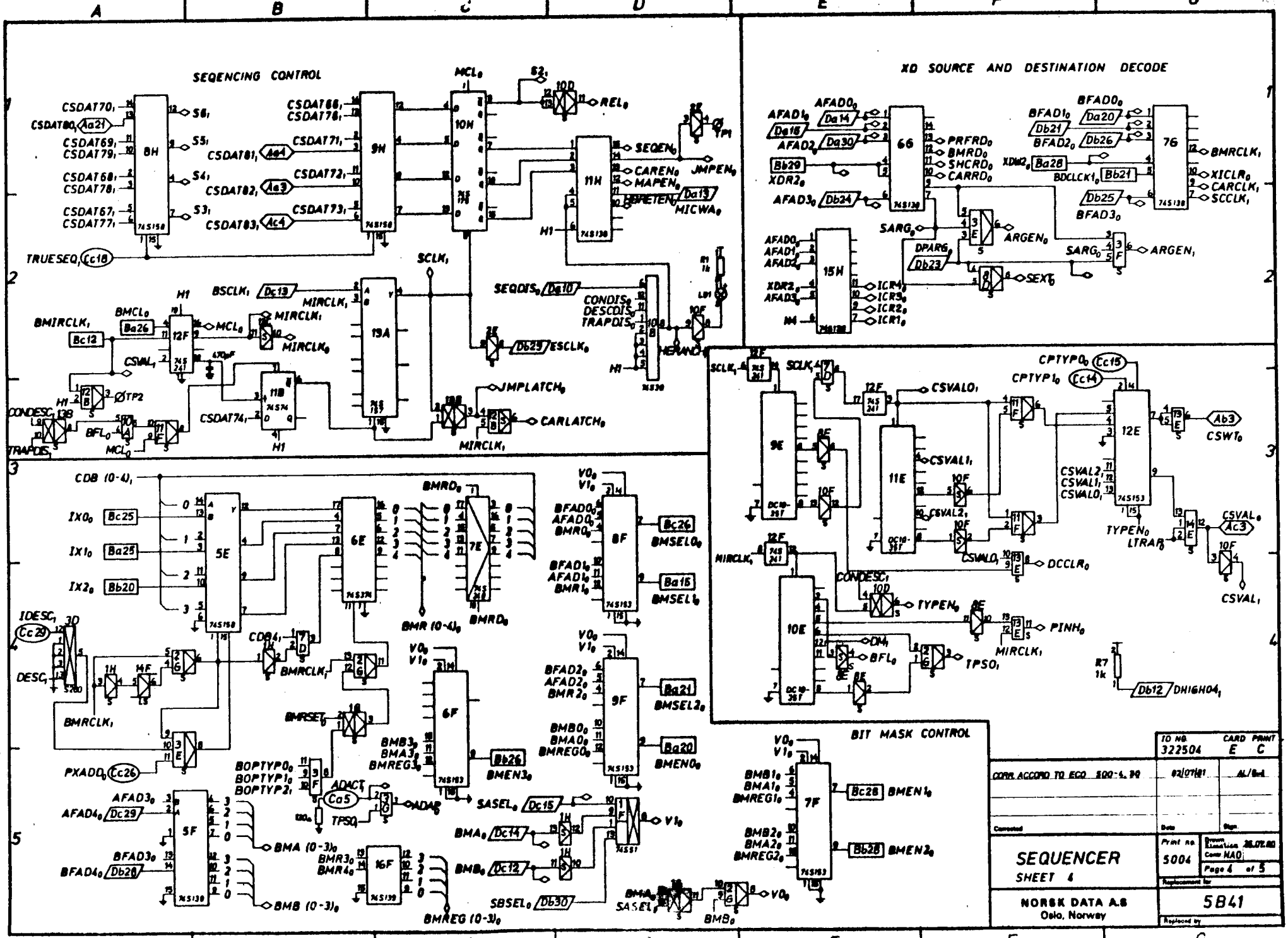


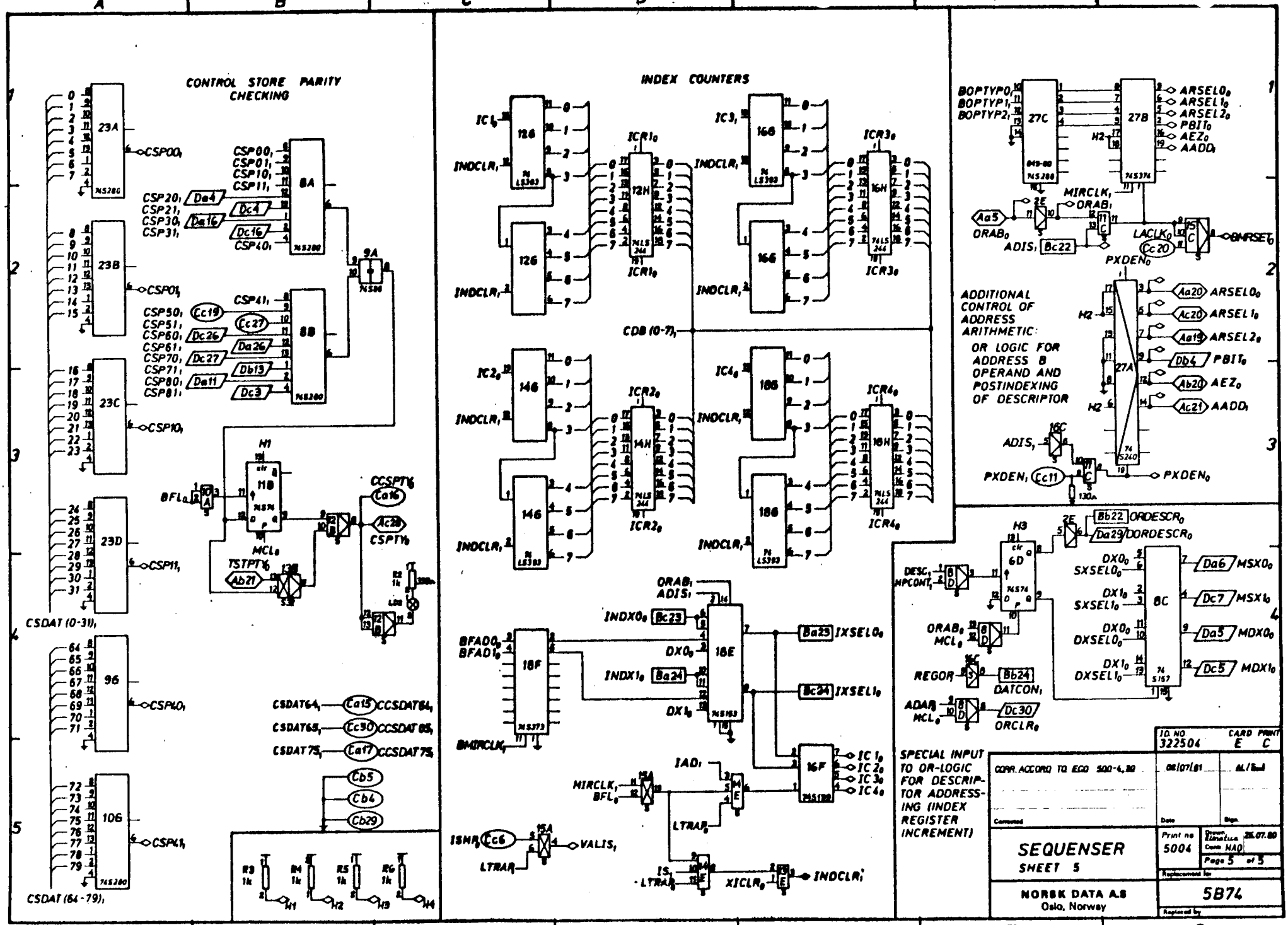
TEKN. 322501	CARD PRINT F	C.F	
CORRECTED ACCORDING TO ECO 800-1.	06/08/80		
ECO 800-10, 12	17/09/81		
CORR ACCORD TO ENG SPEC 81-013 Corrected 015	24/03/81 Date	BW Sign.	
CPU-SLICE Sheet 6	Print no. 5001	Drawn Date 26/04/80	Conn. 1R
		Page 6 of 6	
NORSK DATA A.S Oslo, Norway	Replacement for 5B52		
	Replaced by		

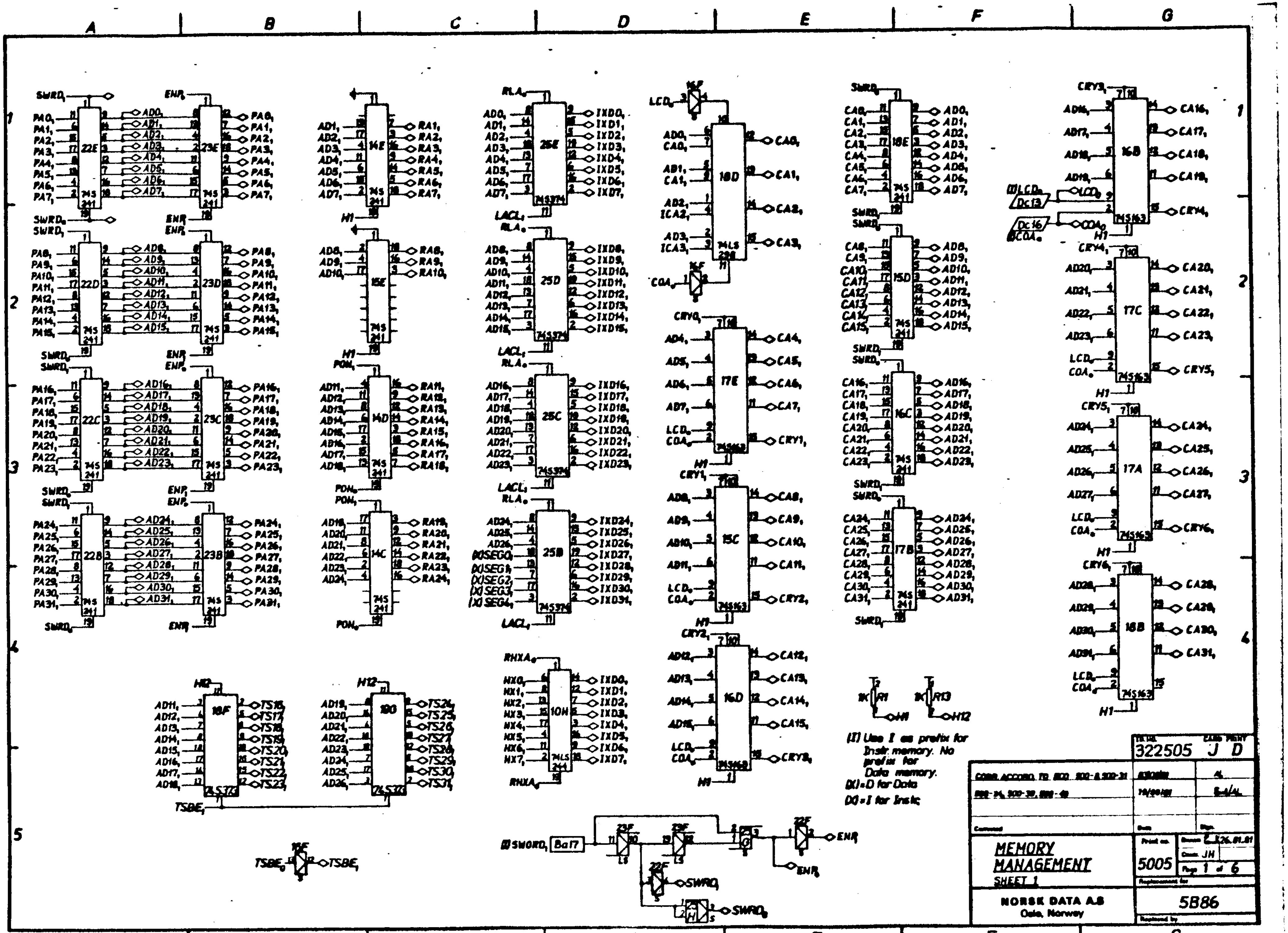

XD-TRANSCEIVERS
CONTROL STORE TRANSCEIVERS
ARGUMENT
CDB (0-31)
XD (0-31)
CSDAT (0-31)
MIR (0-31)
SHIFT COUNT
SEQUENCER
SHEET 1
NORSK DATA A.S
Oslo, Norway
322504
5004
5B38

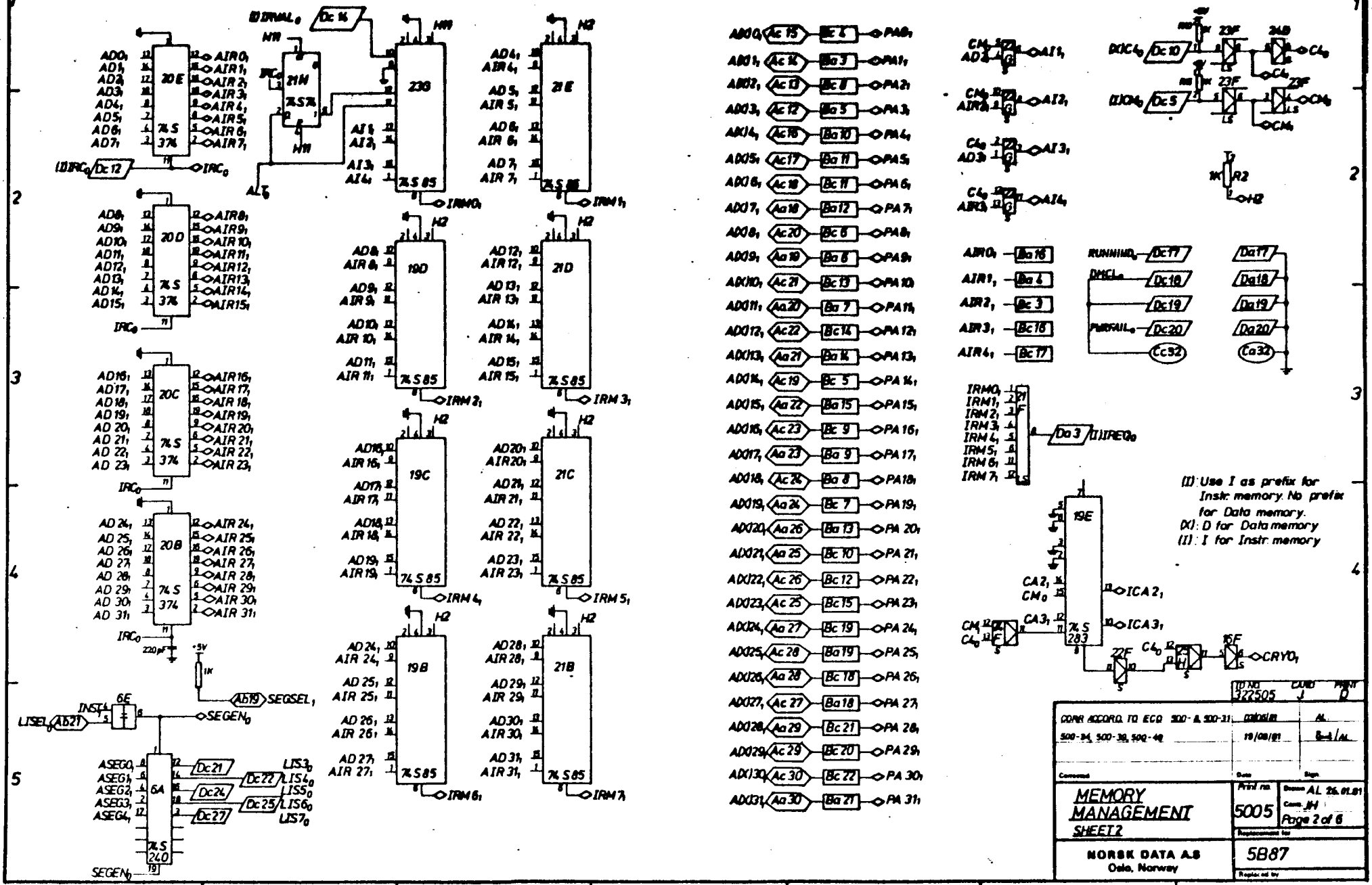

OPCODE MAP
23F
27F
23E
27E
22F
26F
22E
26E
21F
25F
21E
25E
20F
24F
20E
24E
DATLONG MAPEN0
DATSHORT MAPEN0
REGLONG MAPEN0
REGSHORT MAPEN0
COMPUTED ADDRESS
CAREN0
CARCLK1
CARLATCH0
29E
28E
29F
28F
CDB (0-15)1
CAR (0-15)1
EP (0-10)0
SEQUENCER INPUT MULTIPLEXERS
CSA (0-14)1
CAR (0-14)1
CSA (0-13)1
24G
22G
23G
21G
REL0
CSA ANALYZE
1B
2A
5H
MIRCLK1
SEQUENCER
21H
23H
22H
24H
MCL0
SCLK1
S6,
S5,
S4,
S3,
S2,
S21
CARRD0
28G
29G
SEQEN0
SEQEN1
25H
20H
27H
EPI0
REGOR
DATSHORT0
DATLONG 0
REGSHORT0
REGLONG0
ID.NO 322506
CARD PRINT E C
CORR. ACCORD. TO ECO 800-6, 38
08/07/81
AL/Sud
Corrected
Date
Sign
SEQUENCER
SHEET 2
Print no 5004
Drawn Kristiansen
Date 25.07.80
Page 2 of 5
Replacement for
NORSK DATA A.S
Oslo, Norway
5B39
Replaced by

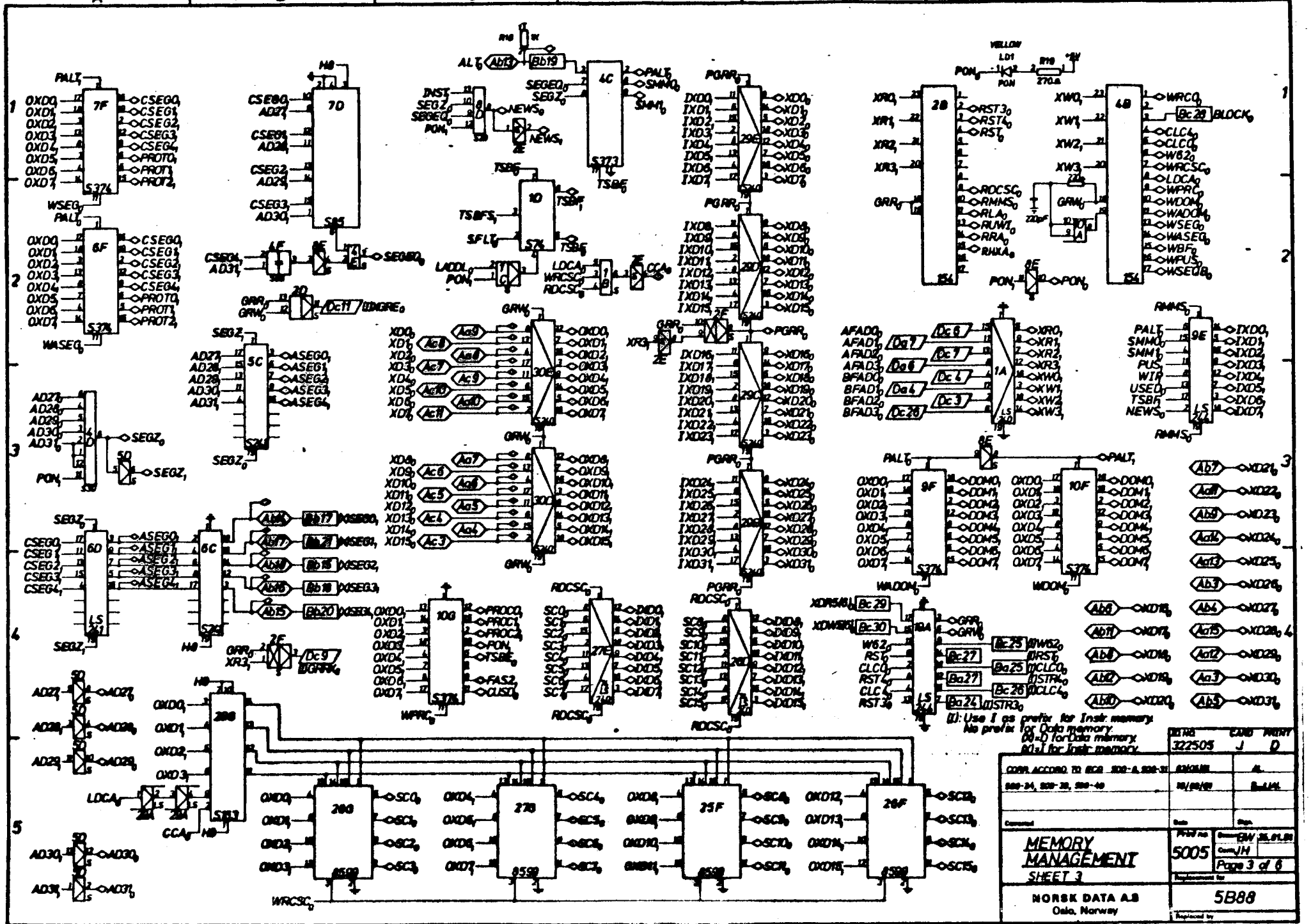

JMP ADDRESS
ENTRY POINTS FOR CONSTANT OPERANDS TO BE ADJUSTED
ENTRY POINTS FOR DESCRIPTORS
ENTRY POINTS FOR TRAPS (AND INTERRUPTS)
PREFETCH (TEST) STATUS
CONTROL OF SPECIAL ENTRY POINTS
CSA REGISTER
MIR(16-29),
JMPLATCH0
JMPEN0
HBRAWCH
HBRETEN0
CSA (0-13),
CDB (0-31),
SEQUENSER
SHEET 3
NORSK DATA A.S
Oslo, Norway
5B40
322504
Print no. 5004
Page 3 of 5

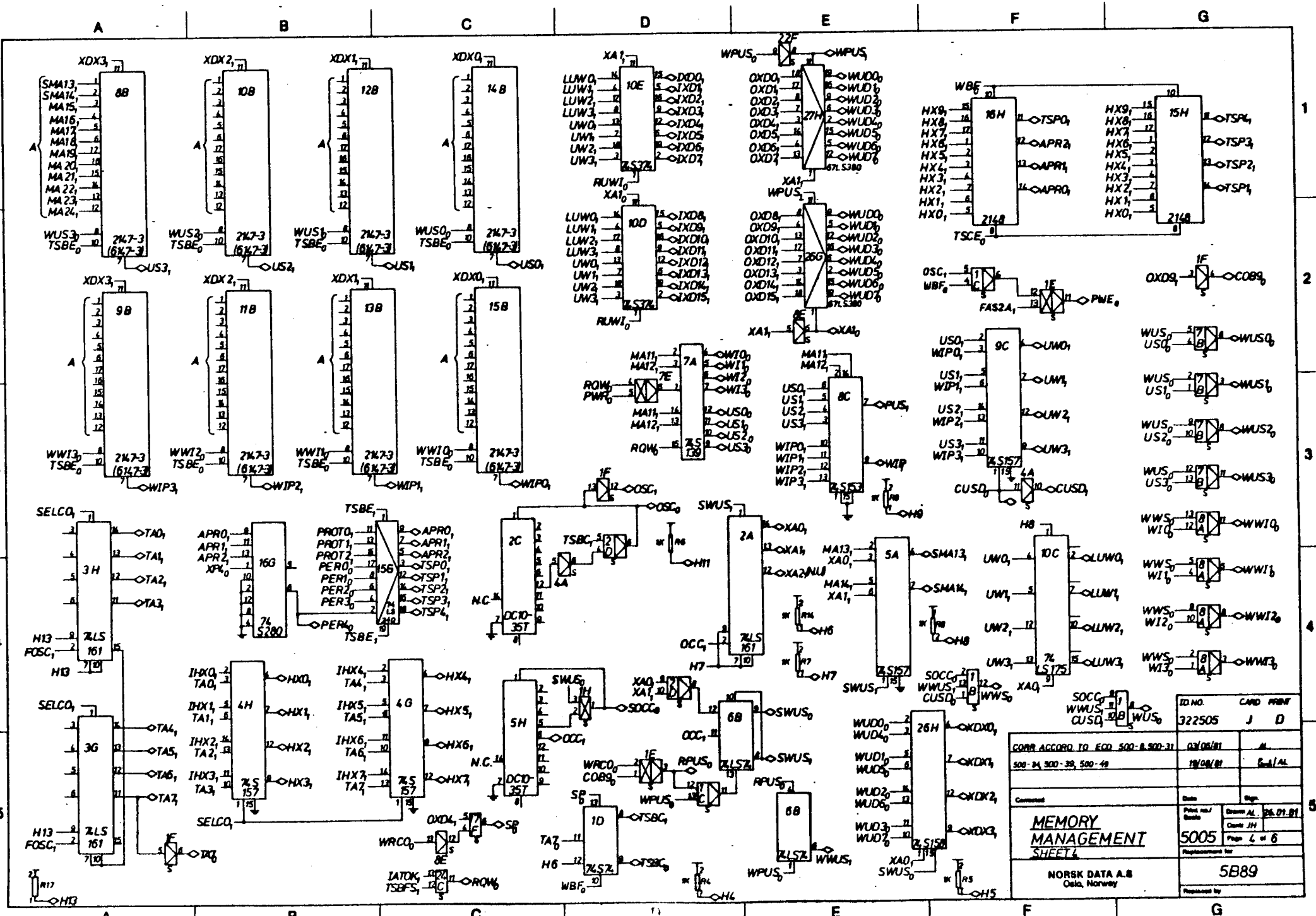

SEQENCING CONTROL
XD SOURCE AND DESTINATION DECODE
BIT MASK CONTROL
SEQUENCER
SHEET 4
NORSK DATA A.S
Oslo, Norway
322504
E C
CORR ACCORD TO ECO S00-6.90
02/07/91
AL/Bnd
Print no.
5004
Page 4 of 5
5841
TRUESEQ
SCLK
MCL
BMIRCLK
MIRCLK
CSVALO
CSVAL1
CSVAL2
CSWT
CARLATCH
JMPLATCH
ESCLK
SEQEN
CAREN
MAPEN
JMPEN
REL
MICWA
CONDESC
IDESC
DESC
PXADO
BMRCLK
BMRSET
BMRO
BMR (0-4)
BMEN3
BMEN0
BMEN1
BMEN2
BMSEL0
BMSEL1
BMSEL2
BMA (0-3)
BMB (0-3)
BMREG (0-3)
SASEL
SBSEL
ADACT
ADAC
TYPEN
PINH
DCCLR
TPSO
CPTYP0
CPTYP1
DHIGH04

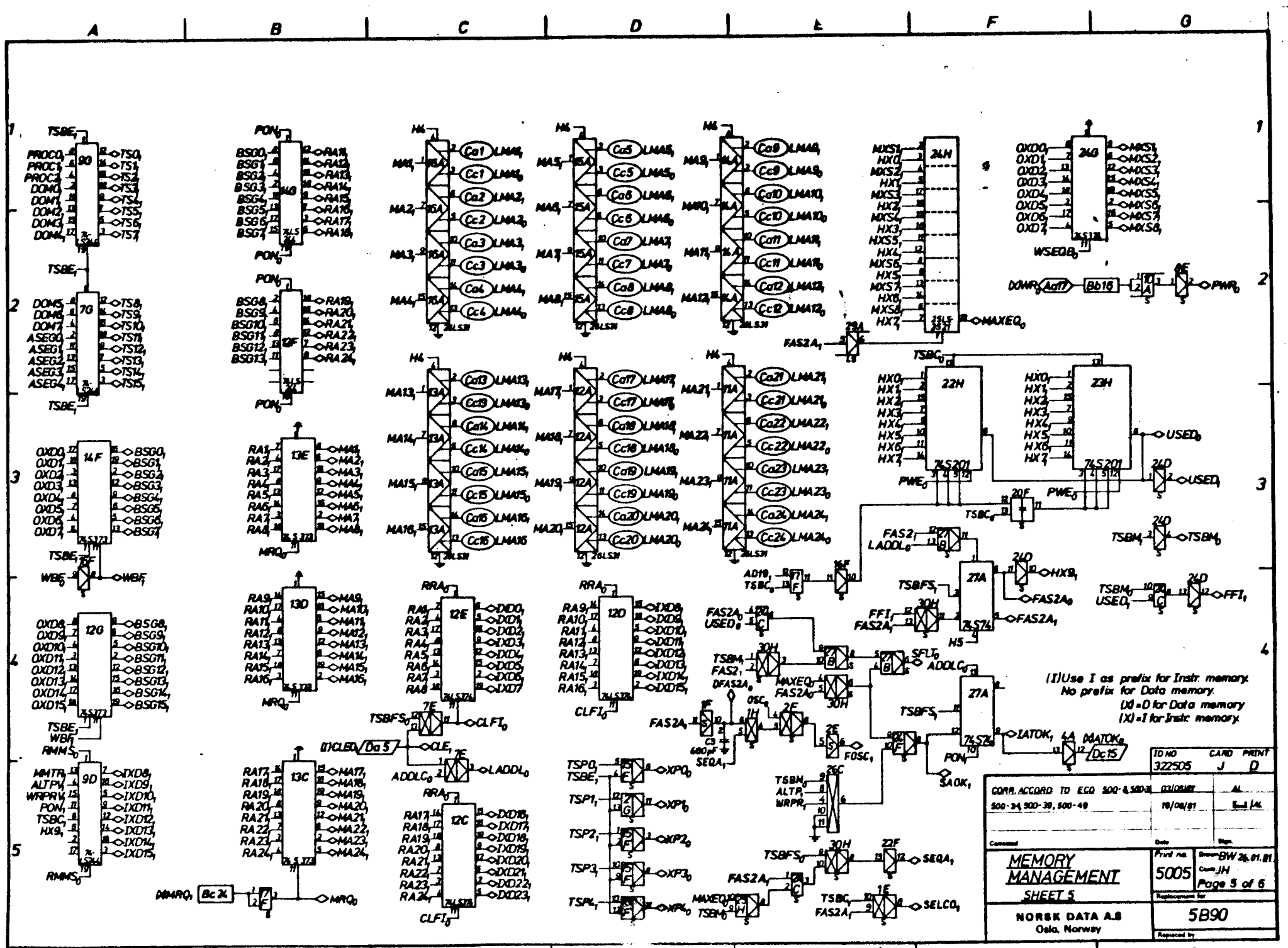

CONTROL STORE PARITY CHECKING
INDEX COUNTERS
ADDITIONAL CONTROL OF ADDRESS ARITHMETIC:
OR LOGIC FOR ADDRESS B OPERAND AND POSTINDEXING OF DESCRIPTOR
SPECIAL INPUT TO OR-LOGIC FOR DESCRIPTOR ADDRESSING (INDEX REGISTER INCREMENT)
CSDAT (0-31),
CSDAT (64-79),
CDB (0-7),
SEQUENSER
SHEET 5
NORSK DATA A.S
Oslo, Norway
ID NO 322504
CARD PRINT E C
Print no 5004
Page 5 of 5
5B74

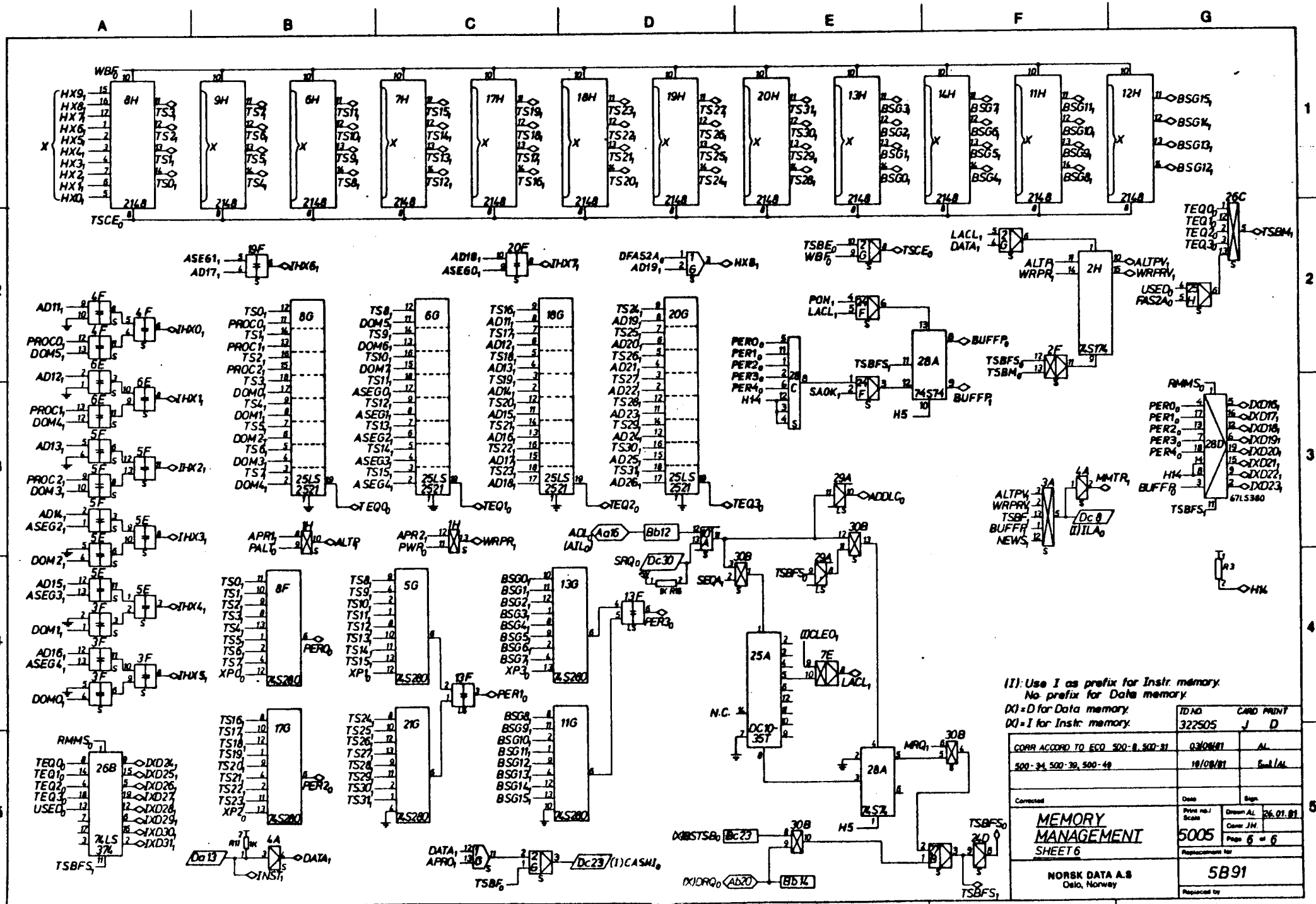

[I] Use I as prefix for Instr. memory. No prefix for Data memory.
(X) = D for Data
(X) = I for Instr.
322505 J D
MEMORY MANAGEMENT
SHEET 1
5005
Page 1 of 6
5B86
NORSK DATA A.S
Oslo, Norway

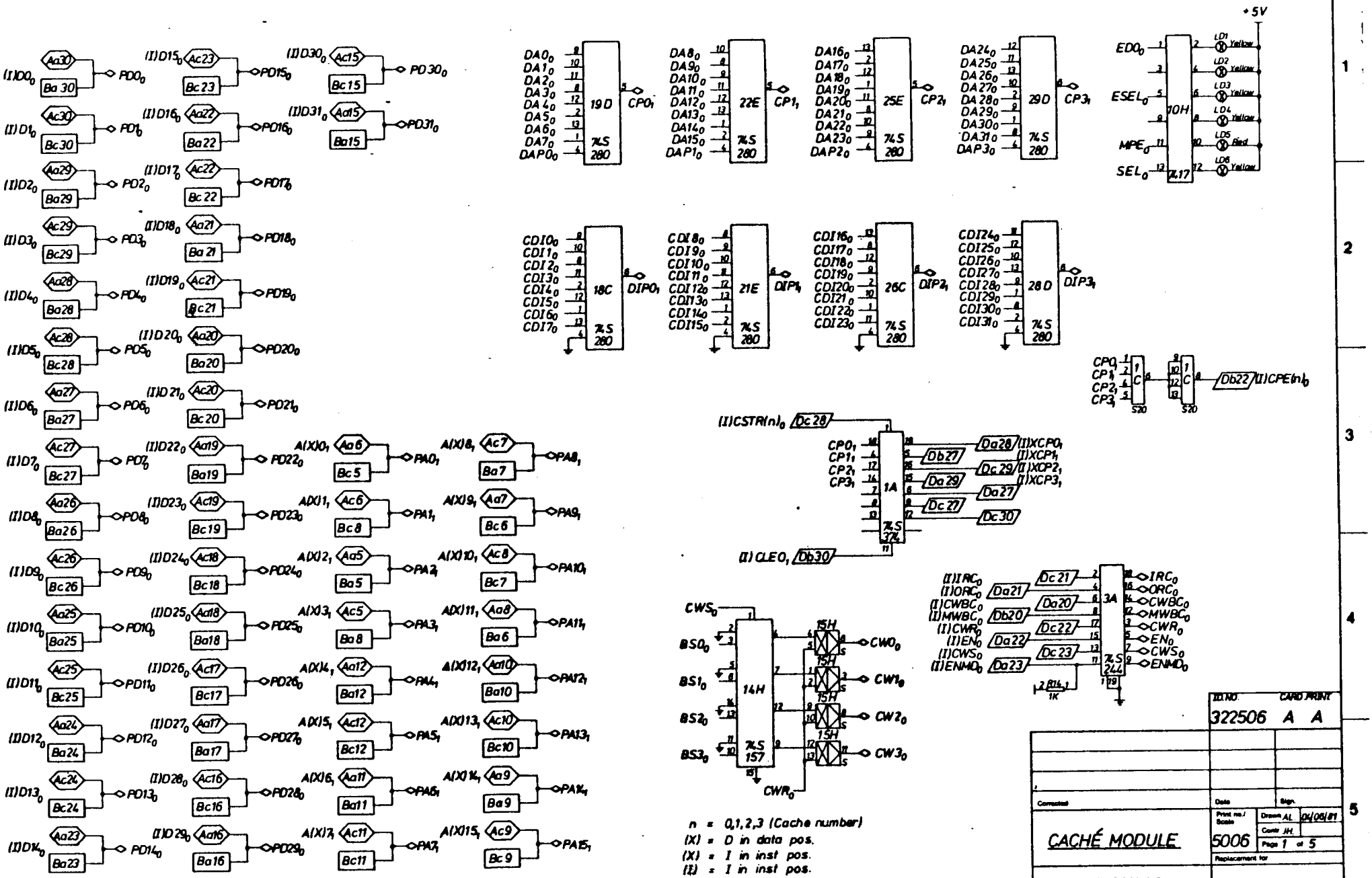

20E
20D
20C
20B
21N
23G
19D
19C
19B
21E
21D
21C
21B
19E
6E
6A
22F
23F
24B
15F
R2
74 S 85
74 S 37
74 S 240
74 S 283
IRM0
IRM1
IRM2
IRM3
IRM4
IRM5
IRM6
IRM7
IRC0
SEGSEL1
SEGEN0
CRYO1
ICA2
ICA3
Da3 (I)IREQ0
(I): Use I as prefix for Instr. memory. No prefix for Data memory.
(X): D for Data memory
(I): I for Instr. memory
MEMORY MANAGEMENT
SHEET 2
5005
Page 2 of 6
NORSK DATA A.S
Oslo, Norway
5887

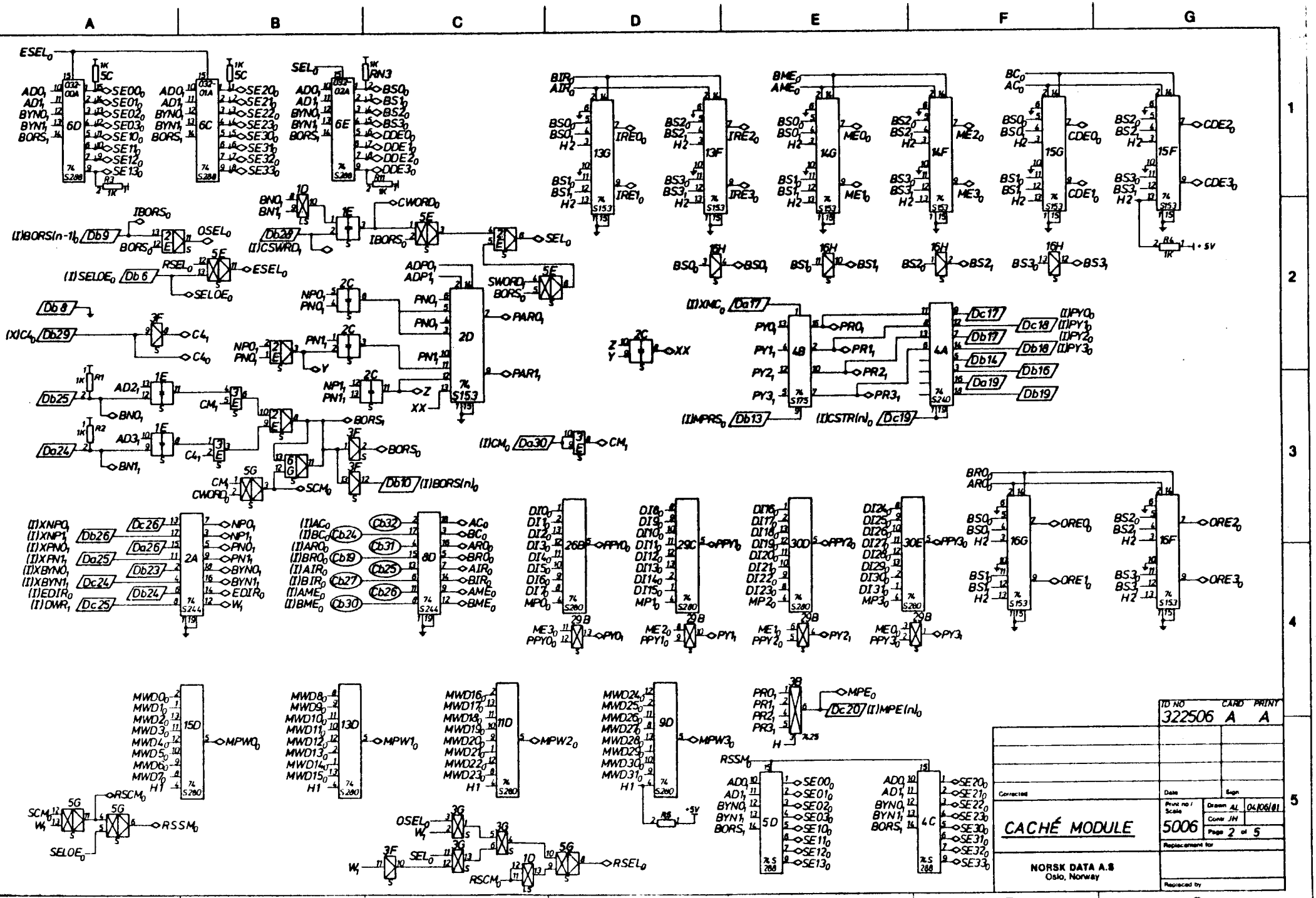

MEMORY MANAGEMENT
SHEET 3
NORSK DATA A.S
Oslo, Norway
5005
Page 3 of 6
5B88
322505
J
D
(1): Use I as prefix for Instr. memory
No prefix for Data memory.
00=0 for Data memory
01=1 for Instr. memory.

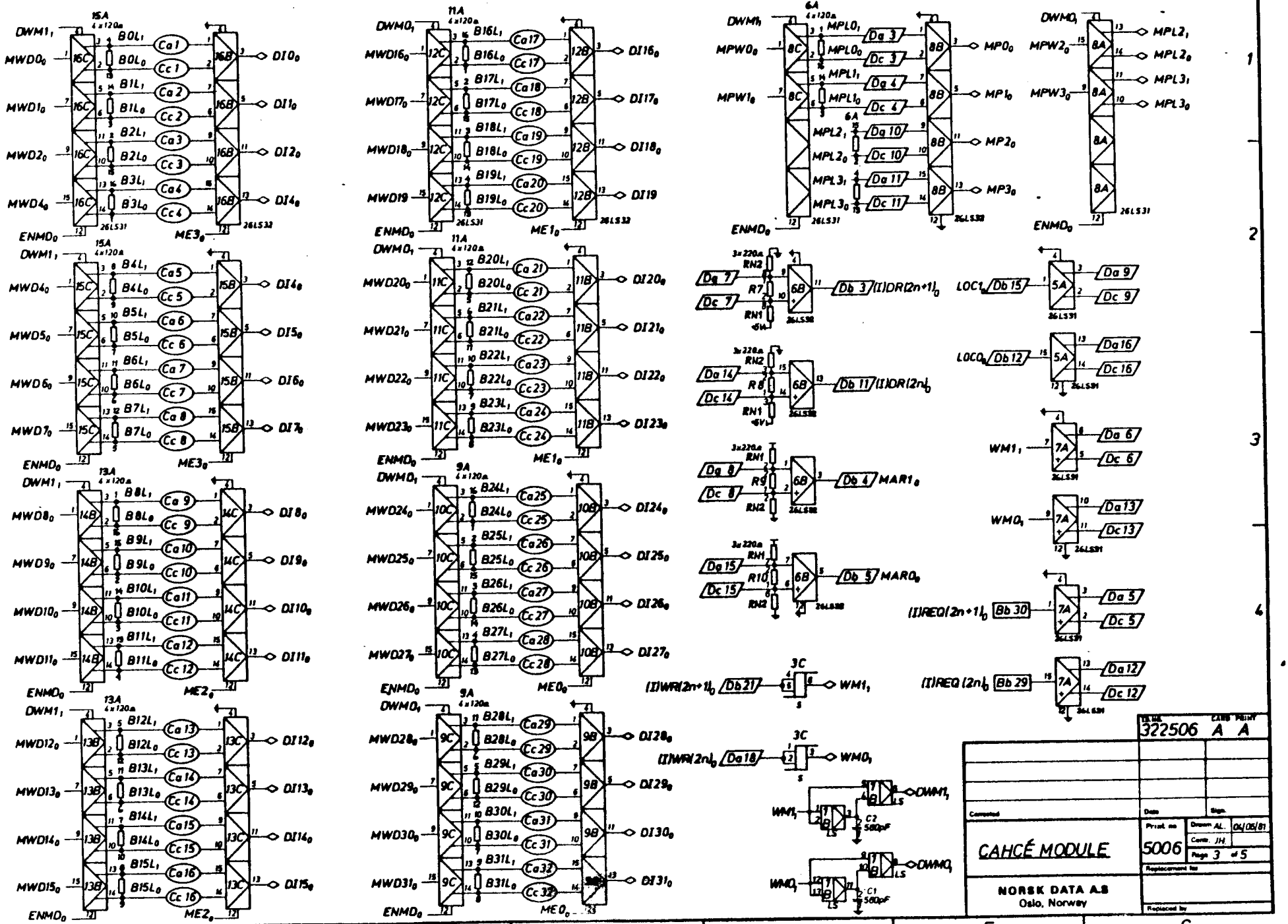

MEMORY MANAGEMENT SHEET 4
NORSK DATA A.S
Oslo, Norway
ID NO. 322505
CARD PRINT J D
CORR ACCORD TO ECO 500-8, 500-31
500-34, 500-38, 500-49
03/08/81
19/08/81
Comment
Date
Sign.
Prod. no./ Seria 5005
Drawn AL 26.01.81
Check JH
Page 4 of 6
Replacement for
5B89
Replaced by
88
108
128
148
98
118
138
158
10E
10D
27H
26G
16H
15H
9C
7A
8C
3H
3G
16G
4H
4G
5H
2C
2A
5A
10C
1D
6B
26H
XDX3
XDX2
XDX1
XDX0
XA1
WPUS
WBE
OXD9
WUS
USO
US1
US2
US3
WWI3
WWI2
WWI1
WWI0
WIP3
WIP2
WIP1
WIP0
SELCO
TSBE
APRO
APR1
APR2
XPR
PROT0
PROT1
PROT2
PERO
PER1
PER2
PER3
PER4
OSC
TSBC
SWUS
XA0
XA2
MA11
MA12
MA13
MA14
OCC
H7
H8
H11
H6
H4
H5
SOCC
WWUS
CUSO
WUS0
TSP1
TSP2
TSP3
TSP4
APR3
APR1
APR0
TSCE
OSC1
WBF0
FAS2A1
PWE
COB9
UWO1
UW1
UW2
UW3
LUWO
LUW1
LUW2
LUW3
WWO
WWI
WWS
SMA13
SMA14
HX0
HX1
HX2
HX3
HX4
HX5
HX6
HX7
TA0
TA1
TA2
TA3
TA4
TA5
TA6
TA7
IHX0
IHX1
IHX2
IHX3
IHX4
IHX5
IHX6
IHX7
OXD0
OXD1
OXD2
OXD3
OXD4
OXD5
OXD6
OXD7
OXD8
OXD9
OXD10
OXD11
OXD12
OXD13
OXD14
OXD15
IXD0
IXD1
IXD2
IXD3
IXD4
IXD5
IXD6
IXD7
IXD8
IXD9
IXD10
IXD11
IXD12
IXD13
IXD14
IXD15
WUD0
WUD1
WUD2
WUD3
WUD4
WUD5
WUD6
WUD7
WRCO
COB9
RPUS
SB
IATOK
TSBFS
ROW
PWR
RUWI
WBF
TSBC
WRCO
N.C.
DCIO-35T
74LS161
74LS157
74LS280
74LS139
74LS174
74LS175
74LS257
74LS374
74LS240
74LS244
74LS273
74LS378
74LS380

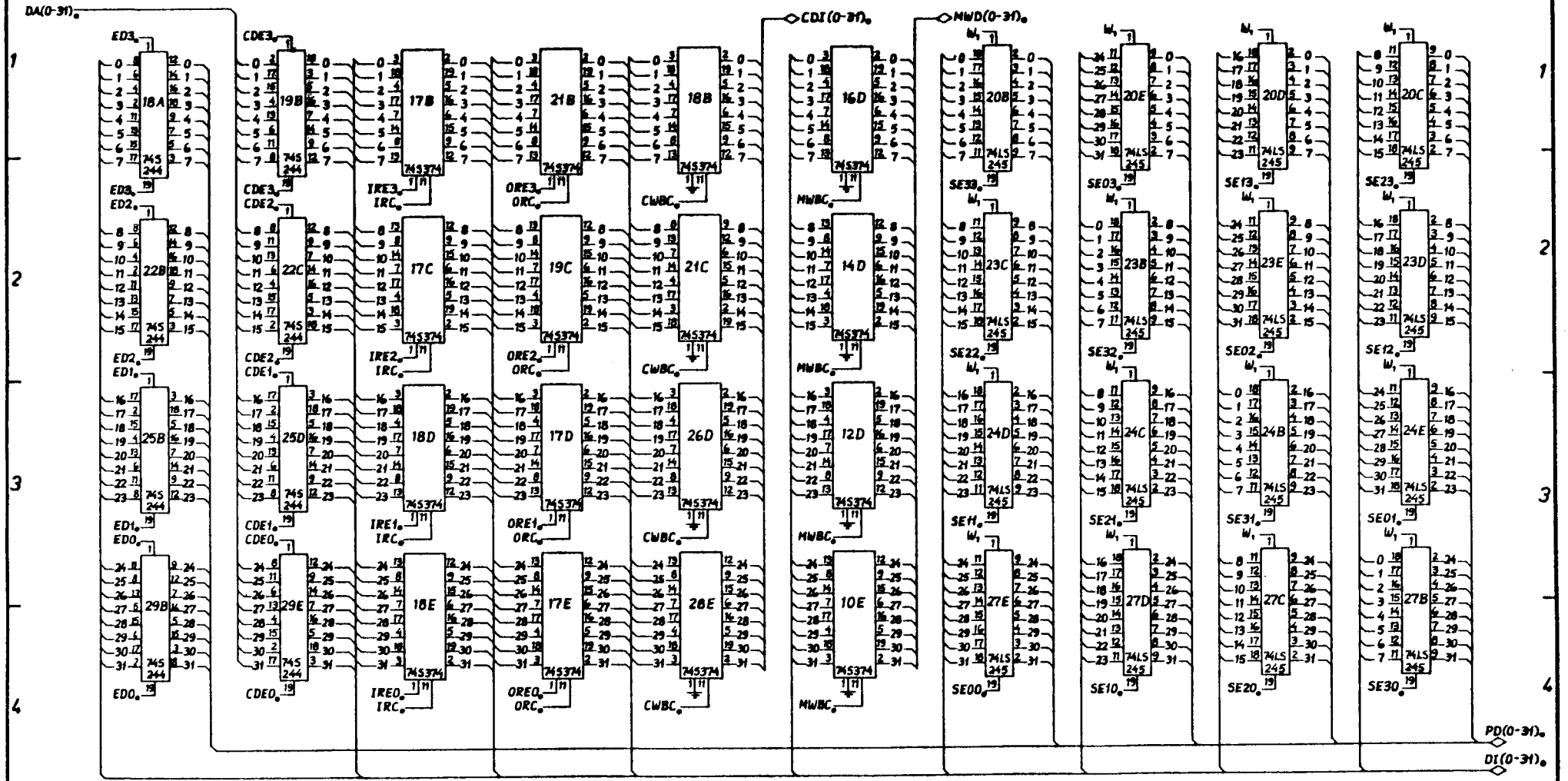

(I)Use I as prefix for Instr. memory.
No prefix for Data memory.
(X)=D for Data memory
(X)=I for Instr. memory
MEMORY MANAGEMENT
SHEET 5
NORSK DATA A.S
Oslo, Norway
5005
5B90
Page 5 of 6
322505
CORR. ACCORD TO ECO 500-6,500-31
500-34, 500-39, 500-49


(I): Use I as prefix for Instr. memory.
No. prefix for Data memory.
(X) = D for Data memory.
(X) = I for Instr. memory.
TD NO. 322505
CARD PRINT J D
CORR ACCORD TO ECO 500-8, 500-31
500-34, 500-39, 500-49
03/08/81
19/08/81
AL
Corrected
Date
Sign
MEMORY MANAGEMENT
SHEET 6
Print no./ Scale 5005
Drawn AL 26.01.81
Check JH
Page 6 of 6
Replacement for 5B91
Replaced by
NORSK DATA A.S
Oslo, Norway


A
B
C
D
E
F
G
1
2
3
4
5
+5V
(I)D0 Aa30 Ba30 Bc30 PD0
(I)D1 Ac30 Bc30 PD1
(I)D2 Aa29 Ba29 PD2
(I)D3 Ac29 Bc29 PD3
(I)D4 Aa28 Ba28 PD4
(I)D5 Ac28 Bc28 PD5
(I)D6 Aa27 Ba27 PD6
(I)D7 Ac27 Bc27 PD7
(I)D8 Aa26 Ba26 PD8
(I)D9 Ac26 Bc26 PD9
(I)D10 Aa25 Ba25 PD10
(I)D11 Ac25 Bc25 PD11
(I)D12 Aa24 Ba24 PD12
(I)D13 Ac24 Bc24 PD13
(I)D14 Aa23 Ba23 PD14
(I)D15 Ac23 Bc23 PD15
(I)D16 Aa22 Ba22 PD16
(I)D17 Ac22 Bc22 PD17
(I)D18 Aa21 Ba21 PD18
(I)D19 Ac21 Bc21 PD19
(I)D20 Aa20 Ba20 PD20
(I)D21 Ac20 Bc20 PD21
(I)D22 Aa19 Ba19 PD22
(I)D23 Ac19 Bc19 PD23
(I)D24 Aa18 Ba18 PD24
(I)D25 Ac18 Bc18 PD25
(I)D26 Aa17 Ba17 PD26
(I)D27 Ac17 Bc17 PD27
(I)D28 Aa16 Ba16 PD28
(I)D29 Ac16 Bc16 PD29
(I)D30 Aa15 Ba15 PD30
(I)D31 Ac15 Bc15 PD31
A(X)0 Aa6 Bc5 PA0
A(X)1 Ac6 Bc8 PA1
A(X)2 Aa5 Ba5 PA2
A(X)3 Ac5 Ba8 PA3
A(X)4 Aa12 Ba12 PA4
A(X)5 Ac12 Bc12 PA5
A(X)6 Aa11 Ba11 PA6
A(X)7 Ac11 Bc11 PA7
A(X)8 Ac7 Ba7 PA8
A(X)9 Aa7 Bc6 PA9
A(X)10 Ac8 Bc7 PA10
A(X)11 Aa8 Ba6 PA11
A(X)12 Aa10 Ba10 PA12
A(X)13 Ac10 Bc10 PA13
A(X)14 Aa9 Ba9 PA14
A(X)15 Ac9 Bc9 PA15
DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 DAP0 19D 74S 280 CP0
DA8 DA9 DA10 DA11 DA12 DA13 DA14 DA15 DAP1 22E 74S 280 CP1
DA16 DA17 DA18 DA19 DA20 DA21 DA22 DA23 DAP2 25E 74S 280 CP2
DA24 DA25 DA26 DA27 DA28 DA29 DA30 DA31 DAP3 29D 74S 280 CP3
EDO ESEL MPE SEL 10H 74S 157 LD1 LD2 LD3 LD4 LD5 LD6 Yellow Red
CDI0 CDI1 CDI2 CDI3 CDI4 CDI5 CDI6 CDI7 18C 74S 280 DIP0
CDI8 CDI9 CDI10 CDI11 CDI12 CDI13 CDI14 CDI15 21E 74S 280 DIP1
CDI16 CDI17 CDI18 CDI19 CDI20 CDI21 CDI22 CDI23 26C 74S 280 DIP2
CDI24 CDI25 CDI26 CDI27 CDI28 CDI29 CDI30 CDI31 28D 74S 280 DIP3
CP0 CP1 CP2 CP3 C S20 Db22 (I)CPE(n)
(I)CSTR(n) Dc28
CP0 CP1 CP2 CP3 1A 74S 374 Db27 Da28 Dc29 Da29 Da27 Dc27 Dc30 (I)XCP0 (I)XCP1 (I)XCP2 (I)XCP3
(I)CLEO Db30
CWS BS0 BS1 BS2 BS3 14H 74S 157 15H CWR0 CW0 CW1 CW2 CW3
(I)IRC (I)ORC (I)CWBC (I)MWBC (I)CWR (I)EN (I)CWS (I)ENMO Dc21 Da21 Da20 Db20 Dc22 Da22 Dc23 Da23 3A 74S 244 IRC ORC CWBC MWBC CWR EN CWS ENMO 2.87kΩ 1K
n = 0,1,2,3 (Cache number)
(X) = 0 in data pos.
(X) = 1 in inst pos.
(I) = I in inst pos.
(I) = in data pos.
ID NO. 322506
CARD PRINT A A
Corrected
Date
Sign.
CACHÉ MODULE
Print no./ Scale 5006
Drawn AL 04/08/81
Contr JH
Page 1 of 5
Replacement for
NORSK DATA A.S
Oslo, Norway
Replaced by


CACHÉ MODULE
NORSK DATA A.S
Oslo, Norway
5006
322506 A A
Page 2 of 5


15A
DWM1
MWD0
MWD1
MWD2
MWD4
ENMD0
ME3
DI0
DI1
DI2
DI4
B0L1
B0L0
B1L1
B1L0
B2L1
B2L0
B3L1
B3L0
Ca1
Cc1
Ca2
Cc2
Ca3
Cc3
Ca4
Cc4
26LS31
26LS32
15A
DWM1
MWD4
MWD5
MWD6
MWD7
ENMD0
ME3
DI4
DI5
DI6
DI7
B4L1
B4L0
B5L1
B5L0
B6L1
B6L0
B7L1
B7L0
Ca5
Cc5
Ca6
Cc6
Ca7
Cc7
Ca8
Cc8
13A
DWM1
MWD8
MWD9
MWD10
MWD11
ENMD0
ME2
DI8
DI9
DI10
DI11
B8L1
B8L0
B9L1
B9L0
B10L1
B10L0
B11L1
B11L0
Ca9
Cc9
Ca10
Cc10
Ca11
Cc11
Ca12
Cc12
13A
DWM1
MWD12
MWD13
MWD14
MWD15
ENMD0
ME2
DI12
DI13
DI14
DI15
B12L1
B12L0
B13L1
B13L0
B14L1
B14L0
B15L1
B15L0
Ca13
Cc13
Ca14
Cc14
Ca15
Cc15
Ca16
Cc16
11A
DWM0
MWD16
MWD17
MWD18
MWD19
ENMD0
ME1
DI16
DI17
DI18
DI19
B16L1
B16L0
B17L1
B17L0
B18L1
B18L0
B19L1
B19L0
Ca17
Cc17
Ca18
Cc18
Ca19
Cc19
Ca20
Cc20
26LS31
26LS32
11A
DWM0
MWD20
MWD21
MWD22
MWD23
ENMD0
ME1
DI20
DI21
DI22
DI23
B20L1
B20L0
B21L1
B21L0
B22L1
B22L0
B23L1
B23L0
Ca21
Cc21
Ca22
Cc22
Ca23
Cc23
Ca24
Cc24
9A
DWM0
MWD24
MWD25
MWD26
MWD27
ENMD0
ME0
DI24
DI25
DI26
DI27
B24L1
B24L0
B25L1
B25L0
B26L1
B26L0
B27L1
B27L0
Ca25
Cc25
Ca26
Cc26
Ca27
Cc27
Ca28
Cc28
9A
DWM0
MWD28
MWD29
MWD30
MWD31
ENMD0
ME0
DI28
DI29
DI30
DI31
B28L1
B28L0
B29L1
B29L0
B30L1
B30L0
B31L1
B31L0
Ca29
Cc29
Ca30
Cc30
Ca31
Cc31
Ca32
Cc32
6A
DWM1
MPW0
MPW1
ENMD0
MPL0 1
MPL0 0
MPL1 1
MPL1 0
MPL2 1
MPL2 0
MPL3 1
MPL3 0
Da 3
Dc 3
Da 4
Dc 4
Da 10
Dc 10
Da 11
Dc 11
MP0
MP1
MP2
MP3
26LS31
26LS32
6A
DWM0
MPW2
MPW3
ENMD0
MPL2 1
MPL2 0
MPL3 1
MPL3 0
26LS31
Da 7
Dc 7
RN2
R7
RN1
Db 3
(I)DR(2n+1)0
Da 14
Dc 14
R8
Db 11
(I)DR(2n)0
Da 8
Dc 8
R9
Db 4
MAR1 0
Da 15
Dc 15
R10
Db 5
MAR0 0
3C
(I)WR(2n+1)0
Db 21
WM1 1
3C
(I)WR(2n)0
Da 18
WM0 1
C2
560pF
C1
560pF
DWM1
DWM0
LOC1
LOC0
Db 15
Db 12
Da 9
Dc 9
Da 16
Dc 16
WM1 1
WM0 1
Da 6
Dc 6
Da 13
Dc 13
(I)REQ(2n+1)0
Bb 30
Da 5
Dc 5
(I)REQ(2n)0
Bb 29
Da 12
Dc 12
7A
5A
6B
8B
8A
14C
16B
16C
15B
15C
12B
12C
10B
10C
9B
9C
11B
11C
13B
13C
26LS31
26LS32
26LS38
LS
322506 A A
CAHCÉ MODULE
5006
Drawn AL 04/05/81
Page 3 of 5
NORSK DATA A.S
Oslo, Norway



TEK NO.	CARD	PRINT
322506	A	A

Corrected | Date | Sign

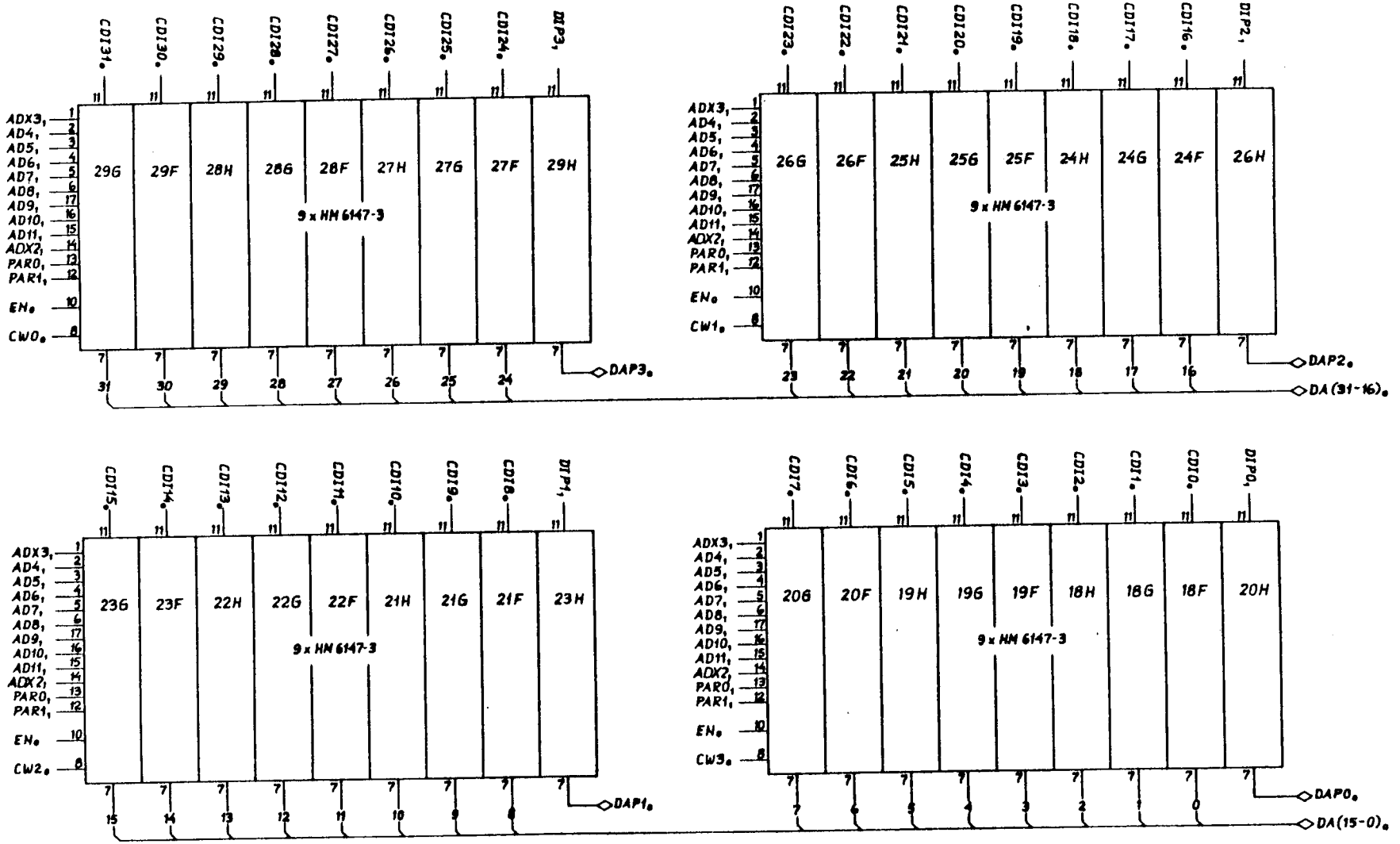
CACHÉ MODULE

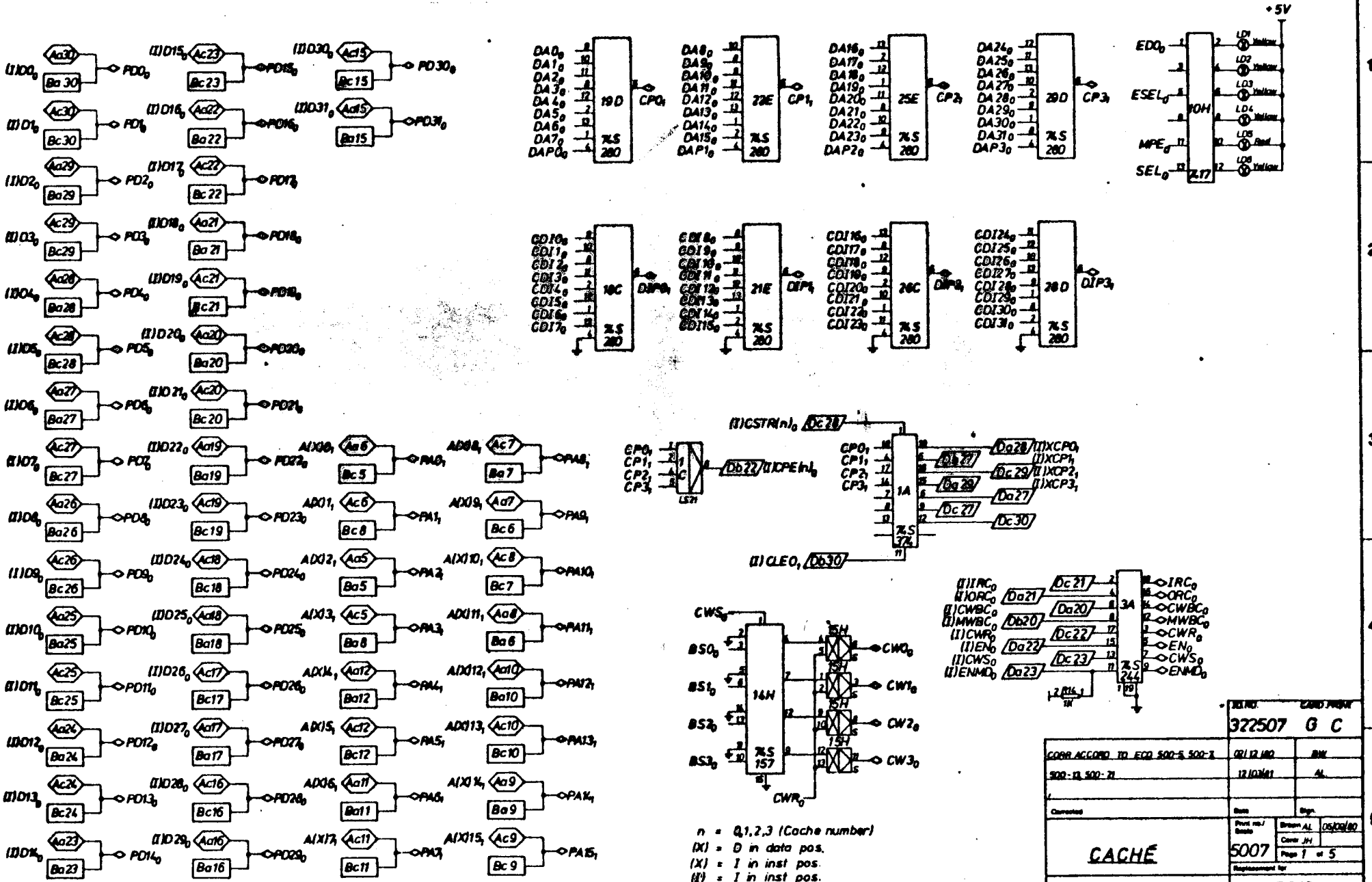
Print no. 5006 | Drawn AL 04/06/81 | Check JH | Page 4 of 5

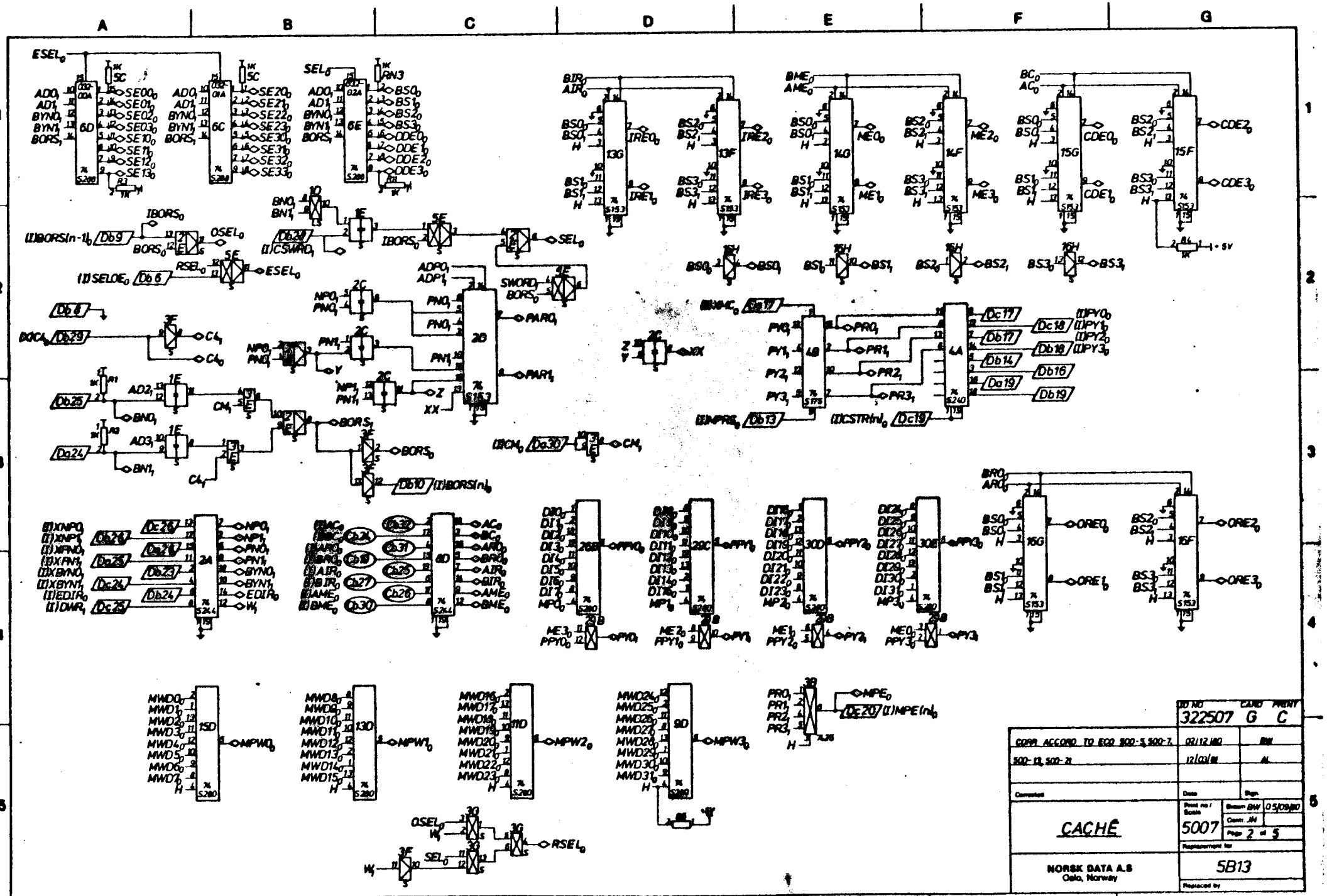
Replacement for

NORSK DATA A.S
Oslo, Norway

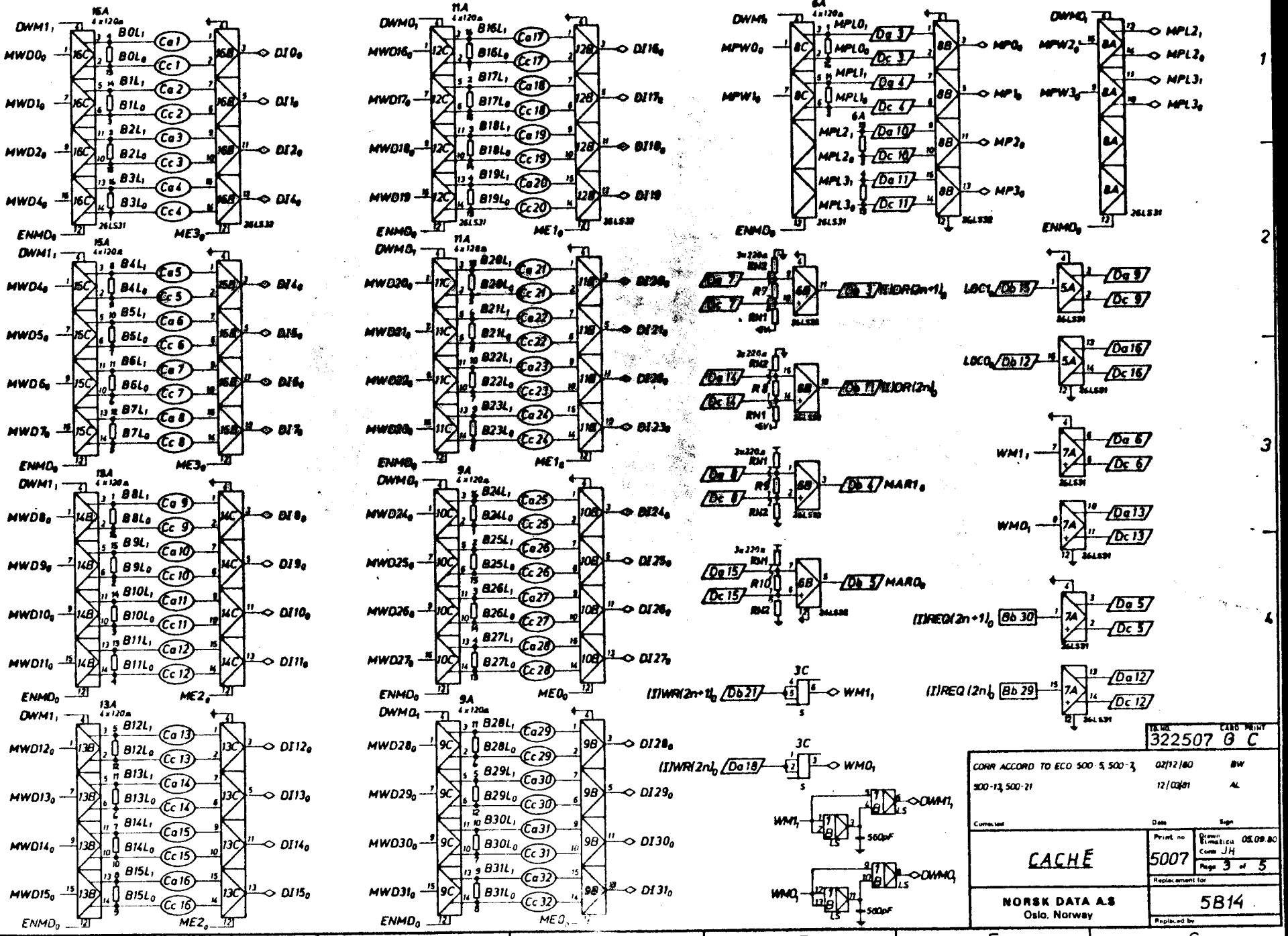
Replaced by

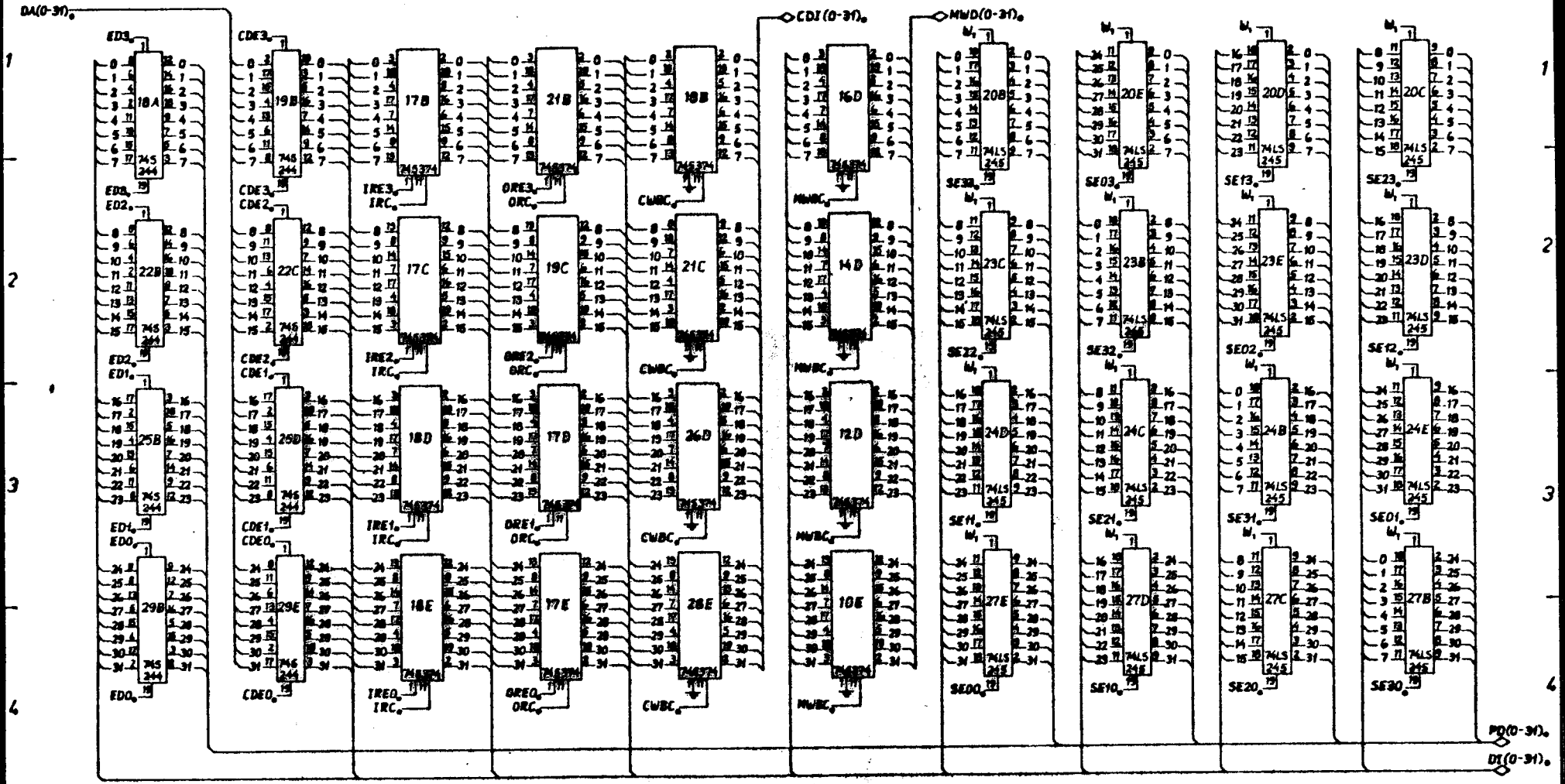

CDI31, CDI30, CDI29, CDI28, CDI27, CDI26, CDI25, CDI24, DIP3,
ADX3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, ADX2, PAR0, PAR1, EN, CW0,
29G 29F 28H 28G 28F 27H 27G 27F 29H
9 x HM 6147-3
DAP3,
31 30 29 28 27 26 25 24
CDI23, CDI22, CDI21, CDI20, CDI19, CDI18, CDI17, CDI16, DIP2,
ADX3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, ADX2, PAR0, PAR1, EN, CW1,
26G 26F 25H 25G 25F 24H 24G 24F 26H
9 x HM 6147-3
DAP2,
DA(31-16),
23 22 21 20 19 18 17 16
CDI15, CDI14, CDI13, CDI12, CDI11, CDI10, CDI9, CDI8, DIP1,
ADX3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, ADX2, PAR0, PAR1, EN, CW2,
23G 23F 22H 22G 22F 21H 21G 21F 23H
9 x HM 6147-3
DAP1,
15 14 13 12 11 10 9 8
CDI7, CDI6, CDI5, CDI4, CDI3, CDI2, CDI1, CDI0, DIP0,
ADX3, AD4, AD5, AD6, AD7, AD8, AD9, AD10, AD11, ADX2, PAR0, PAR1, EN, CW3,
20G 20F 19H 19G 19F 18H 18G 18F 20H
9 x HM 6147-3
DAP0,
DA(15-0),
7 6 5 4 3 2 1 0
CM, C4, AD2, AD12, AD3, AD13,
30C
74 S153
ADX2, ADX3,
DDE0, EDIR, DDE1, EDIR, DDE2, EDIR, DDE3, EDIR,
8F
ED0, ED1, ED2, ED3,
CM, C4, AD12, AD13, AD14, AD13, AD14, AD15,
30H
74 S153
ADP0, ADP1,
TS NO. 322506
CARD PRINT A A
Corrected
Date
Sign
CACHÉ MODULE
Print no 5006
Drawn AL 04/06/81
Cons JN
Page 5 of 5
Replacement for
NORSK DATA A.S
Oslo, Norway
Replaced by


(I)DO0 Aa30 Ba30 PD0
(I)DO1 Ac30 Bc30 PD1
(I)DO2 Aa29 Ba29 PD2
(I)DO3 Ac29 Bc29 PD3
(I)DO4 Aa28 Ba28 PD4
(I)DO5 Ac28 Bc28 PD5
(I)DO6 Aa27 Ba27 PD6
(I)DO7 Ac27 Bc27 PD7
(I)DO8 Aa26 Ba26 PD8
(I)DO9 Ac26 Bc26 PD9
(I)DO10 Aa25 Ba25 PD10
(I)DO11 Ac25 Bc25 PD11
(I)DO12 Aa24 Ba24 PD12
(I)DO13 Ac24 Bc24 PD13
(I)DO14 Aa23 Ba23 PD14
(I)DO15 Ac23 Bc23 PD15
(I)DO16 Aa22 Ba22 PD16
(I)DO17 Ac22 Bc22 PD17
(I)DO18 Aa21 Ba21 PD18
(I)DO19 Ac21 Bc21 PD19
(I)DO20 Aa20 Ba20 PD20
(I)DO21 Ac20 Bc20 PD21
(I)DO22 Aa19 Ba19 PD22
(I)DO23 Ac19 Bc19 PD23
(I)DO24 Aa18 Ba18 PD24
(I)DO25 Ac18 Bc18 PD25
(I)DO26 Aa17 Ba17 PD26
(I)DO27 Ac17 Bc17 PD27
(I)DO28 Aa16 Ba16 PD28
(I)DO29 Ac16 Bc16 PD29
(I)DO30 Aa15 Ba15 PD30
(I)DO31 Ac15 Bc15 PD31
A(X)00 Aa6 Bc5 PA0
A(X)01 Ac6 Bc8 PA1
A(X)02 Aa5 Ba5 PA2
A(X)03 Ac5 Ba8 PA3
A(X)04 Aa12 Ba12 PA4
A(X)05 Ac12 Bc12 PA5
A(X)06 Aa11 Ba11 PA6
A(X)07 Ac11 Bc11 PA7
A(X)08 Ac7 Ba7 PA8
A(X)09 Aa7 Bc6 PA9
A(X)10 Ac8 Bc7 PA10
A(X)11 Aa8 Ba6 PA11
A(X)12 Aa10 Ba10 PA12
A(X)13 Ac10 Bc10 PA13
A(X)14 Aa9 Ba9 PA14
A(X)15 Ac9 Bc9 PA15
DA0 DA1 DA2 DA3 DA4 DA5 DA6 DA7 DAP0 19D CP0
DA8 DA9 DA10 DA11 DA12 DA13 DA14 DA15 DAP1 22E CP1
DA16 DA17 DA18 DA19 DA20 DA21 DA22 DA23 DAP2 25E CP2
DA24 DA25 DA26 DA27 DA28 DA29 DA30 DA31 DAP3 28D CP3
74S 280
EDO ESEL MPE SEL 10H 74S 17
LD1 LD2 LD3 LD4 LD5 LD6
+5V
CDI0 CDI1 CDI2 CDI3 CDI4 CDI5 CDI6 CDI7 18C DIP0
CDI8 CDI9 CDI10 CDI11 CDI12 CDI13 CDI14 CDI15 21E DIP1
CDI16 CDI17 CDI18 CDI19 CDI20 CDI21 CDI22 CDI23 26C DIP2
CDI24 CDI25 CDI26 CDI27 CDI28 CDI29 CDI30 CDI31 28D DIP3
(I)CSTR(n)0 Dc28
CP0 CP1 CP2 CP3 LS11 Db22 (I)CPE(n)0
CP0 CP1 CP2 CP3 1A 74S 174
Da28 Db27 Dc29 Da29 Da27 Dc27 Dc30
(I)XCP0 (I)XCP1 (I)XCP2 (I)XCP3
(I)CLEO Db30
CWS BS0 BS1 BS2 BS3 14H 74S 157 CWR0
15H CW0 CW1 CW2 CW3
(I)IRC0 (I)ORC0 (I)CWBC0 (I)MWBC0 (I)CWR0 (I)EN0 (I)CWS0 (I)ENMO0
Dc21 Da21 Dc20 Db20 Dc22 Da22 Dc23 Da23
3A 74S 244
IRC0 ORC0 CWBC0 MWBC0 CWR0 EN0 CWS0 ENMO0
2 R16 1K
n = 0,1,2,3 (Cache number)
(X) = 0 in data pos.
(X) = 1 in inst pos.
(H) = 1 in inst pos.
(I) = in data pos.
322507 G C
CORR ACCORD TO ECO 500-5, 500-7 02.12.80 BW
500-13, 500-21 12.03.81 AL
Corrected Date Sign.
Prod. no./ Serie 5007
Drawn AL 05.09.80
Check JH
Page 1 of 5
Replacement for
CACHE
NORSK DATA A.S Oslo, Norway
5B12
Replaced by

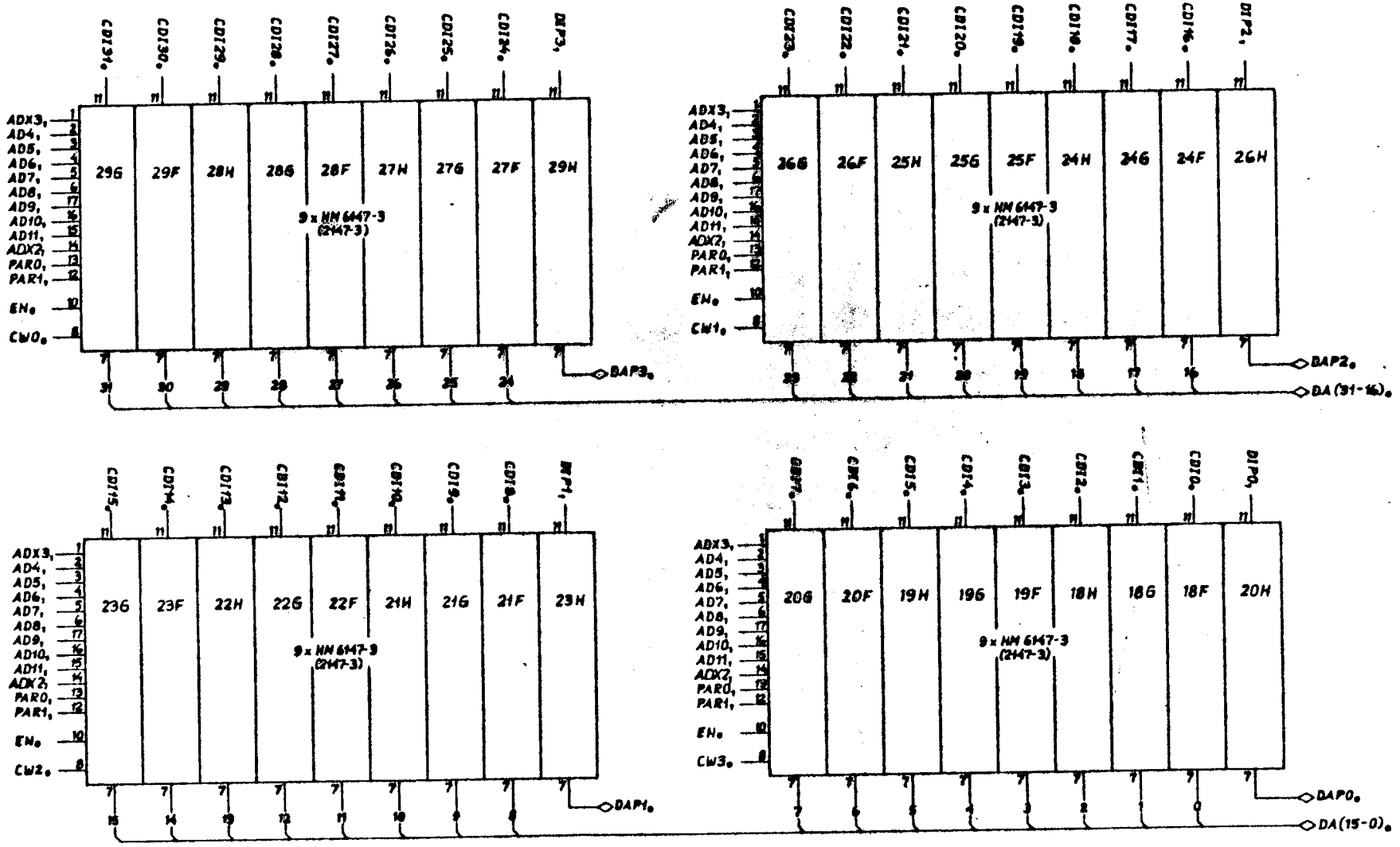


DD NO	CARD	PRINT	
322507	G	C	
CORR ACCORD TO ECO 500-5, 500-7, 500-13, 500-21	02/12/80	BW	
	12/03/81	AL	
Correction	Date	Sign	
CACHE	Print no / Scale: 5007	Drawn BW 05/09/80; Contr. JN	
	Page 2 of 5		
NORSK DATA A.S, Oslo, Norway	Replacement for: 5B13		
	Replaced by		

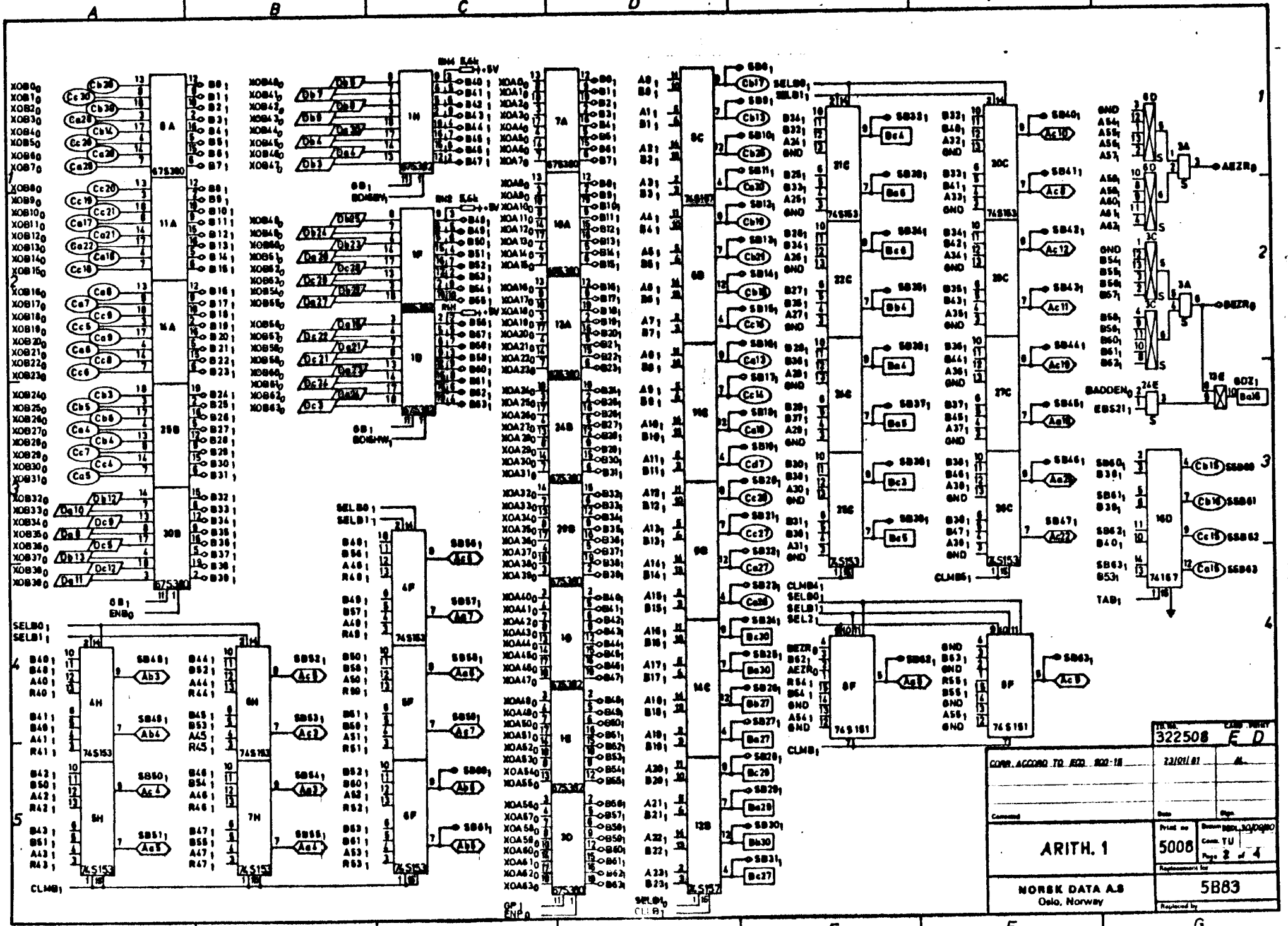

A
B
C
D
E
F
G
1
2
3
4
5
15A
4 x 120n
DWM1₁
MWD0₀
MWD1₀
MWD2₀
MWD4₀
ENMD₀
B0L₁
B0L₀
B1L₁
B1L₀
B2L₁
B2L₀
B3L₁
B3L₀
Ca1
Cc1
Ca2
Cc2
Ca3
Cc3
Ca4
Cc4
DI0₀
DI1₀
DI2₀
DI4₀
ME3₀
26LS31
26LS32
11A
DWM0₁
MWD16₀
MWD17₀
MWD18₀
MWD19
ENMD₀
B16L₁
B16L₀
B17L₁
B17L₀
B18L₁
B18L₀
B19L₁
B19L₀
Ca17
Cc17
Ca18
Cc18
Ca19
Cc19
Ca20
Cc20
DI16₀
DI17₀
DI18₀
DI19
ME1₀
6A
DWM1₀
MPW0₀
MPW1₀
ENMD₀
MPL0₁
MPL0₀
MPL1₁
MPL1₀
MPL2₁
MPL2₀
MPL3₁
MPL3₀
Da 3
Dc 3
Da 4
Dc 4
Da 10
Dc 10
Da 11
Dc 11
MP0₀
MP1₀
MP2₀
MP3₀
DWM0₀
MPW2₀
MPW3₀
ENMD₀
MPL2₁
MPL2₀
MPL3₁
MPL3₀
15A
DWM1₁
MWD4₀
MWD5₀
MWD6₀
MWD7₀
ENMD₀
B4L₁
B4L₀
B5L₁
B5L₀
B6L₁
B6L₀
B7L₁
B7L₀
Ca5
Cc5
Ca6
Cc6
Ca7
Cc7
Ca8
Cc8
DI4₀
DI5₀
DI6₀
DI7₀
ME3₀
11A
DWM0₁
MWD20₀
MWD21₀
MWD22₀
MWD23₀
ENMD₀
B20L₁
B20L₀
B21L₁
B21L₀
B22L₁
B22L₀
B23L₁
B23L₀
Ca21
Cc21
Ca22
Cc22
Ca23
Cc23
Ca24
Cc24
DI20₀
DI21₀
DI22₀
DI23₀
ME1₀
3x220n
RN2
RN1
Da 7
Dc 7
R7
6B
Db 3
[I]DRQ(2n+1)₀
LBC1₀
Db 15
5A
Da 9
Dc 9
Da 14
Dc 14
R8
Db 11
[I]DRQ(2n)₀
LBC0₀
Db 12
Da 16
Dc 16
WM1₁
7A
Da 6
Dc 6
Da 8
Dc 8
R9
Db 4
MAR1₀
WM0₁
Da 13
Dc 13
Da 15
Dc 15
R10
Db 5
MAR0₀
[I]REQ(2n+1)₀
Bb 30
Da 5
Dc 5
[I]WR(2n+1)₀
Db 21
3C
WM1₁
[I]REQ(2n)₀
Bb 29
Da 12
Dc 12
[I]WR(2n)₀
Da 18
WM0₁
WM1₁
WM0₁
DWM1₁
DWM0₁
560pF
500pF
LS
8B
13A
DWM1₁
MWD8₀
MWD9₀
MWD10₀
MWD11₀
ENMD₀
B8L₁
B8L₀
B9L₁
B9L₀
B10L₁
B10L₀
B11L₁
B11L₀
Ca9
Cc9
Ca10
Cc10
Ca11
Cc11
Ca12
Cc12
DI8₀
DI9₀
DI10₀
DI11₀
ME2₀
9A
DWM0₁
MWD24₀
MWD25₀
MWD26₀
MWD27₀
ENMD₀
B24L₁
B24L₀
B25L₁
B25L₀
B26L₁
B26L₀
B27L₁
B27L₀
Ca25
Cc25
Ca26
Cc26
Ca27
Cc27
Ca28
Cc28
DI24₀
DI25₀
DI26₀
DI27₀
ME0₀
13A
DWM1₁
MWD12₀
MWD13₀
MWD14₀
MWD15₀
ENMD₀
B12L₁
B12L₀
B13L₁
B13L₀
B14L₁
B14L₀
B15L₁
B15L₀
Ca13
Cc13
Ca14
Cc14
Ca15
Cc15
Ca16
Cc16
DI12₀
DI13₀
DI14₀
DI15₀
ME2₀
9A
DWM0₁
MWD28₀
MWD29₀
MWD30₀
MWD31₀
ENMD₀
B28L₁
B28L₀
B29L₁
B29L₀
B30L₁
B30L₀
B31L₁
B31L₀
Ca29
Cc29
Ca30
Cc31
Ca31
Cc31
Ca32
Cc32
DI28₀
DI29₀
DI30₀
DI31₀
ME0₀
TR NO. 322507 G C
CARD PRINT
CORR ACCORD TO ECO 500-5, 500-3, 500-13, 500-21
02/12/80 BW
12/03/81 AL
Corrected
Date
Sign
CACHE
Print no 5007
Drawn Tomasica 05.09.80
Cont JH
Page 3 of 5
Replacement for
NORSK DATA A.S
Oslo, Norway
5B14
Replaced by



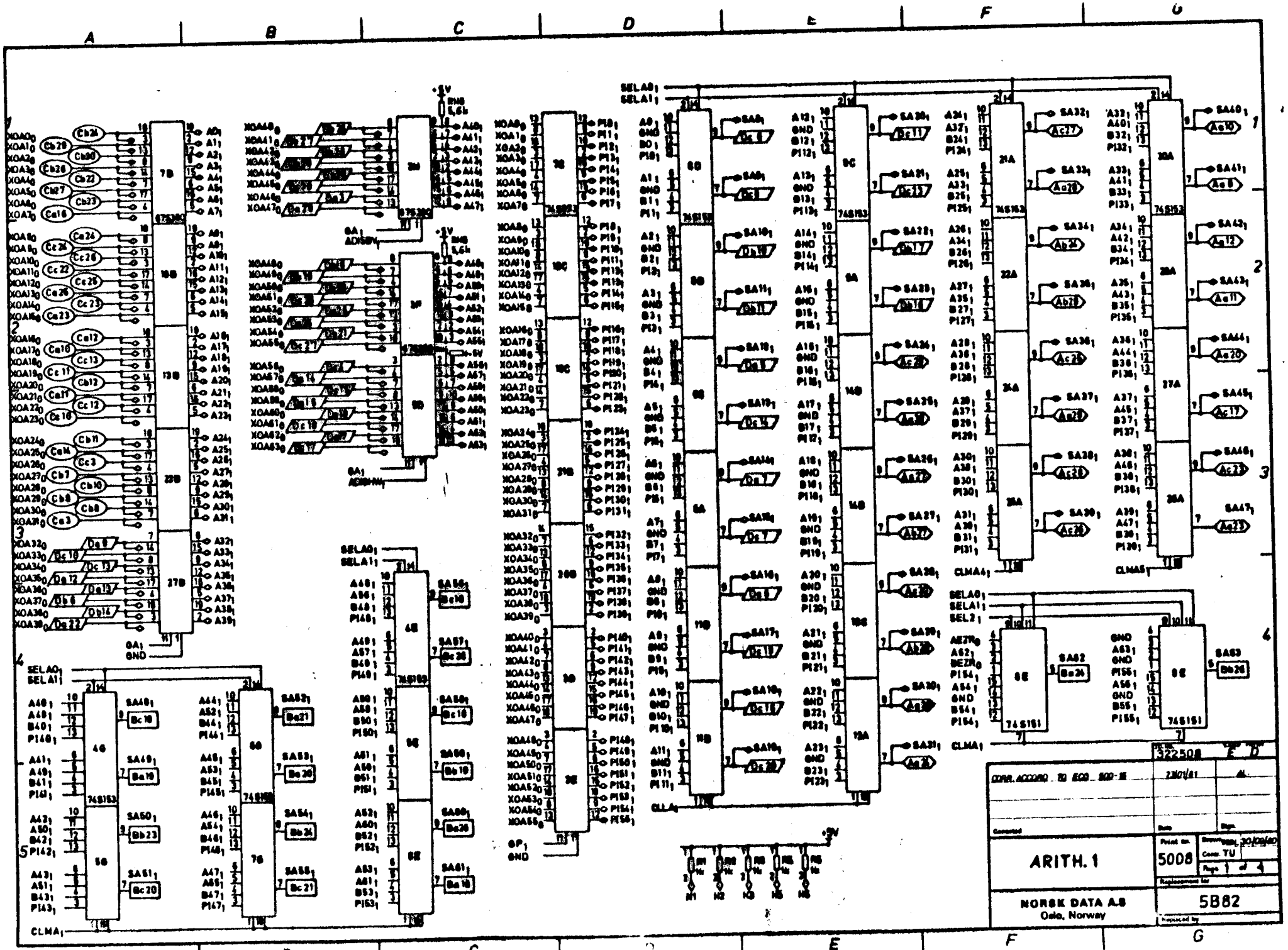
		TECHN.	CARD PRINT
		322507	G C
CORR. ACCORD. TO ECO 500-5, 500-7	02/12/80	BW	
509-13, 500-21	12/03/81	AL	
Comment	Date	Sign	
CACHE	Print no. 5007	Drawn Check DE 06.80 Conn JH Page 4 of 5	
	Replacement for		
NORSK DATA A.S Oslo, Norway	5B15		
	Replaced by		

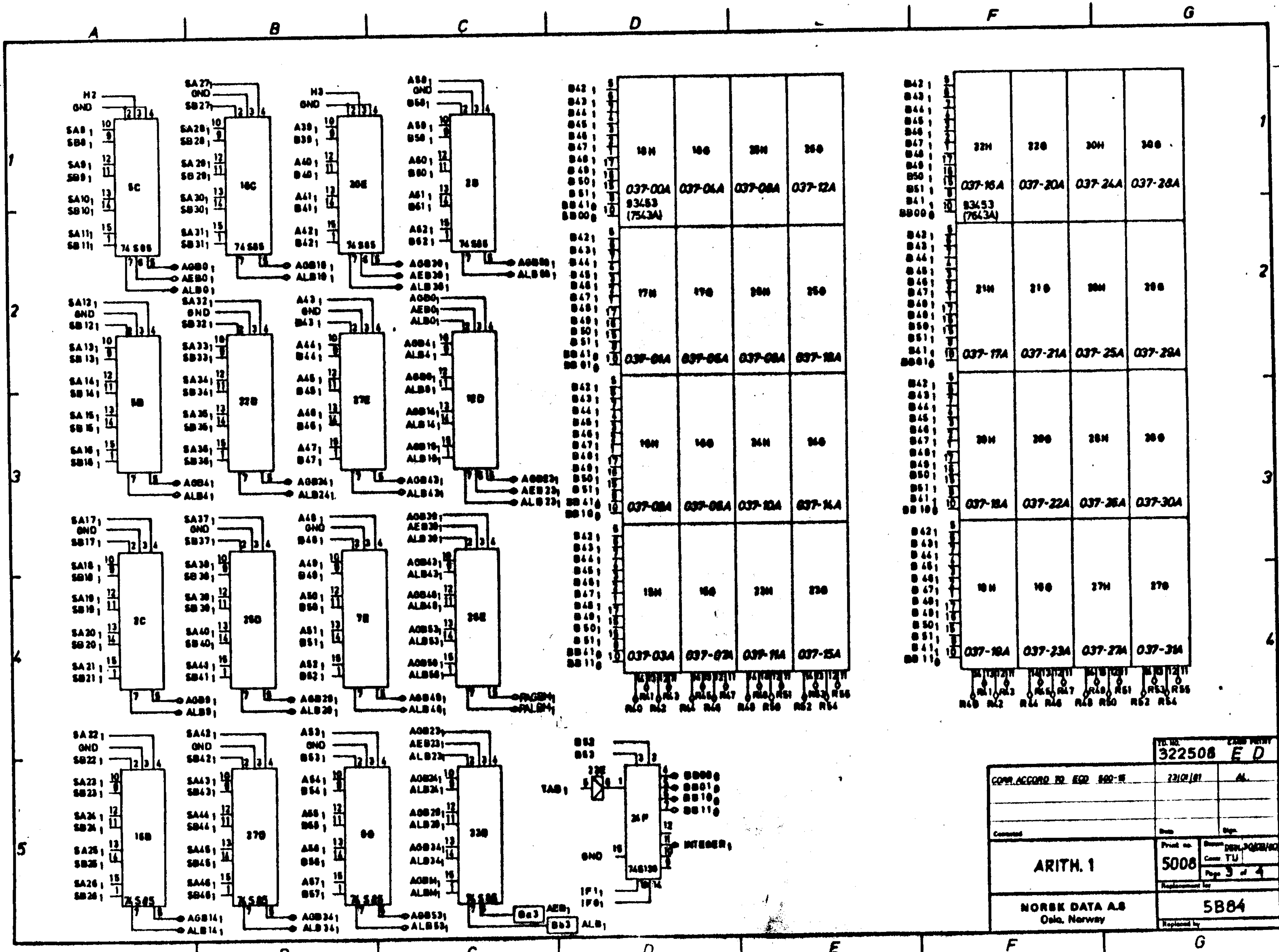


TS. NR. 322507	CARD PRINT G C		
CORR ACCORD TO ECO 500-5, 500-7, 500-13, 500-71	02/12/80 12/03/81	BW AL	
Constructed	Date	Sign	
CACHE	Print no 5007	Drawn BW 05.09.80 Contr JH	Page 5 of 5
NORSK DATA A.S Oslo, Norway	Replacement for 5B69		
	Registered by		

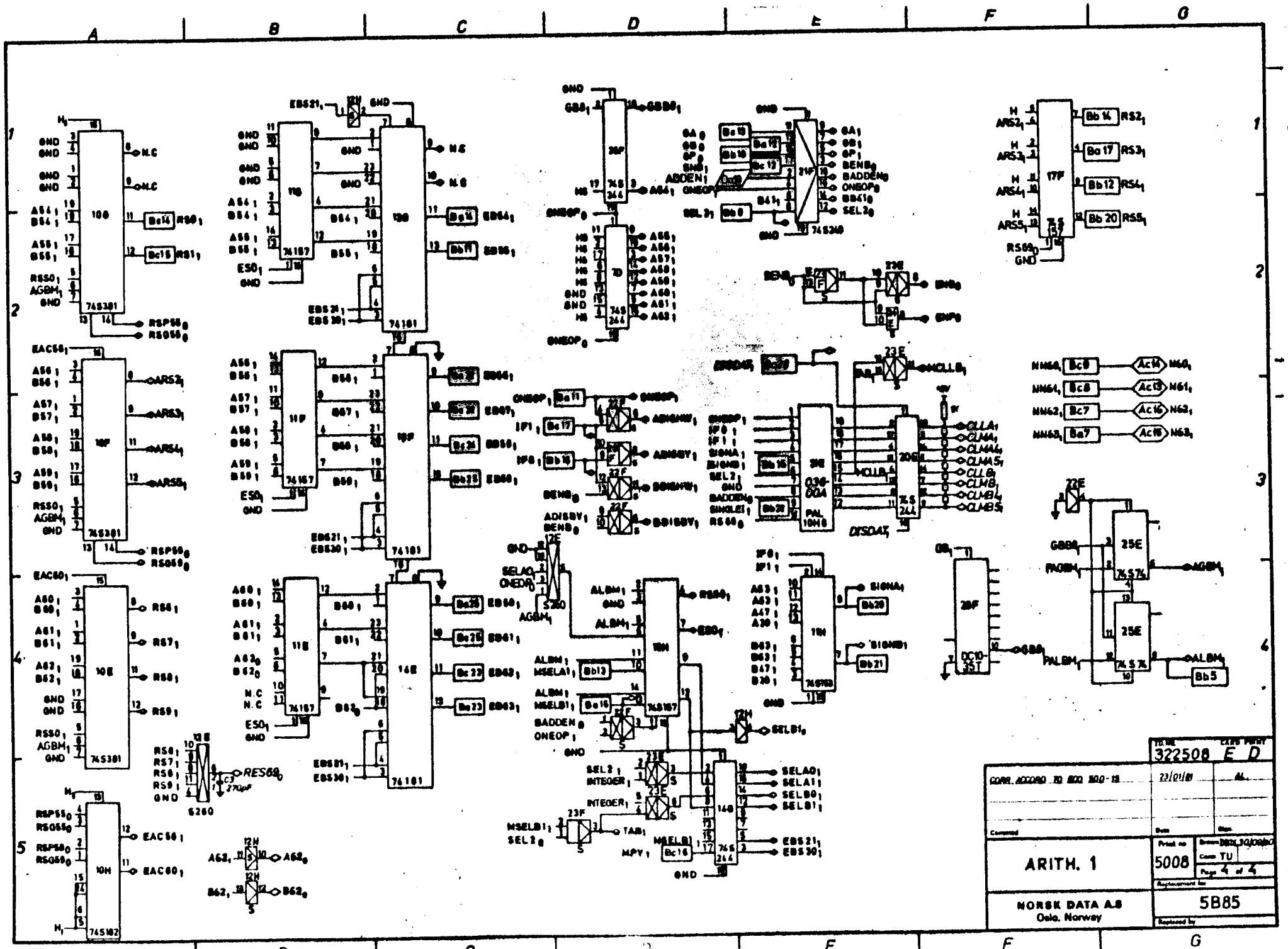


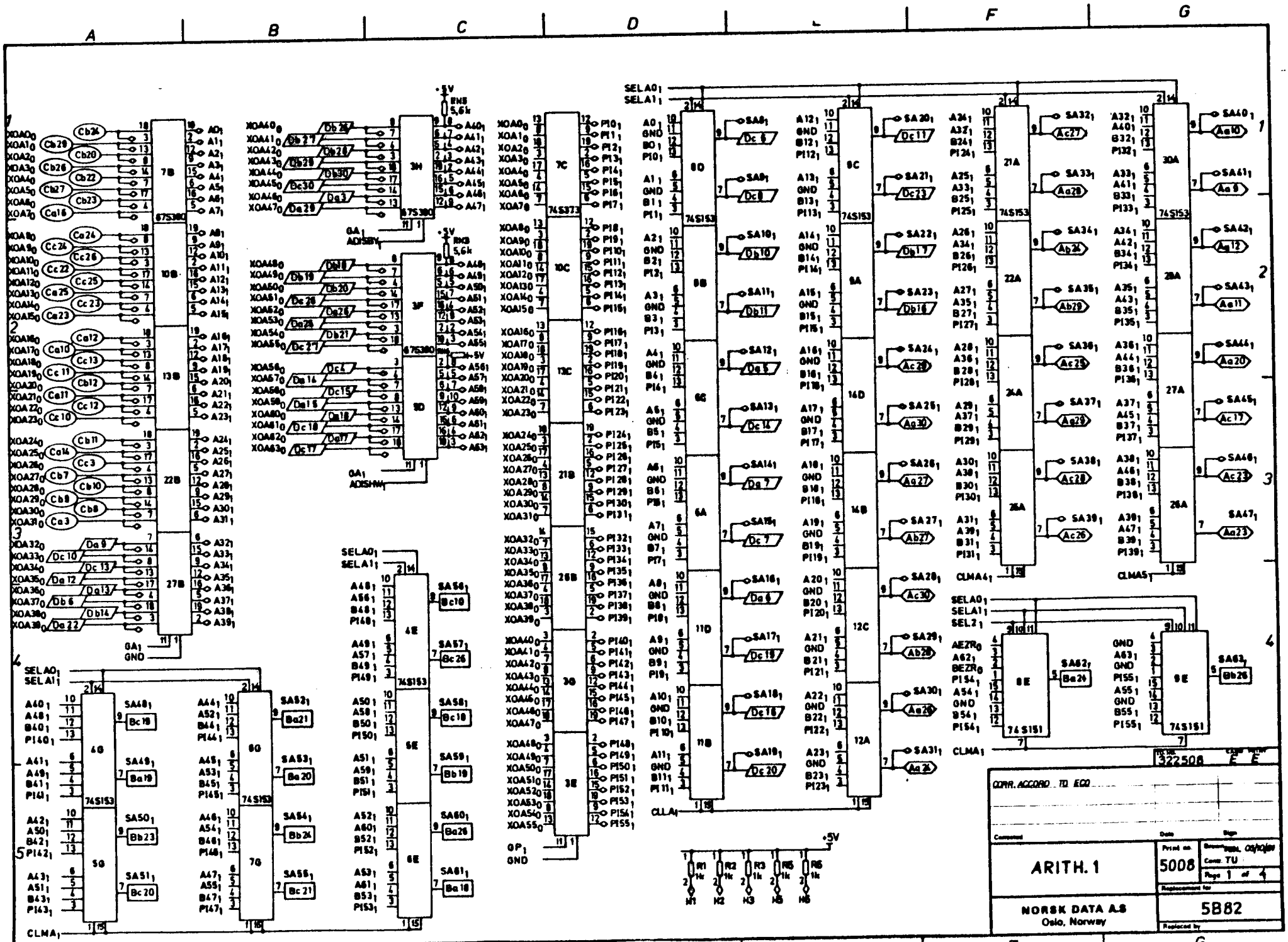
TEK NR	322508
CORR. ACCORD TO ISO 102-18	23/01/81
Comment	Date / Sign
ARITH. 1	Print no 5008
NORSK DATA A.S Oslo, Norway	5B83

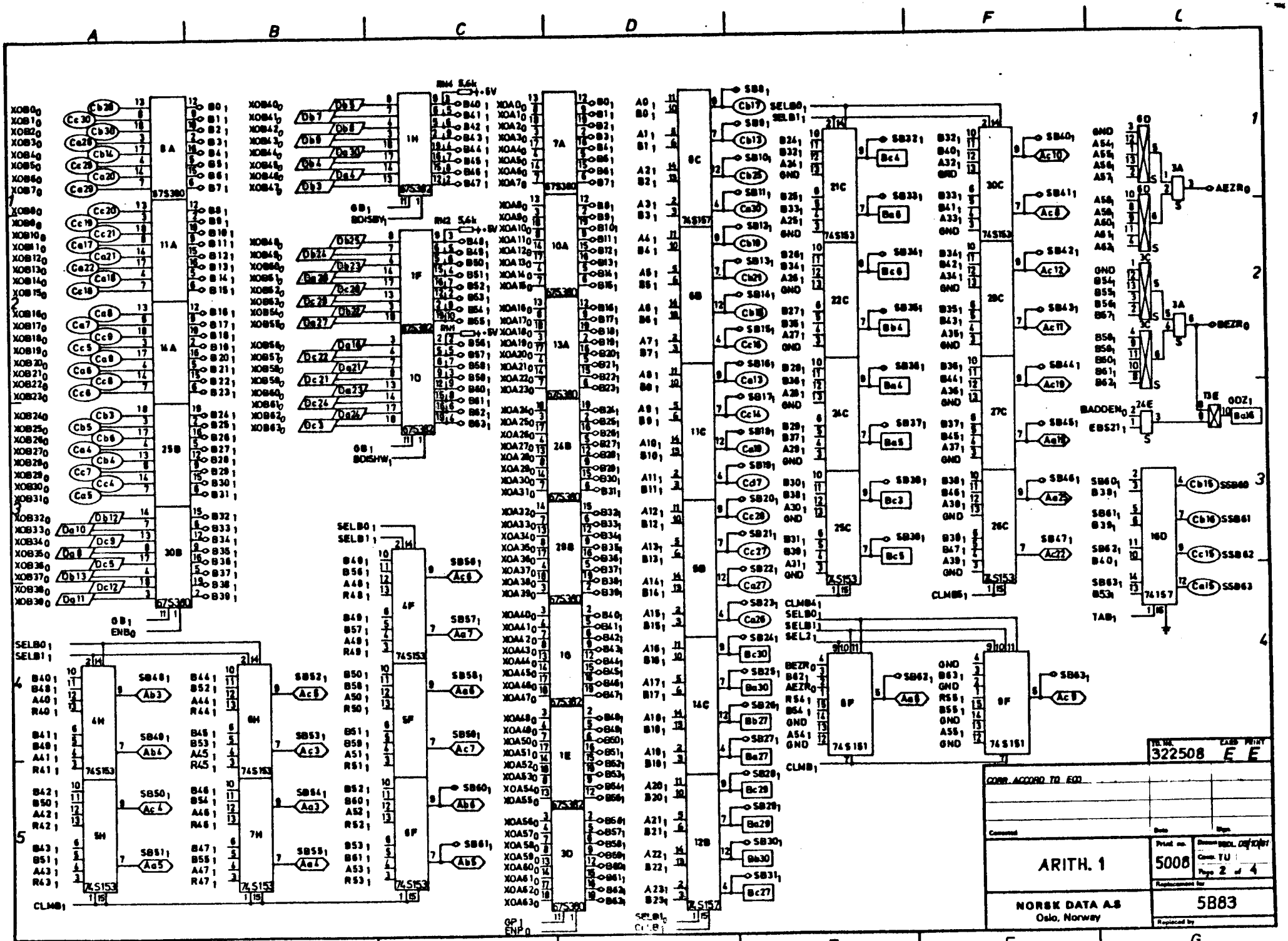

ARITH. 1
NORSK DATA A.S
Oslo, Norway
5008
5882
322508
CORR. ACCORD. TO ECO - 800 - 16
23/01/81
Drawn TU
30/09/80
Page 1 of 4
Replacement for
Replaced by
74S153
74S151
74S157
74S158
CLMA1
CLMA2
CLMA3
CLMA4
SELA0
SELA1
SEL2
GND
+5V

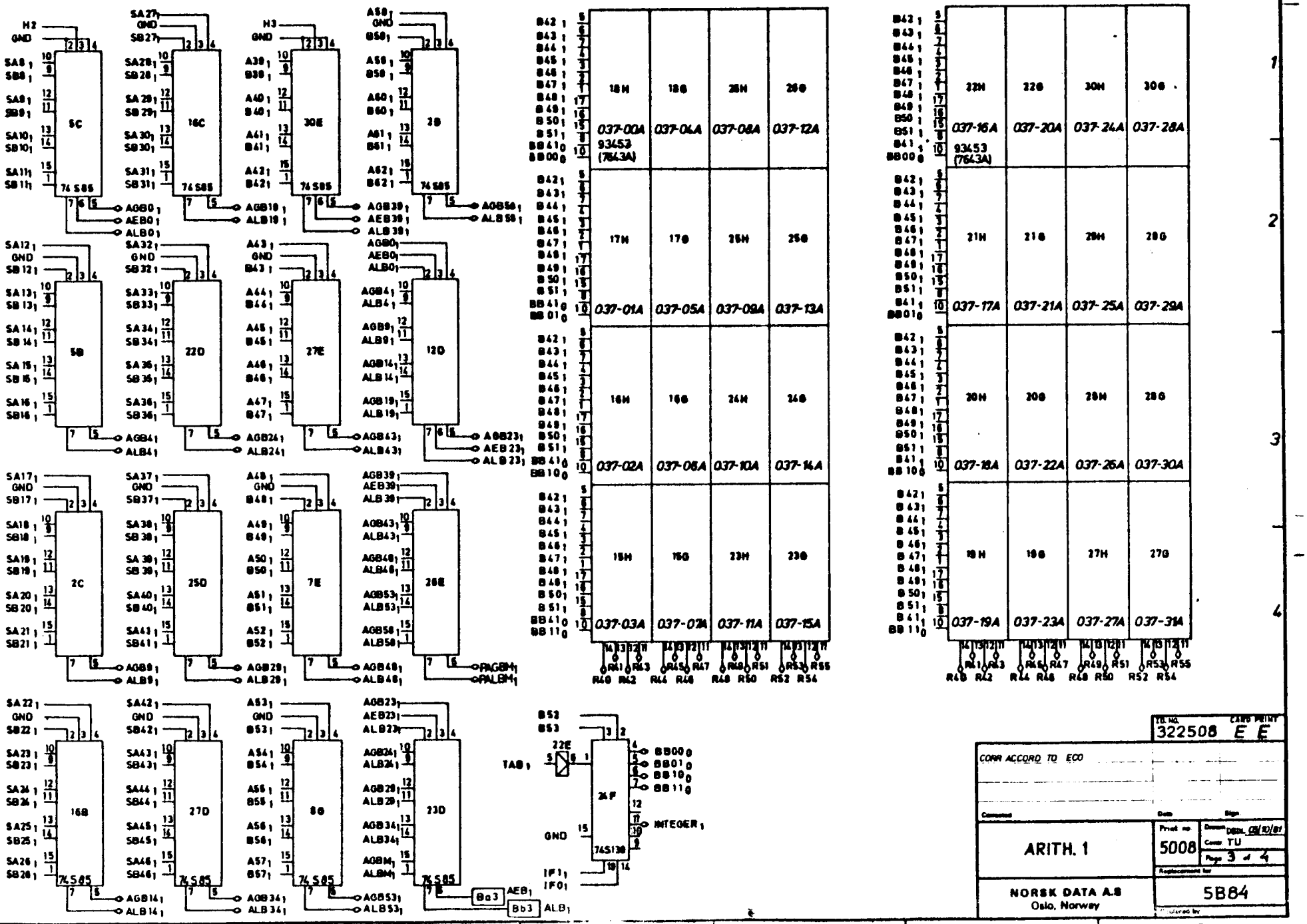


322508 E D
COPR.ACCORD TO ECO 800-15
23/01/81
ARITH. 1
5008
NORSK DATA A.S
Oslo, Norway
5B84

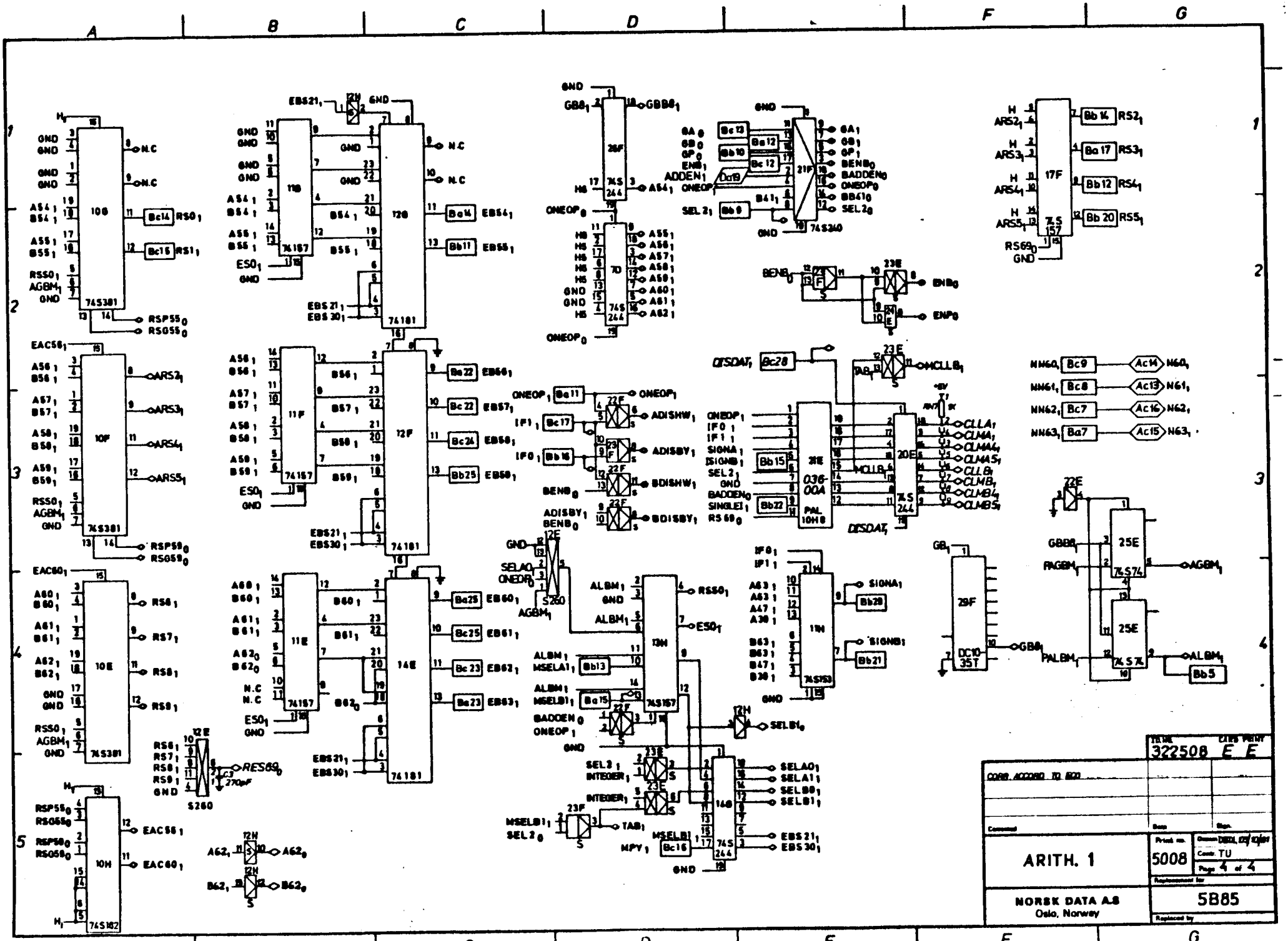

ARITH. 1
NORSK DATA A.S
Oslo. Norway
5008
5B85
322508 E D
23/01/81
TU
Page 4 of 4
74S381
74S181
74S167
74S260
74S162
74S244
74S240
74S153
74S74
PAL 10H8
RES68
C3 270pF

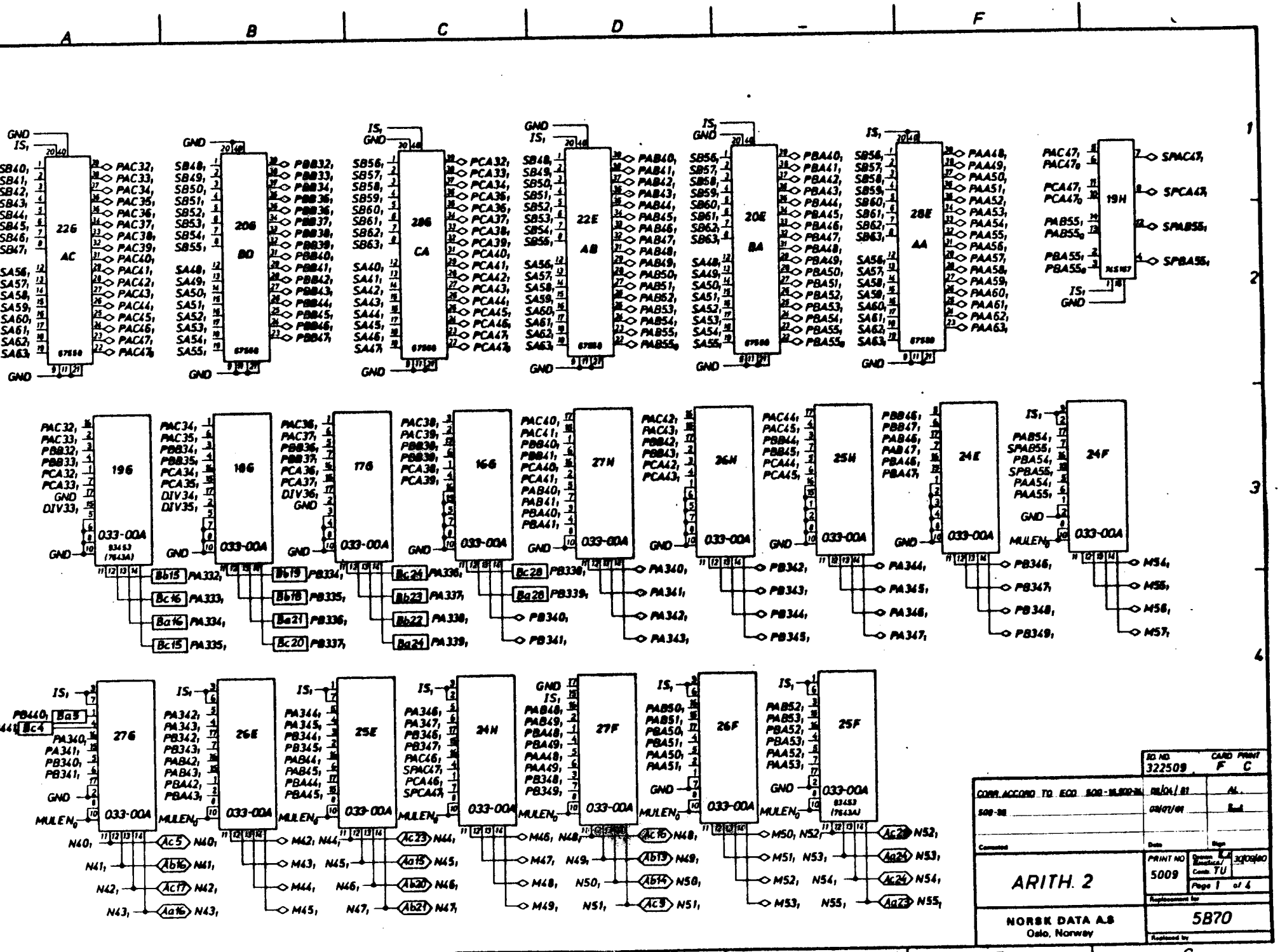

ARITH. 1
NORSK DATA A.S
Oslo, Norway
5008
5882
322508
CORR. ACCORD. TO ECO
Page 1 of 4
74S153
74S373
74S151
675380

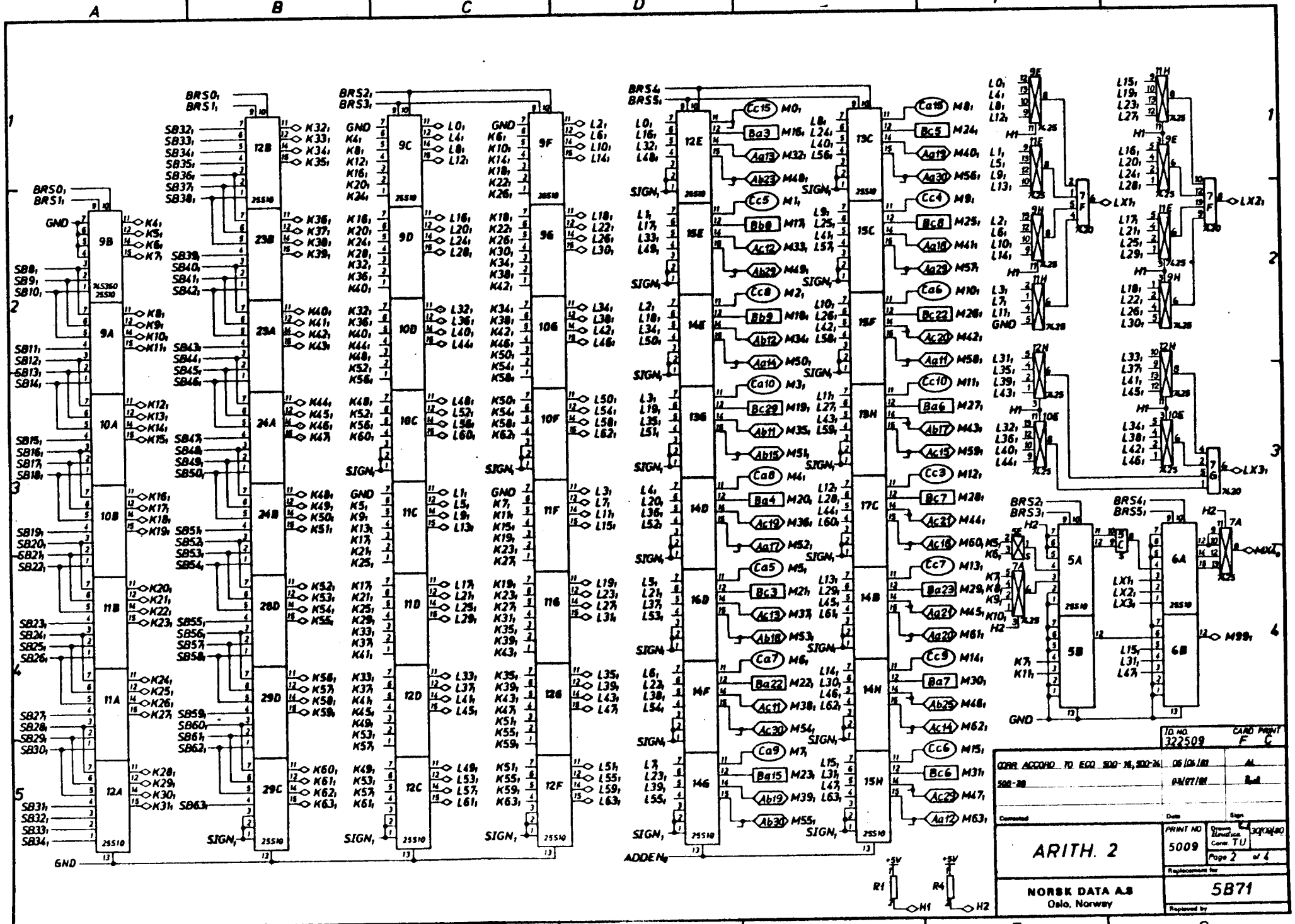

ARITH. 1
322508
5008
5883
NORSK DATA A.S
Oslo, Norway
Print no.
Replacement for
Replaced by
Page 2 of 4
CORR. ACCORD TO ECO
Comment
Date
Sign.
74S153
74S157
74S181
74S151
8A
11A
14A
25B
30B
1H
1F
1D
7A
10A
13A
24B
29B
1B
1E
3D
8C
11C
14C
12B
21C
22C
24C
25C
30C
29C
27C
26C
8F
9F
16D
3A
24E
13E
00Z1
4F
5F
6F
4H
5H
6H
7H

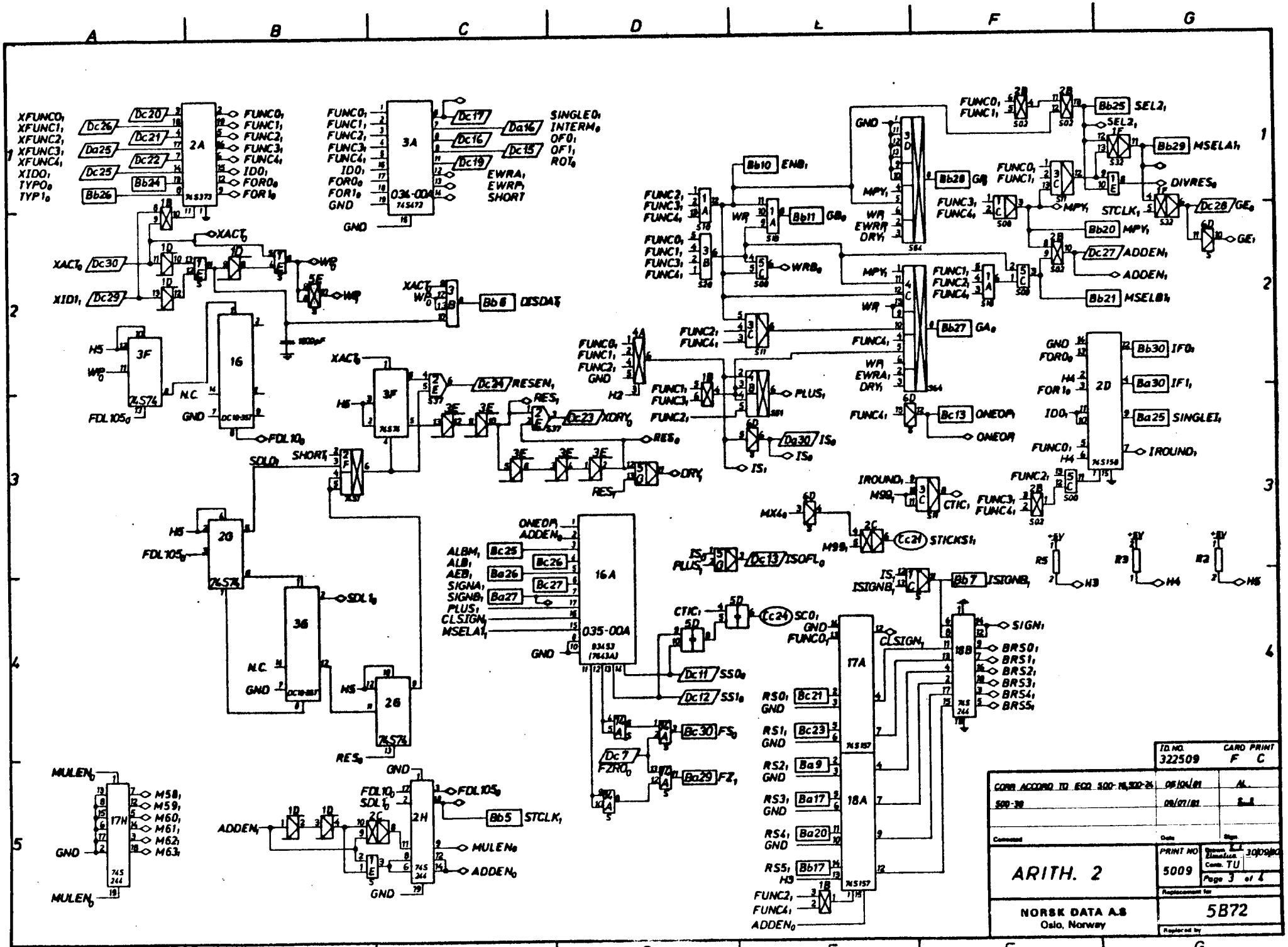


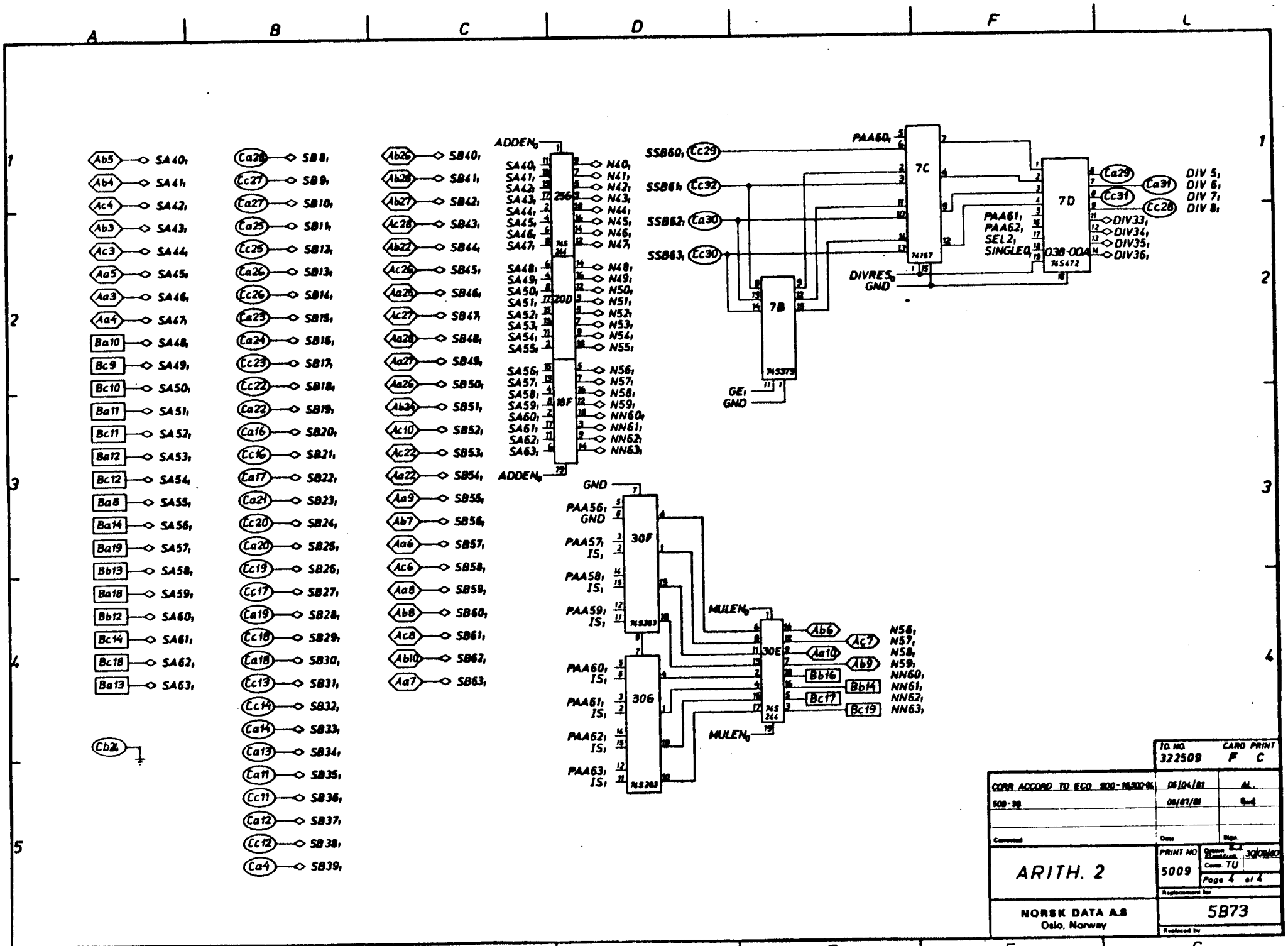
TD. NO. 322508	CARD PRINT E E
CORR ACCORD TO ECO	
Checked / Date / Sign	
ARITH. 1	Print no. 5008
	Drawn DBSK 08/10/81
	Check TU
	Page 3 of 4
	Replacement for
NORSK DATA A.S Oslo, Norway	5B84
	Approved by

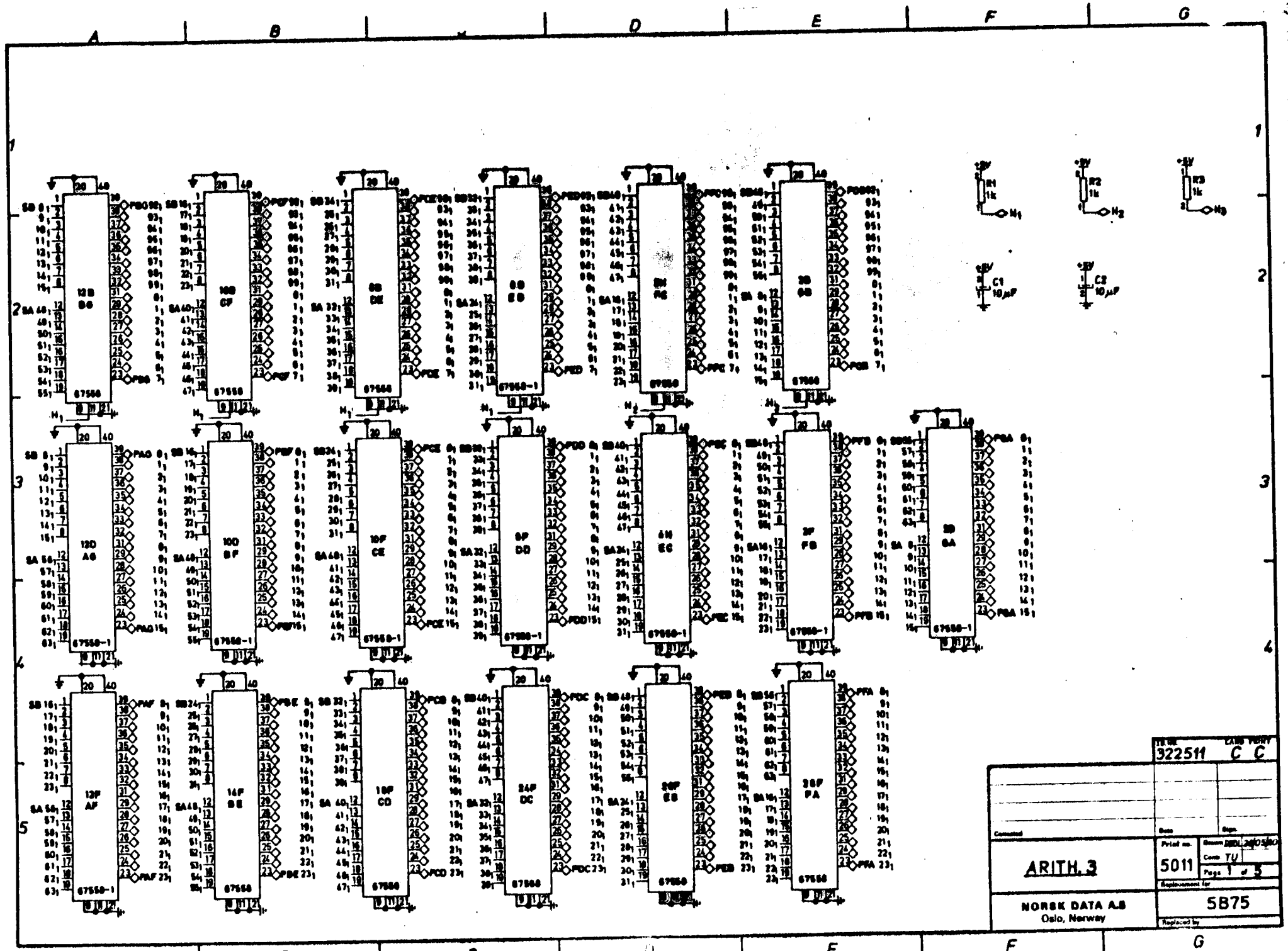

ARITH. 1
NORSK DATA A.S
Oslo, Norway
322508 E E
5008
5B85
Page 4 of 4
74S381
74S157
74S244
74S240
74S260
74S162
74S74
74S153
74S197
74S181
74S86
74S00
74S04
74S08
74S32
74S10
74S20
74S30
74S51
74S64
74S74
74S86
74S112
74S138
74S139
74S151
74S153
74S157
74S158
74S161
74S162
74S163
74S174
74S175
74S181
74S182
74S189
74S194
74S195
74S196
74S197
74S240
74S241
74S244
74S251
74S253
74S257
74S258
74S260
74S273
74S280
74S283
74S287
74S288
74S289
74S299
74S373
74S374
74S377
74S378
74S379
74S381
74S382
74S387
74S399
74S412
74S414
74S415
74S416
74S417
74S418
74S419
74S420
74S421
74S422
74S423
74S424
74S425
74S426
74S427
74S428
74S429
74S430
74S431
74S432
74S433
74S434
74S435
74S436
74S437
74S438
74S439
74S440
74S441
74S442
74S443
74S444
74S445
74S446
74S447
74S448
74S449
74S450
74S451
74S452
74S453
74S454
74S455
74S456
74S457
74S458
74S459
74S460
74S461
74S462
74S463
74S464
74S465
74S466
74S467
74S468
74S469
74S470
74S471
74S472
74S473
74S474
74S475
74S476
74S477
74S478
74S479
74S480
74S481
74S482
74S483
74S484
74S485
74S486
74S487
74S488
74S489
74S490
74S491
74S492
74S493
74S494
74S495
74S496
74S497
74S498
74S499
74S500
74S501
74S502
74S503
74S504
74S505
74S506
74S507
74S508
74S509
74S510
74S511
74S512
74S513
74S514
74S515
74S516
74S517
74S518
74S519
74S520
74S521
74S522
74S523
74S524
74S525
74S526
74S527
74S528
74S529
74S530
74S531
74S532
74S533
74S534
74S535
74S536
74S537
74S538
74S539
74S540
74S541
74S542
74S543
74S544
74S545
74S546
74S547
74S548
74S549
74S550
74S551
74S552
74S553
74S554
74S555
74S556
74S557
74S558
74S559
74S560
74S561
74S562
74S563
74S564
74S565
74S566
74S567
74S568
74S569
74S570
74S571
74S572
74S573
74S574
74S575
74S576
74S577
74S578
74S579
74S580
74S581
74S582
74S583
74S584
74S585
74S586
74S587
74S588
74S589
74S590
74S591
74S592
74S593
74S594
74S595
74S596
74S597
74S598
74S599
74S600
74S601
74S602
74S603
74S604
74S605
74S606
74S607
74S608
74S609
74S610
74S611
74S612
74S613
74S614
74S615
74S616
74S617
74S618
74S619
74S620
74S621
74S622
74S623
74S624
74S625
74S626
74S627
74S628
74S629
74S630
74S631
74S632
74S633
74S634
74S635
74S636
74S637
74S638
74S639
74S640
74S641
74S642
74S643
74S644
74S645
74S646
74S647
74S648
74S649
74S650
74S651
74S652
74S653
74S654
74S655
74S656
74S657
74S658
74S659
74S660
74S661
74S662
74S663
74S664
74S665
74S666
74S667
74S668
74S669
74S670
74S671
74S672
74S673
74S674
74S675
74S676
74S677
74S678
74S679
74S680
74S681
74S682
74S683
74S684
74S685
74S686
74S687
74S688
74S689
74S690
74S691
74S692
74S693
74S694
74S695
74S696
74S697
74S698
74S699
74S700
74S701
74S702
74S703
74S704
74S705
74S706
74S707
74S708
74S709
74S710
74S711
74S712
74S713
74S714
74S715
74S716
74S717
74S718
74S719
74S720
74S721
74S722
74S723
74S724
74S725
74S726
74S727
74S728
74S729
74S730
74S731
74S732
74S733
74S734
74S735
74S736
74S737
74S738
74S739
74S740
74S741
74S742
74S743
74S744
74S745
74S746
74S747
74S748
74S749
74S750
74S751
74S752
74S753
74S754
74S755
74S756
74S757
74S758
74S759
74S760
74S761
74S762
74S763
74S764
74S765
74S766
74S767
74S768
74S769
74S770
74S771
74S772
74S773
74S774
74S775
74S776
74S777
74S778
74S779
74S780
74S781
74S782
74S783
74S784
74S785
74S786
74S787
74S788
74S789
74S790
74S791
74S792
74S793
74S794
74S795
74S796
74S797
74S798
74S799
74S800
74S801
74S802
74S803
74S804
74S805
74S806
74S807
74S808
74S809
74S810
74S811
74S812
74S813
74S814
74S815
74S816
74S817
74S818
74S819
74S820
74S821
74S822
74S823
74S824
74S825
74S826
74S827
74S828
74S829
74S830
74S831
74S832
74S833
74S834
74S835
74S836
74S837
74S838
74S839
74S840
74S841
74S842
74S843
74S844
74S845
74S846
74S847
74S848
74S849
74S850
74S851
74S852
74S853
74S854
74S855
74S856
74S857
74S858
74S859
74S860
74S861
74S862
74S863
74S864
74S865
74S866
74S867
74S868
74S869
74S870
74S871
74S872
74S873
74S874
74S875
74S876
74S877
74S878
74S879
74S880
74S881
74S882
74S883
74S884
74S885
74S886
74S887
74S888
74S889
74S890
74S891
74S892
74S893
74S894
74S895
74S896
74S897
74S898
74S899
74S900
74S901
74S902
74S903
74S904
74S905
74S906
74S907
74S908
74S909
74S910
74S911
74S912
74S913
74S914
74S915
74S916
74S917
74S918
74S919
74S920
74S921
74S922
74S923
74S924
74S925
74S926
74S927
74S928
74S929
74S930
74S931
74S932
74S933
74S934
74S935
74S936
74S937
74S938
74S939
74S940
74S941
74S942
74S943
74S944
74S945
74S946
74S947
74S948
74S949
74S950
74S951
74S952
74S953
74S954
74S955
74S956
74S957
74S958
74S959
74S960
74S961
74S962
74S963
74S964
74S965
74S966
74S967
74S968
74S969
74S970
74S971
74S972
74S973
74S974
74S975
74S976
74S977
74S978
74S979
74S980
74S981
74S982
74S983
74S984
74S985
74S986
74S987
74S988
74S989
74S990
74S991
74S992
74S993
74S994
74S995
74S996
74S997
74S998
74S999
74S1000

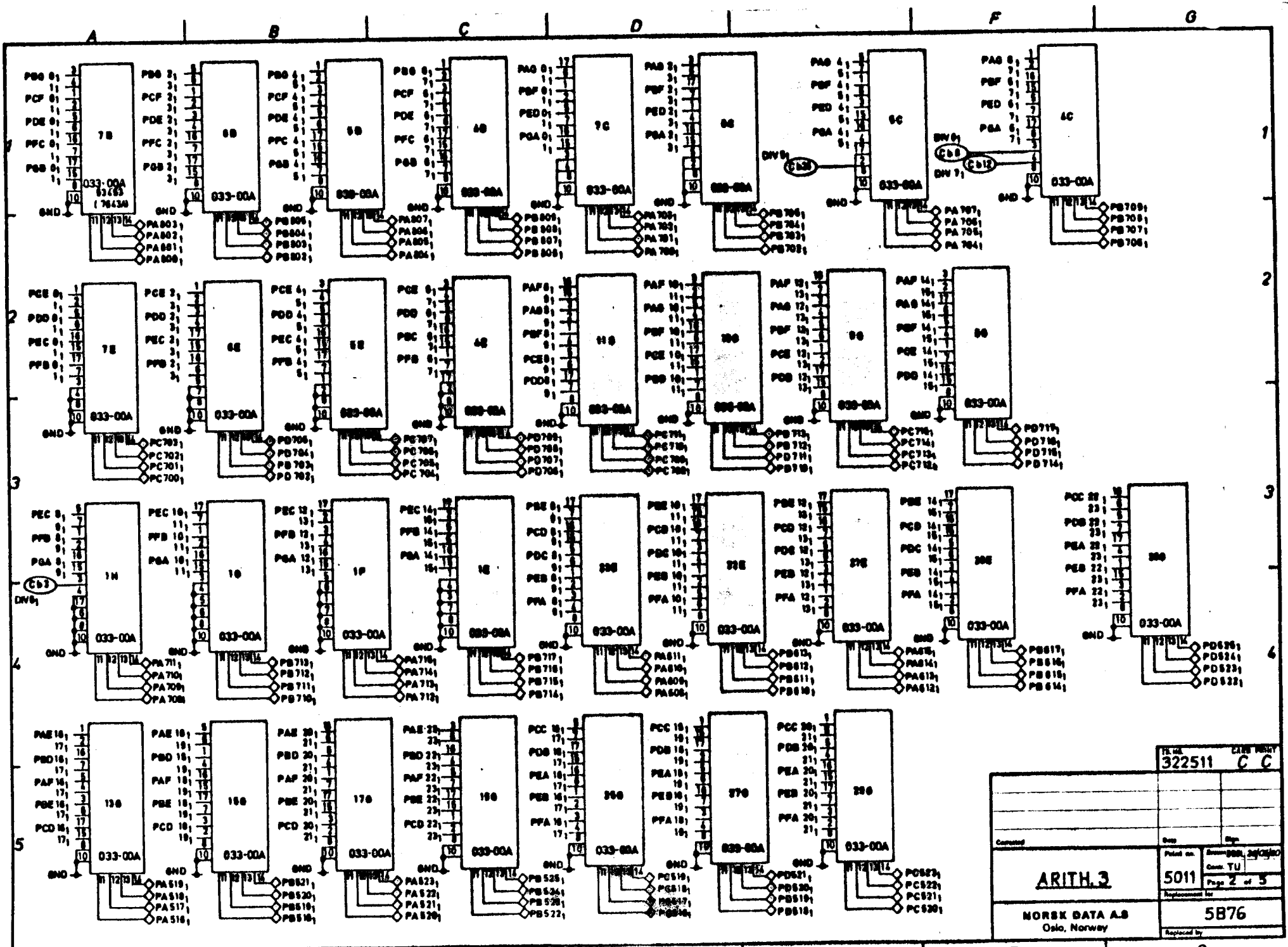

A
B
C
D
F
1
2
3
4
5
GND
IS
SB40 SB41 SB42 SB43 SB44 SB45 SB46 SB47
SA56 SA57 SA58 SA59 SA60 SA61 SA62 SA63
226 AC
PAC32 PAC33 PAC34 PAC35 PAC36 PAC37 PAC38 PAC39 PAC40 PAC41 PAC42 PAC43 PAC44 PAC45 PAC46 PAC47
208 BD
PBB32 PBB33 PBB34 PBB35 PBB36 PBB37 PBB38 PBB39 PBB40 PBB41 PBB42 PBB43 PBB44 PBB45 PBB46 PBB47
SB48 SB49 SB50 SB51 SB52 SB53 SB54 SB55
SA48 SA49 SA50 SA51 SA52 SA53 SA54 SA55
286 CA
PCA32 PCA33 PCA34 PCA35 PCA36 PCA37 PCA38 PCA39 PCA40 PCA41 PCA42 PCA43 PCA44 PCA45 PCA46 PCA47
SB56 SB57 SB58 SB59 SB60 SB61 SB62 SB63
SA40 SA41 SA42 SA43 SA44 SA45 SA46 SA47
22E AB
PAB40 PAB41 PAB42 PAB43 PAB44 PAB45 PAB46 PAB47 PAB48 PAB49 PAB50 PAB51 PAB52 PAB53 PAB54 PAB55
20E BA
PBA40 PBA41 PBA42 PBA43 PBA44 PBA45 PBA46 PBA47 PBA48 PBA49 PBA50 PBA51 PBA52 PBA53 PBA54 PBA55
28E AA
PAA48 PAA49 PAA50 PAA51 PAA52 PAA53 PAA54 PAA55 PAA56 PAA57 PAA58 PAA59 PAA60 PAA61 PAA62 PAA63
PAC47 PAC47 PCA47 PCA47 PAB55 PAB55 PBA55 PBA55
19H
SPAC47 SPCA47 SPAB55 SPBA55
PAC32 PAC33 PBB32 PBB33 PCA32 GND DIV33
196
033-00A
PAC34 PAC35 PBB34 PBB35 PCA34 PCA35 DIV34 DIV35
186
PAC36 PAC37 PBB36 PBB37 PCA36 PCA37 DIV36 GND
176
PAC38 PAC39 PBB38 PBB39 PCA38 PCA39
166
PAC40 PAC41 PBB40 PBB41 PCA40 PCA41 PAB40 PAB41 PBA40 PBA41
27H
PAC42 PAC43 PBB42 PBB43 PCA42 PCA43
26H
PAC44 PAC45 PBB44 PBB45 PCA44 PCA45
25H
PBB46 PBB47 PAB46 PAB47 PBA46 PBA47
24E
PAB54 SPAB55 PBA54 SPBA55 PAA54 PAA55
MULEN0
24F
Bb15 Bc16 Ba16 Bc15 PA332 PA333 PA334 PA335
Bb19 Bb18 Ba21 Bc20 PB334 PB335 PB336 PB337
Bc24 Bb23 Bb22 Ba24 PA336 PA337 PA338 PA339
Bc28 Ba28 PB338 PB339 PB340 PB341
PA340 PA341 PA342 PA343
PB342 PB343 PB344 PB345
PA344 PA345 PA348 PA347
PB346 PB347 PB348 PB349
M54 M55 M56 M57
PB440 Ba5 PB441 Bc4
276
PA340 PA341 PB340 PB341
PA342 PA343 PB342 PB343 PAB42 PAB43 PBA42 PBA43
26E
PA344 PA345 PB344 PB345 PAB44 PAB45 PBA44 PBA45
25E
PA346 PA347 PB346 PB347 PAC46 SPAC47 PCA46 SPCA47
24H
PAB48 PAB49 PBA48 PBA49 PAA48 PAA49 PB348 PB349
27F
PAB50 PAB51 PBA50 PBA51 PAA50 PAA51
26F
PAB52 PAB53 PBA52 PBA53 PAA52 PAA53
25F
N40 N41 N42 N43
Ac5 Ab16 Ac17 Aa16
N42 N44 N43 N45 N44 N46 N45 N47
M46 M48 M47 N49 M48 N50 M49 N51
Ac16 Ab19 Ab14 Ac9
M50 N52 M51 N53 M52 N54 M53 N55
Ac23 Aa15 Ab20 Ab21
Ac28 Aa24 Ac24 Aa23
N40 N41 N42 N43 N44 N45 N46 N47 N48 N49 N50 N51 N52 N53 N54 N55
BD NO 322509
CARD PRINT F C
CORR ACCORD TO ECO 500-16,820-16
RELEASE / 81
500-98
Comment
Date
Page
PRINT NO 5009
Drawn Checked / Comp TU
Page 1 of 4
ARITH. 2
NORSK DATA A.S
Oslo, Norway
Replacement for 5B70
Replaced by

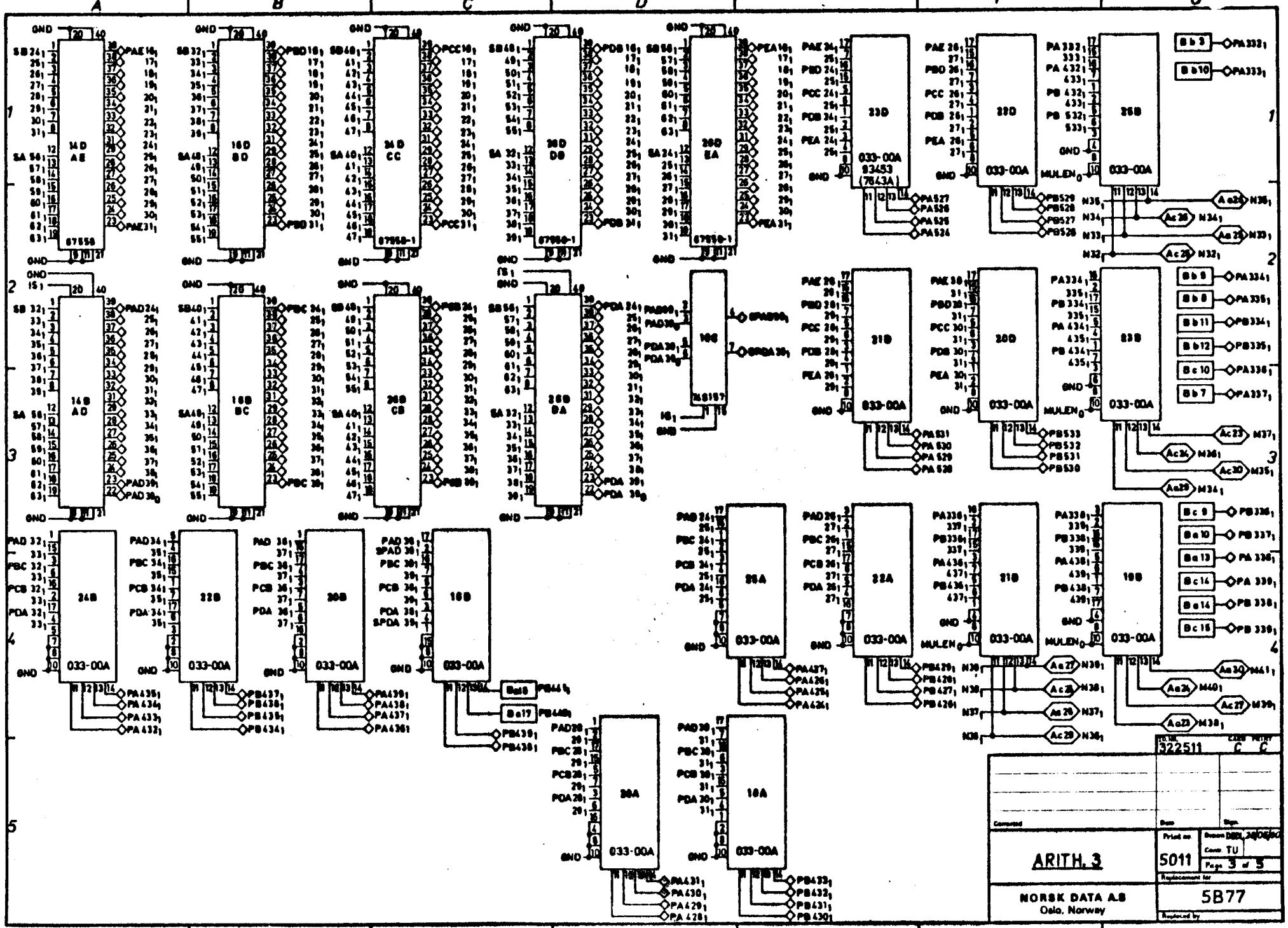

ARITH. 2
NORSK DATA A.S
Oslo, Norway
PRINT NO 5009
Page 2 of 4
5B71
TD NO 322509
CARD PRINT F C
CORR ACCORD TO ECO 500-16, 500-26 05/05/81 AL
500-28 03/07/81 Bod
Comment Date Sign
Replacement for
Replaced by
12E
15E
14E
14D
16D
14F
14G
12A
9B
9A
10A
10B
11B
11A
12B
23B
23A
24A
24B
28D
29D
29C
9C
9D
10D
10C
11C
11D
12D
12C
9F
9G
10G
10F
11F
11G
12F
13C
15C
15F
13H
17C
14B
14H
15H
5A
5B
6A
6B
9E
11E
9H
11H
12N
10E
7A
7F
7G
M99
AUX0
LX1
LX2
LX3
R1
R4
H1
H2
+5V
GND

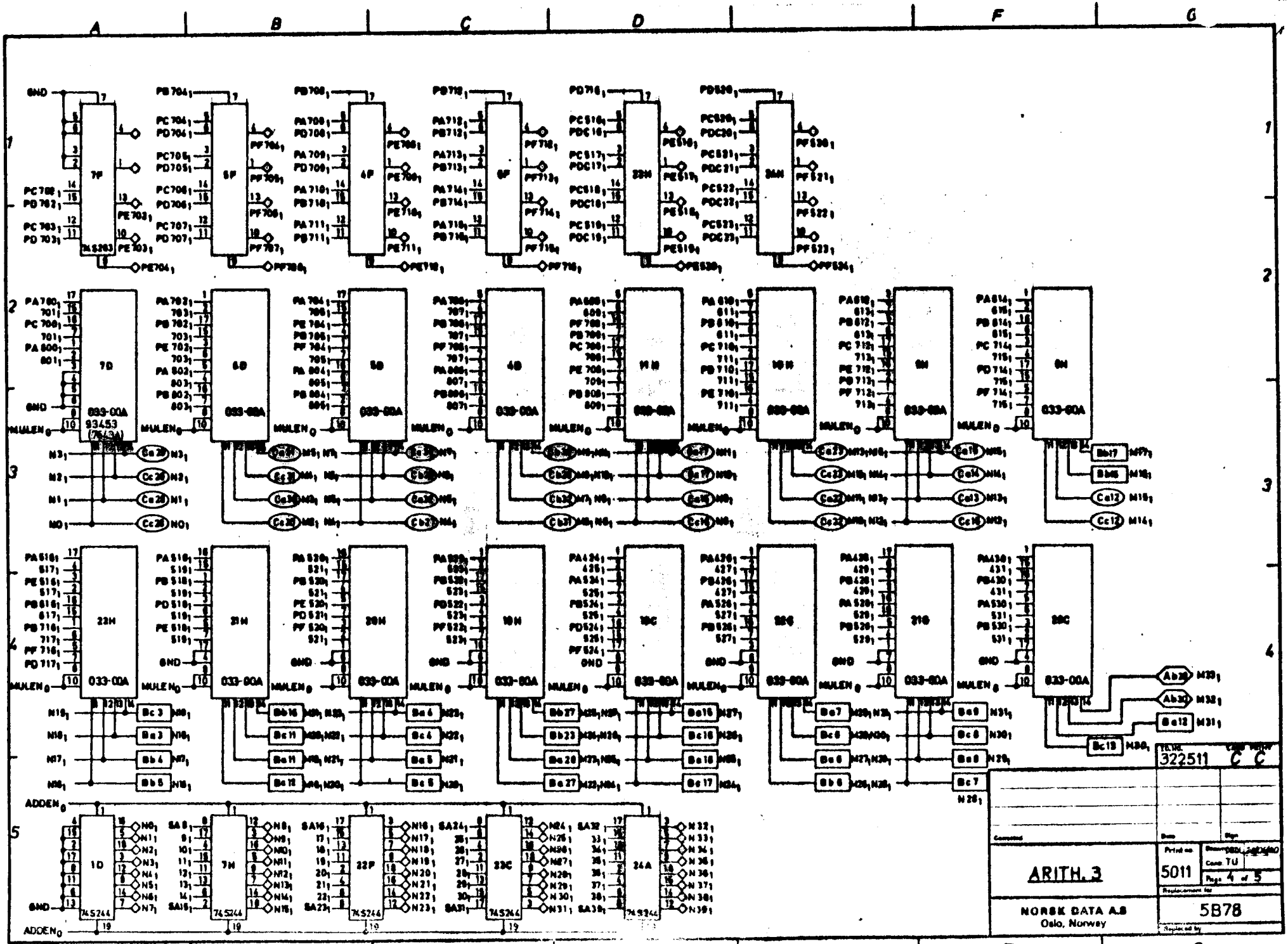

ARITH. 2
NORSK DATA A.S
Oslo, Norway
322509
CARD PRINT F C
PRINT NO 5009
Page 3 of 4
5B72
CORR ACCORD TO ECO S00-16,S02-26
S00-30
2A
3A
036-00A
3F
16
2D
16A
035-00A
17A
18A
18B
17H
2H
2G
2F
2E
3E
2C
3C
3D
4A
4C
4D
5A
5C
5D
5E
5F
5G
1A
1C
1D
1E
2A
2B
2C
2D
2E
2F
2G
2H
3A
3B
3C
3D
3E
3F
4A
4C
4D
5A
5C
5D
5E
5F
5G
XFUNC0,
XFUNC1,
XFUNC2,
XFUNC3,
XFUNC4,
XIDO,
TYPO0
TYP1
FUNC0,
FUNC1,
FUNC2,
FUNC3,
FUNC4,
IDO,
FOR0
FOR1
GND
SINGLE0
INTERM0
OF0,
OF1,
ROT0
EWRA,
EWRB,
SHORT
XACT0
WR0
WR1
XIDI,
DISDAT
HS
N.C.
FDL105
FDL10
RESEN,
RES0
RES1
XDRY0
DRY1
SOL0
SHORT1
SDL0
SDL1
ONEOP,
ADDEN0
ALBM,
ALB,
AEB,
SIGNA,
SIGNB,
PLUS,
CLSIGN,
MSELA1,
ENB,
GB0
WRB0
GA0
MPY,
WR
EWRA,
DRY,
PLUS1
IS0
IS1
ONEOP1
IROUND,
MX4
M99,
STICKS1
ISOFL0
ISIGNB,
SC0,
SS0
SS1
FS0
FZ1
F2R0
RS0,
RS1,
RS2,
RS3,
RS4,
RS5,
H3
H4
H2
H5
SIGN,
BRS0,
BRS1,
BRS2,
BRS3,
BRS4,
BRS5
MULEN0
M58,
M59,
M60,
M61,
M62,
M63,
ADDEN1
STCLK,
SEL2,
MSELA1,
DIVRES0
GE0
ADDEN1
MSELB1,
IF0,
IF1,
SINGLE1,
IROUND1
R5
R3
R2
+5V

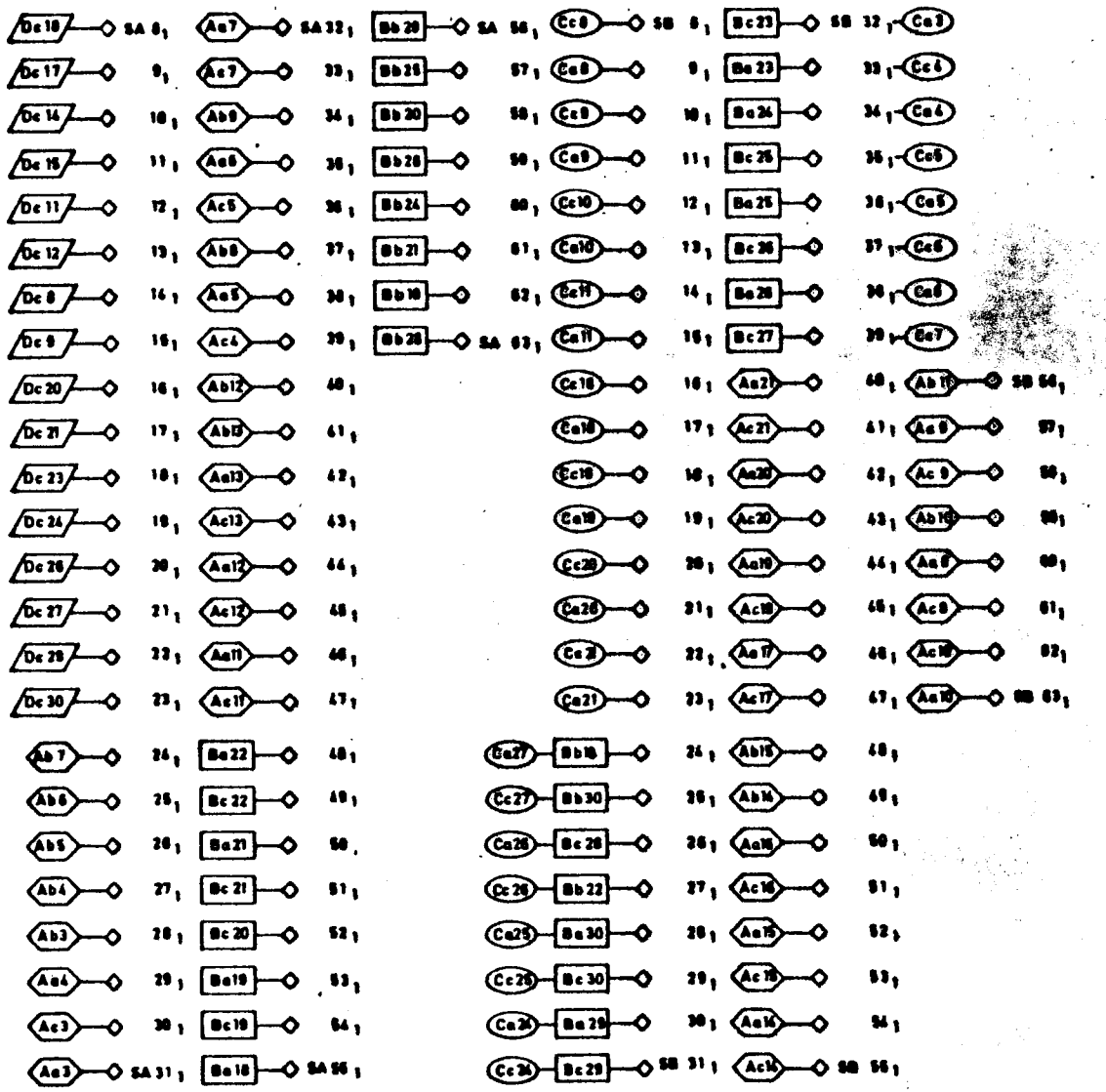

Ab5 SA40,
Ab4 SA41,
Ac4 SA42,
Ab3 SA43,
Ac3 SA44,
Aa5 SA45,
Aa3 SA46,
Aa4 SA47,
Ba10 SA48,
Bc9 SA49,
Bc10 SA50,
Ba11 SA51,
Bc11 SA52,
Ba12 SA53,
Bc12 SA54,
Ba8 SA55,
Ba14 SA56,
Ba19 SA57,
Bb13 SA58,
Ba18 SA59,
Bb12 SA60,
Bc14 SA61,
Bc18 SA62,
Ba13 SA63,
Cb24
Ca28 SB8,
Cc27 SB9,
Ca27 SB10,
Ca25 SB11,
Cc25 SB12,
Ca26 SB13,
Cc26 SB14,
Ca23 SB15,
Ca24 SB16,
Cc23 SB17,
Cc22 SB18,
Ca22 SB19,
Ca16 SB20,
Cc16 SB21,
Ca17 SB22,
Ca21 SB23,
Cc20 SB24,
Ca20 SB25,
Cc19 SB26,
Cc17 SB27,
Ca19 SB28,
Cc18 SB29,
Ca18 SB30,
Cc13 SB31,
Cc14 SB32,
Ca14 SB33,
Ca13 SB34,
Ca11 SB35,
Cc11 SB36,
Ca12 SB37,
Cc12 SB38,
Ca4 SB39,
Ab26 SB40,
Ab28 SB41,
Ab27 SB42,
Ac28 SB43,
Ab22 SB44,
Ac26 SB45,
Aa25 SB46,
Ac27 SB47,
Aa28 SB48,
Aa27 SB49,
Aa26 SB50,
Ab24 SB51,
Ac10 SB52,
Ac22 SB53,
Aa22 SB54,
Aa9 SB55,
Ab7 SB56,
Aa6 SB57,
Ac6 SB58,
Aa8 SB59,
Ab8 SB60,
Ac8 SB61,
Ab10 SB62,
Aa7 SB63,
ADDEN0
SA40, SA41, SA42, SA43, SA44, SA45, SA46, SA47,
SA48, SA49, SA50, SA51, SA52, SA53, SA54, SA55,
SA56, SA57, SA58, SA59, SA60, SA61, SA62, SA63,
ADDEN0
256
20D
18F
N40, N41, N42, N43, N44, N45, N46, N47,
N48, N49, N50, N51, N52, N53, N54, N55,
N56, N57, N58, N59, NN60, NN61, NN62, NN63,
SSB60, Cc29
SSB61, Cc32
SSB62, Ca30
SSB63, Cc30
PAA60,
7C
7B
7D
PAA61, PAA62, SEL2, SINGLE0,
038-004
DIVRES0
GND
GE1
GND
Ca29 DIV 5,
Ca31 DIV 6,
Cc31 DIV 7,
Cc28 DIV 8,
DIV33, DIV34, DIV35, DIV36,
GND
PAA56, GND
PAA57, IS1,
PAA58, IS1,
PAA59, IS1,
PAA60, IS1,
PAA61, IS1,
PAA62, IS1,
PAA63, IS1,
30F
30G
30E
MULEN0
MULEN0
Ab6 Ac7 Aa10 Ab9 Bb16 Bb14 Bc17 Bc19
N56, N57, N58, N59, NN60, NN61, NN62, NN63,
JO. NO. 322509
CARD PRINT F C
CORR ACCORD TO ECO 900-16300-01 08/04/81 AL
509-30 09/07/81 B-4
Corrected Date Sign.
ARITH. 2
PRINT NO 5009
Drawn TU
Page 4 of 4
NORSK DATA AS
Oslo, Norway
5873


A
B
C
D
E
F
G
1
2
3
4
5
12B BG
16D CF
8D DE
8D EB
8N AE
8N AB
12D AG
16D BF
16F CE
8P DD
8N EC
8N FB
8D BA
12F AF
14F BE
16F CD
8P DC
8N EB
8N FA
R1 1k
R2 1k
R3 1k
C1 10µF
C2 10µF
322511
C C
ARITH.3
5011
Page 1 of 5
NORSK DATA A.S
Oslo, Norway
5B75

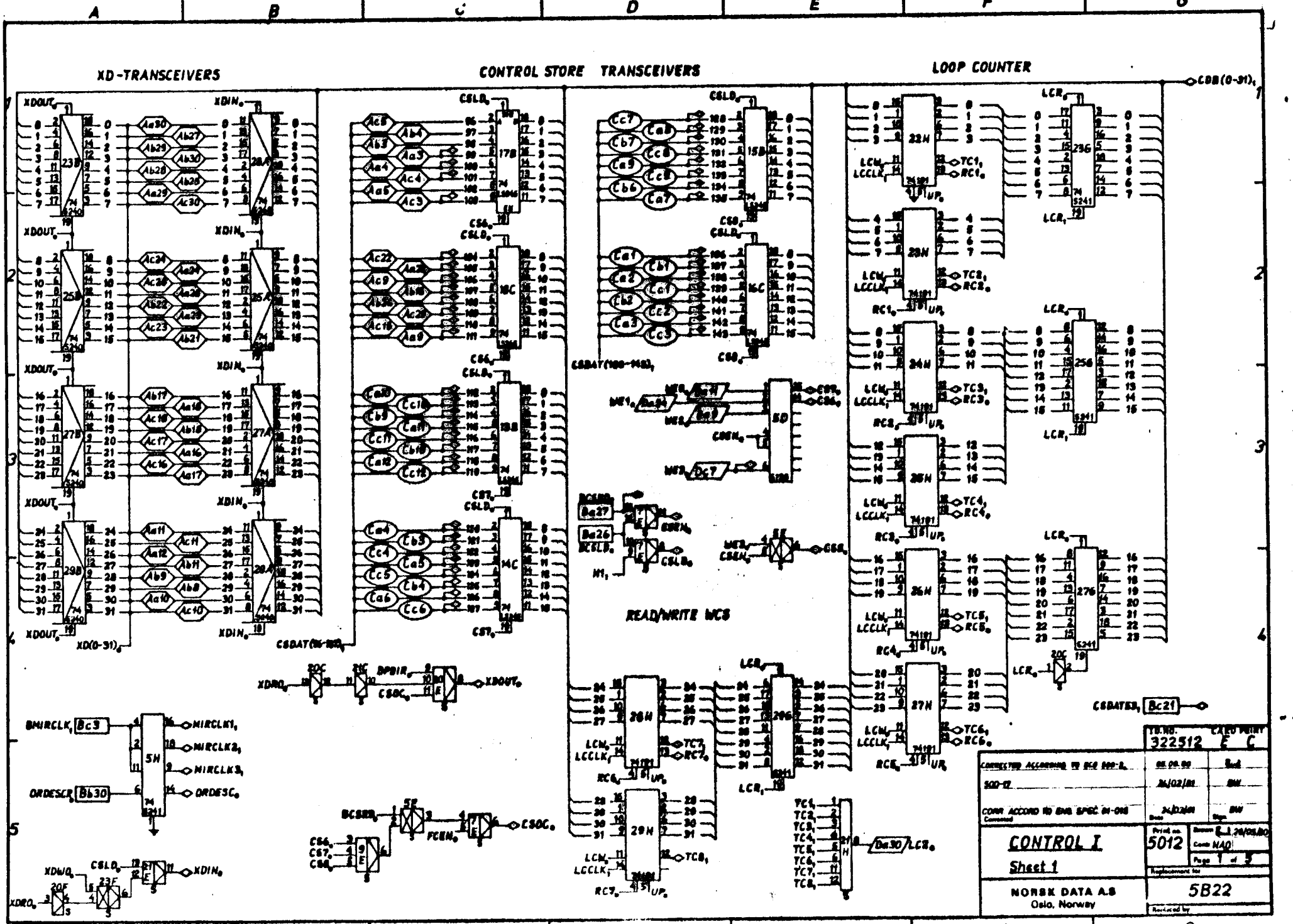

A
B
C
D
F
G
1
2
3
4
5
7B
6B
5B
4B
7C
6C
5C
4C
7E
6E
5E
4E
11E
10E
9E
8E
1N
1O
1P
1R
33E
32E
31E
30E
36E
37E
38E
033-00A
ARITH.3
322511
5011
5B76
NORSK DATA A.S
Oslo, Norway
Page 2 of 5

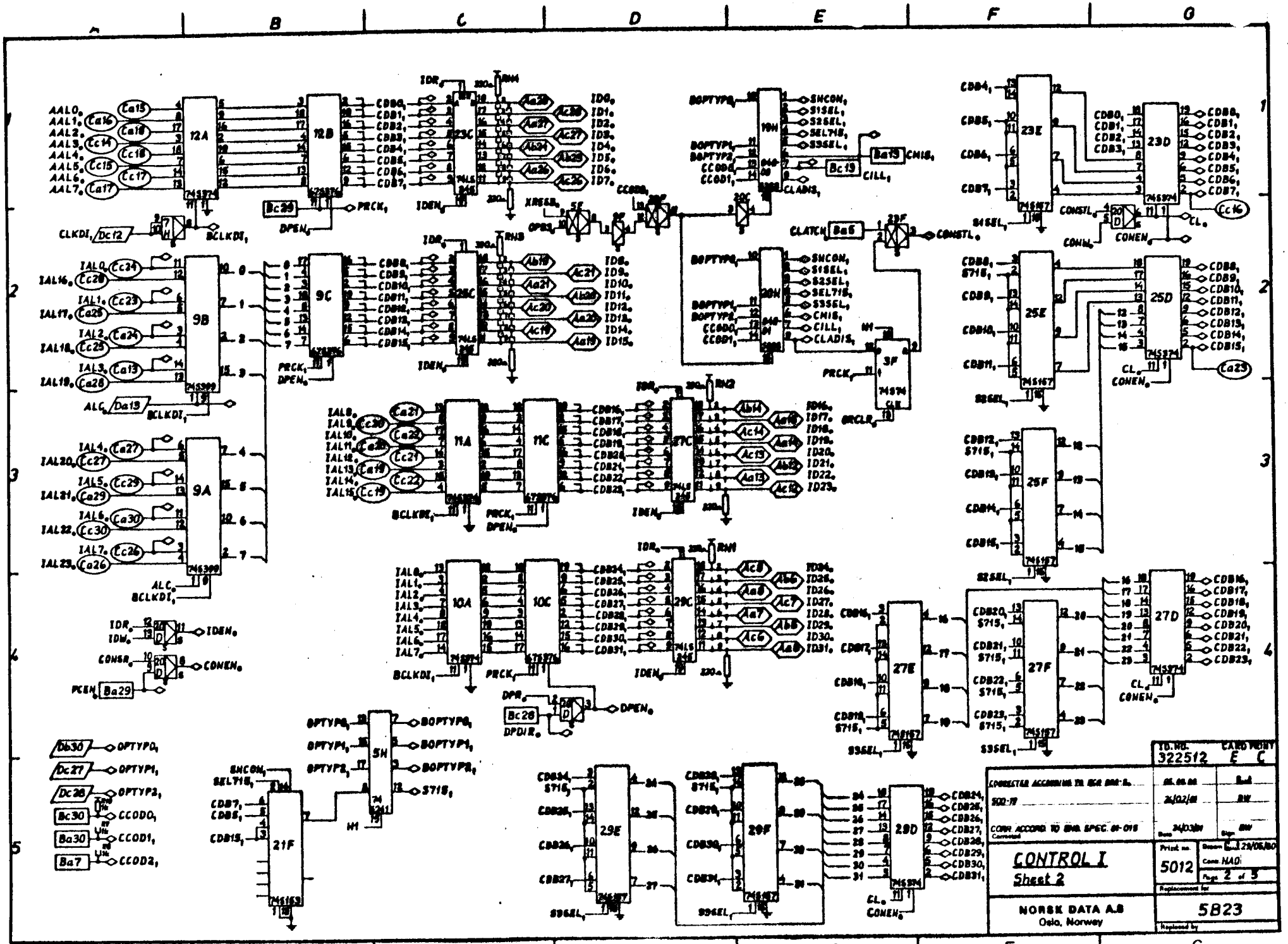

ARITH. 3
322511
5011
Page 3 of 5
NORSK DATA A.S
Oslo, Norway
5B77
TU

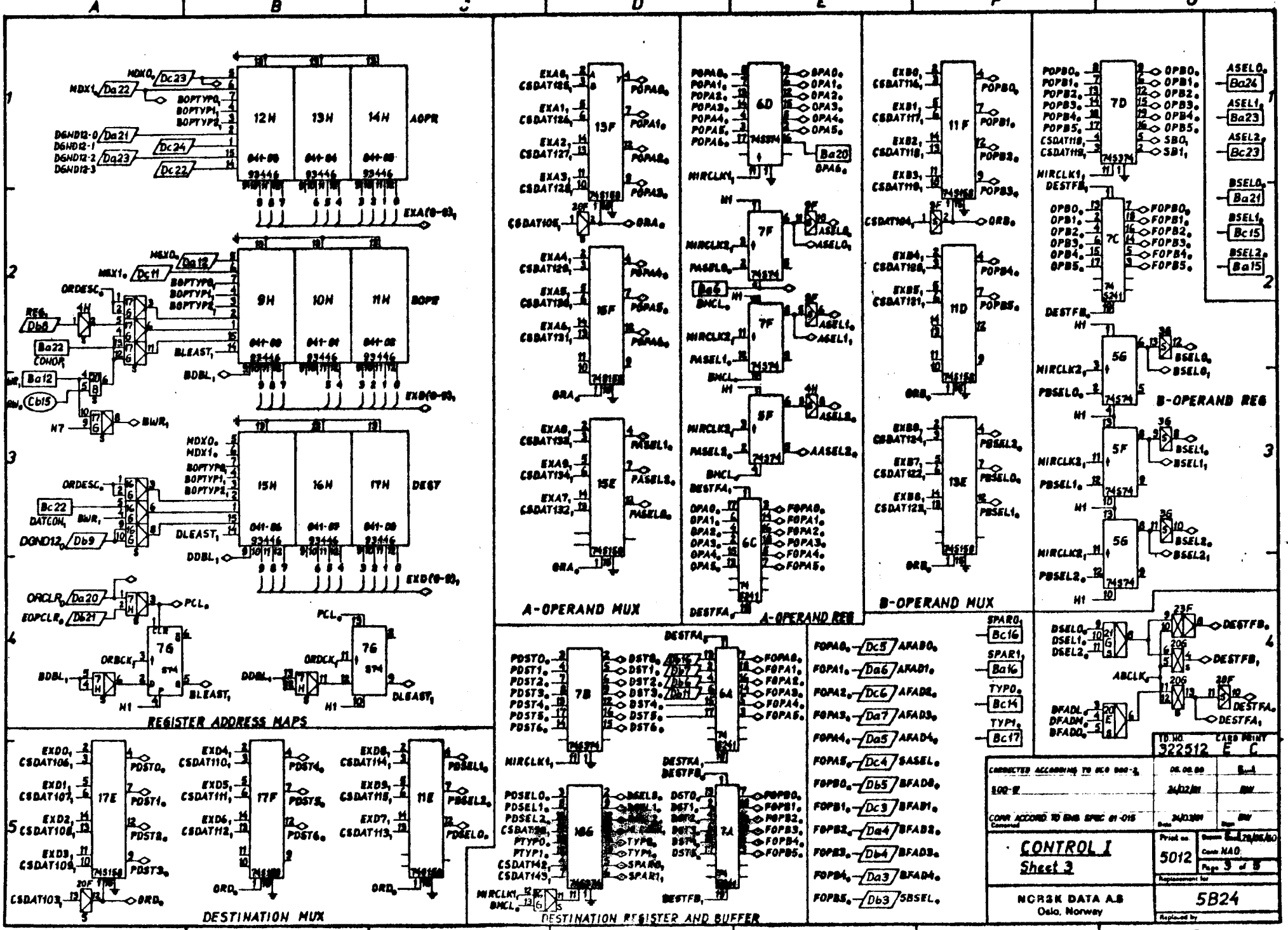

7P
6P
4P
3P
2HH
1HH
7D
6D
5D
4D
1HH
1GC
2GC
2HD
2GC
033-00A
1D
7H
22P
23C
24A
ARITH. 3
5011
NORSK DATA A.S
Oslo, Norway
5878
322511

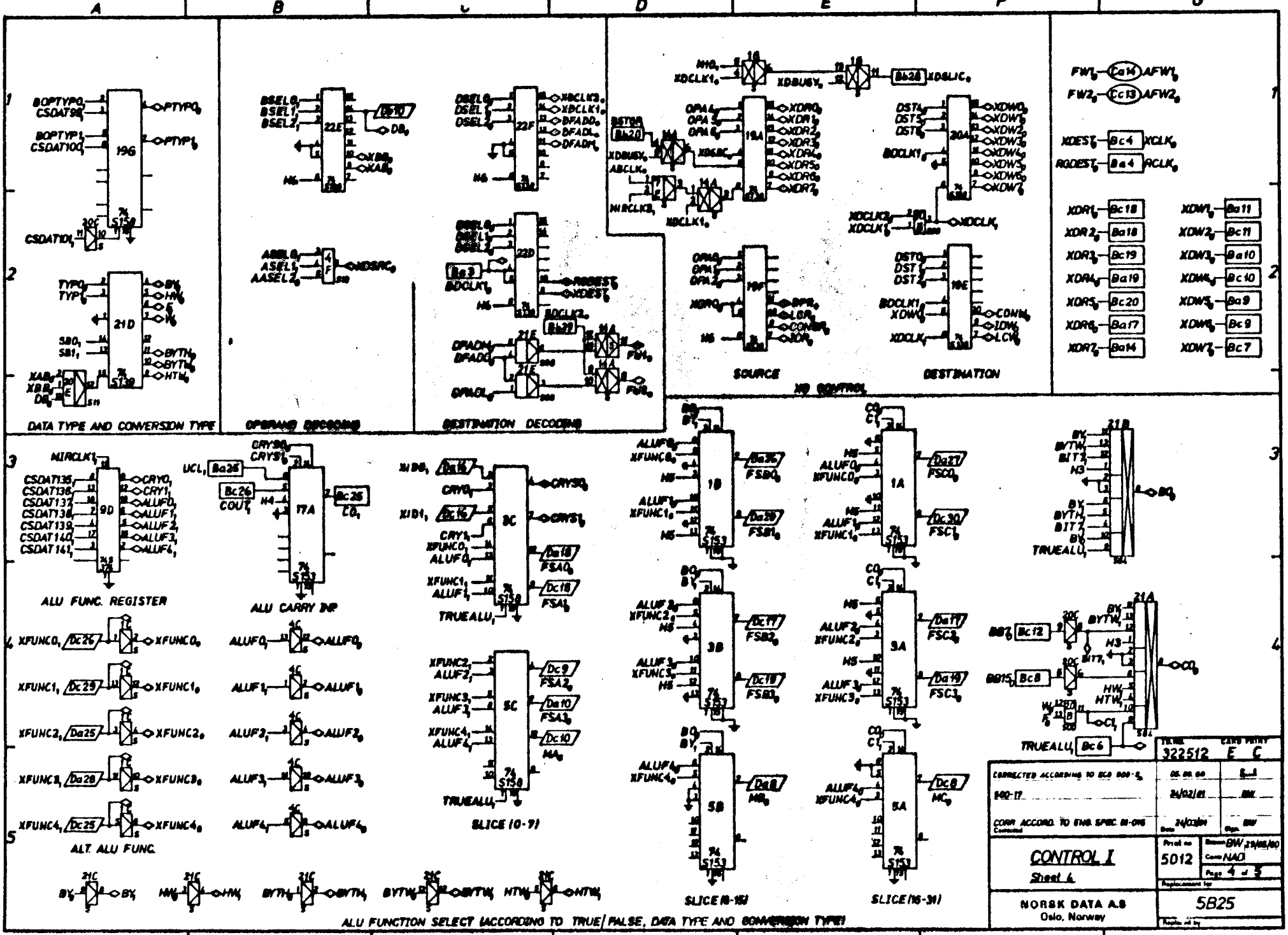


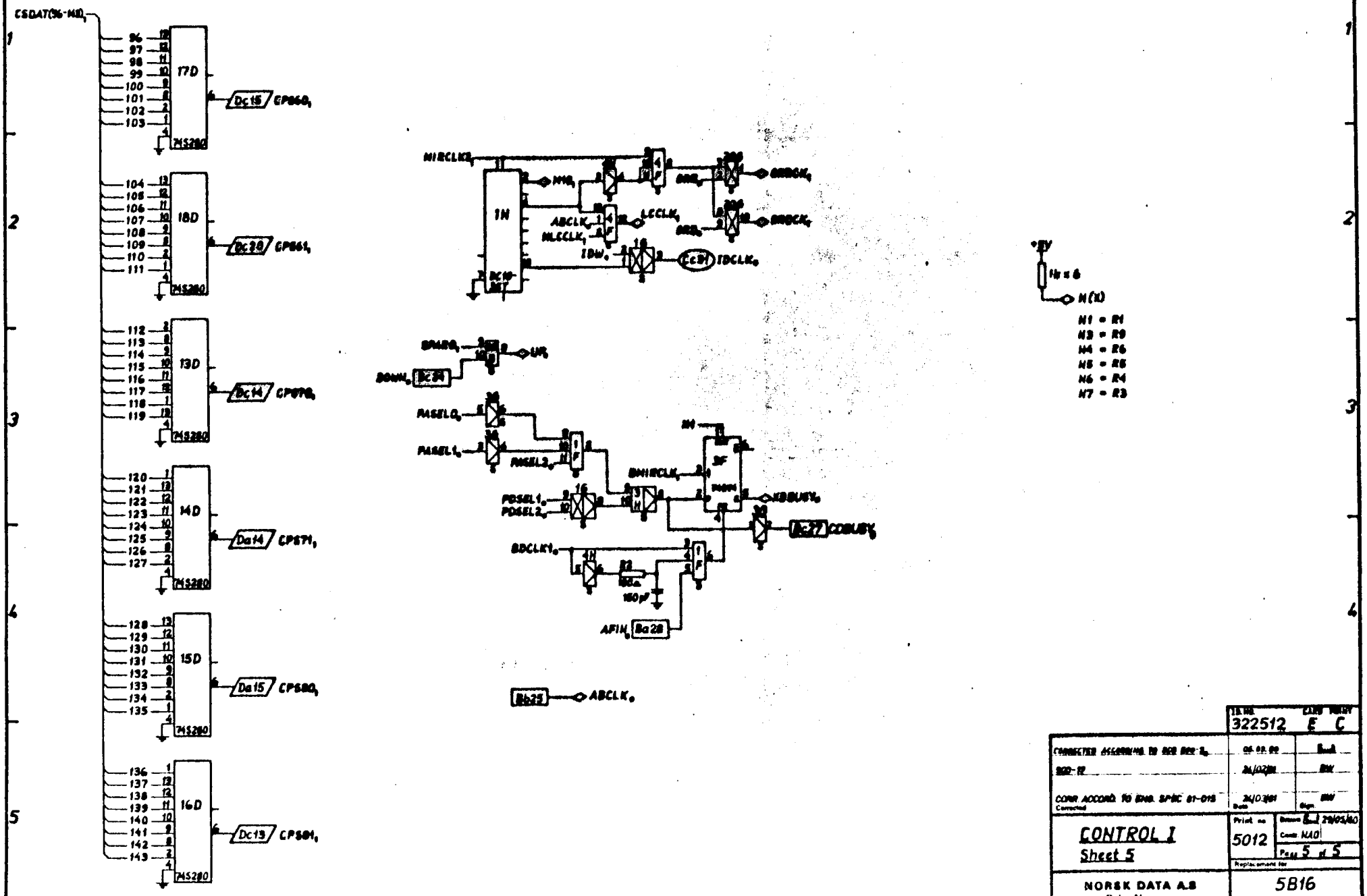
REVNR. 322511	CARD PARTY C	C	
ARITH. 3	Print no 5011	Page 5 of 5	
NORSK DATA A.S Oslo, Norway	5879		


XD-TRANSCEIVERS
CONTROL STORE TRANSCEIVERS
LOOP COUNTER
READ/WRITE WCS
CONTROL I
Sheet 1
NORSK DATA A.S
Oslo, Norway
5B22
322512

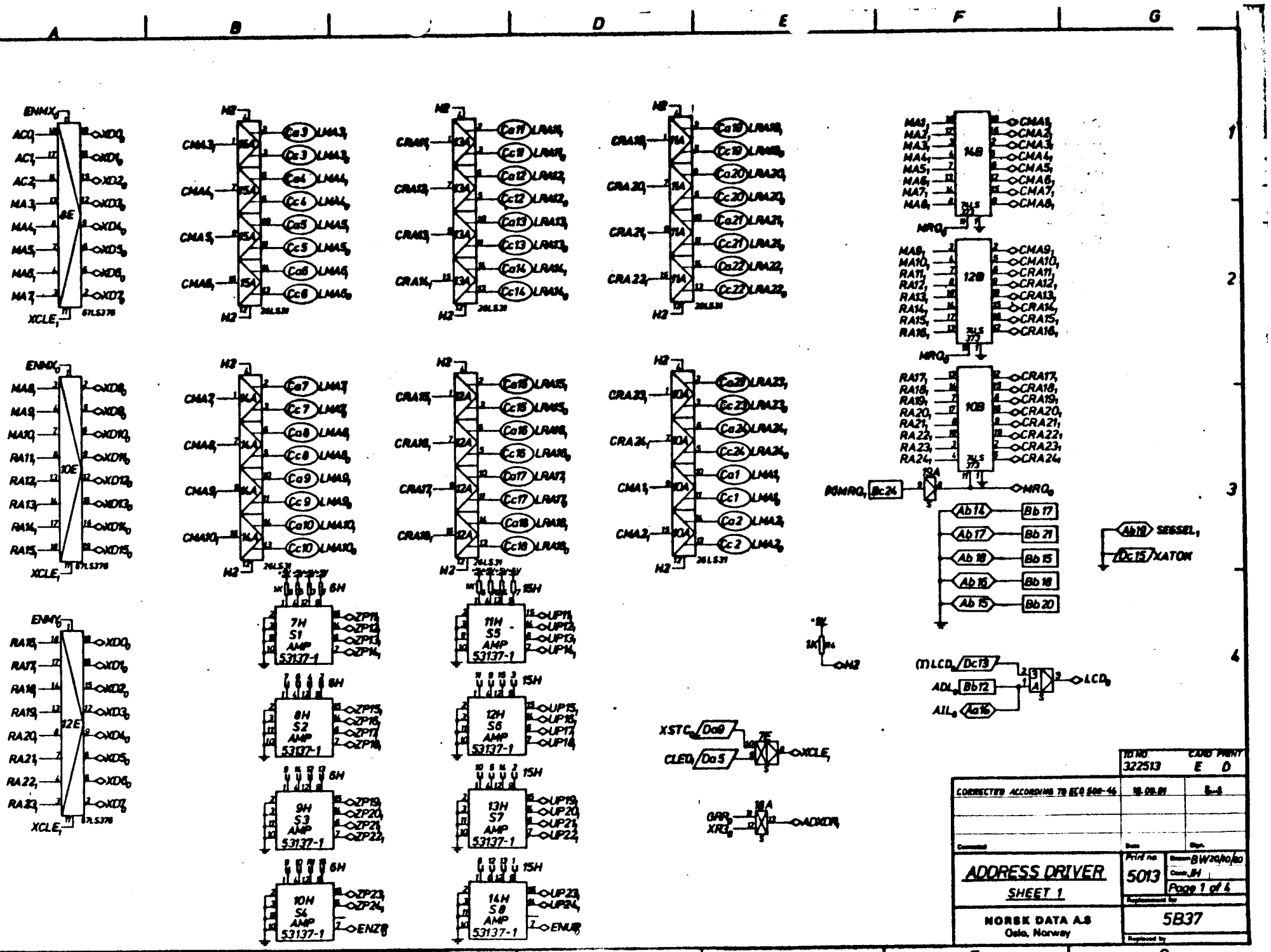

12A
12B
23C
19H
23E
23D
9B
9C
28C
28H
25E
25D
9A
11A
11C
27C
25F
10A
10C
29C
27E
27F
27D
5H
21F
29E
29F
29D
3F
CONTROL I
Sheet 2
5012
322512
NORSK DATA A.S
Oslo, Norway
5823

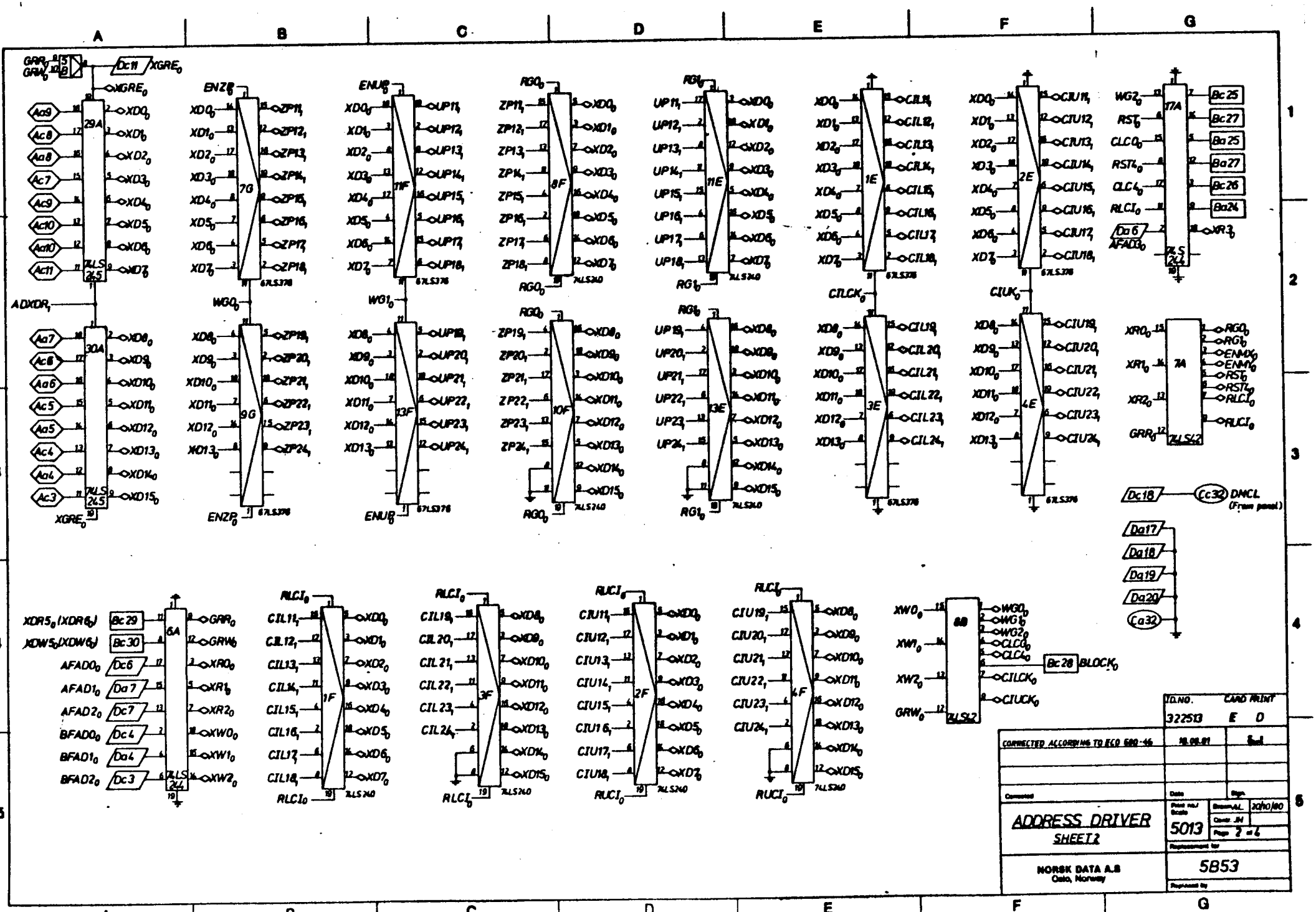

REGISTER ADDRESS MAPS
A-OPERAND MUX
A-OPERAND REG
B-OPERAND MUX
B-OPERAND REG
DESTINATION MUX
DESTINATION REGISTER AND BUFFER
CONTROL I
Sheet 3
NORSK DATA A.S
Oslo, Norway
5012
5B24
322512

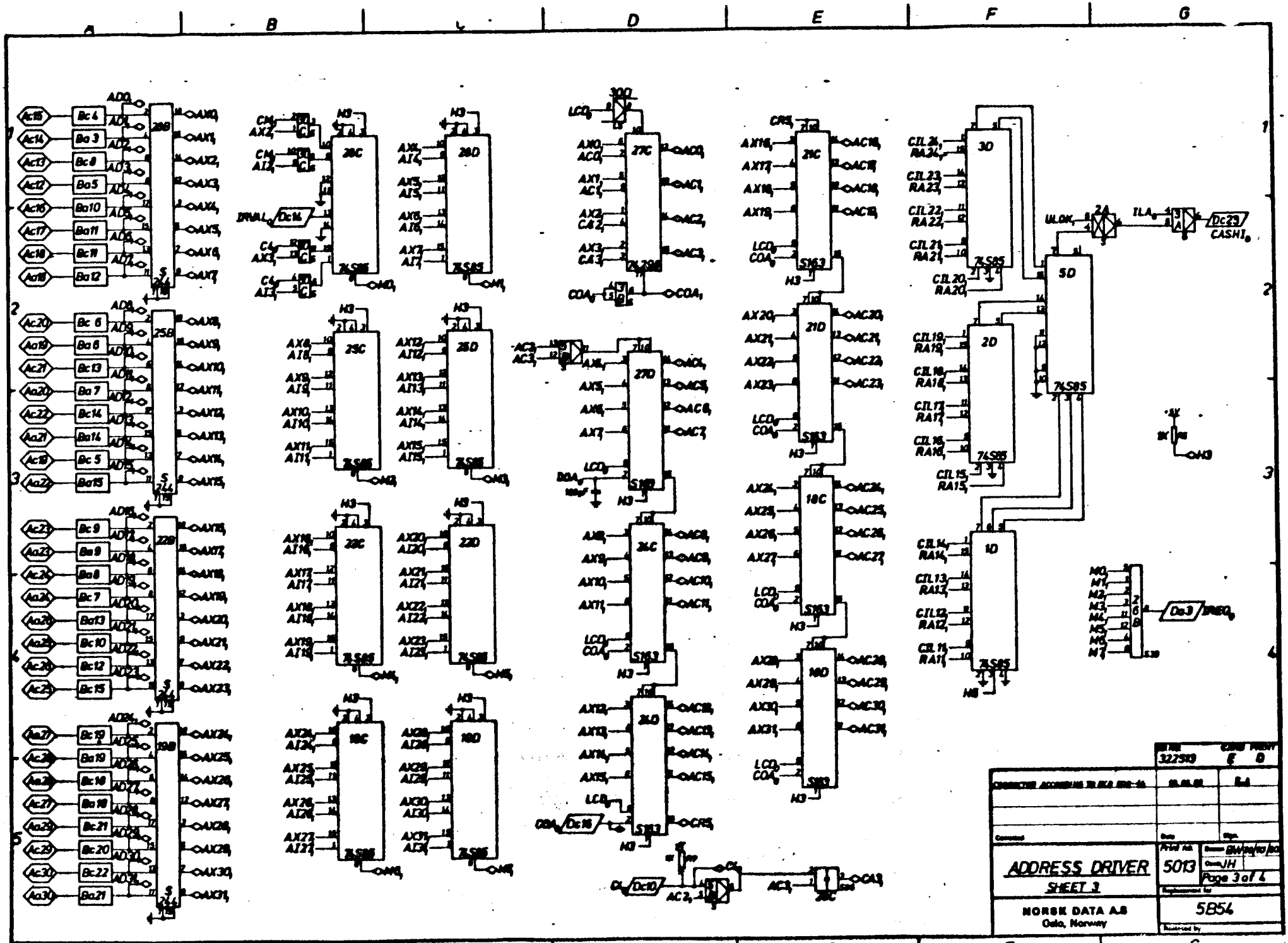

DATA TYPE AND CONVERSION TYPE
OPERAND DECODING
DESTINATION DECODING
SOURCE
DESTINATION
MD CONTROL
ALU FUNC. REGISTER
ALU CARRY INP
SLICE (0-7)
SLICE (8-15)
SLICE (16-31)
ALT. ALU FUNC.
ALU FUNCTION SELECT (ACCORDING TO TRUE/FALSE, DATA TYPE AND CONVERSION TYPE)
CONTROL I
Sheet 4
NORSK DATA A.S
Oslo, Norway
322512
5012
5825

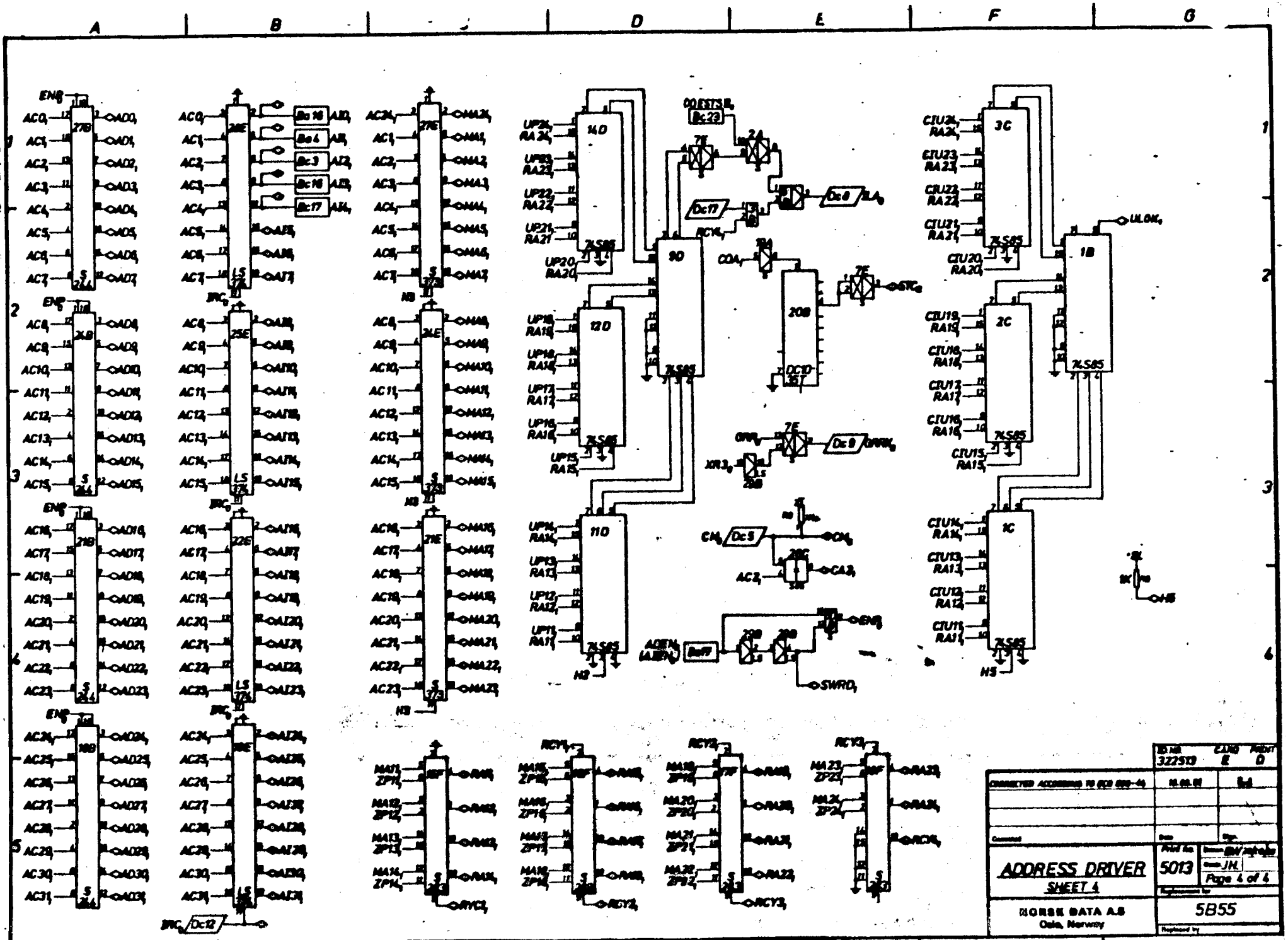


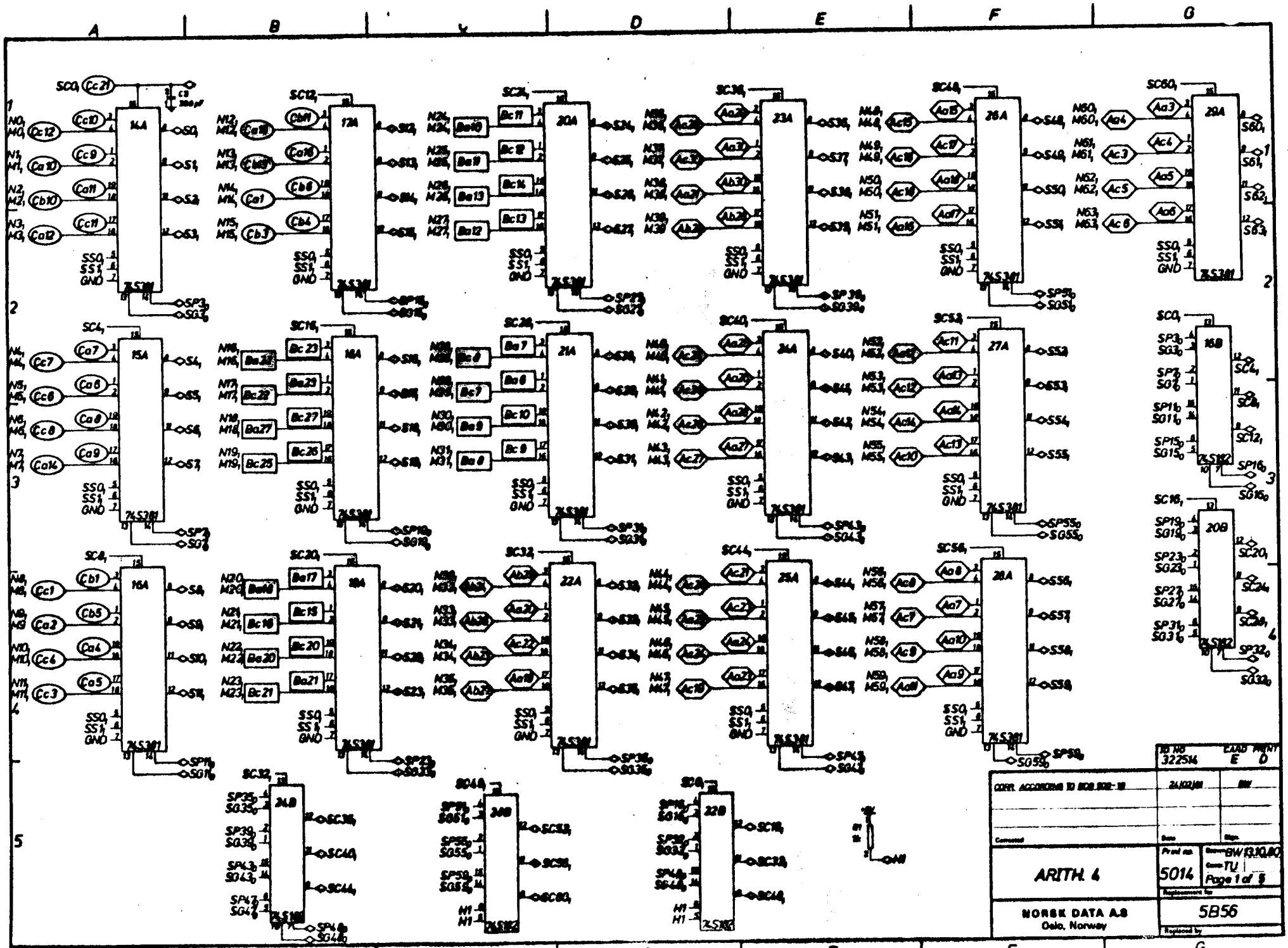
TR NO 322512		EXP INDEX E C
CORRECTED ACCORDING TO SCR REG.	06.02.80	
SCD-TF	26/02/80	
CORR ACCORD TO ENG. SPEC 81-015 Corrected	26/03/80 Date	Sign.
CONTROL I Sheet 5	Print no 5012	Drawn 29/05/80 Conn MAO Page 5 of 5
NORSK DATA A.S Oslo, Norway	5B16	Replacement for / Replaced by

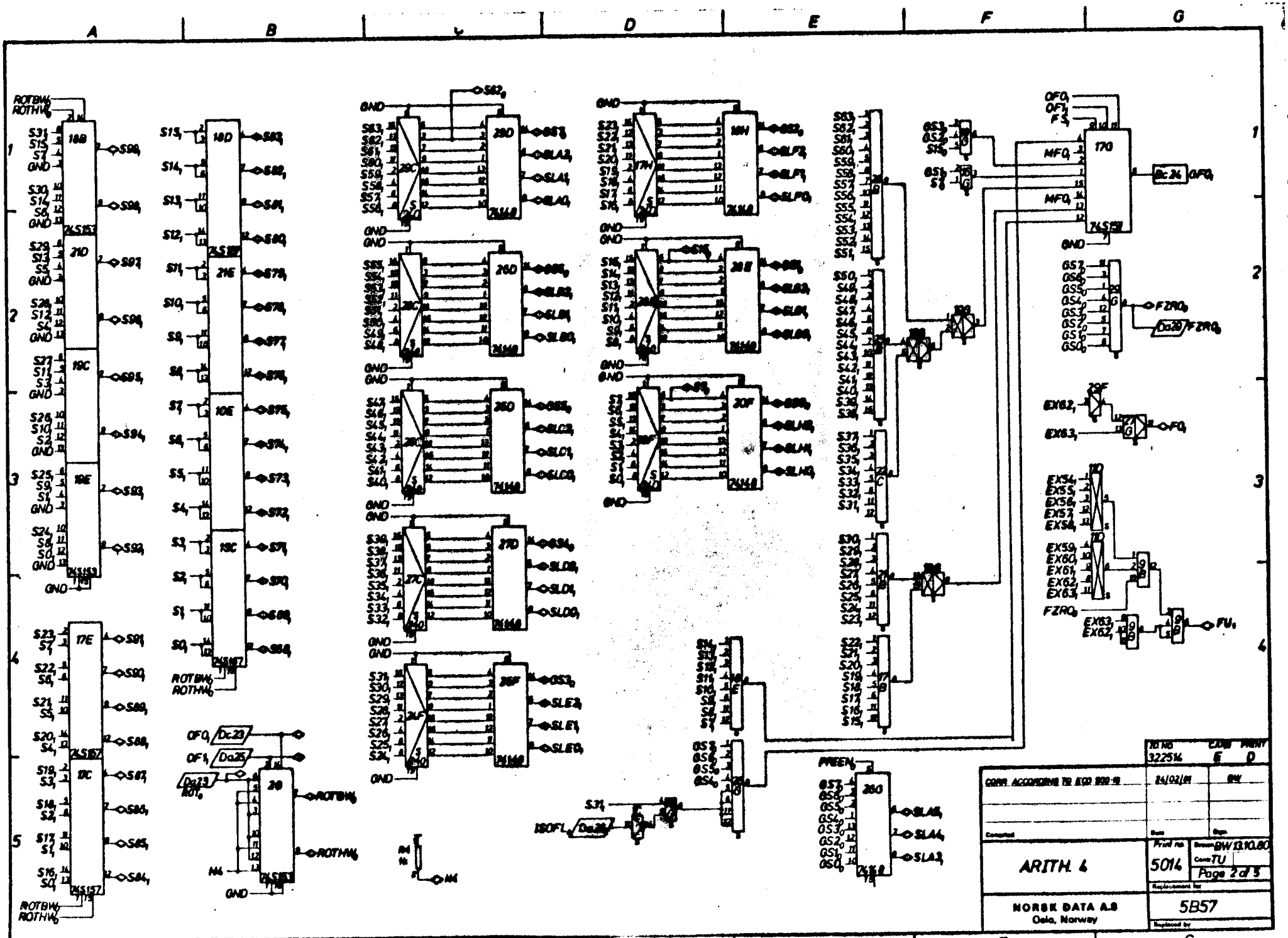

8E
10E
12E
67LS378
M2
26LS31
7H S1 AMP 53137-1
8H S2 AMP 53137-1
9H S3 AMP 53137-1
10H S4 AMP 53137-1
11H S5 AMP 53137-1
12H S6 AMP 53137-1
13H S7 AMP 53137-1
14H S8 AMP 53137-1
14B
12B
10B
74LS 373
ADDRESS DRIVER
SHEET 1
5013
322513
NORSK DATA A.S
Oslo, Norway
5B37
Page 1 of 4

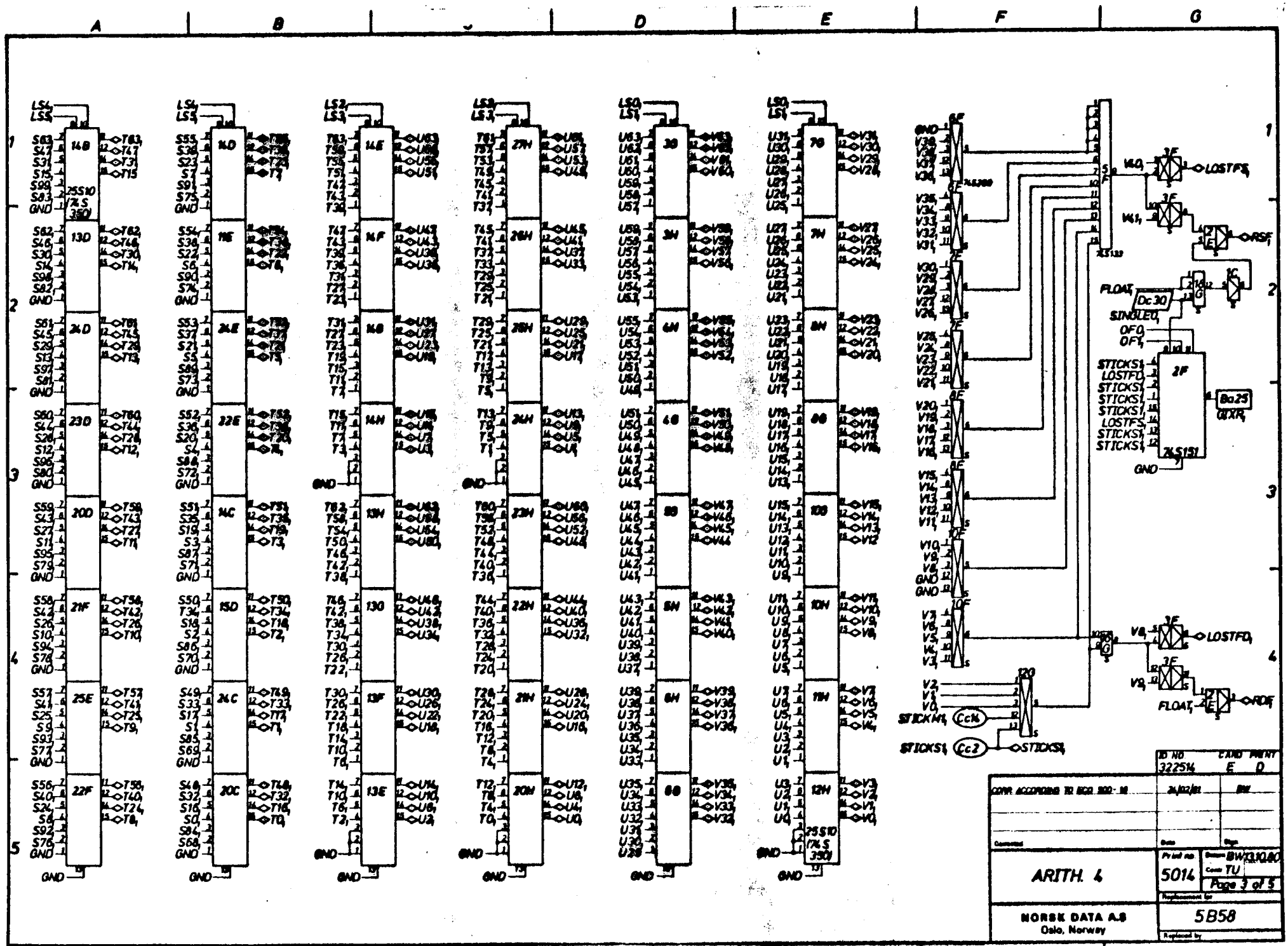

A
B
C
D
E
F
G
1
2
3
4
5
GRR0
GRW0
Dc11
XGRE0
Ac9
Ac8
Aa8
Ac7
Ac9
Ac10
Ac11
29A
74LS 245
XD00
XD10
XD20
XD30
XD40
XD50
XD60
XD70
ADXDR1
Aa7
Ac6
Aa6
Ac5
Aa5
Ac4
Aa4
Ac3
30A
XD80
XD90
XD100
XD110
XD120
XD130
XD140
XD150
ENZP0
7G
9G
67LS378
WG00
ZP110
ZP120
ZP130
ZP140
ZP150
ZP160
ZP170
ZP180
ZP190
ZP200
ZP210
ZP220
ZP230
ZP240
ENUP0
11F
13F
WG01
UP110
UP120
UP130
UP140
UP150
UP160
UP170
UP180
UP190
UP200
UP210
UP220
UP230
UP240
RG00
8F
10F
74LS240
RG10
11E
13E
1E
3E
2E
4E
CILCK0
CIUCK0
CIL10
CIL11
CIL12
CIL13
CIL14
CIL15
CIL16
CIL17
CIL18
CIL19
CIL20
CIL21
CIL22
CIL23
CIL24
CIU10
CIU11
CIU12
CIU13
CIU14
CIU15
CIU16
CIU17
CIU18
CIU19
CIU20
CIU21
CIU22
CIU23
CIU24
WG20
RST0
CLC00
RSTL0
CLC40
RLCI0
Da6
AFAD00
17A
74LS 244
Bc25
Bc27
Ba25
Ba27
Bc26
Ba24
XR30
XRR0
XR10
XR20
GRR0
7A
74LS42
RG00
RG10
ENMX0
ENM10
RST0
RSTL0
RLCI0
RLCI0
Dc18
Cc32
DMCL
(From panel)
Da17
Da18
Da19
Da20
Ca32
XDR5 (XDR6)
XDW5 (XDW6)
AFAD00
AFAD10
AFAD20
BFAD00
BFAD10
BFAD20
Bc29
Bc30
Dc6
Da7
Dc7
Dc4
Da4
Dc3
6A
74LS 244
GRR0
GRW0
XR00
XR10
XR20
XW00
XW10
XW20
RLCI0
CIL11
CIL12
CIL13
CIL14
CIL15
CIL16
CIL17
CIL18
1F
3F
2F
4F
CIU11
CIU12
CIU13
CIU14
CIU15
CIU16
CIU17
CIU18
CIU19
CIU20
CIU21
CIU22
CIU23
CIU24
XW0
XW1
XW2
GRW0
8B
74LS42
WG00
WG10
WG20
CLC00
CLC40
Bc28
BLOCK0
CILCK0
CIUCK0
T.D.NO.
322513
CARD PRINT
E
D
CORRECTED ACCORDING TO ECO 600-46
ADDRESS DRIVER
SHEET 2
5013
NORSK DATA A.S
Oslo, Norway
5853

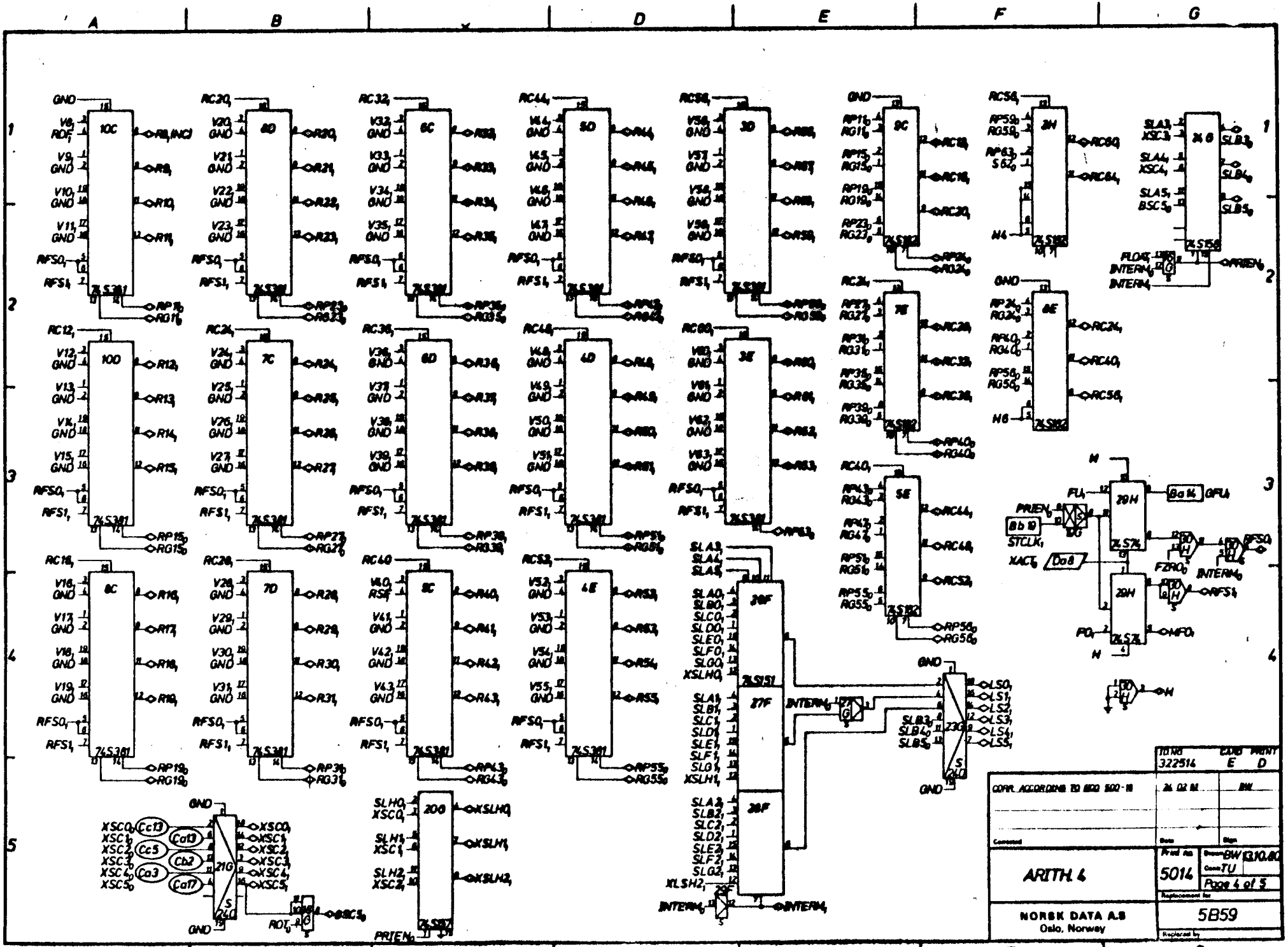

ADDRESS DRIVER
SHEET 3
NORSK DATA A.S
Oslo, Norway
5013
Page 3 of 4
5854
322510
ULOK
ILA
CASH1
DRIVEQ
74S85
74S86
74S163
74S240
74S244
74S241
74S299
74S373

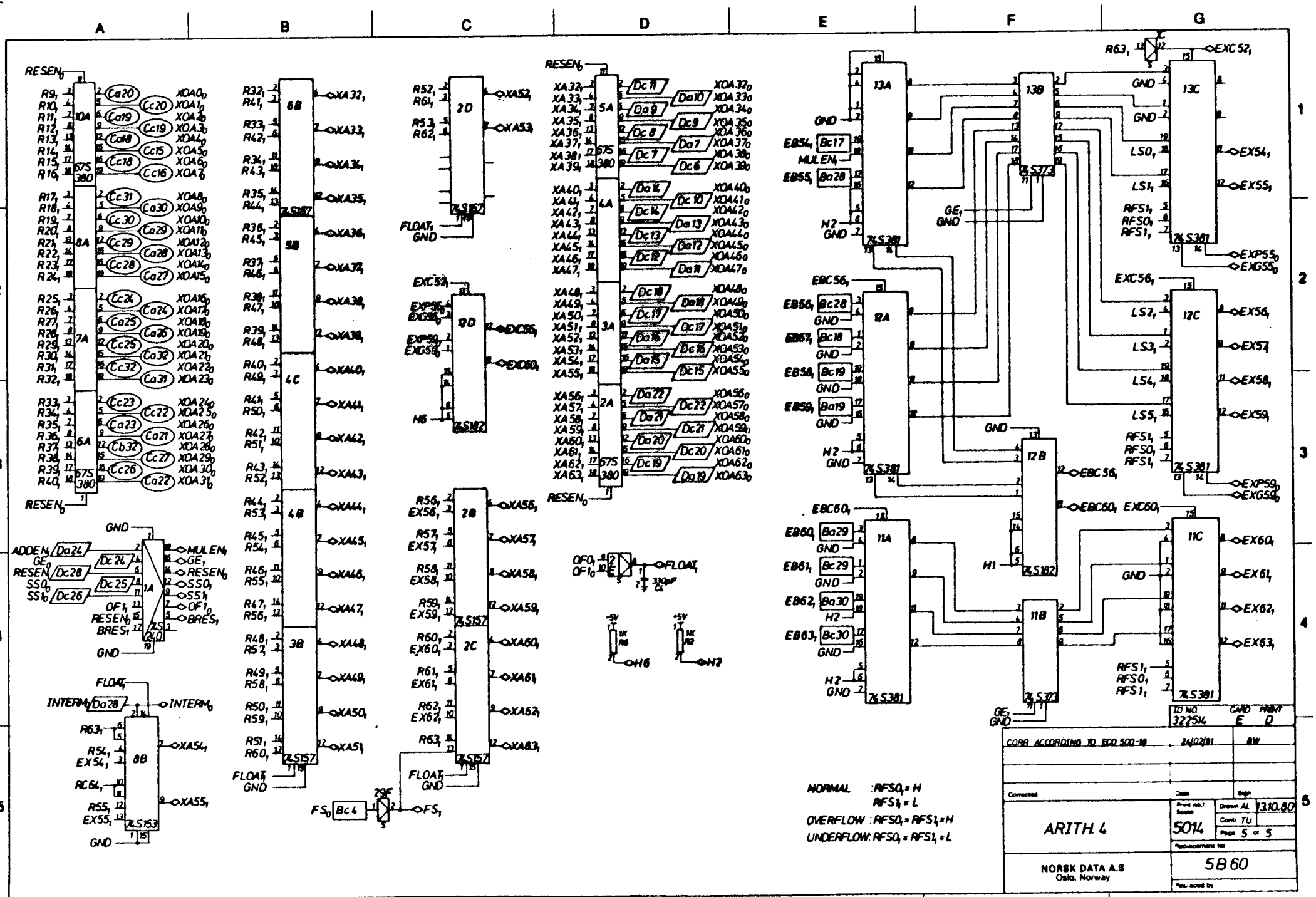

ADDRESS DRIVER
SHEET 4
5013
Page 4 of 4
NORSK DATA A.S
Oslo, Norway
5B55
322513
JH.

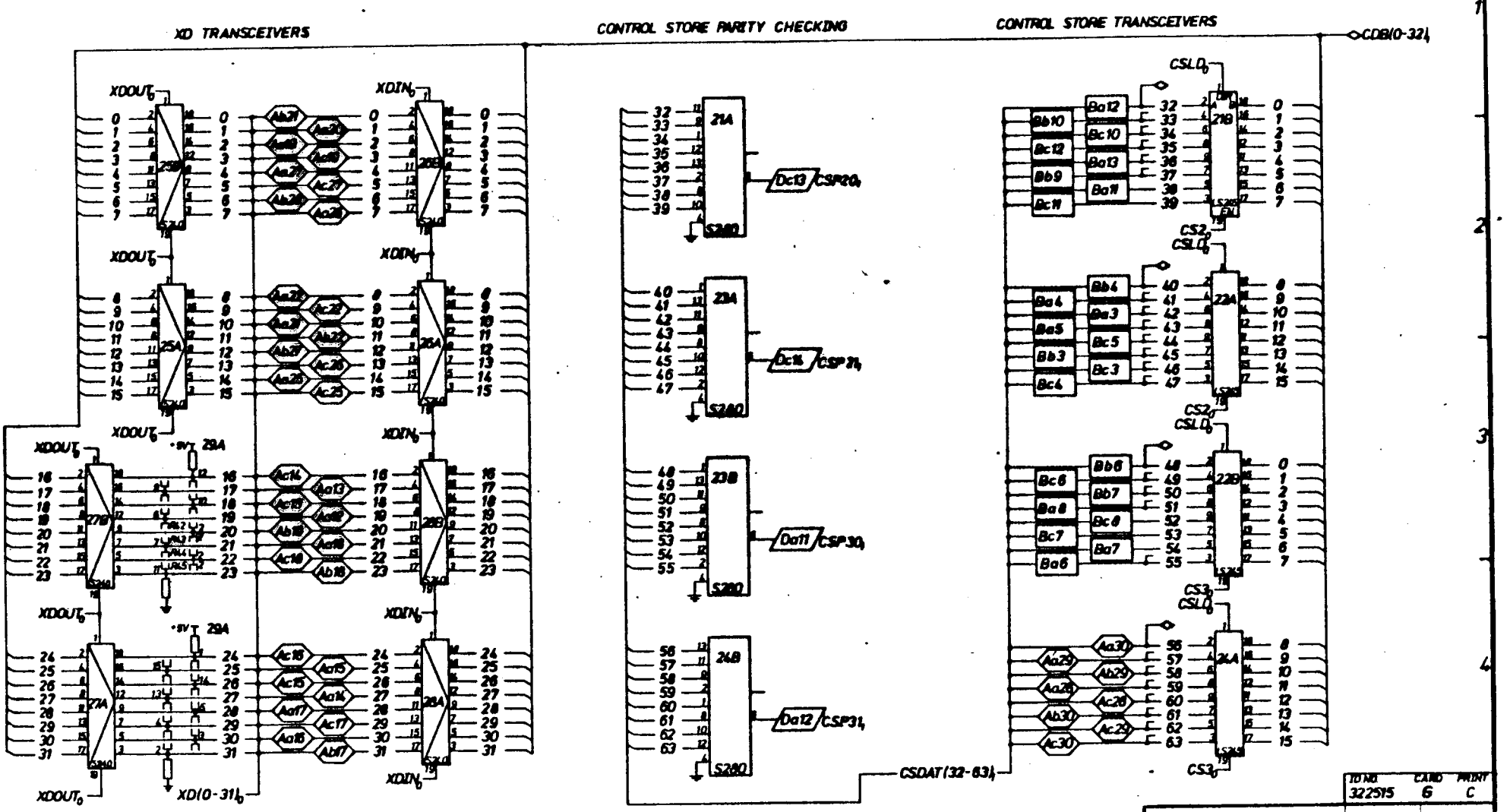

14A
17A
20A
23A
26A
29A
15A
18A
21A
24A
27A
16B
16A
19A
22A
25A
28A
20B
24B
20B
22B
ARITH. 4
5014
NORSK DATA A.S
Oslo, Norway
5B56
322514
Page 1 of 8


ARITH. 4
NORSK DATA A.S
Oslo, Norway
5014
5B57
Page 2 of 5
24/02/81
BW 13.10.80
TU
322514

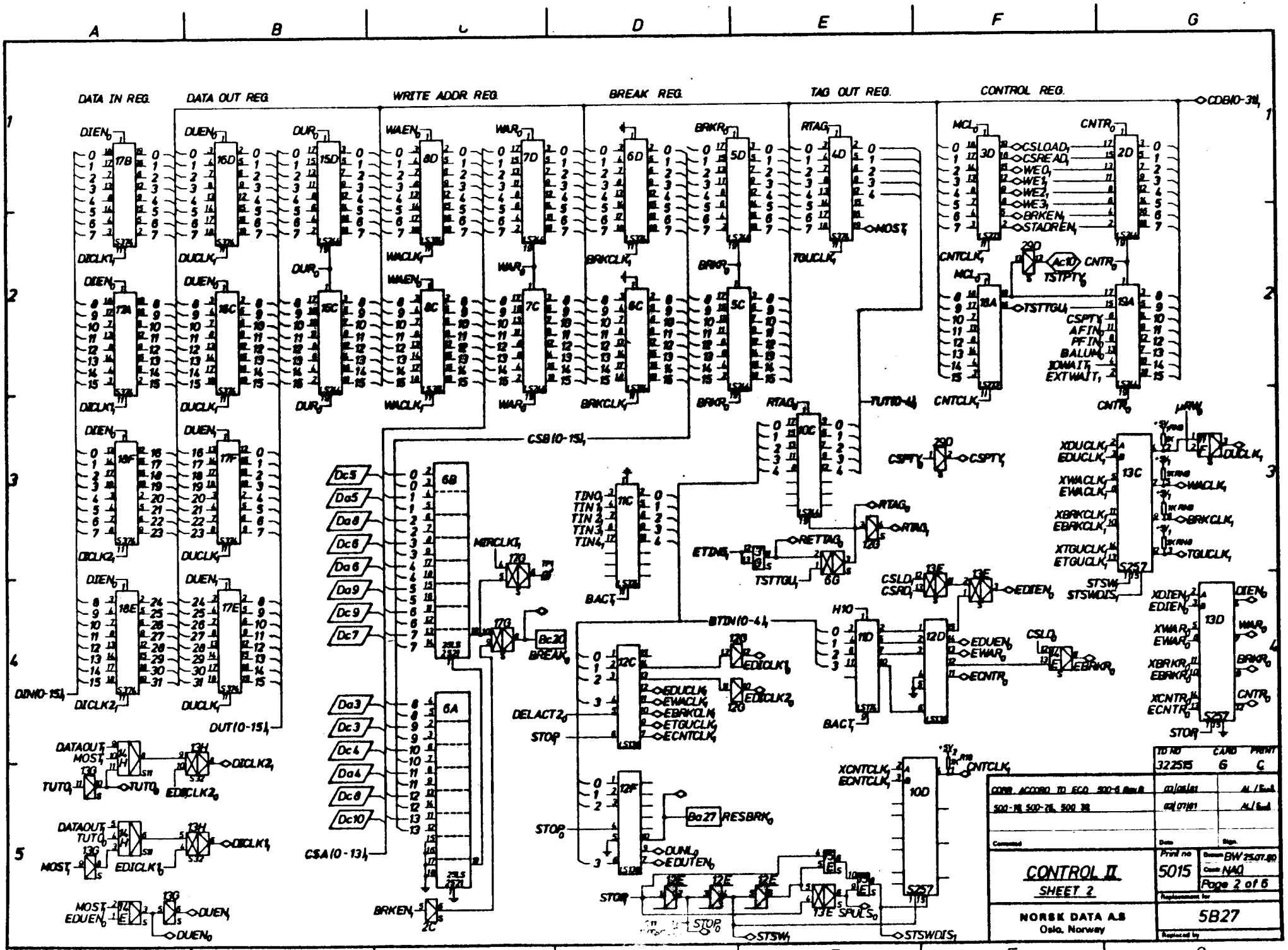

A
B
D
E
F
G
1
2
3
4
5
14B
13D
24D
23D
20D
21F
25E
22F
14D
11E
24E
22E
14C
15D
24C
20C
14E
14F
14B
14N
13N
13P
13E
27H
26H
25H
24H
23H
22H
21H
20H
30
3N
4N
4B
5B
6N
6B
7B
7N
8N
8B
10N
11N
12N
25S10
74LS 350
74LS139
74LS151
74LS00
74LS20
74LS04
74LS08
74LS32
74LS86
74LS240
74LS244
74LS245
74LS299
74LS373
74LS374
74LS377
74LS378
74LS379
74LS399
LOSTFS
RSF
FLOAT
Dc30
SINGLEC
OFO
OFI
STICKS
LOSTFD
Ba25
QIXR
LOSTFD
RDF
STICKM
Cc1
Cc2
GND
ID NO 322514
EAND PRINT E D
CORR ACCORDING TO ECO 800-16 24/02/81 BW
ARITH. 4
Proj no 5014
Drawn BW 13.10.80
Chkd TU
Page 3 of 5
NORSK DATA A.S
Oslo, Norway
5B58

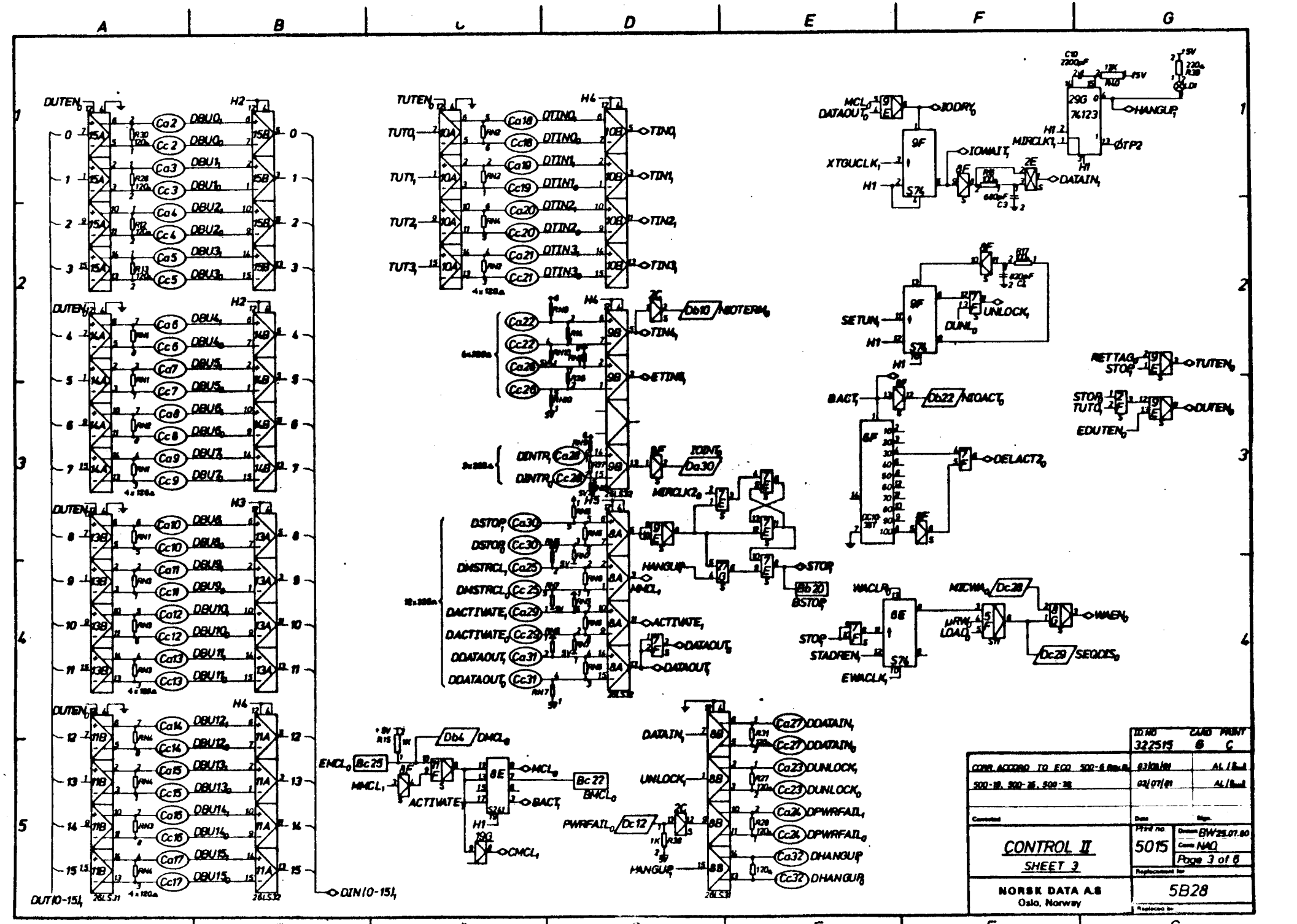

10C
8D
8C
9D
3D
9C
2H
X 8
7E
6E
10D
7C
6D
4D
3E
5E
8C
7D
8C
4E
20G
21G
30F
27F
28F
23G
29H
29H
ARITH. 4
5014
NORSK DATA A.S
Oslo, Norway
5B59
322516
Page 4 of 5

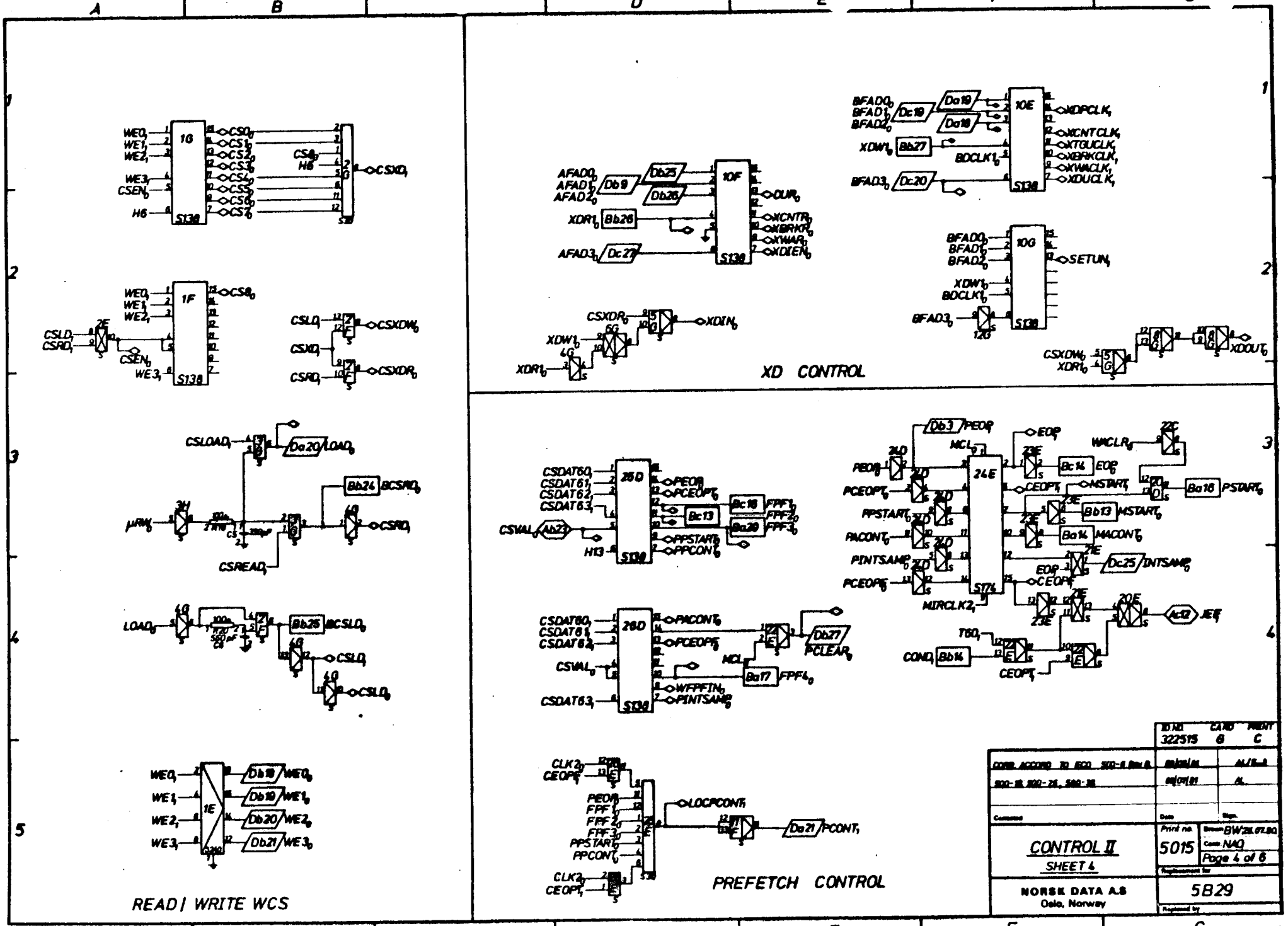

A
B
C
D
E
F
G
1
2
3
4
5
10A
8A
7A
6A
5A
4A
3A
2A
1A
6B
5B
4C
4B
3B
2D
1D
2B
2C
8B
13A
13B
13C
12A
12B
12C
11A
11B
11C
ARITH. 4
5014
NORSK DATA A.S
Oslo, Norway
5860
CARD PRINT
E D
322514
CORR ACCORDING TO ECO 500-18
24/02/81
BW
Drawn AL
13.10.80
Contr TU
Page 5 of 5
NORMAL : RFS0 = H
RFS1 = L
OVERFLOW : RFS0 = RFS1 = H
UNDERFLOW: RFS0 = RFS1 = L

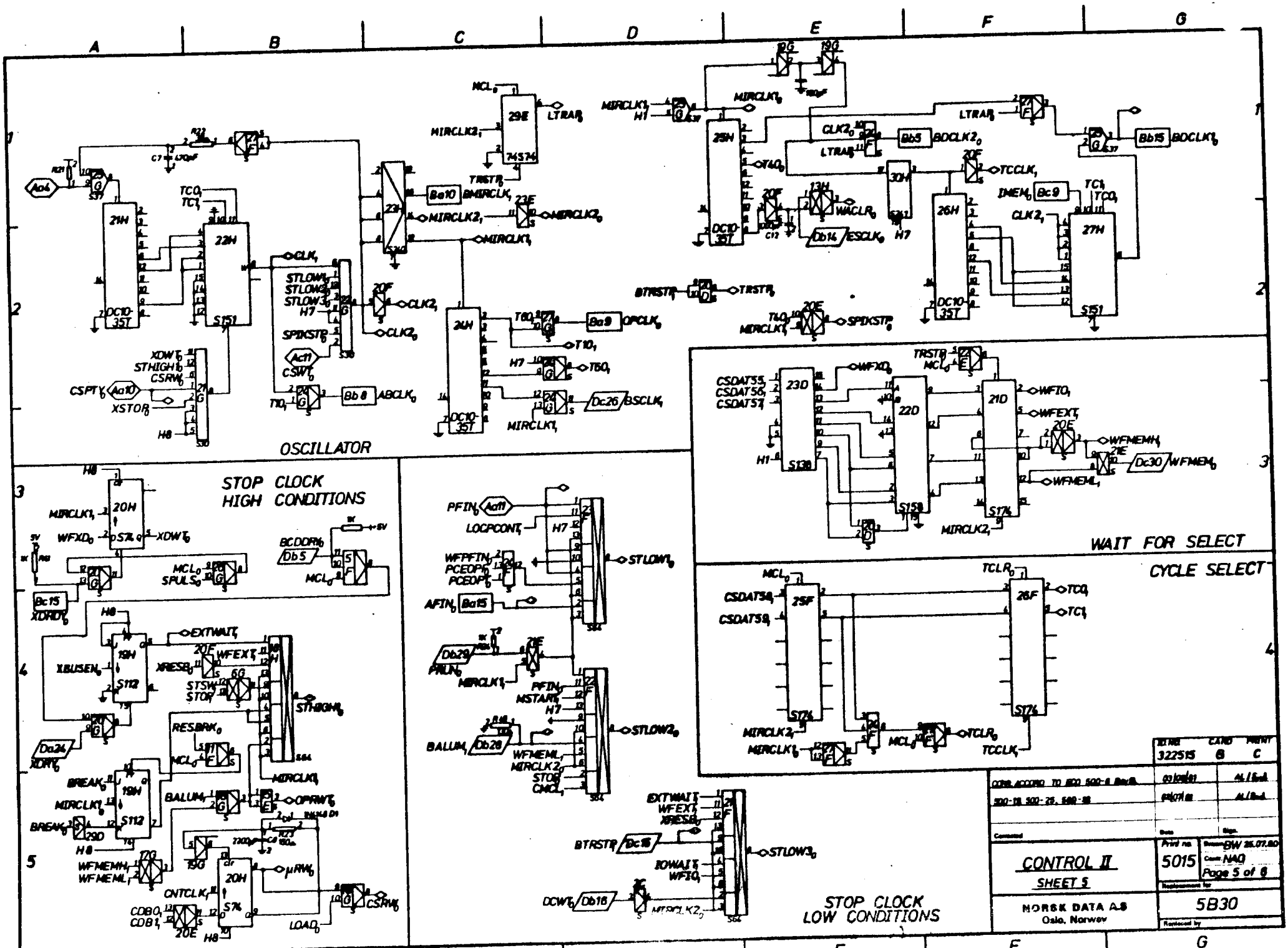


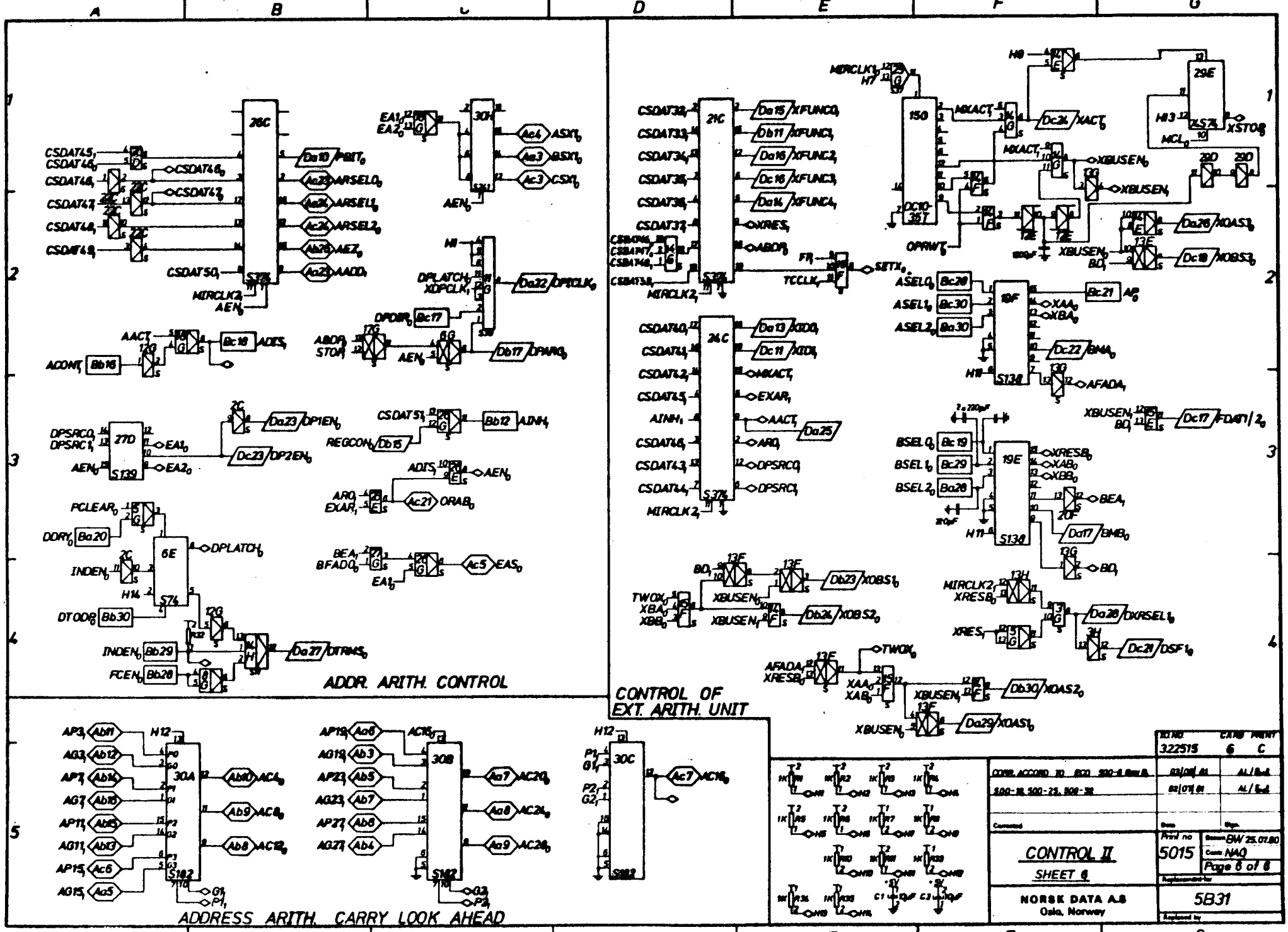
TD NO. 322515	CARD 6	PRINT C	
CORR. ACCORD TO ECO 500-6 Rev.B	83/08/81	AL/Sud	
502-18, 500-25, 500-32	09/07/81	AL/Sud	
Comment	Date	Sign.	
CONTROL II	Print no. 5015	Date BW 25.07.80	
SHEET 1		Code NAO	
		Page 1 of 6	
NORSK DATA A.S Oslo, Norway	Replacement for 5826		
	Replaced by		

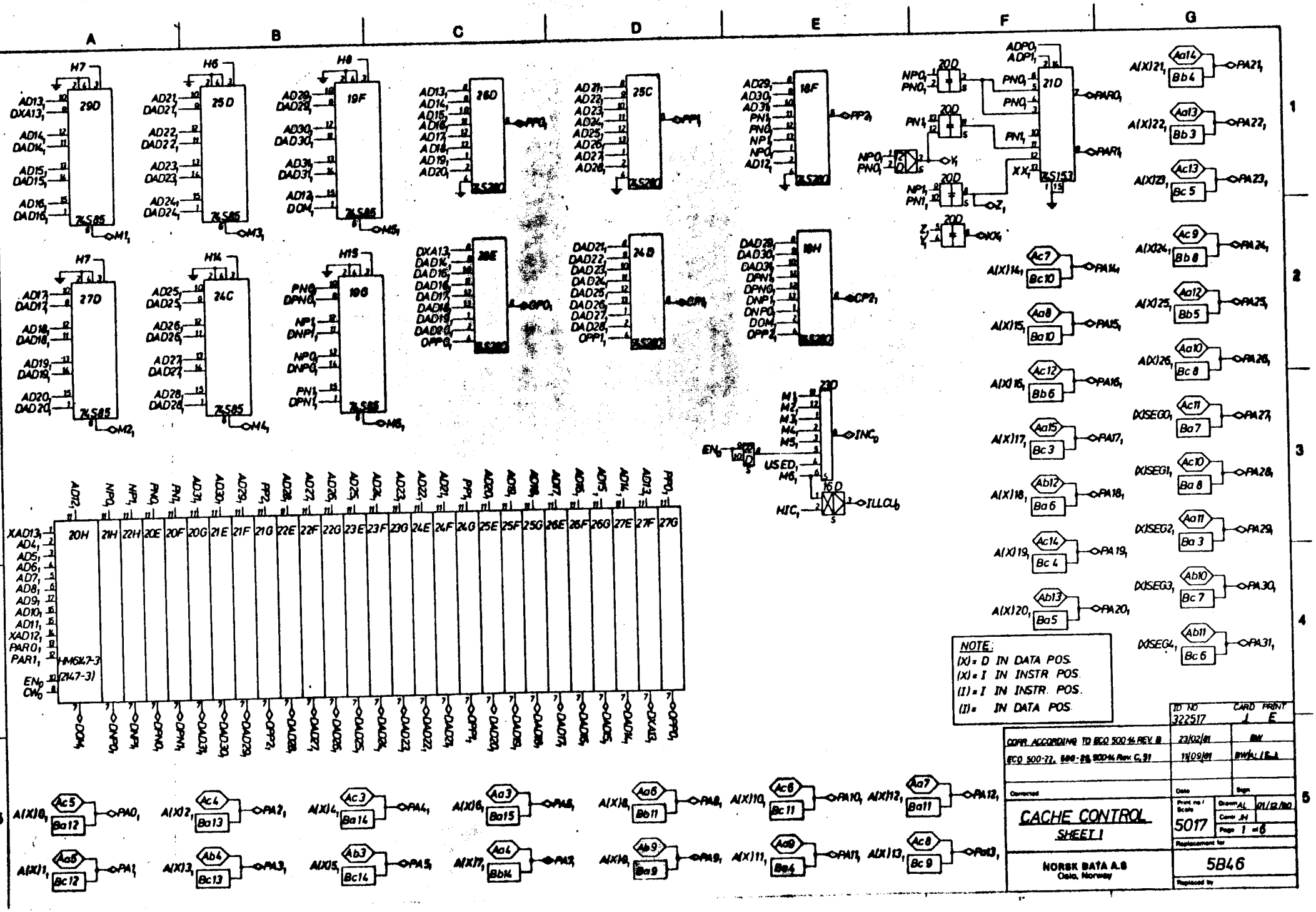

DATA IN REG.
DATA OUT REG.
WRITE ADDR REG.
BREAK REG.
TAG OUT REG.
CONTROL REG.
CONTROL II
SHEET 2
NORSK DATA A.S
Oslo, Norway
5015
5827
Page 2 of 6
BW 25.07.80
NAG

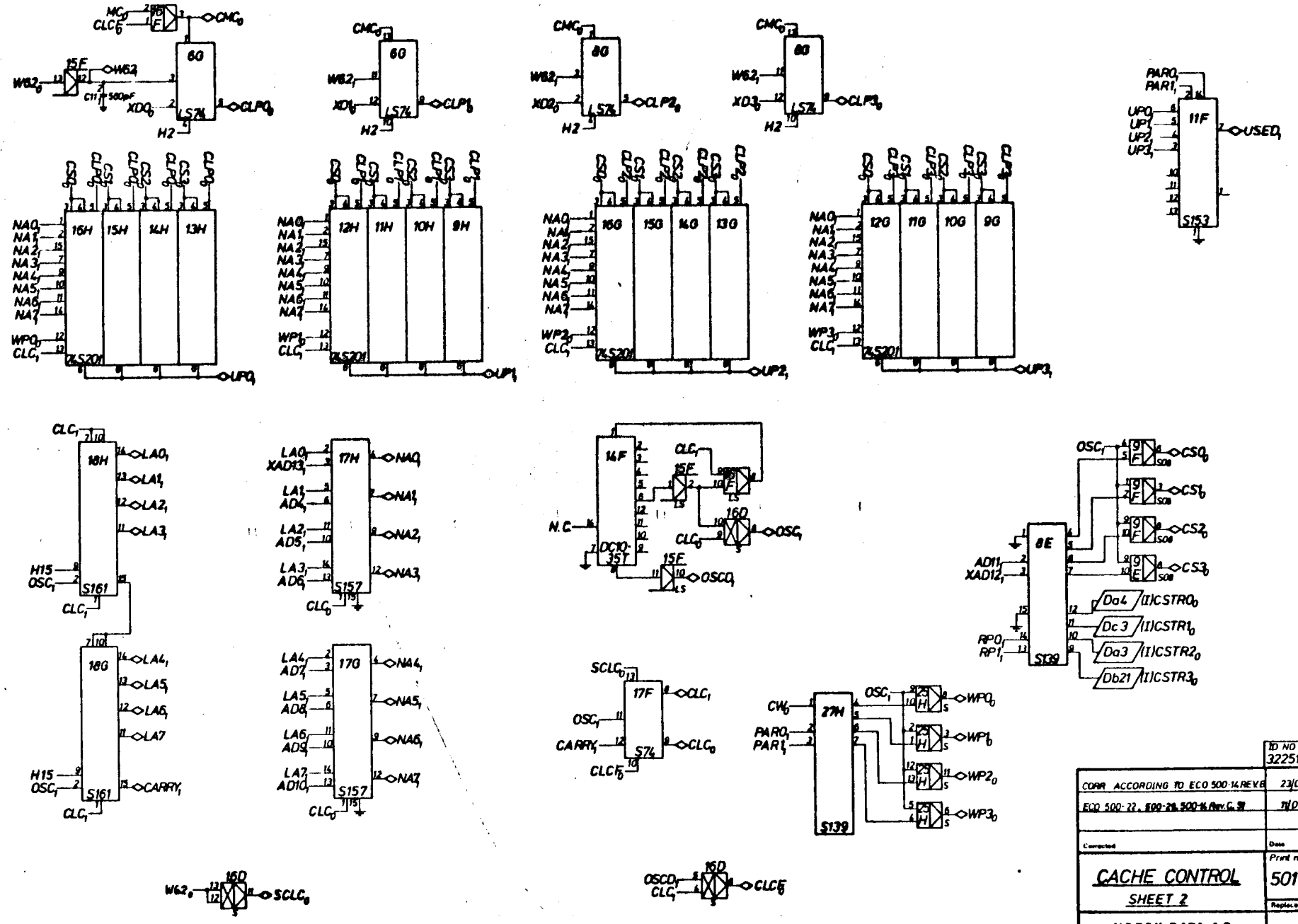

A
B
C
D
E
F
G
DUTEN0
H2
Ca2
Cc2
DBU0
DBU0
Ca3
Cc3
DBU1
DBU1
Ca4
Cc4
DBU2
DBU2
Ca5
Cc5
DBU3
DBU3
DUTEN1
Ca6
Cc6
DBU4
DBU4
Ca7
Cc7
DBU5
DBU5
Ca8
Cc8
DBU6
DBU6
Ca9
Cc9
DBU7
DBU7
H3
DUTEN2
Ca10
Cc10
DBU8
DBU8
Ca11
Cc11
DBU9
DBU9
Ca12
Cc12
DBU10
DBU10
Ca13
Cc13
DBU11
DBU11
H4
DUTEN3
Ca14
Cc14
DBU12
DBU12
Ca15
Cc15
DBU13
DBU13
Ca16
Cc16
DBU14
DBU14
Ca17
Cc17
DBU15
DBU15
DUT(0-15)1
DIN(0-15)1
TUTEN0
TUT0
TUT1
TUT2
TUT3
Ca18
Cc18
DTIN0
DTIN0
Ca19
Cc19
DTIN1
DTIN1
Ca20
Cc20
DTIN2
DTIN2
Ca21
Cc21
DTIN3
DTIN3
TIN0
TIN1
TIN2
TIN3
Ca22
Cc22
Ca28
Cc28
Db10
NEOTERM0
TIN4
ETIN4
DINTR1
DINTR0
Ca28
Cc28
IOINT0
Da30
DSTOP1
DSTOP0
Ca30
Cc30
DMSTRCL1
DMSTRCL0
Ca25
Cc25
DACTIVATE1
DACTIVATE0
Ca29
Cc29
DDATAOUT1
DDATAOUT0
Ca31
Cc31
MIRCLK2
HANGUP
STOP
Bb20
BSTOP
MMCL1
ACTIVATE1
DATAOUT1
DATAOUT1
Db4
DMCL0
EMCL0
Bc25
MMCL1
ACTIVATE1
MCL0
BACT1
Bc22
BMCL0
H1
CMCL1
DATAIN1
UNLOCK1
PWRFAIL0
Bc12
HANGUP1
Ca27
DDATAIN1
Cc27
DDATAIN0
Ca23
DUNLOCK1
Cc23
DUNLOCK0
Ca24
DPWRFAIL1
Cc24
DPWRFAIL0
Ca32
DHANGUP1
Cc32
DHANGUP0
MCL0
DATAOUT0
IODRY0
XTGUCLK1
H1
IOWAIT1
DATAIN1
MIRCLK1
HANGUP1
ØTP2
SETUN1
H1
DUNL0
UNLOCK1
BACT1
Db22
BIOACT0
DELACT20
RETTAG0
STOP0
TUTEN0
STOP0
TUT01
EDUTEN0
DUTEN0
MWCLR0
STOP0
STADREN1
EWACLK1
MRW1
LOAD0
MRWA0
Dc28
WAEN0
Dc29
SEQDES0
ID NO
322515
CARD PRINT
6
C
CORR ACCORD TO ECO 500-6 Rev.A
03/08/81
AL / Bud
500-19, 500-26, 500-28
02/07/81
AL / Bud
Comment
Date
Sign.
CONTROL II
SHEET 3
Print no
5015
Drawn BW 25.07.80
Conn NAO
Page 3 of 6
Replacement for
NORSK DATA A.S
Oslo, Norway
5B28
Replaced by


XD CONTROL
READ/ WRITE WCS
PREFETCH CONTROL
CONTROL II
SHEET 4
NORSK DATA A.S
Oslo, Norway
322515
5015
5829
Page 4 of 6

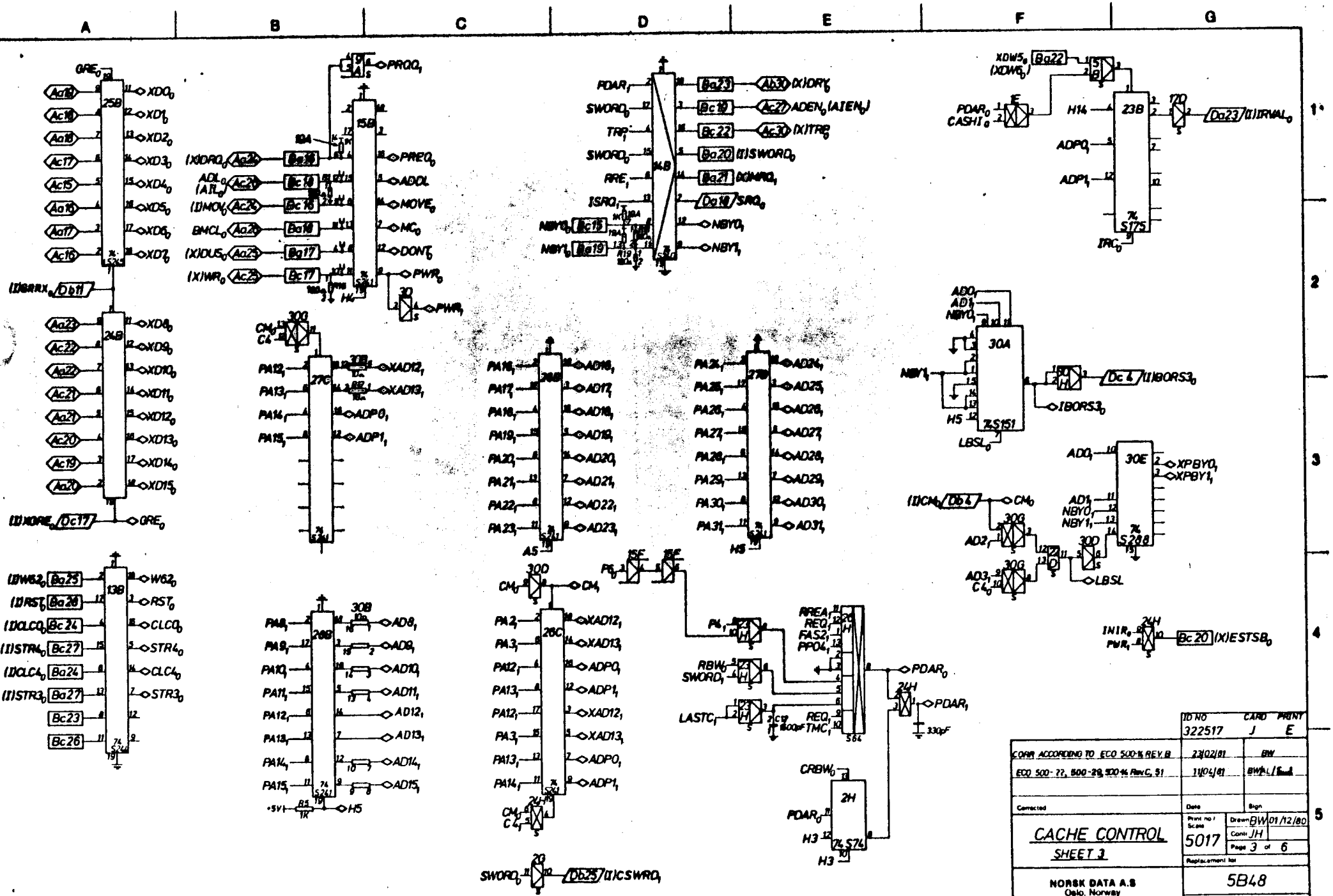

OSCILLATOR
STOP CLOCK HIGH CONDITIONS
WAIT FOR SELECT
CYCLE SELECT
STOP CLOCK LOW CONDITIONS
CONTROL II
SHEET 5
NORSK DATA A.S
Oslo, Norway
322515
5015
5B30
Page 5 of 8

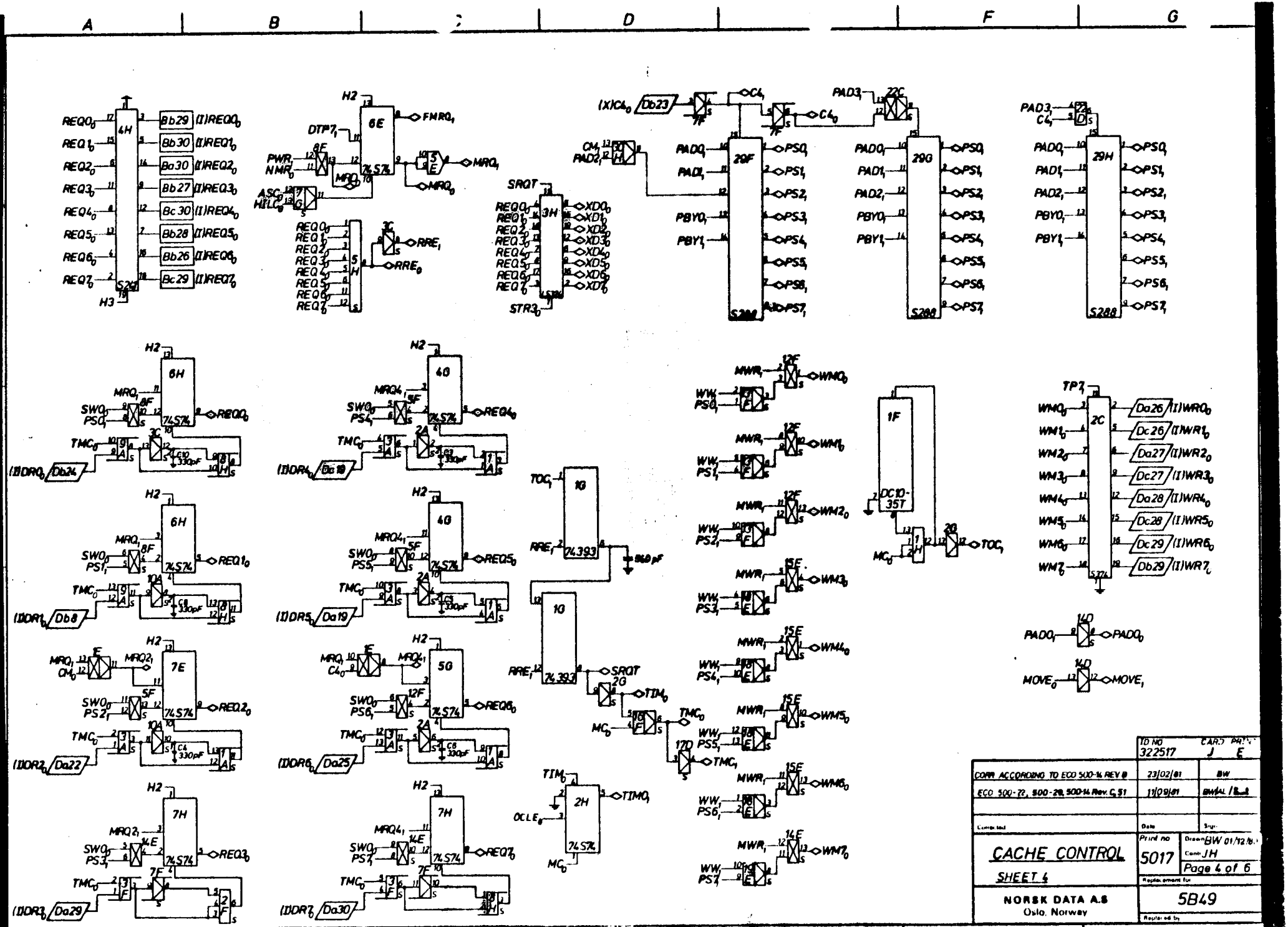

ADDR. ARITH. CONTROL
CONTROL OF EXT. ARITH. UNIT
ADDRESS ARITH. CARRY LOOK AHEAD
CONTROL II
SHEET 6
NORSK DATA A.S
Oslo, Norway
322515
5015
5831
Page 6 of 6

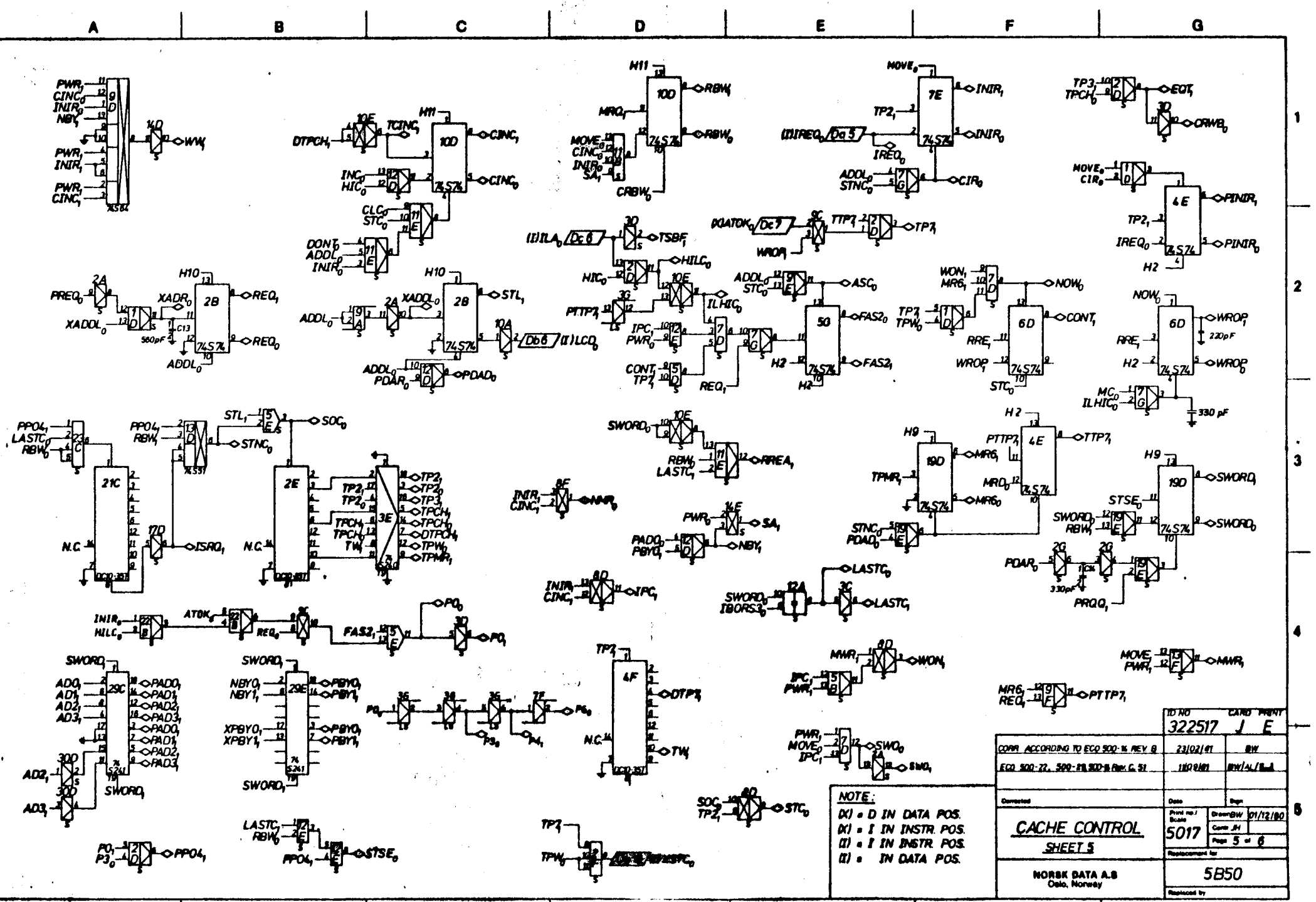

A
B
C
D
E
F
G
1
2
3
4
5
H7
29D
H6
25D
H8
19F
26D
25C
16F
20D
21D
H7
27D
H14
24C
H15
19G
28E
24B
19H
22D
16D
20H
21H
22H
20E
20F
20G
21E
21F
21G
22E
22F
22G
23E
23F
23G
24E
24F
24G
25E
25F
25G
26E
26F
26G
27E
27F
27G
(M6147-3)
(2147-3)
NOTE:
(X) = D IN DATA POS.
(X) = I IN INSTR. POS.
(I) = I IN INSTR. POS.
(I) = IN DATA POS.
ID NO 322517
CARD PRINT I E
CACHE CONTROL
SHEET 1
Print no / Scale 5017
Drawn AL 01/12/80
Page 1 of 6
NORSK DATA A.S
Oslo, Norway
5B46

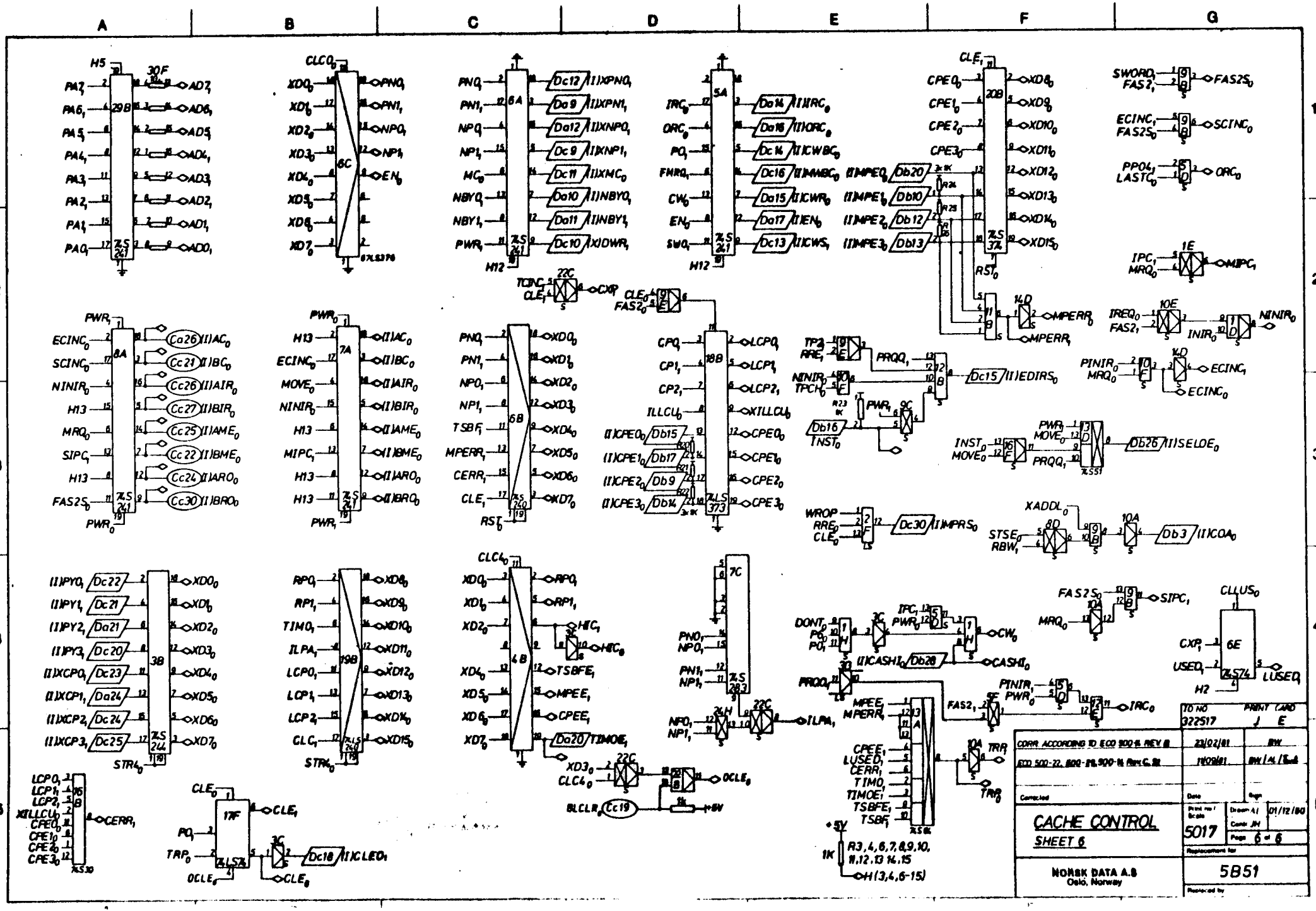


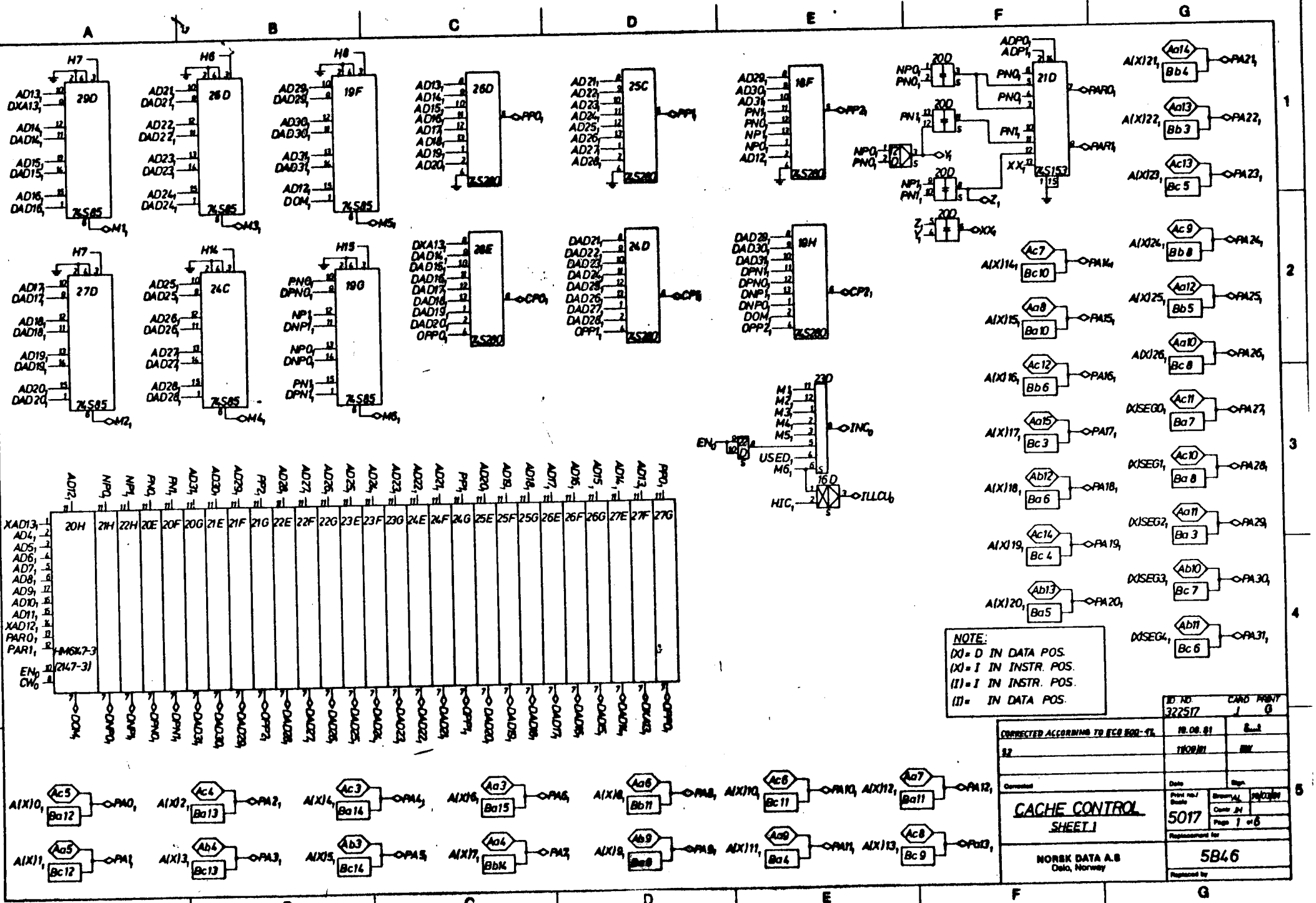
ID NO 322517		CARD J	PRINT E
CORR ACCORDING TO ECO 500-14 REV E	23/02/81	BW	
ECO 500-22, 500-23, 500-14 Rev G, SI	11/09/81	BW/AL/	
Corrected	Date	Sign	
CACHE CONTROL SHEET 2	Print no 5017	Drawn BW 01/12/80 Cont JH Page 2 of 6	
NORSK DATA A.S Oslo, Norway	Replacement for 5B47		
	Replaced by		

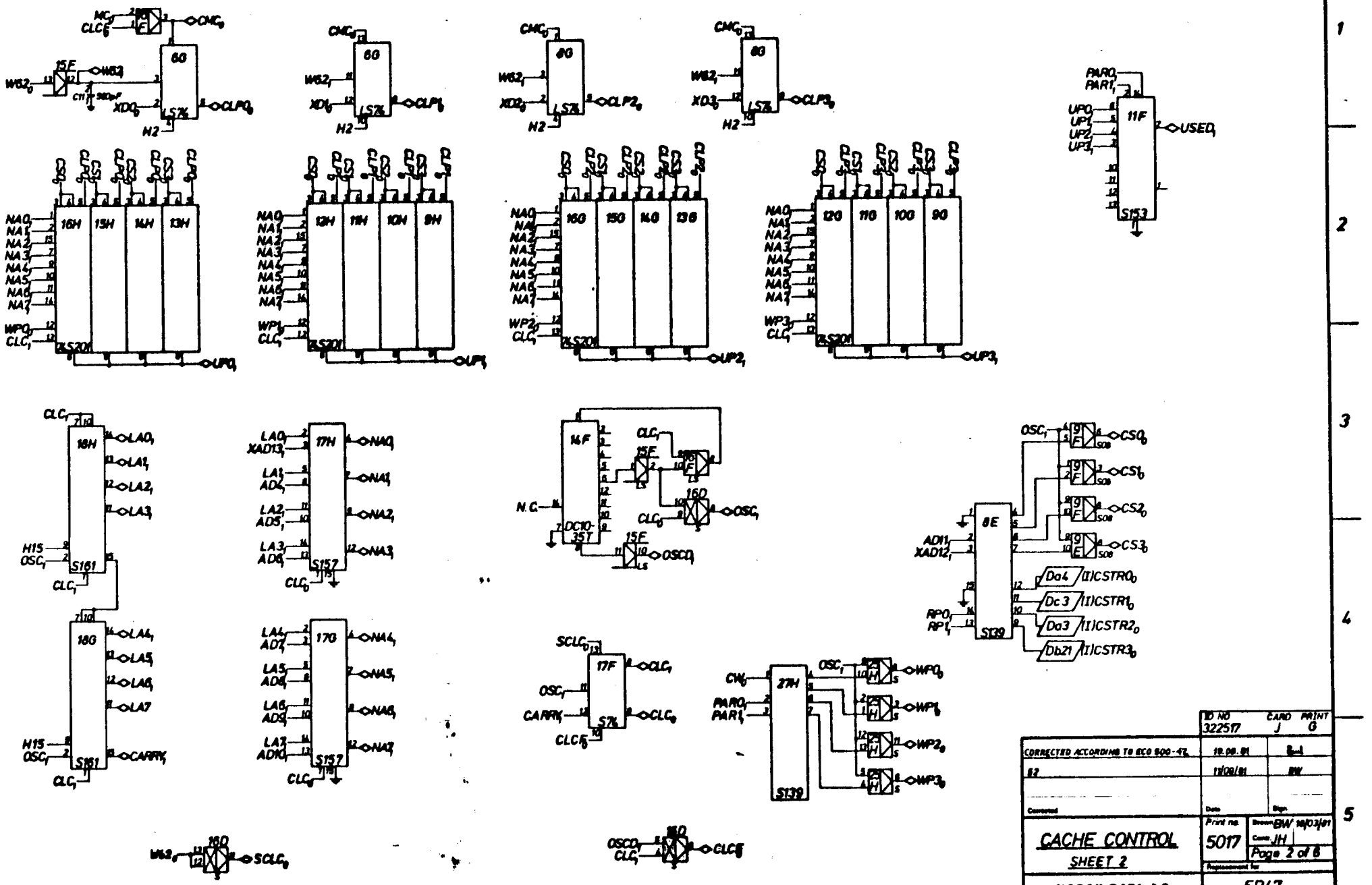

CACHE CONTROL
SHEET 3
NORSK DATA A.S
Oslo, Norway
ID NO 322517
CARD J
PRINT E
Print no / Scale 5017
Drawn BW 01/12/80
Page 3 of 6
Replacement for 5B48
Replaced by
CORR ACCORDING TO ECO 500-% REV. B 23/02/81 BW
ECO 500-77, 500-28, 500-% Rev C, 81 11/04/81 BW

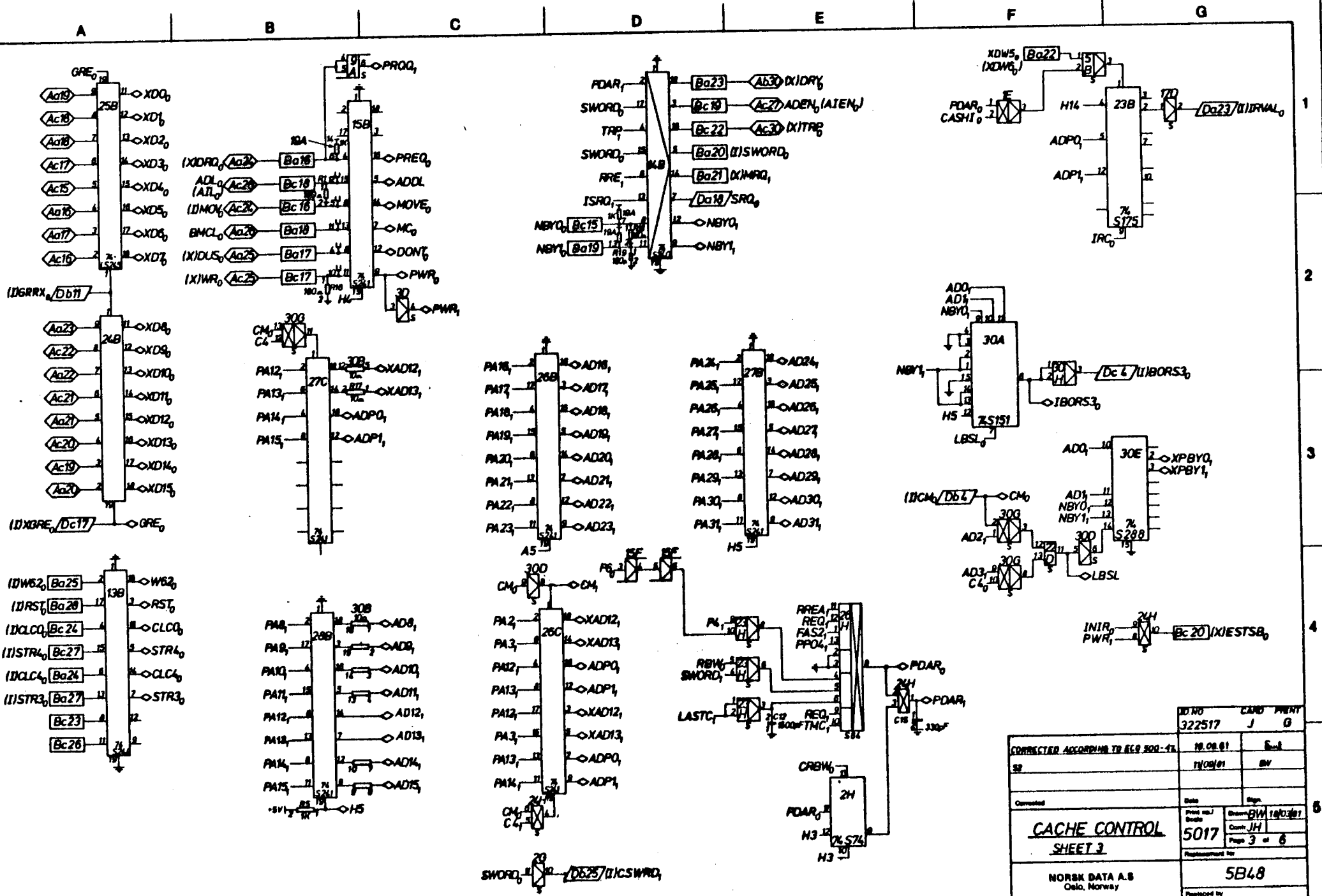

A
B
C
D
E
F
G
4H
6E
3H
20F
29G
29H
6H
4G
5G
7E
7H
1G
2H
1F
2C
TP7
MWR1
MWR2
MWR3
MWR4
MWR5
MWR6
MWR7
WM0
WM1
WM2
WM3
WM4
WM5
WM6
WM7
PAD0
MOVE
TOC
TIM
SRQT
FMRQ
MRQ
RRE
XD0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
PS0
PS1
PS2
PS3
PS4
PS5
PS6
PS7
REQ0
REQ1
REQ2
REQ3
REQ4
REQ5
REQ6
REQ7
(I)REQ0
(I)REQ1
(I)REQ2
(I)REQ3
(I)REQ4
(I)REQ5
(I)REQ6
(I)REQ7
(I)WRQ0
(I)WR1
(I)WR2
(I)WR3
(I)WR4
(I)WR5
(I)WR6
(I)WR7
(I)DRQ0
(I)DR1
(I)DR2
(I)DR3
(I)DR4
(I)DR5
(I)DR6
(I)DR7
Bb29
Bb30
Ba30
Bb27
Bc30
Bb28
Bb26
Bc29
Db24
Db8
Da22
Da29
Da18
Da19
Da25
Da30
Db23
Da26
Dc26
Da27
Dc27
Da28
Dc28
Dc29
Db29
74S74
74S00
74393
74S32
74S04
74S08
74S86
74S38
74S10
74S20
74S30
74S51
74S64
74S74
DC10-357
330pF
560pF
CORR ACCORDING TO ECO 500-14 REV B
23/02/81
BW
ECO 500-22, 500-28, 500-14 Rev. C, 51
11/09/81
BW/AL / BW
CACHE CONTROL
SHEET 4
Print no
5017
Drawn BW 01/12/81
Cont JH
Page 4 of 6
NORSK DATA A.S
Oslo, Norway
5B49
TD NO
322517
CARD PAT'N
J E

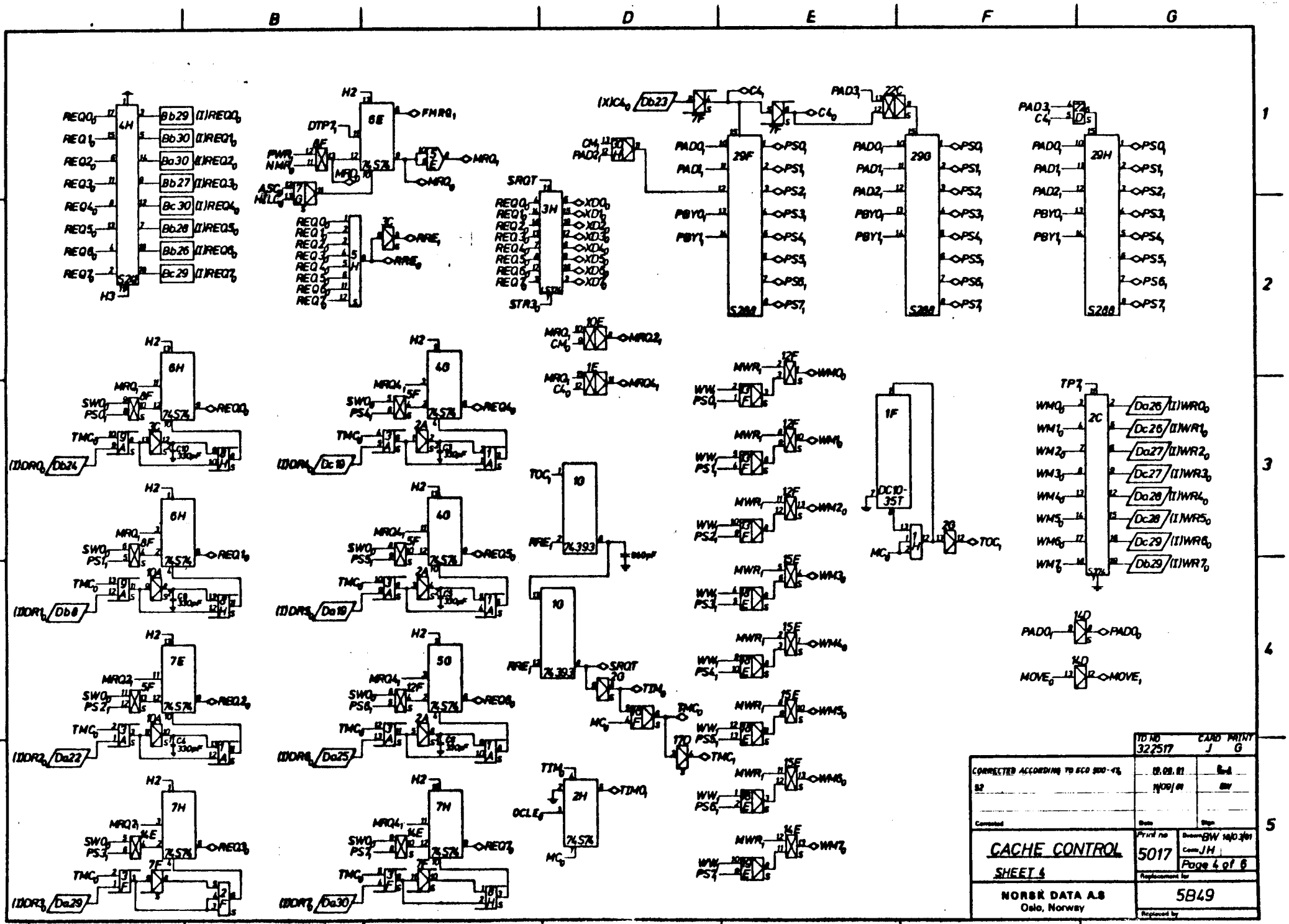

NOTE:
(X) = D IN DATA POS.
(X) = I IN INSTR. POS.
(I) = I IN INSTR. POS.
(I) = IN DATA POS.
CACHE CONTROL
SHEET 5
NORSK DATA A.S
Oslo, Norway
322517
5017
5850
CORR ACCORDING TO ECO 500-14 REV B
ECO 500-22, 500-19, 500-8 Rev C, 51
23/02/81
11/08/81
01/12/80
Sheet 5 of 6

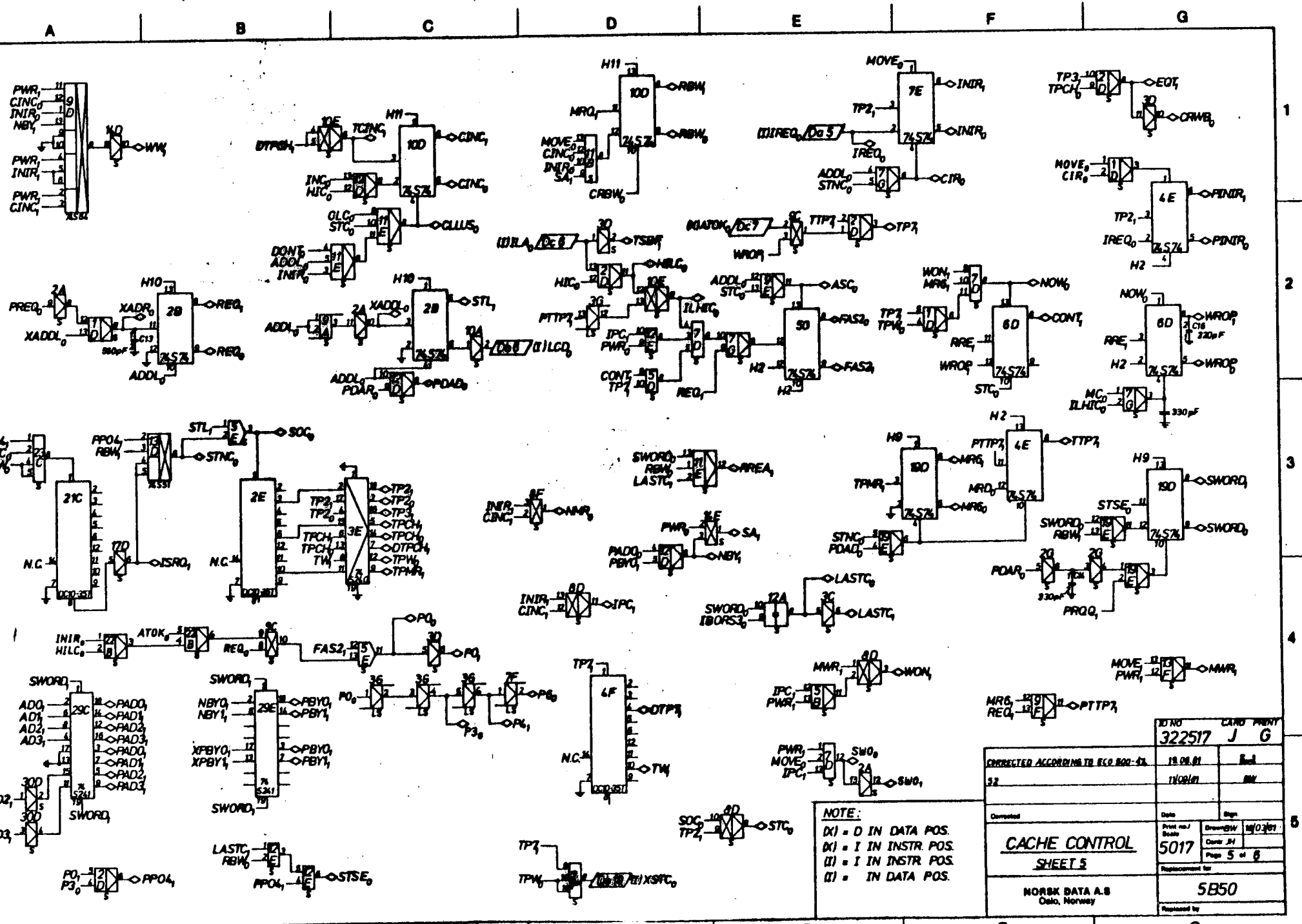

CACHE CONTROL
SHEET 6
NORSK DATA A.S
Oslo, Norway
5B51
5017
CORR ACCORDING TO ECO 900 % REV B
23/02/81
ECO 500-22, 800-28, 900-16 Rev C, D
19/08/81
Drawn AI
01/12/80
Page 6 of 6
TO NO 922517
PRINT CARD J E
R3,4,6,7,8,9,10,11,12,13 14,15
R(3,4,6-15)
1K
+5V

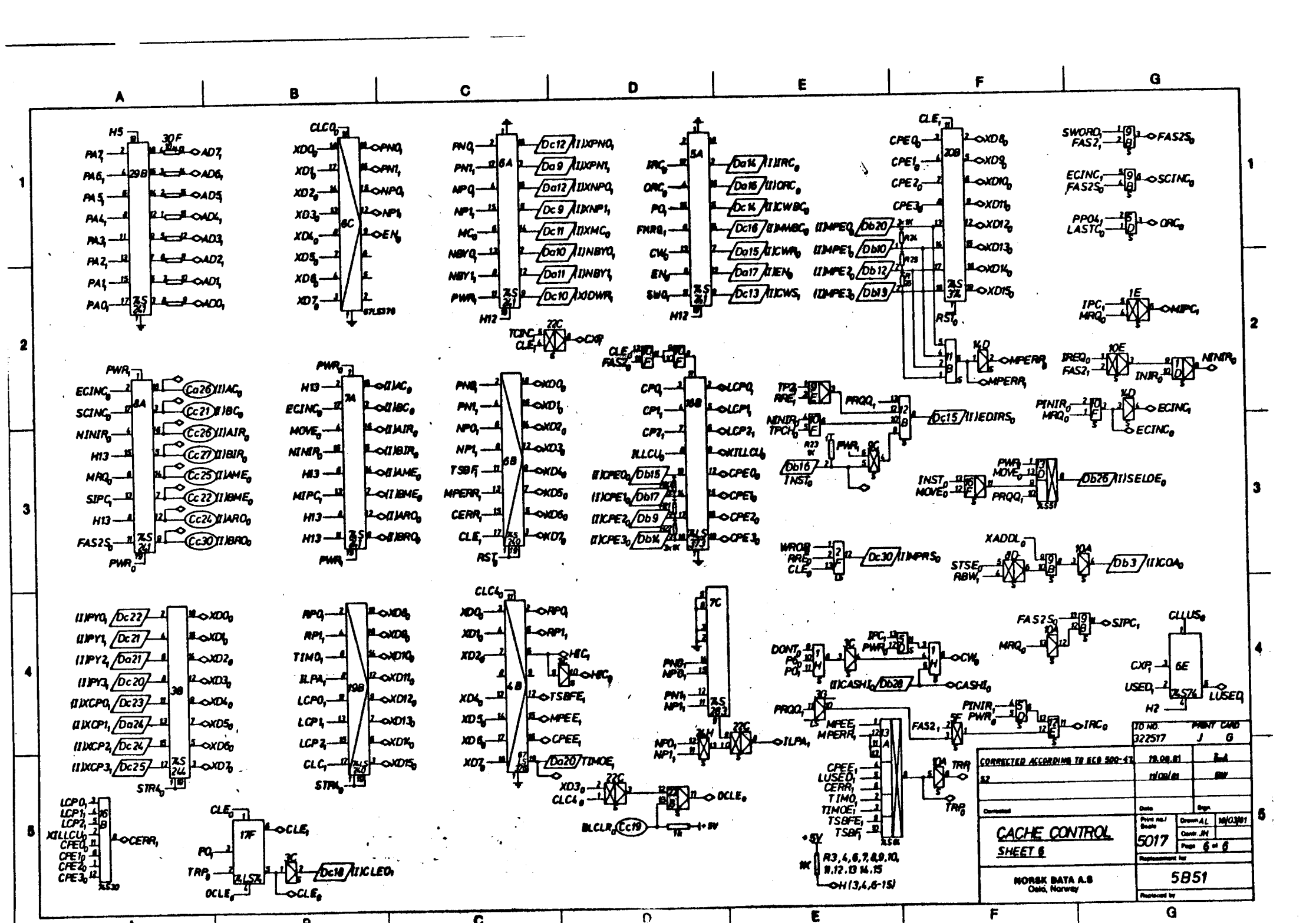

H7
29D
H6
28D
H8
19F
26D
25C
18F
20D
21D
H7
27D
H14
24C
H15
19G
26E
24D
18H
23D
16D
20H
21H
22H
20E
20F
20G
21E
21F
21G
22E
22F
22G
23E
23F
23G
24E
24F
24G
25E
25F
25G
26E
26F
26G
27E
27F
27G
HM6X7-3
(2147-3)
NOTE:
(X) = D IN DATA POS.
(X) = I IN INSTR. POS.
(I) = I IN INSTR. POS.
(I) = IN DATA POS.
CACHE CONTROL
SHEET 1
5017
5B46
NORSK DATA A.S
Oslo, Norway

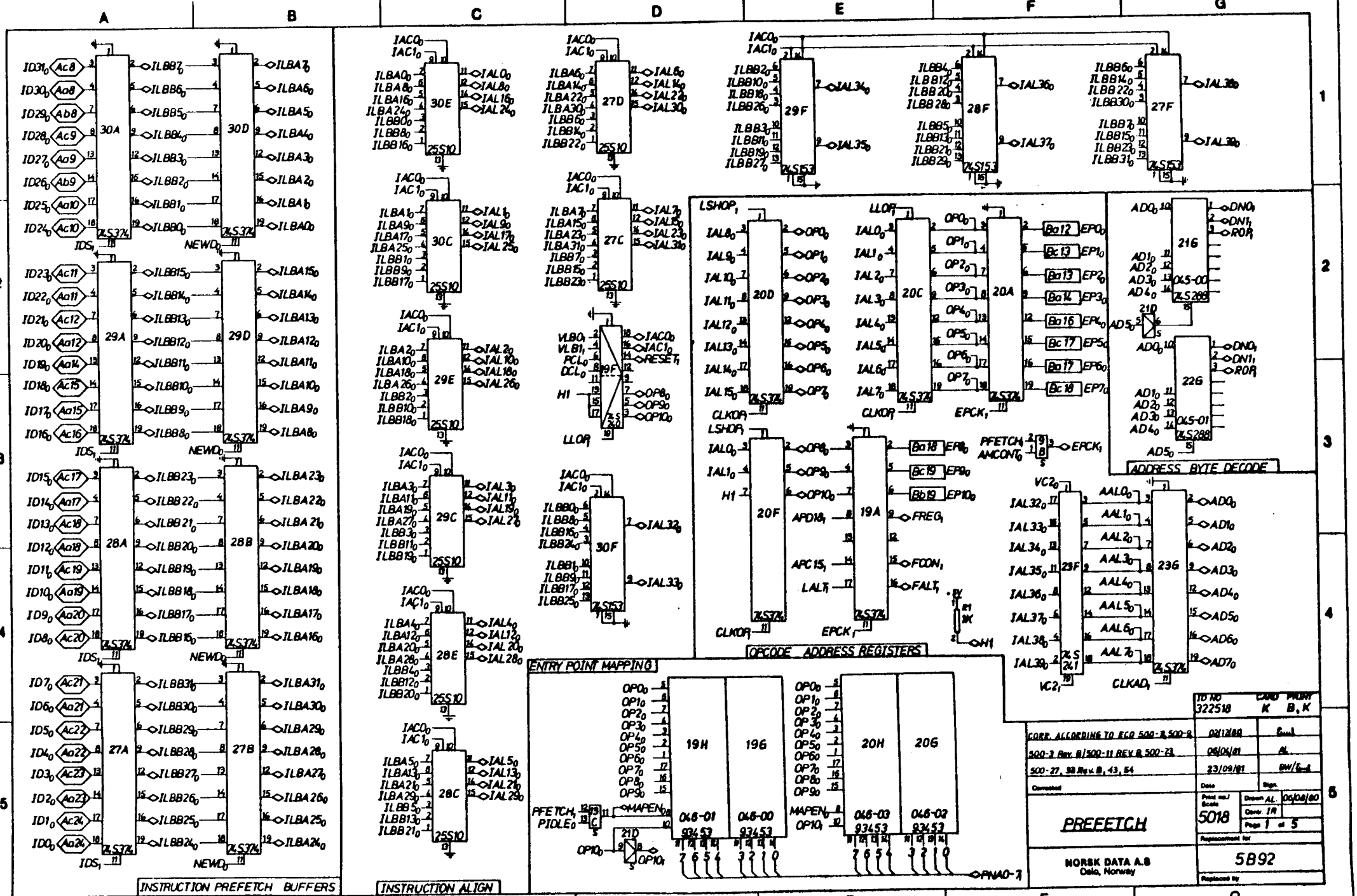

A
B
D
F
G
1
2
3
4
5
6G
15E
16H
15H
14H
13H
12H
11H
10H
9H
16G
15G
14G
13G
12G
11G
10G
9G
11F
S153
S201
18H
18G
S161
17H
17G
S157
14F
16D
DC10-357
8E
S139
27H
17F
S74
16D
S08
CSQ0
CS10
CS20
CS30
Da4 (I)CSTR0
Dc3 (I)CSTR1
Da3 (I)CSTR2
Db21 (I)CSTR3
WP0
WP1
WP2
WP3
USED
CLP0
CLP1
CLP2
CLP3
SCLC0
CLC0
CARRY
ID NO 322517
CARD J
PRINT G
CORRECTED ACCORDING TO ECO 500-47
10.09.81
B=1
B2
13/09/81
BW
Comment
Date
Sign
CACHE CONTROL
SHEET 2
Print no. 5017
Drawn BW 16/03/81
Contr. JH
Page 2 of 8
NORSK DATA A.S
Oslo, Norway
5847
Replaced by

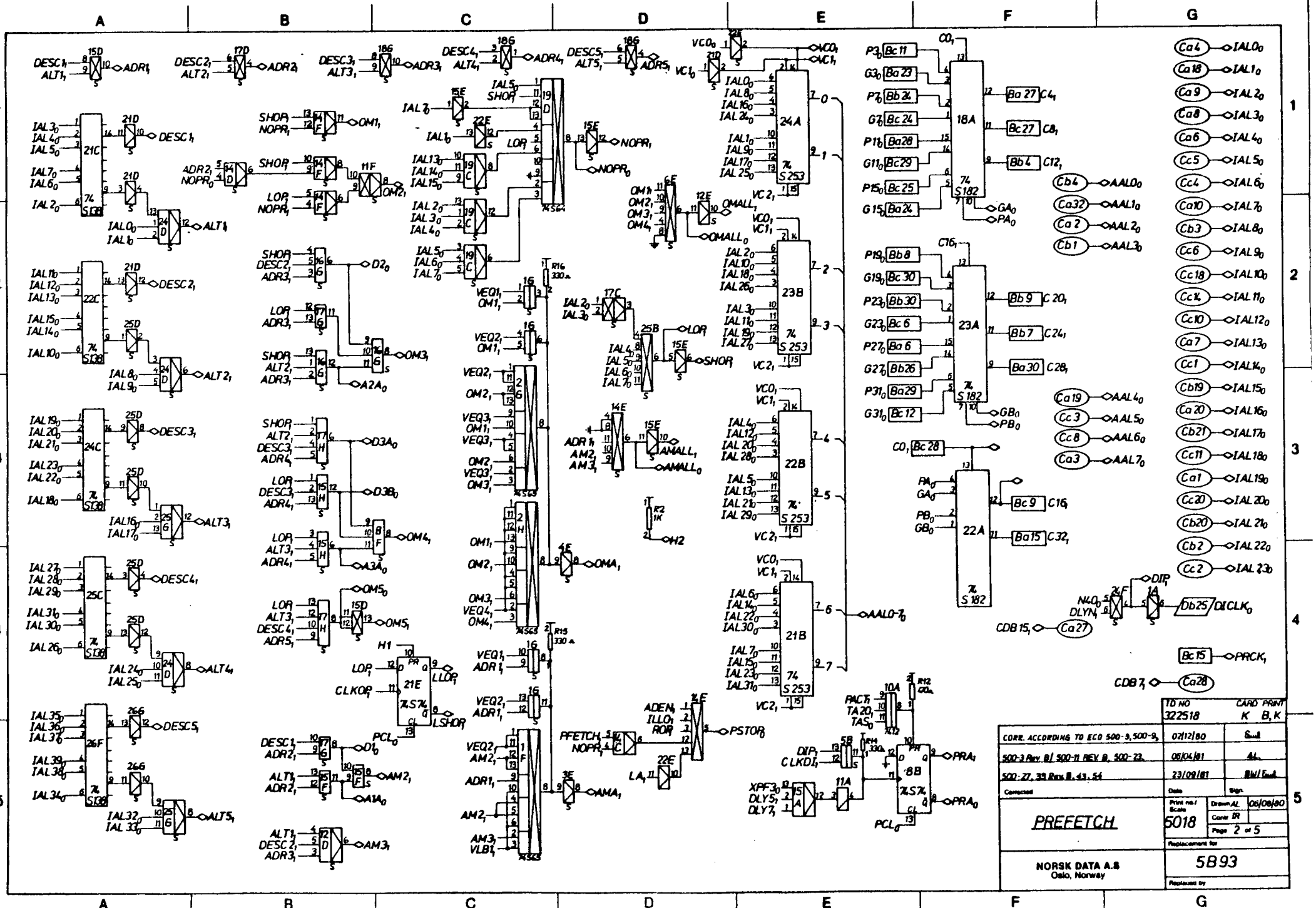

CACHE CONTROL
SHEET 3
NORSK DATA A.S
Oslo, Norway
5017
5B48
322517
CORRECTED ACCORDING TO ECO 500-15
CACHE
PROQ
PREQ
ADOL
MOVE
MC
DONE
PWR
HC
XDRQ
ADL
MOV
BMCL
DUS
WR
XAD12
XAD13
ADP0
ADP1
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
H5
A5
CM
CM4
C4
XDO0
XD1
XD2
XD3
XD4
XD5
XD6
XD7
XD8
XD9
XD10
XD11
XD12
XD13
XD14
XD15
GRE
XGRE
GRRX
W62
RST
CLC0
STR4
CLC4
STR3
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
PDAR
SWORD
TRP
RRE
ISRQ
NBY0
NBY1
DRY
ADEN
IXTRP
SWORD
IXMRQ
SRQ
IRVAL
ADP0
ADP1
IRC
ADO
AD1
BORS3
LBSL
XPBY0
XPBY1
AD2
AD3
LBSL
INIR
PWR
IESTSB
RREA
REQ
FAS2
PPO4
RBW
SWORD
LASTC
REQ
THC
CRBW
H3

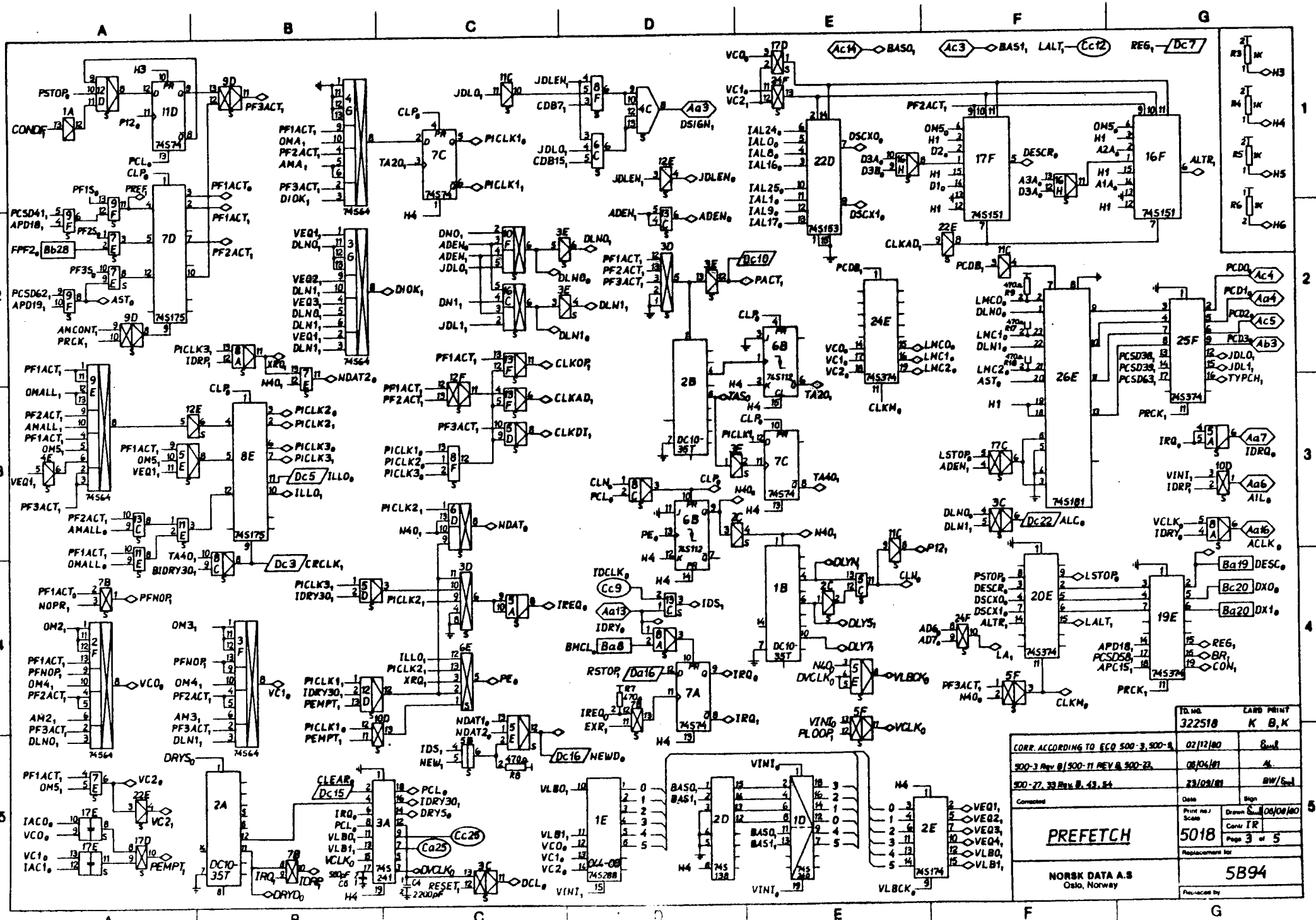

B
D
E
F
G
1
2
3
4
5
4H
6E
3H
29F
29G
29H
3C
6H
4G
5F
2A
7E
5G
12F
15F
14E
1F
DC10-35T
2C
10
2H
1C
1D
1E
1O
2O
7H
7F
10A
8F
8E
10E
12E
14E
15E
2B
1O
TP7
WM0 0
WM1 0
WM2 0
WM3 0
WM4 0
WM5 0
WM6 0
WM7 0
Da26 (I)WR0 0
Dc26 (I)WR1 0
Da27 (I)WR2 0
Dc27 (I)WR3 0
Da28 (I)WR4 0
Dc28 (I)WR5 0
Dc29 (I)WR6 0
Db29 (I)WR7 0
PADO1
PADO0
MOVE0
MOVE1
TOC1
TOC0
MRQ2 1
MRQ4 1
MRQ1
MRQ0
FMRQ1
RRE1
RRE0
SRQT
STR3 0
TIM1
TIM0
OCLE0
MC0
TMC1
TMC0
(I)DRQ0 Db24
(I)DRQ1 Db8
(I)DRQ2 Da22
(I)DRQ3 Da29
(I)DRQ4 Dc18
(I)DRQ5 Da18
(I)DRQ6 Da25
(I)DRQ7 Da30
(X)CA0 Db23
(I)REQ0 0
(I)REQ1 0
(I)REQ2 0
(I)REQ3 0
(I)REQ4 0
(I)REQ5 0
(I)REQ6 0
(I)REQ7 0
Db29
Bb30
Ba30
Bb27
Bc30
Bb28
Bb26
Bc29
XDO0
XDO1
XDO2
XDO3
XDO4
XDO5
XDO6
XDO7
PS0 1
PS1 1
PS2 1
PS3 1
PS4 1
PS5 1
PS6 1
PS7 1
PADO1
PAD1 1
PAD2 1
PBY0 1
PBY1 1
C4 1
C4 0
PAD3 1
C4 1
WW PS0 1
WW PS1 1
WW PS2 1
WW PS3 1
WW PS4 1
WW PS5 1
WW PS6 1
WW PS7 1
MWR 1
WM0 0
WM1 0
WM2 0
WM3 0
WM4 0
WM5 0
WM6 0
WM7 0
S288
7%393
7%S74
330pF
680pF
CORRECTED ACCORDING TO ECO 5100-4%
B2
Corrected
Date
Sign
TD NO 322517
CARD PRINT J G
CACHE CONTROL
SHEET 4
Print no 5017
Drawn BW 14/03/81
Chk JH
Page 4 of 6
Replacement for
NORSK DATA A.S
Oslo, Norway
5849
Replaced by

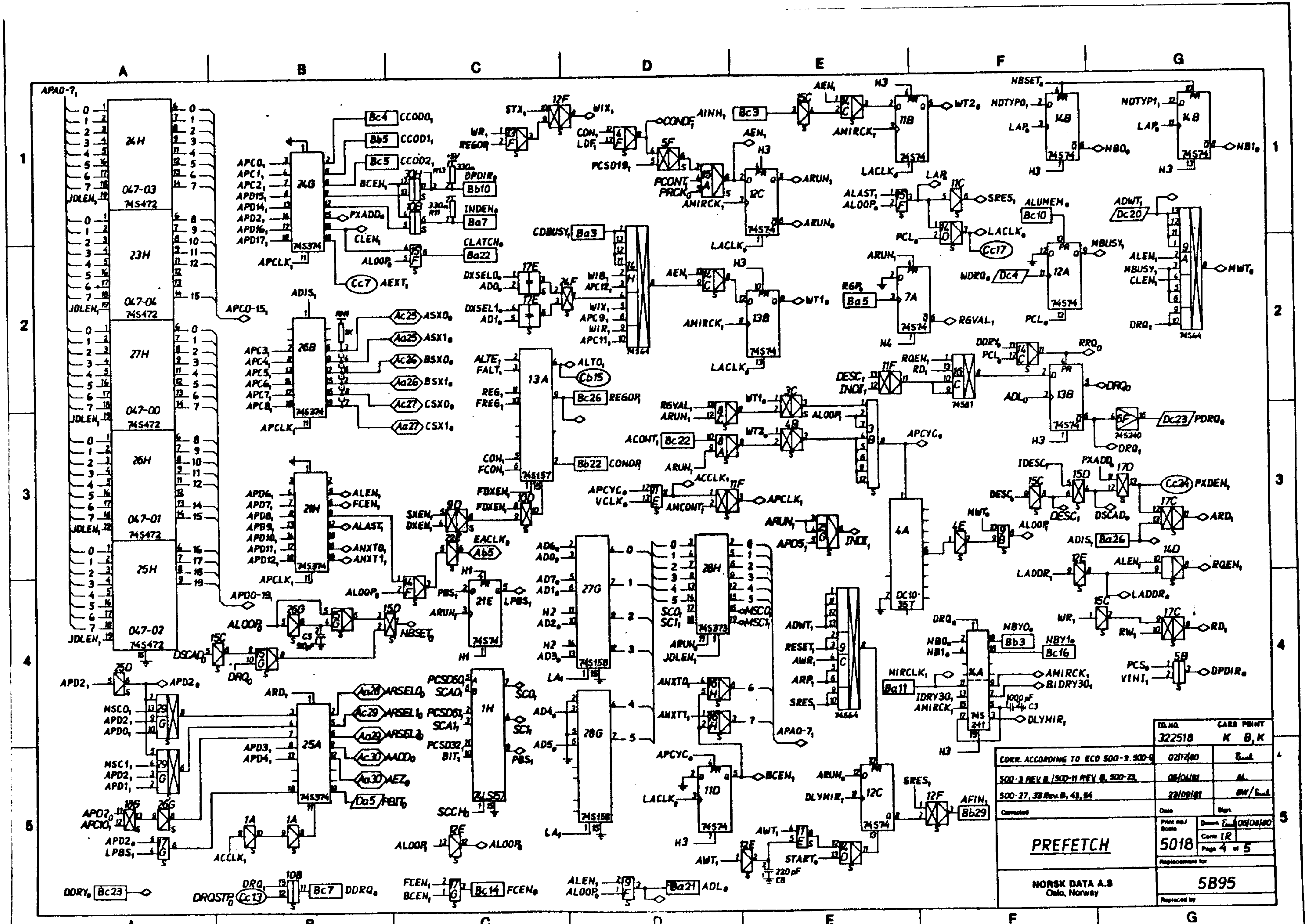

NOTE:
(X) = D IN DATA POS.
(X) = I IN INSTR. POS.
(I) = I IN INSTR. POS.
(I) = IN DATA POS.
ID NO 322517 CARD PRINT J G
CORRECTED ACCORDING TO ECO 800-42 19.06.81
CACHE CONTROL
SHEET 5
NORSK DATA A.S
Oslo, Norway
5017
5B50
Page 5 of 6

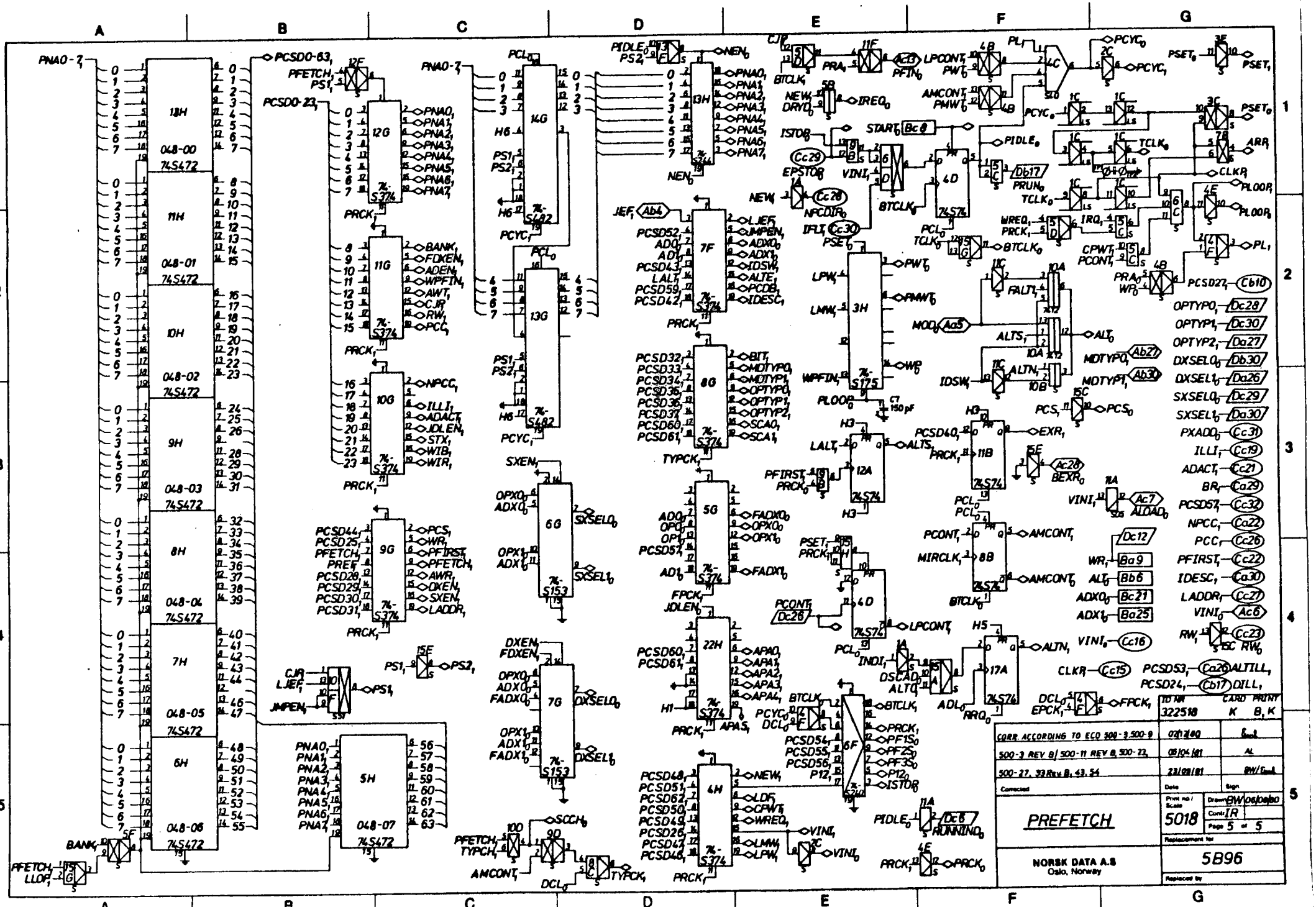

CACHE CONTROL
SHEET 6
NORSK DATA A.S
Oslo, Norway
5017
5851
322517
CORRECTED ACCORDING TO ECO 500-47
19.08.81
Drawn AL
Check JH
Page 6 of 6
Replacement for
Replaced by
R3,4,6,7,8,9,10,
11,12,13 14,15
H(3,4,6-15)

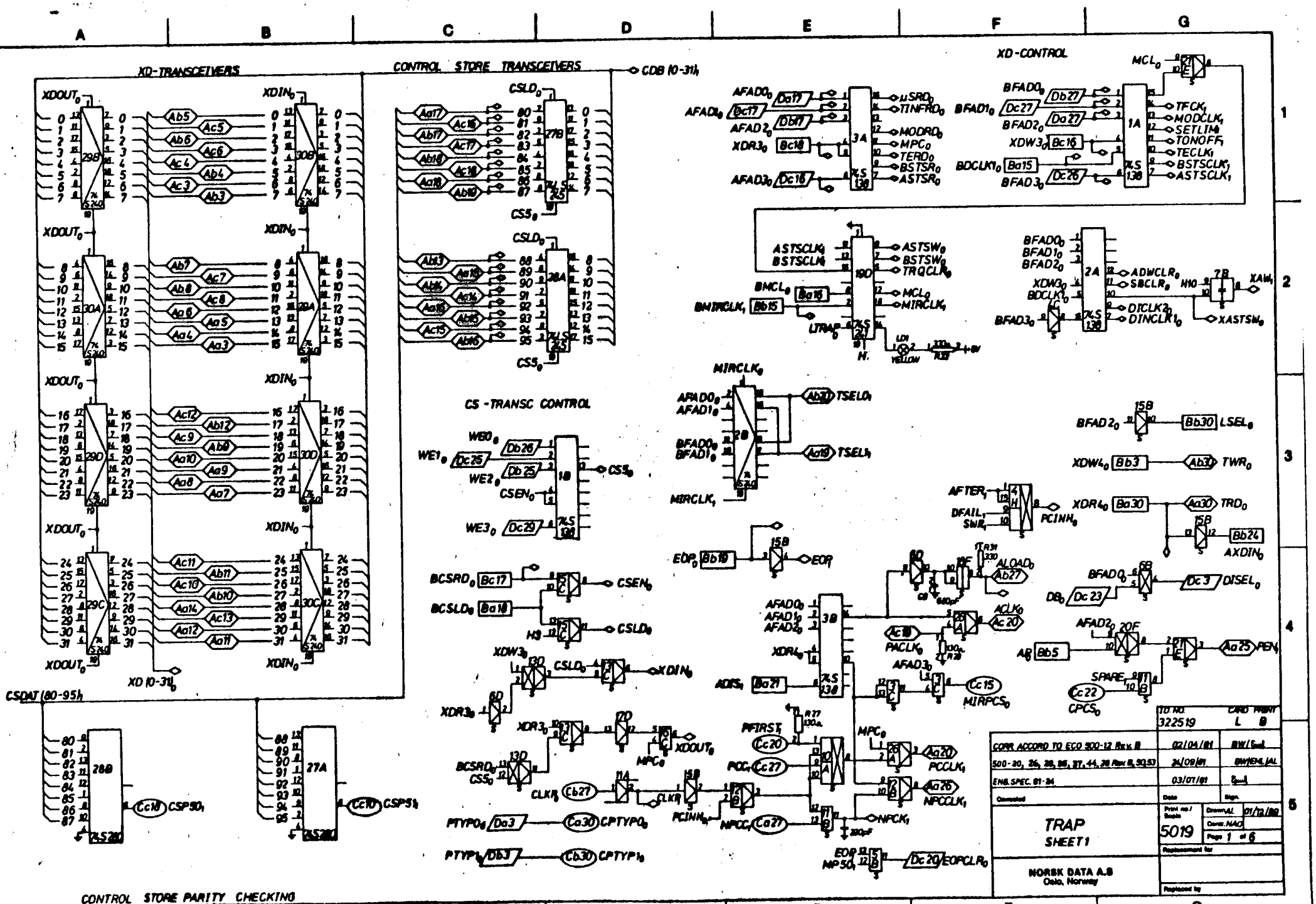

INSTRUCTION PREFETCH BUFFERS
INSTRUCTION ALIGN
OPCODE ADDRESS REGISTERS
ENTRY POINT MAPPING
ADDRESS BYTE DECODE
PREFETCH
NORSK DATA A.S
Oslo, Norway
5892
5018
322518
CORR. ACCORDING TO ECO 500-8,500-9
500-3 Rev. B/500-11 REV B 500-23
500-27, 38 Rev. B, 43, 54
02/12/80
06/04/81
23/09/81
Page 1 of 5

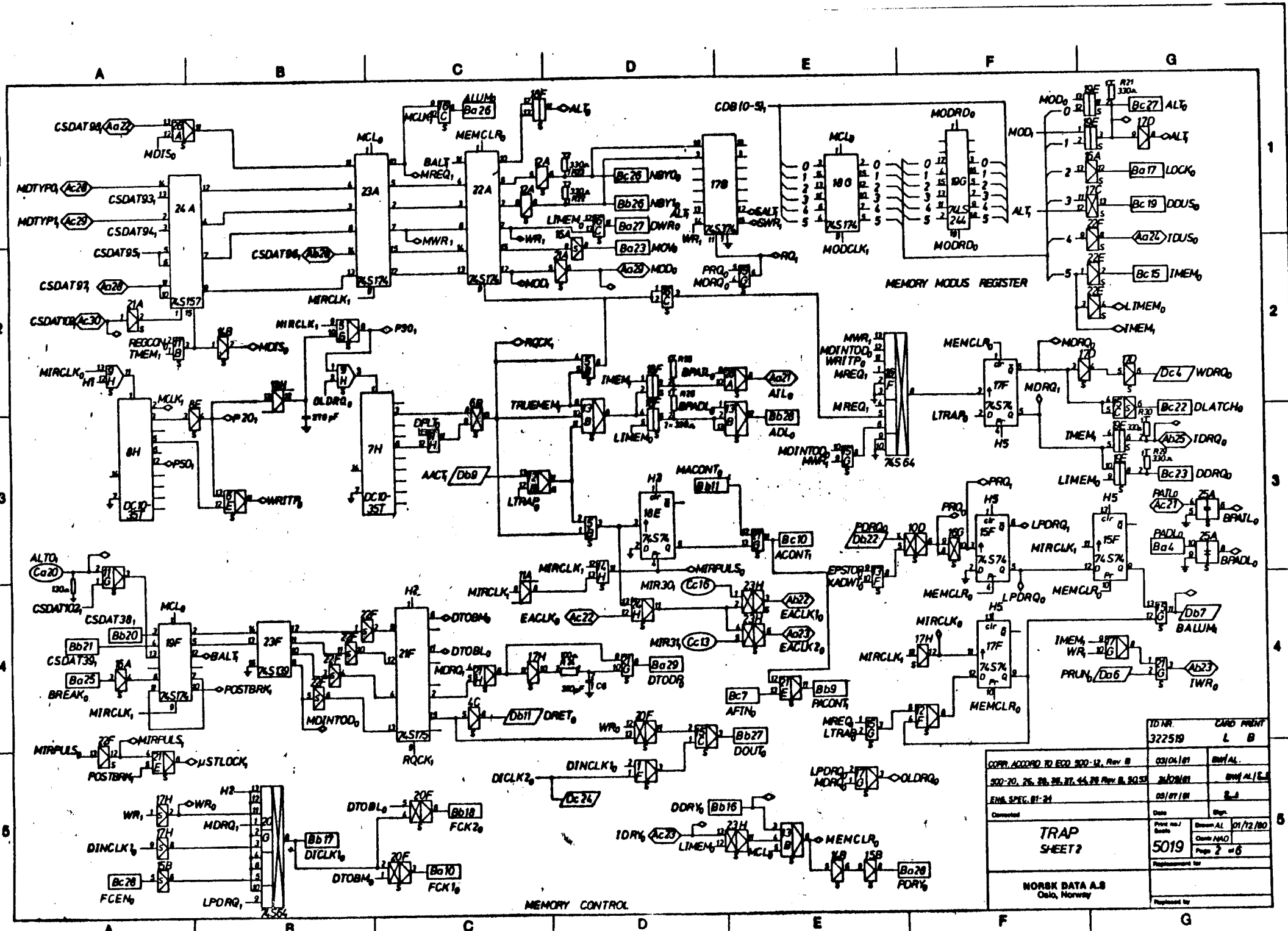

A
B
C
D
E
F
G
1
2
3
4
5
DESC1, ALT1, 15D, ADR1,
DESC2, ALT2, 17D, ADR2,
DESC3, ALT3, 18G, ADR3,
DESC4, ALT4, 18G, ADR4,
DESC5, ALT5, 18G, ADR5,
21C, 74S08, DESC1, ALT1, ALT2, DESC2,
22C, 74S08, DESC2, ALT2, ALT3, DESC3,
24C, 74S08, DESC3, ALT3, ALT4, DESC4,
25C, 74S08, DESC4, ALT4, ALT5, DESC5,
26F, 74S08, DESC5, ALT5,
SHOR, NOPR, OM1, OM2, LOR, OM3, OM4, OM5, A2A0, D2, D3A0, D3B0, A3A0, D1, AM2, A1A0, AM3,
21E, 74S74, LLOR, LSHOR, PCL0,
IAL5, SHOR, LOR, NOPR1, NOPR0, 24S64,
IAL7, IAL6, IAL4, IAL3, IAL2, 24S64,
VEQ1, OM1, VEQ2, OM1, VEQ2, OM2, VEQ3, OM1, VEQ3, OM2, VEQ2, OM3, VEQ4, OM4, 24S63,
R16 330A, R15 330A, R2 1K, H2, OMA1, AMA1,
ADR1, AM2, AM3, VLB1, 24S63,
IAL2, IAL3, 17C, 25B, LOR, IAL4, IAL5, IAL6, IAL7, 15E, SHOR,
ADR1, AM2, AM3, 14E, 15E, AMALL1, AMALL0,
OM1, OM2, OM3, OM4, 6E, 12E, OMALL1, OMALL0,
ADEN, ILLO, ROR, 14E, PSTOR0,
PFETCH, NOPR, 22E, LA11,
VCO0, VC0, VC1, VC1, VC2, 24A, IAL0, IAL8, IAL16, IAL24, IAL1, IAL9, IAL17, IAL25, 74S253,
VCO1, VC1, VC2, 23B, IAL2, IAL10, IAL18, IAL26, IAL3, IAL11, IAL19, IAL27, 74S253,
VCO1, VC1, VC2, 22B, IAL4, IAL12, IAL20, IAL28, IAL5, IAL13, IAL21, IAL29, 74S253,
VCO1, VC1, VC2, 21B, IAL6, IAL14, IAL22, IAL30, IAL7, IAL15, IAL23, IAL31, 74S253,
AALO-7,
CO1, P3 Bc11, G3 Ba23, P7 Bb24, G7 Bc24, P11 Ba28, G11 Bc29, P15 Bc25, G15 Ba24, 18A, 74S182, Ba27 C4, Bc27 C8, Bb4 C12, GA0, PA0,
C16, P19 Bb8, G19 Bc30, P23 Bb30, G23 Bc6, P27 Ba6, G27 Bb26, P31 Ba29, G31 Bc12, 23A, 74S182, Bb9 C20, Bb7 C24, Ba30 C28, GB0, PB0,
CO, Bc28, PA0, GA0, PB0, GB0, 22A, 74S182, Bc9 C16, Ba15 C32,
Cb4 AALO0, Ca32 AAL10, Ca2 AAL20, Cb1 AAL30,
Ca19 AAL40, Cc3 AAL50, Cc8 AAL60, Ca3 AAL70,
Ca4 IALO0, Ca18 IAL10, Ca9 IAL20, Ca8 IAL30, Ca6 IAL40, Cc5 IAL50, Cc4 IAL60, Ca10 IAL70, Cb3 IAL80, Cc6 IAL90, Cc18 IAL100, Cc14 IAL110, Cc10 IAL120, Ca7 IAL130, Cc1 IAL140, Cb19 IAL150, Ca20 IAL160, Cb21 IAL170, Cc11 IAL180, Ca1 IAL190, Cc20 IAL200, Cb20 IAL210, Cb2 IAL220, Cc2 IAL230,
DIP, 14, N40, DLYN, 24F, Db25/DICLK0, CDB15, Ca27,
Bc15 PRCK1, CDB7, Ca28,
PACT, TA20, TAS0, 10A, R12 220A, XX12, 58, RM 330A, DIP, CLKDI, 8B, PRA1, PRA0, XPF30, DLY5, DLY7, 11A, PCL0,
TO NO 322518, CARD PRINT K B,K
CORR. ACCORDING TO ECO 500-3, 500-9, 07/12/80, Emil
500-3 Rev B/ 500-11 REV B, 500-23, 06/04/81, AL
500-27, 33 Rev B, 43, 54, 23/09/81, Emil/Emil
Corrected, Date, Sign.
PREFETCH
Print no./Scale 5018
Drawn AL 06/08/80
Contr BR
Page 2 of 5
Replacement for 5B93
NORSK DATA A.S Oslo, Norway
Replaces by

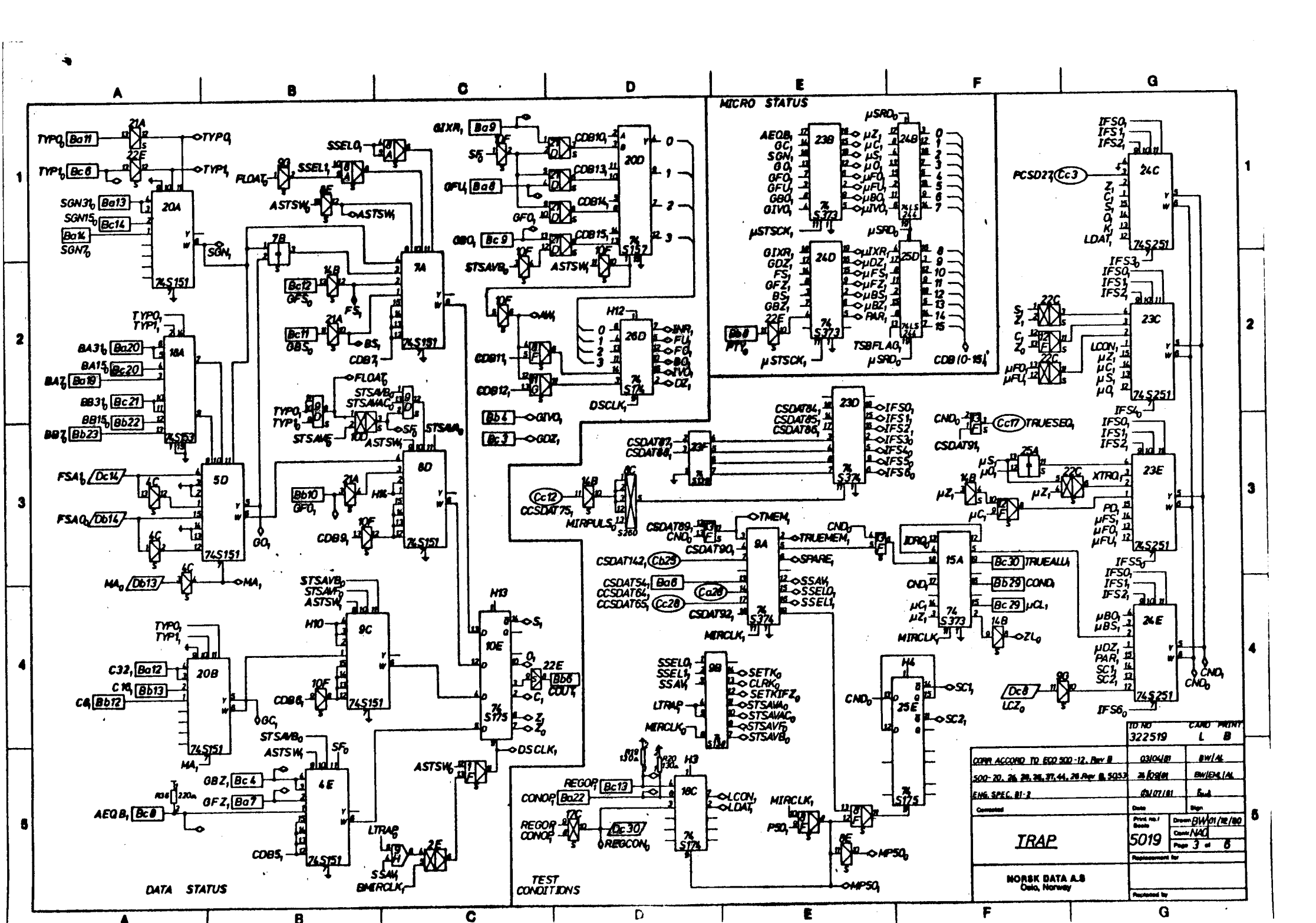

PREFETCH
NORSK DATA A.S
Oslo, Norway
322518
K 8,K
5018
5B94
Page 3 of 5
CORR. ACCORDING TO ECO 500-3, 500-9
500-3 Rev 8/500-11 REV 8 500-23
500-27, 33 Rev 8, 43, 54
02/12/80
08/04/81
23/09/81
Drawn 08/09/80
Cont TR
PSTOP0
CONDF1
PF1S0
PCSD41,5
APD18,4
FPF2,Bb28
PF2S1
PF3S10
PCSD62,9
APD19,10
AMCONT,9
PRCK1,
PCL0
CLP0
PF1ACT0
PF1ACT1
PF2ACT0
AST0
PF1ACT1,9
OMALL1,
PF2ACT1,10
AMALL1,
PF1ACT1,4
OM5,5
VEQ1,6
PF3ACT1,
PF2ACT,10
AMALL0,
PF1ACT,10
OMALL0,
TA40,10
BIDRY30,
PF1ACT,2
NOPR1,
OM2,1
PF1ACT,13
PFNOP1,
OM4,10
PF2ACT,5
AM2,6
PF3ACT,2
DLN0,3
OM3,1
PFNOP,13
OM4,10
PF2ACT,5
AM3,6
PF3ACT,2
DLN1,3
PF1ACT,4
OM5,5
IAC0,10
VC0,3
VC1,13
IAC1,12
DRYS0
DRYO0
IRQ,9
IDRP
PICLK3,13
IDRP1,12
XRQ,13
N40,12
PICLK2,1
N40,10
PICLK3,1
IDRY30,2
PICLK1,1
IDRY30,2
PEMPT,13
PICLK1,12
PEMPT1,11
PICLK2,1
PICLK3,2
PICLK1,13
PICLK2,1
PICLK3,2
PF1ACT,13
OM5,10
VEQ1,11
PF1ACT,13
PF2ACT,12
PF3ACT,10
PF1ACT,13
PF2ACT,12
PF3ACT,10
PF1ACT,
PF2ACT,
PF3ACT,
OM5,
VEQ1,
PF1ACT,
OM5,
VEQ1,
PF2ACT,
AMALL0,
PF1ACT,
OMALL0,
TA40,
BIDRY30,
PICLK2,
N40,
PICLK3,
IDRY30,
PICLK2,
PICLK1,
IDRY30,
PEMPT,
PICLK1,
PEMPT1,
ILL0,
PICLK2,
XRQ,
NDAT1,
NDAT2,
IDS,
NEW,
CLEAR,
DC15
IRQ,
PCL,
VLB0,
VLB1,
VCLK0
RESET,
C4 2200pF
H4
VLB0,
VLB1,
VCO,
VC1,
VC2,
VINT,
BASO,
BAS1,
VINT,
VINT,
H4
VLBCK,
VEQ1,
VEQ2,
VEQ3,
VEQ4,
VLB0,
VLB1,
VCO0,
VC1,
VC2,
PF1ACT,
PF2ACT,
PF3ACT,
DLN0,
VEQ1,
DLN0,
VEQ2,
DLN1,
VEQ3,
DLN0,
DLN1,
VEQ1,
DLN1,
PICLK3,
IDRP1,
XRQ,
N40,
NDAT2,
DIOK1,
DNO,
ADEN0,
ADEN,
JDL0,
DN1,
JDL1,
DLN0,
DLN0,
DLN1,
DLN1,
PF1ACT,
PF2ACT,
PF3ACT,
PACT,
PF1ACT,
PF2ACT,
PF3ACT,
CLKOP,
CLKAD,
CLKDI,
PICLK1,
PICLK2,
PICLK3,
JDL0,
JDLEN,
CDB7,
CDB15,
JDLEN,
JDLEN0
ADEN1,
ADEN0
CLP0
TA20,
H4
PICLK1,
PICLK1,
JDL0,
JDLEN1,
ADEN1,
ADEN0
CLP0
TA20,
H4
TAS0
DC10-357
CLP0
PICLK1,
TA40,
CLN0,
PCL0
CLP0
N40,
H4
PE0,
H4
IDCLK0,
Cc9
Aa13
IDRY0,
BMCL,
Ba8
RSTOP,
Da16
IREQ0,
EXR1,
IDS1,
IRQ0,
IRQ1,
NDAT0,
NDAT2,
IDS,
NEW,
Dc16
NEWD0
VLB0,
VLB1,
VCO0,
VC1,
VC2,
VINT,
BASO,
BAS1,
VINT0,
VINT0,
H4
VLBCK0,
VEQ1,
VEQ2,
VEQ3,
VEQ4,
VLB0,
VLB1,
PF2ACT,
DSCX0,
DSCX1,
PF1ACT,
PF2ACT,
PF3ACT,
VCO0,
VC1,
VC2,
CLKAD,
PCDB,
CLKM0,
LMC0,
LMC1,
LMC2,
AST0,
H1
PCSD38,
PCSD39,
PCSD63,
PRCK1,
PCD0,
PCD1,
PCD2,
PCD3,
JDL0,
JDL1,
TYPCH1,
LSTOP0,
ADEN1,
DLN0,
DLN1,
VCLK0,
IDRY0,
PSTOP0,
DESCR0,
DSCX0,
DSCX1,
ALTR0,
AD6,
AD7,
LA1,
PF3ACT1,
N40,
CLKM0,
APD18,
PCSD58,
APC15,
PRCK1,
REG1,
BR1,
CON1,
IRQ0,
VINT1,
IDRP1,
VCLK0,
IDRY0,
LSTOP0,
DESC0,
DXO0,
DX10,
LALT1,
IRQ0,
VINT1,
IDRP1,
DLN0,
DLN1,
Dc22
ALC0,
LSTOP0,
ADEN1,
PCDB1,
LMC0,
DLN0,
LMC1,
DLN1,
LMC2,
AST0,
H1
PRCK1,
PCD0,
PCD1,
PCD2,
PCD3,
JDL0,
JDL1,
TYPCH1,
PF1ACT,
PF2ACT,
PF3ACT,
Dc10
PACT1,
PF2ACT1,
DSCX0,
DSCX1,
ALTR1,
DESCR0,
ALTR0,
CLKAD1,
PCDB1,
Ac14
BAS0,
Ac3
BAS1,
LALT1,
Cc12
REG1,
Dc7
VC0,
VC1,
VC2,
IAL24,
IAL0,
IAL8,
IAL16,
IAL25,
IAL1,
IAL9,
IAL17,
OM5,
H1
D2,
D1,
H1
D3A,
D3B,
A3A,
D3A,
OM5,
H1
A2A,
A1A,
H1
R3 1K
R4 1K
R5 1K
R6 1K
H3
H4
H5
H6
Dc5
ILL0,
Dc3
CRCLK1,
Dc15
PCL0
IDRY30,
DRYS0
Ca25
Cc26
OVCLK0
DCL0
Aa3
DSIGN1
Dc16
NEWD0
Aa7
IDRQ0
Aa6
AIL0
Aa16
ACLK0
Ba19
DESC0
Bc20
DXO0
Ba20
DX10
REG1
BR1
CON1
Ac4
Aa4
Ac5
Ab3
Dc22
ALC0
Dc10
PACT1
Dc5
ILL0
Dc3
CRCLK1
Dc15
Dc16
NEWD0
Aa7
IDRQ0
Aa6
AIL0
Aa16
ACLK0
Ba19
DESC0
Bc20
DXO0
Ba20
DX10
REG1
BR1
CON1
Ac4
Aa4
Ac5
Ab3

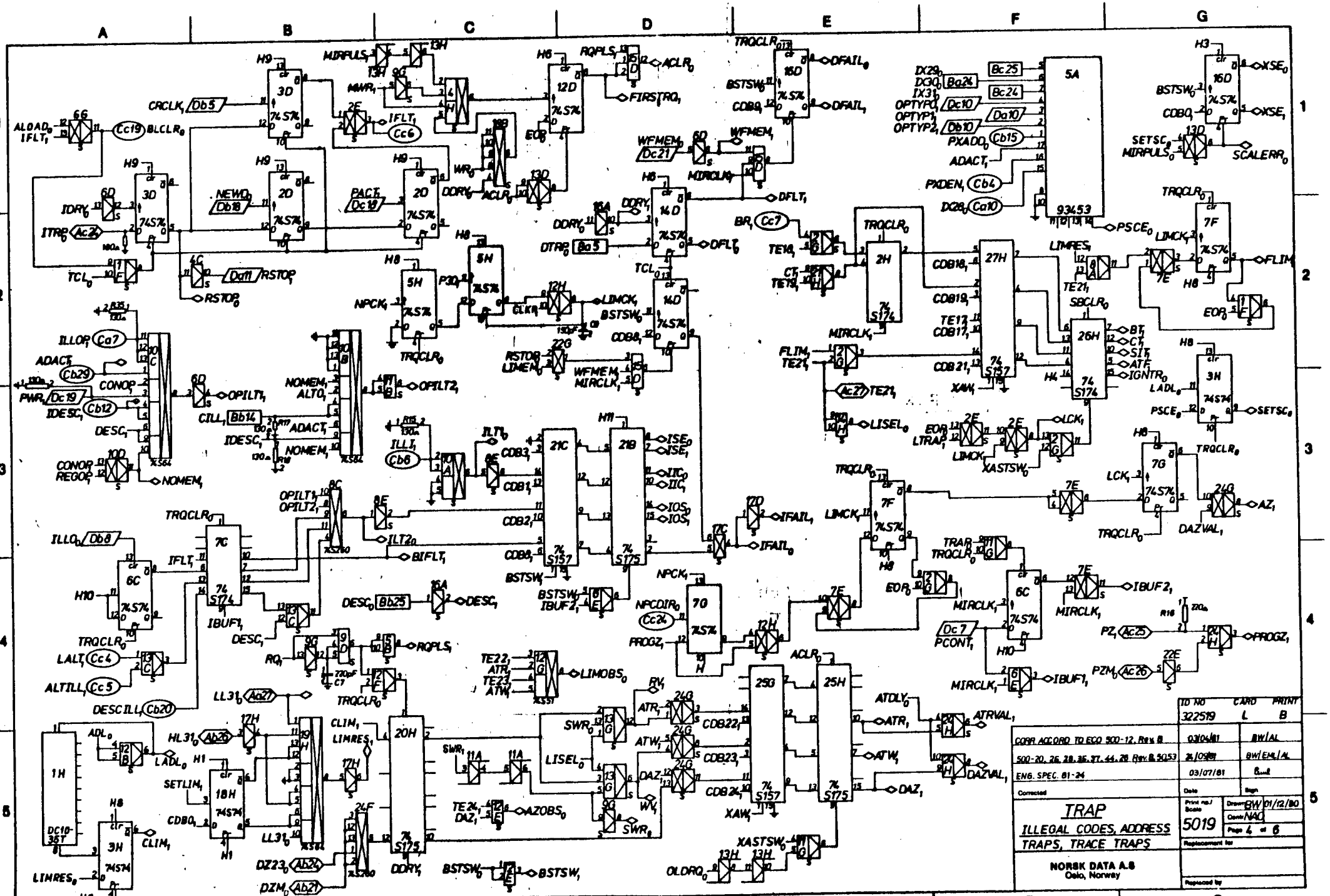

PREFETCH
NORSK DATA A.S
Oslo, Norway
ID. NO. 322518
CARD PRINT K B, K
CORR. ACCORDING TO ECO 500-3. 500-6 02/12/80
500-3 REV B, 500-11 REV B, 500-23, 08/06/81
500-27, 33 Rev B, 43, 64 23/09/81
Print no./Scale 5018
Drawn 05/08/80
Cont. IR
Page 4 of 5
5B95

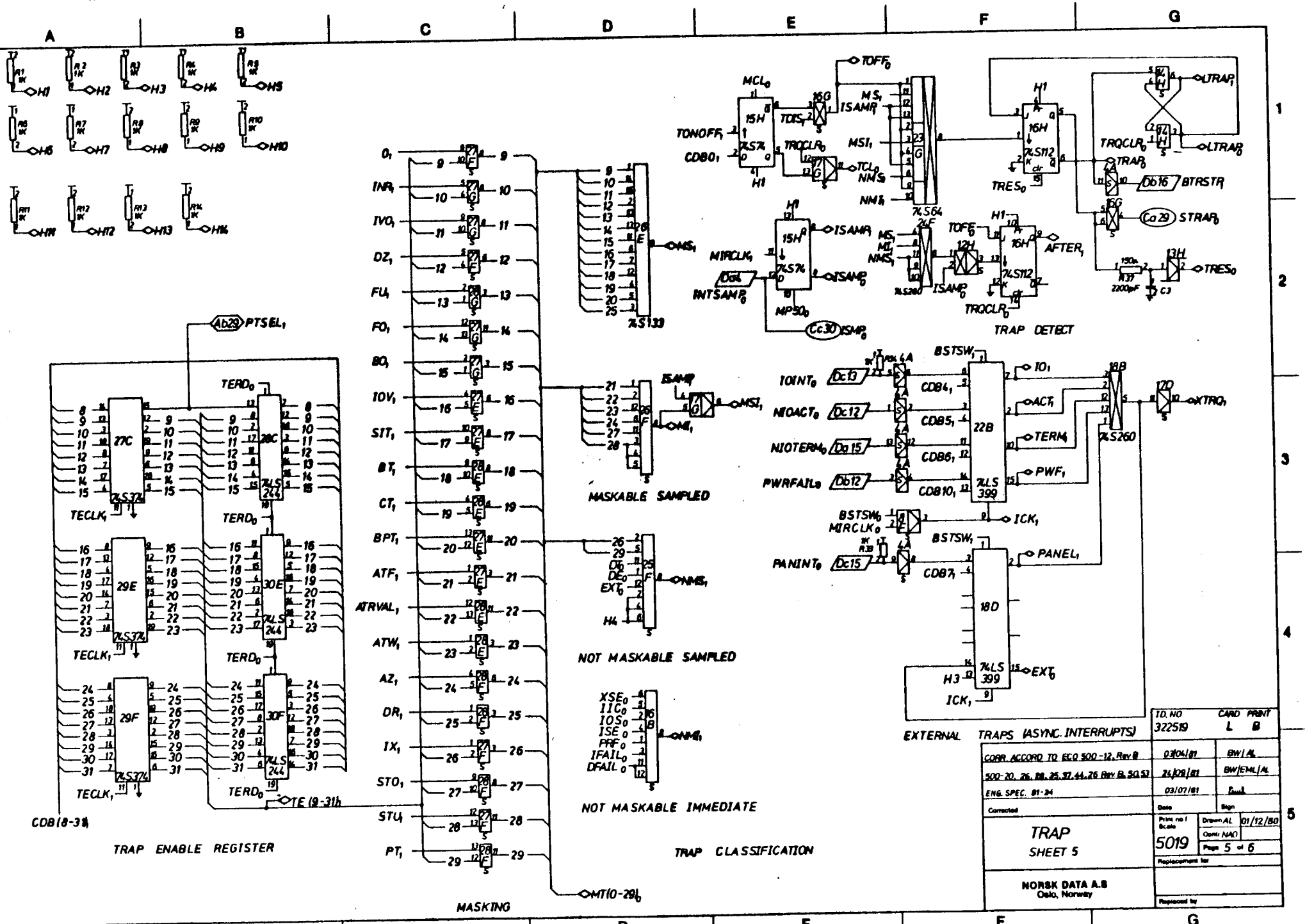

PREFETCH
NORSK DATA A.S
Oslo, Norway
5018
5B96
322518
CARD PRINT
PAGE 5 of 5

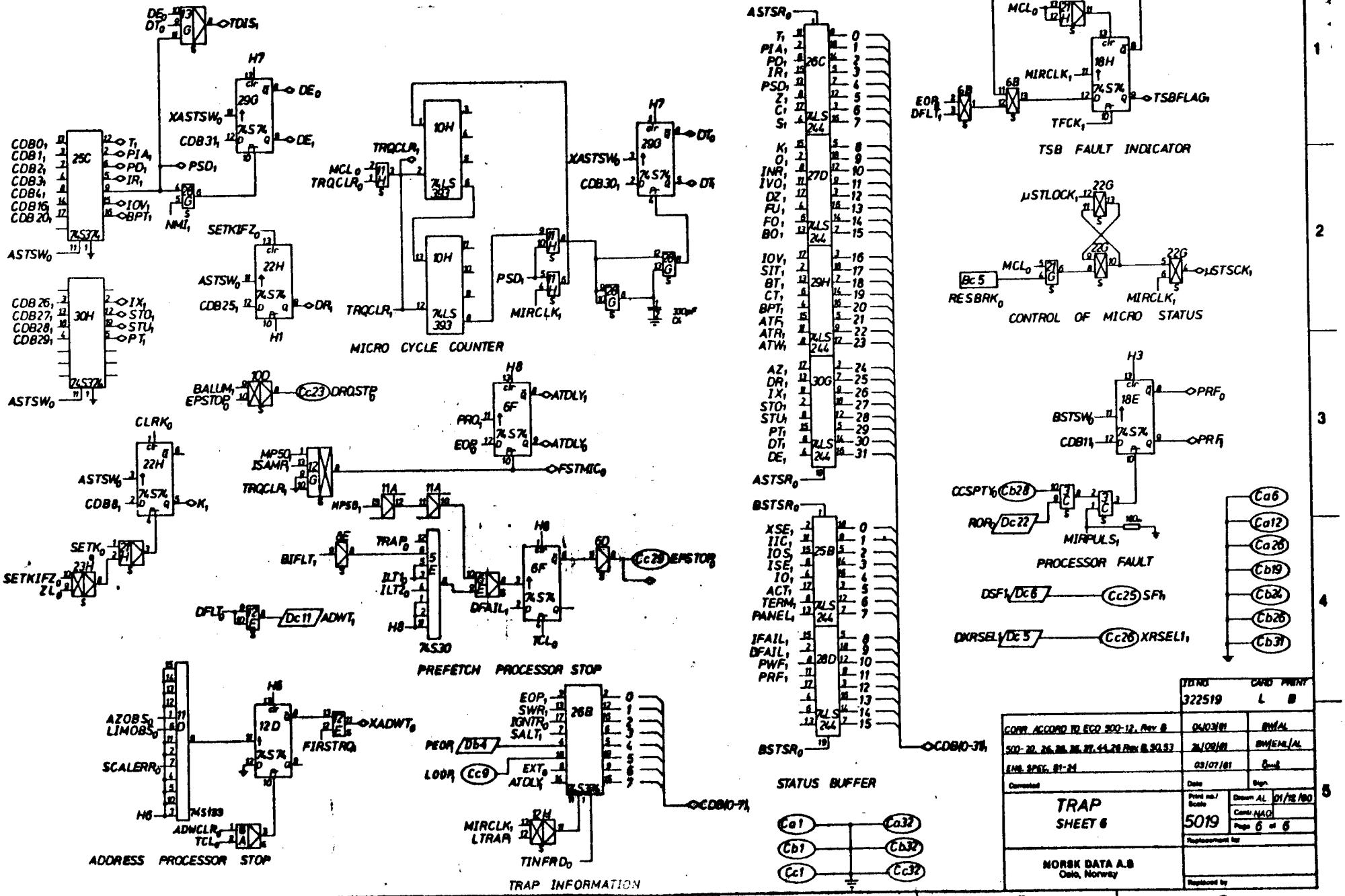

XD-TRANSCEIVERS
CONTROL STORE TRANSCEIVERS
CDB 10-31
XD-CONTROL
CS-TRANSC CONTROL
CONTROL STORE PARITY CHECKING
CSDAT (80-95)
XD 10-31
TRAP
SHEET1
NORSK DATA A.S
Oslo, Norway
TO NO 322519
CARD PRINT L B
COPY ACCORD TO ECO 500-12 Rev. B
ENG. SPEC. 01-24
Print no 5019
Page 1 of 6

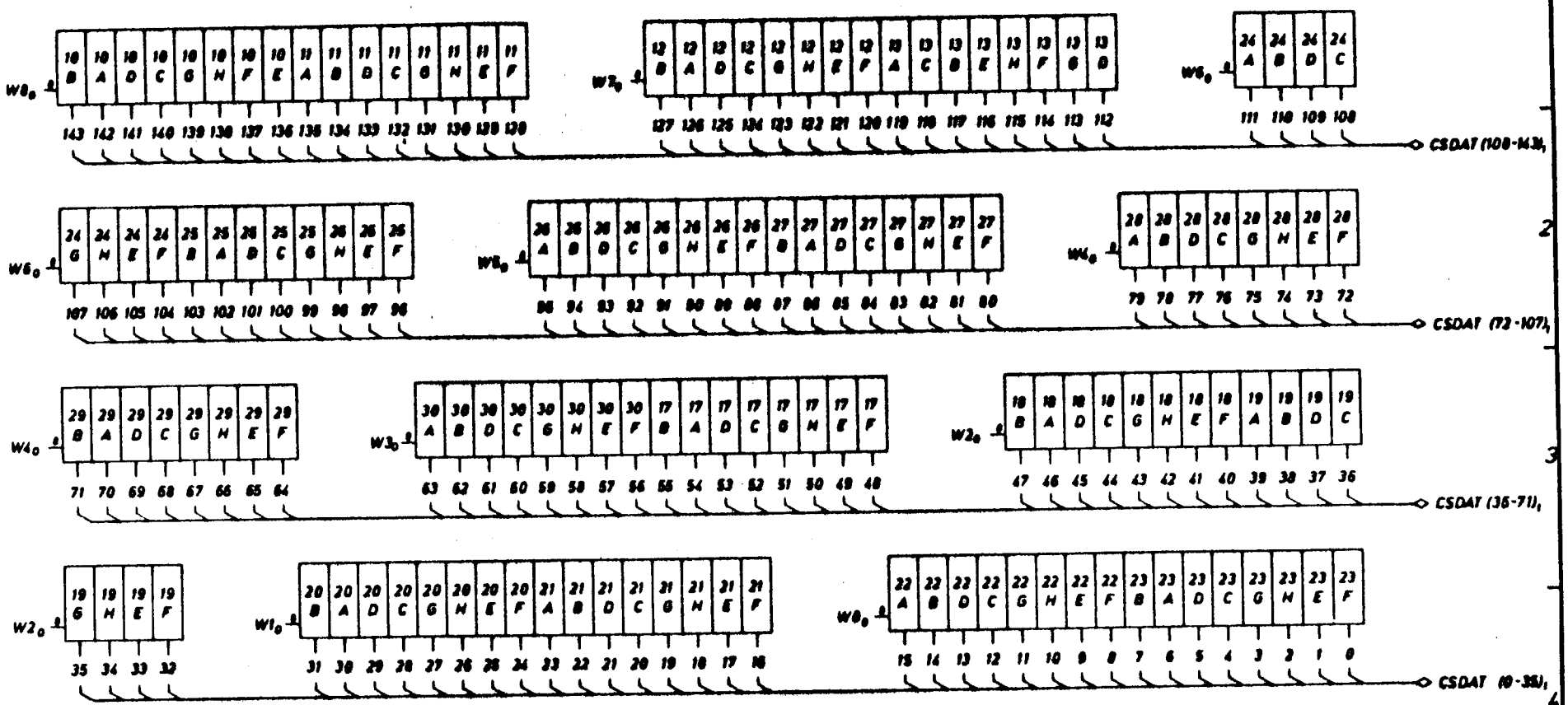

MEMORY MODUS REGISTER
MEMORY CONTROL
TRAP
SHEET 2
NORSK DATA A.S
Oslo, Norway
TD NR. 322519
CARD PRINT L B
5019
Drawn AL 01/12/80
Page 2 of 6


MICRO STATUS
DATA STATUS
TEST CONDITIONS
TRAP
NORSK DATA A.S
Oslo, Norway
322519
5019
Page 3 of 6

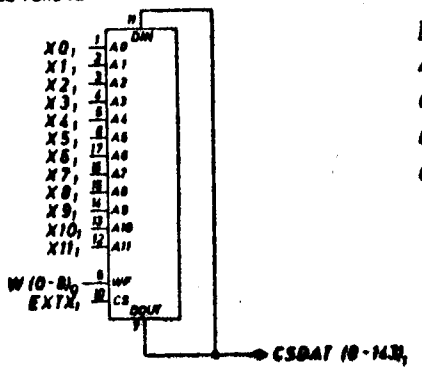

TRAP
ILLEGAL CODES, ADDRESS TRAPS, TRACE TRAPS
NORSK DATA A.S
Oslo, Norway
ID NO 322519
CARD L
PRINT B
CORR ACCORD TO ECO 500-12, Rev. B
500-20, 26, 28, 35, 37, 44, 28 Rev. B, 5053
ENG. SPEC. 81-24
Corrected
03/04/81
26/09/80
03/07/81
Date
Sign
BW/AL
BW/EML/AL
Print no./ Scale 5019
Drawn BW 01/12/80
Cont. NAO
Page 4 of 6
Replacement list
Replaced by


TRAP ENABLE REGISTER
MASKING
TRAP CLASSIFICATION
MASKABLE SAMPLED
NOT MASKABLE SAMPLED
NOT MASKABLE IMMEDIATE
TRAP DETECT
EXTERNAL TRAPS (ASYNC. INTERRUPTS)
TRAP
SHEET 5
NORSK DATA A.S
Oslo, Norway
5019
322519
Page 5 of 6


MICRO CYCLE COUNTER
PREFETCH PROCESSOR STOP
ADDRESS PROCESSOR STOP
TRAP INFORMATION
STATUS BUFFER
TSB FAULT INDICATOR
CONTROL OF MICRO STATUS
PROCESSOR FAULT
TRAP
SHEET 6
NORSK DATA A.S
Oslo, Norway
322519
5019



The memory IC's, Hitachi 6147-3 (Intel 2147-3), should be connected as follows:



The address lines X (0-10) are equal to:

AB (0-10), if the IC is placed coloumns A or B on the card

CD (0-10), ——— C or D ———

EF (0-10), ——— E or F ———

GH (0-10), ——— G or H ———

The EXTX signal is equal to:

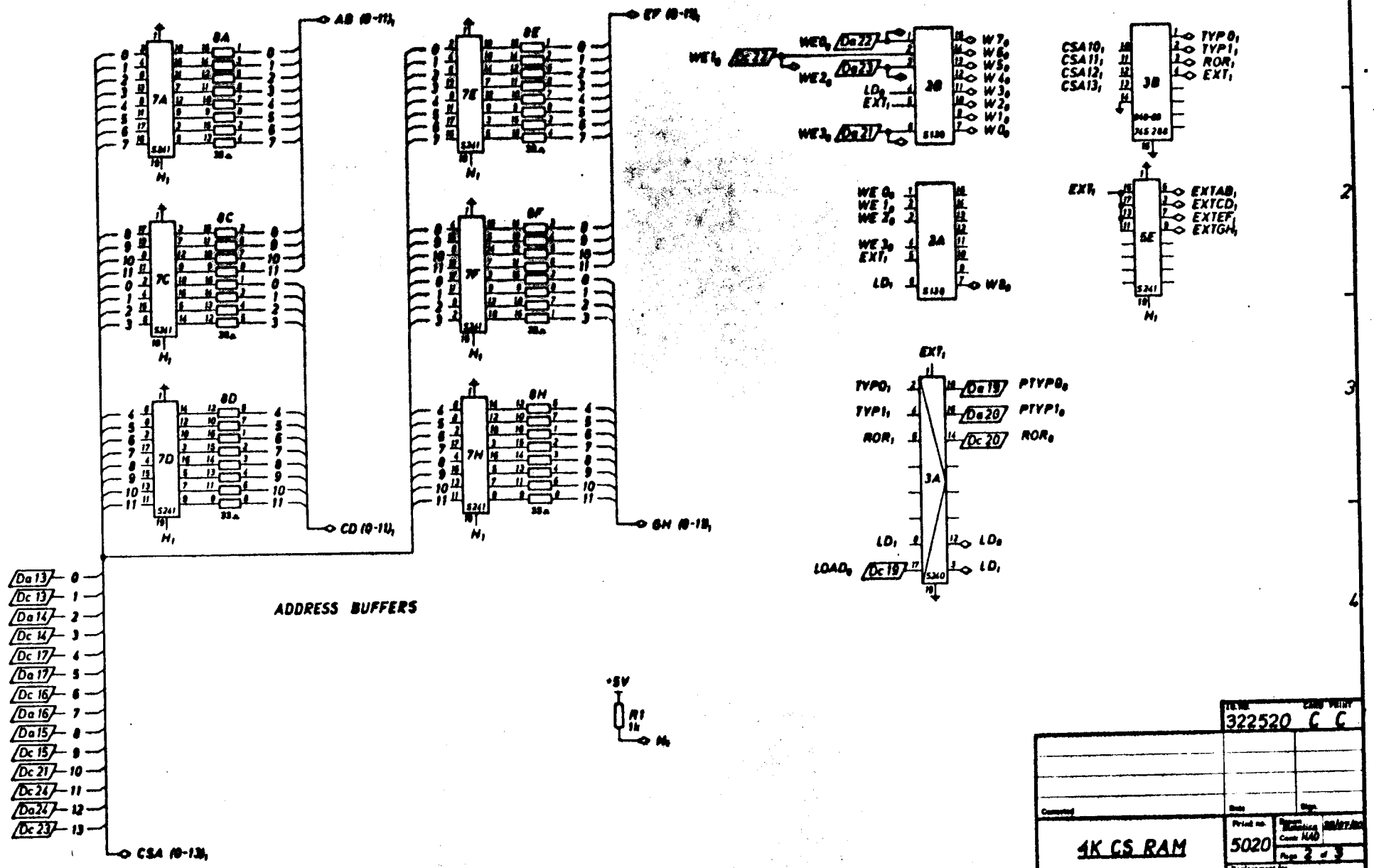
EXTAB, if the IC is placed in coloumns A or B on the card

EXTCD, ——— C or D ———

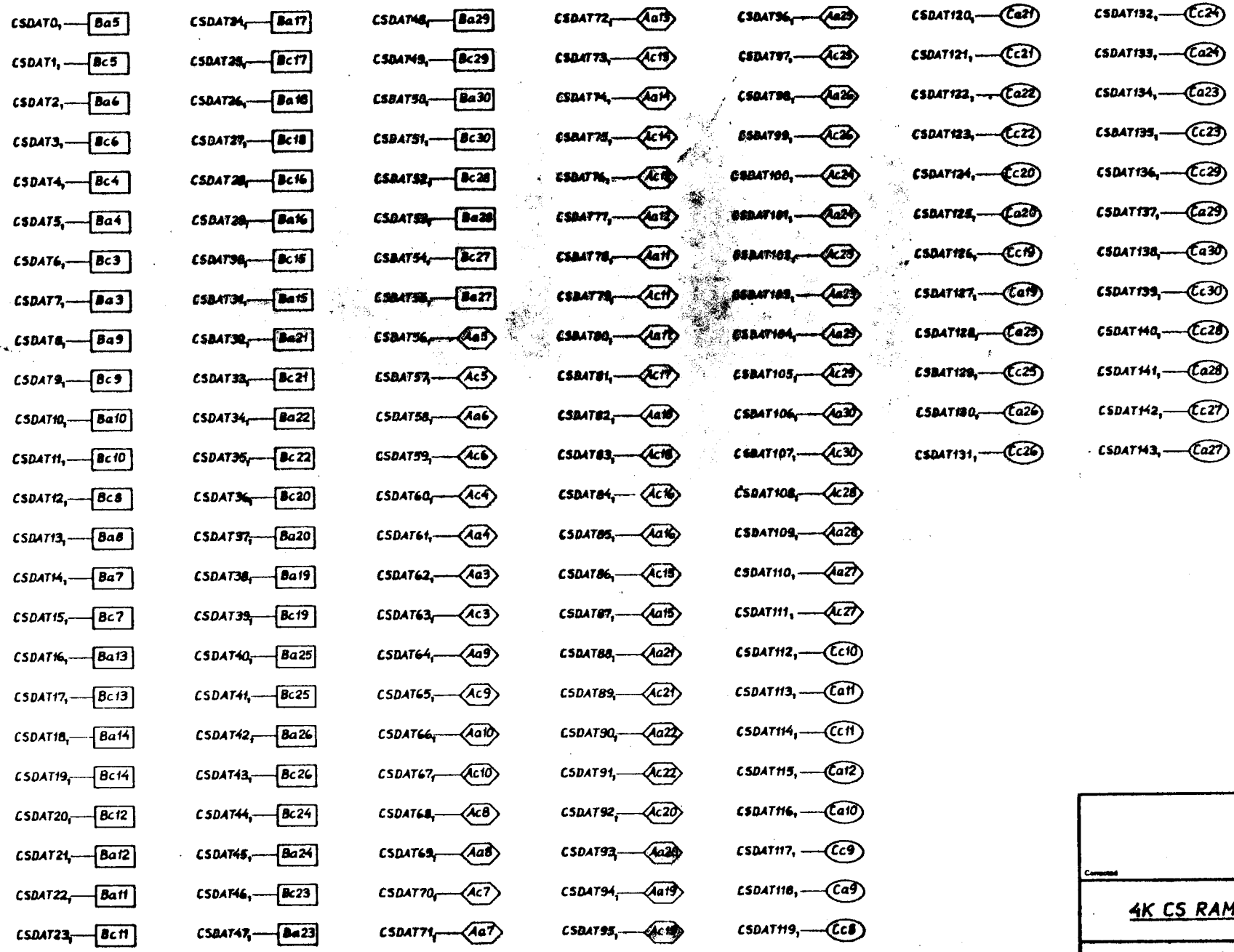
EXTEF, ——— E or F ———

EXTGH, ——— G or H ———

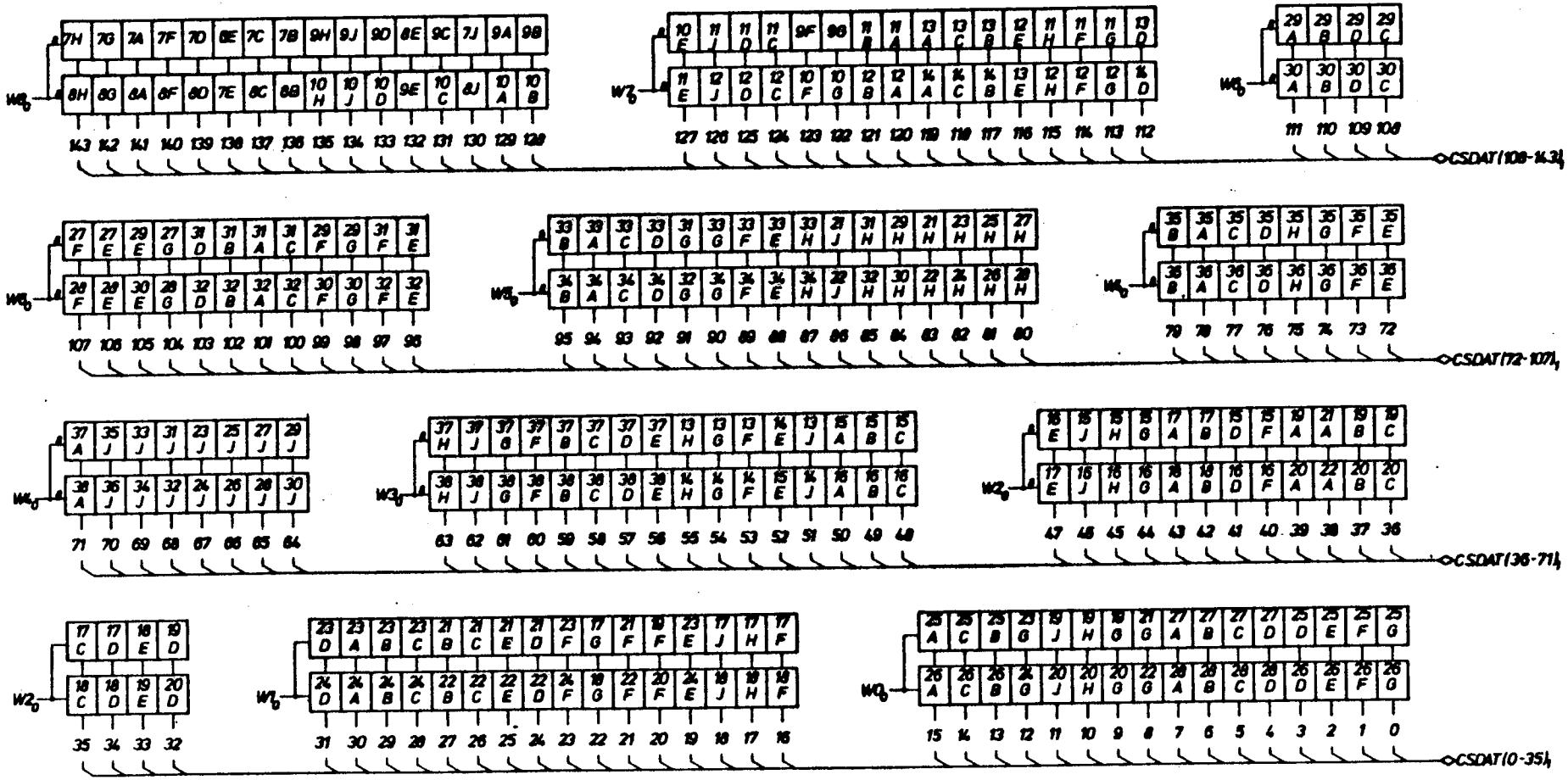
	TYPE NO. 322520	CARD ISSUE C
4K CS RAM	Print no. 5020	Card NAD Page 1 of 3
NORSK DATA A.S Oslo, Norway		5B66



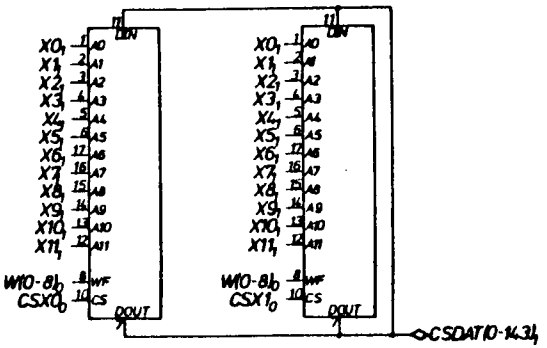
	322520	C C
4K CS RAM	5020	Page 2 of 3
NORSK DATA A.S Oslo, Norway		5B67



		ID. NO. 322520	CARD PRINT C C
Comment	Date	Sign	
4K CS RAM	Print no 5020	Drawn Lund 28/07/80 Const NAO Page 3 of 3	
	Replacement for		
NORSK DATA A.S Oslo, Norway	5B68	Replaced by	



The memory IC's Hitachi 6147-3 should be connected as follows:



X(0-11)$_i$ and CSX(0-1)$_n$ are connected as follows:

AB(0-11)$_i$: (n)A n=7-38, (n)B n=7-38, (n)C n=31-38
CD(0-11)$_i$: (n)C n=7-30, (n)D n=7-38, (n)E n=23-38
EF(0-11)$_i$: (n)E n=6-22, (n)F n=7-38, (n)G n=15-38
GH(0-11)$_i$: (n)G n=7-14, (n)H n=7-38, (n)J n=7-38

CSAB0$_n$: (n+2)A n=5-35, (n+2)B n=5-35
CSAB1$_n$: (n+2)A n=6-36, (n+2)B n=6-36
CSCD0$_n$: (n+2)C n=5-35, (n+2)D n=5-35
CSCD1$_n$: (n+2)C n=6-36, (n+2)D n=6-36, (n+2)E n=22-36
CSEF0$_n$: (n+2)E n=4-16, (n+2)E n=19-35, (n+2)F n=5-35
CSEF1$_n$: (n+2)E n=5-17,22E (n+2)F n=6-36, (n+2)G n=12-36
CSGH0$_n$: (n+2)G n=5-35, (n+2)H n=5-35, (n+2)J n=5-35
CSGH1$_n$: (n+2)G n=6-10, (n+2)H n=6-36, (n+2)J n=6-36

The above text changed 17.08.81/Eual

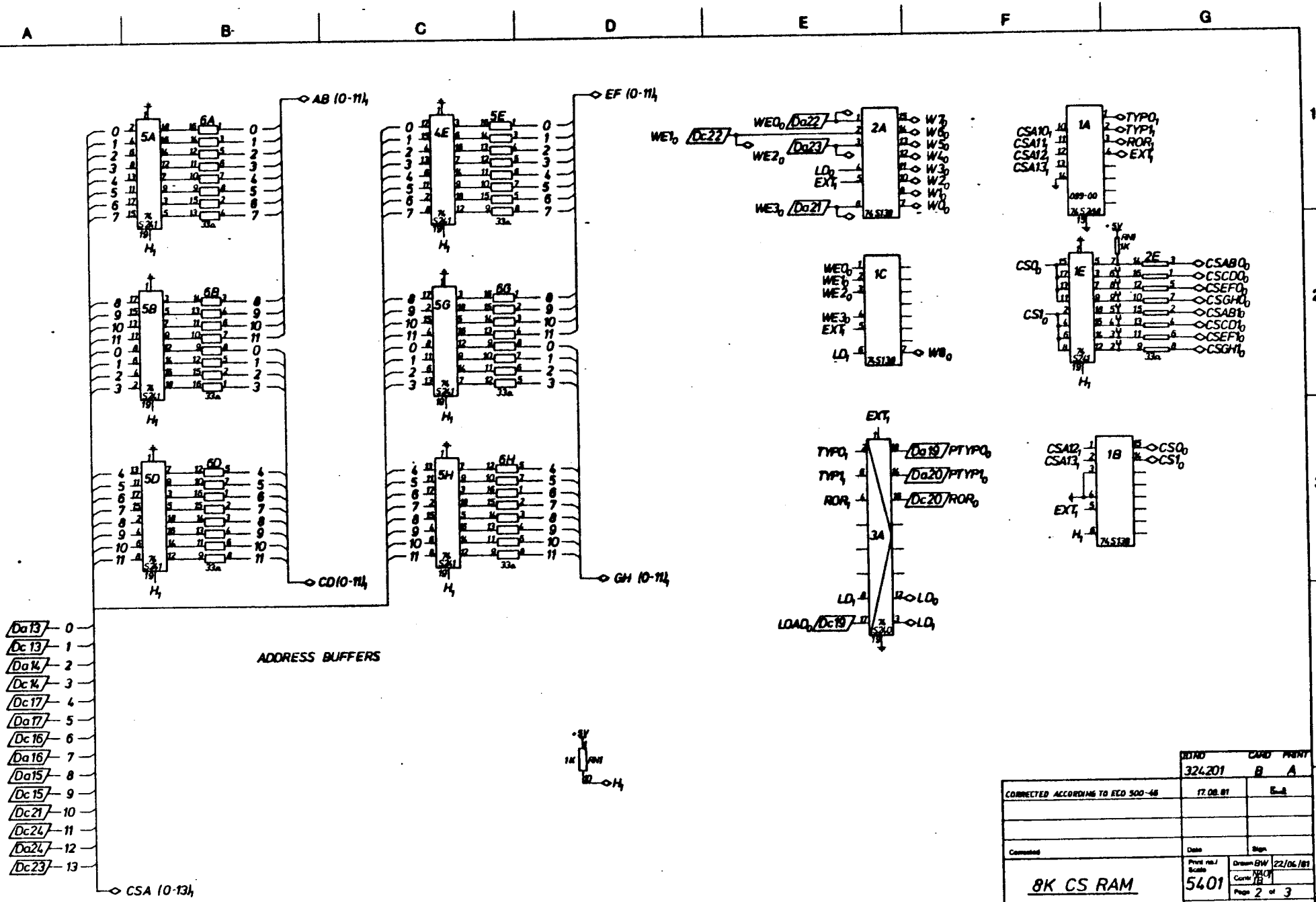
DWG	CARD	PRINT
324201	B	A

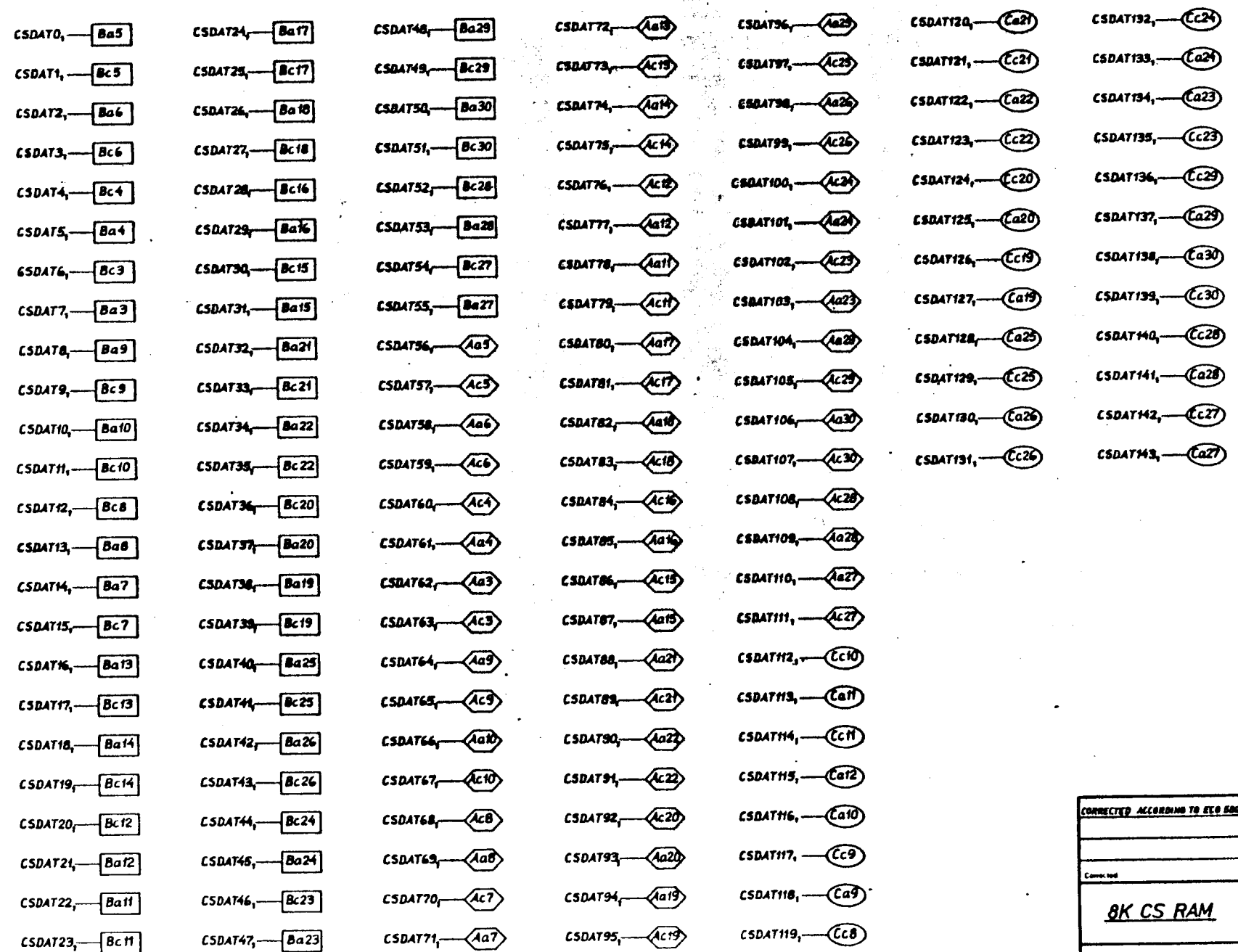
CORRECTED ACCORDING TO ECO 500-46	17.08.81	Eual
Corrected	Date	Sign.

8K CS RAM

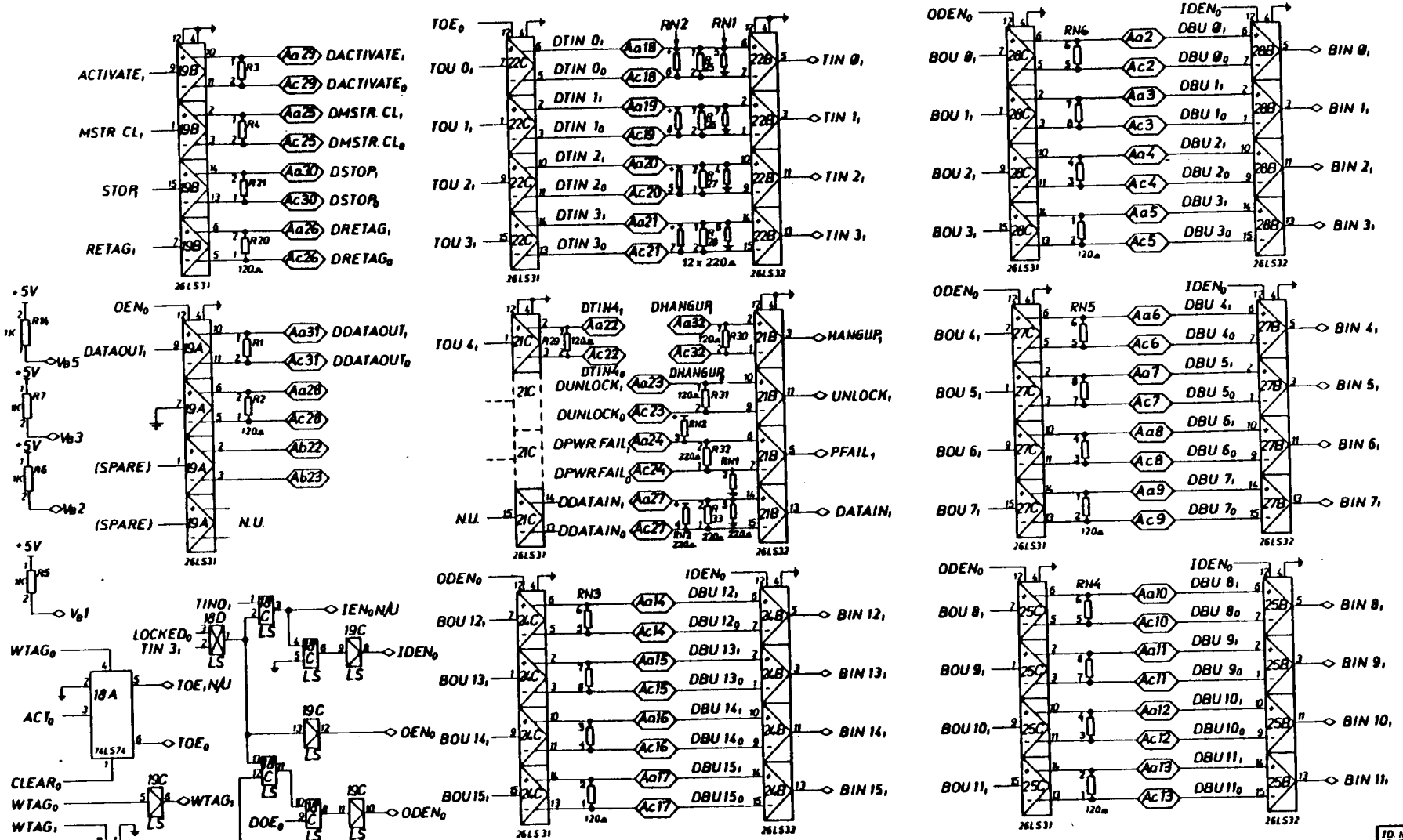
Print no./ Scale	Drawn BW 22/06/81
5401	Cont. Page 1 of 3
Replacement for	
Replaced by	

NORSK DATA A.S
Oslo, Norway

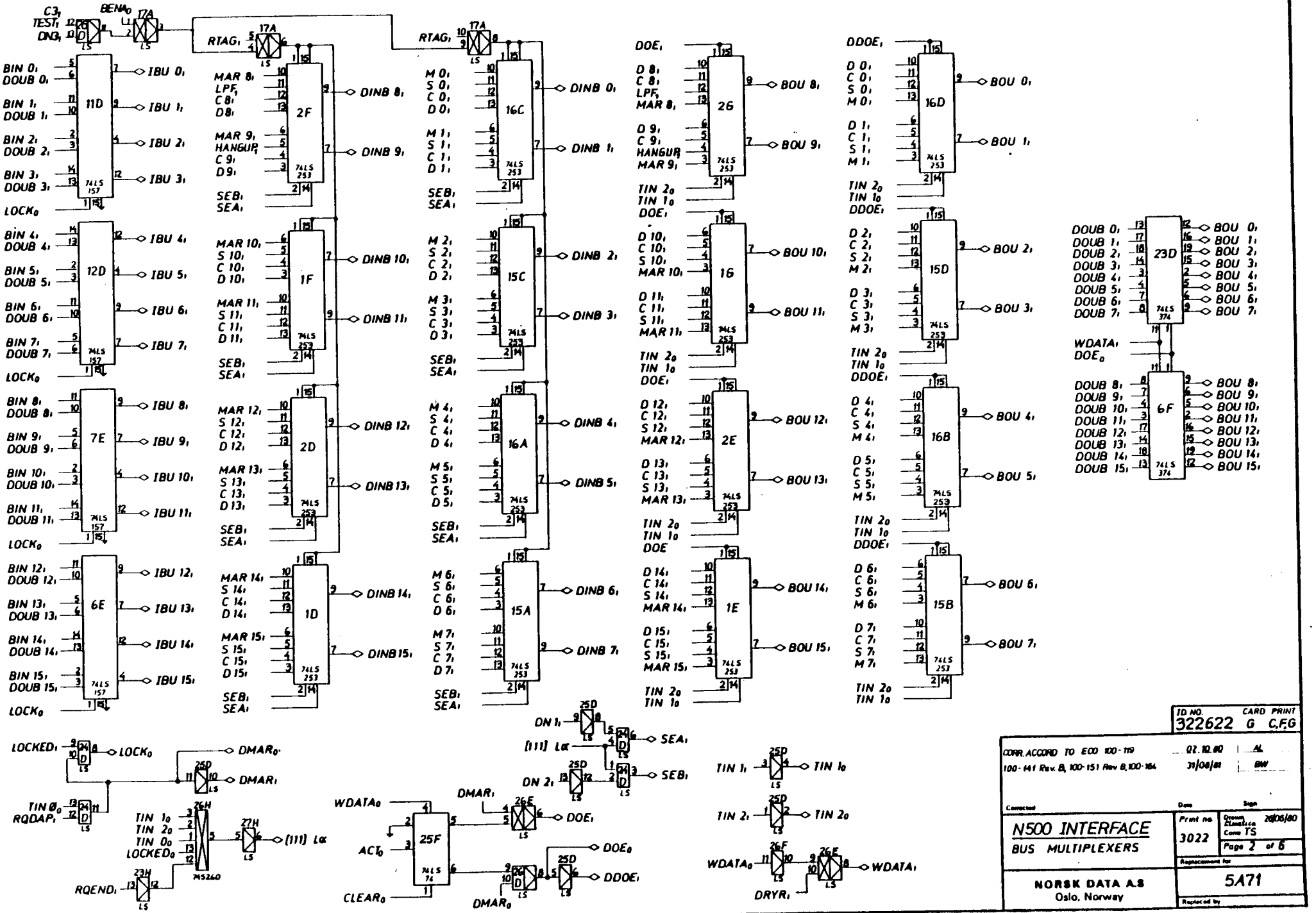

AB (0-11)
CD (0-11)
EF (0-11)
GH (0-11)
ADDRESS BUFFERS
CSA (0-13)
Da13 0
Dc13 1
Da14 2
Dc14 3
Dc17 4
Da17 5
Dc16 6
Da16 7
Da15 8
Dc15 9
Dc21 10
Dc24 11
Da24 12
Dc23 13
WE1 Dc22
WE0 Da22
WE2 Da23
WE3 Da21
EXT
TYPO
TYP1
ROR
Da19 PTYP0
Da20 PTYP1
Dc20 ROR
LOAD Dc19
CSA10
CSA11
CSA12
CSA13
CSAB0
CSCD0
CSEF0
CSGH0
CSAB1
CSCD1
CSEF1
CSGH1
CS0
CS1
+5V
1K RN1
8K CS RAM
NORSK DATA A.S
Oslo, Norway
DOC NO 324.201
CARD B
PRINT A
CORRECTED ACCORDING TO ECO 500-48
17.08.81
Print no./ Scale 5401
Drawn BW 22/06/81
Page 2 of 3



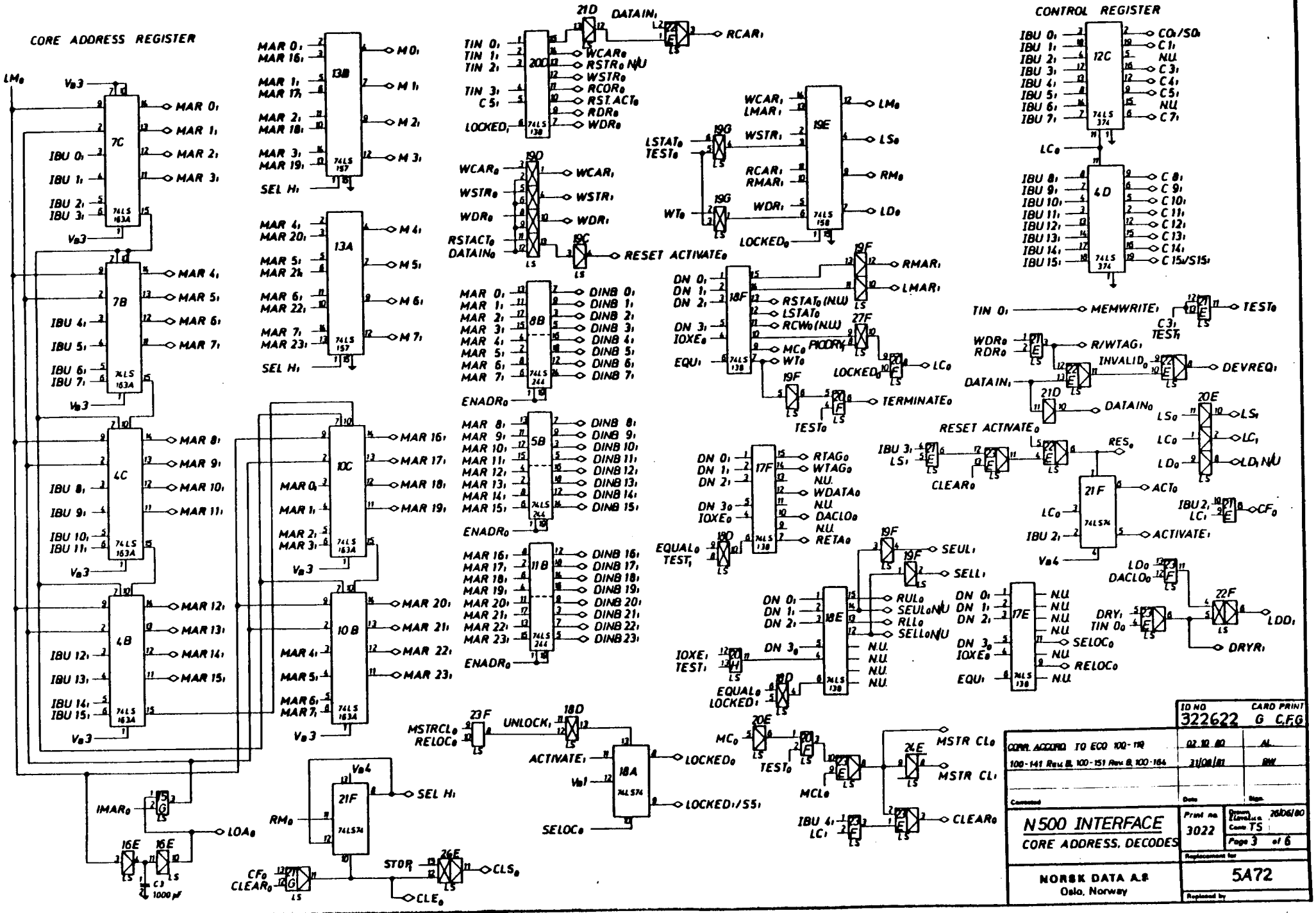
		TS. NR. 324201	CARD PRINT B A
CORRECTED ACCORDING TO ECO 500-48	17.06.81	B.A	
Corrected	Date	Sign	
8K CS RAM	Proj. no 5401	Drawn B.A 22/06/81	
		Check 9201 18	
		Page 3 of 3	
		Replacement for	
NORSK DATA A.S Oslo, Norway		Replaced by	

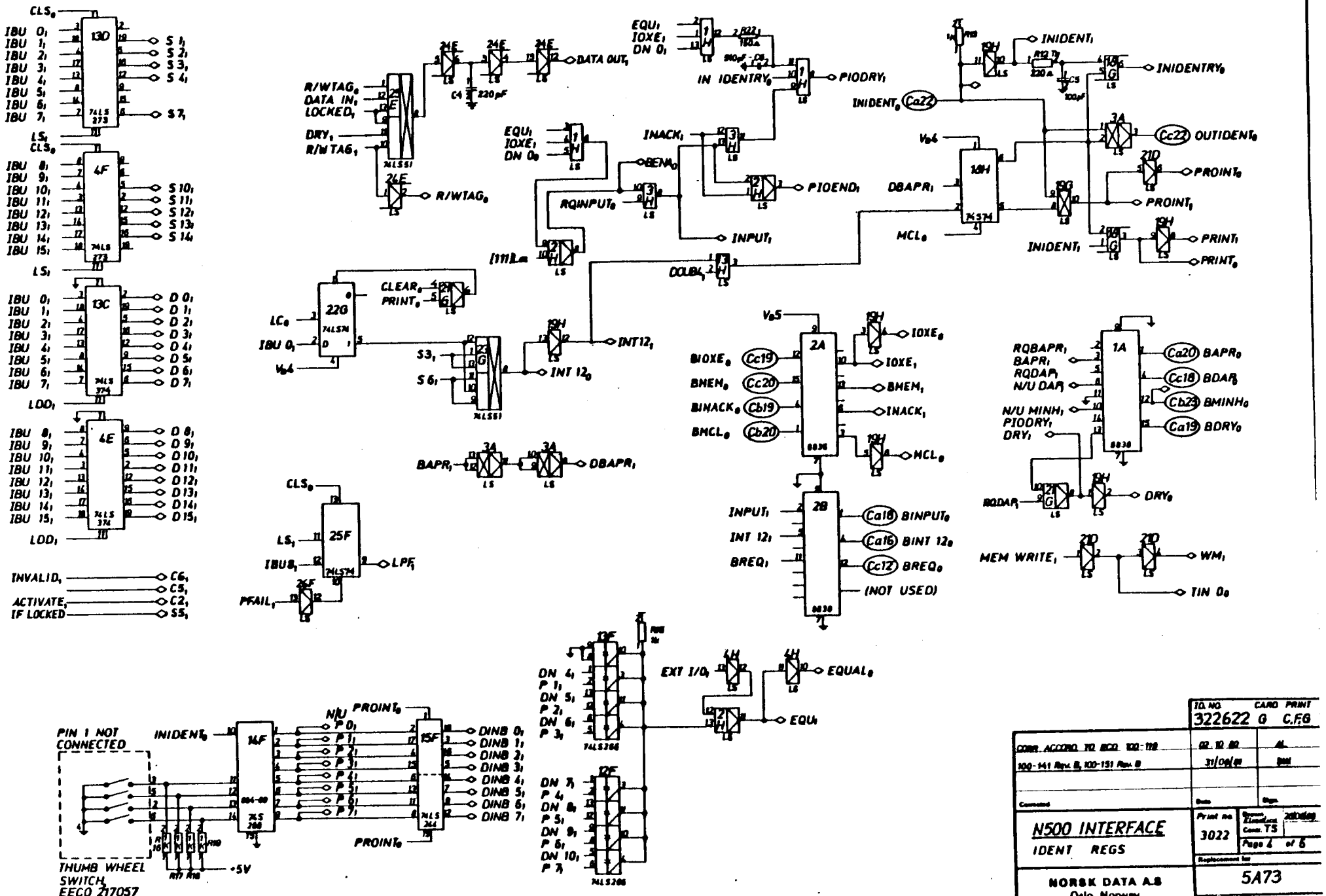


ID NO 322622	CARD PRINT G C.F.G
CORR ACCORD TO ECO 100-119, 100-141 Rev B, 100-151 Rev B, 100-164	31/08/81 BMY
Corrected	Date Sign
N500 INTERFACE TAG BUS TRANSCEIVER	Print no 3022 · Drawn Tinelius 26/06/80 · Conn TS · Page 1 of 6
NORSK DATA A.S Oslo, Norway	Replacement for 5A70 · Replaced by

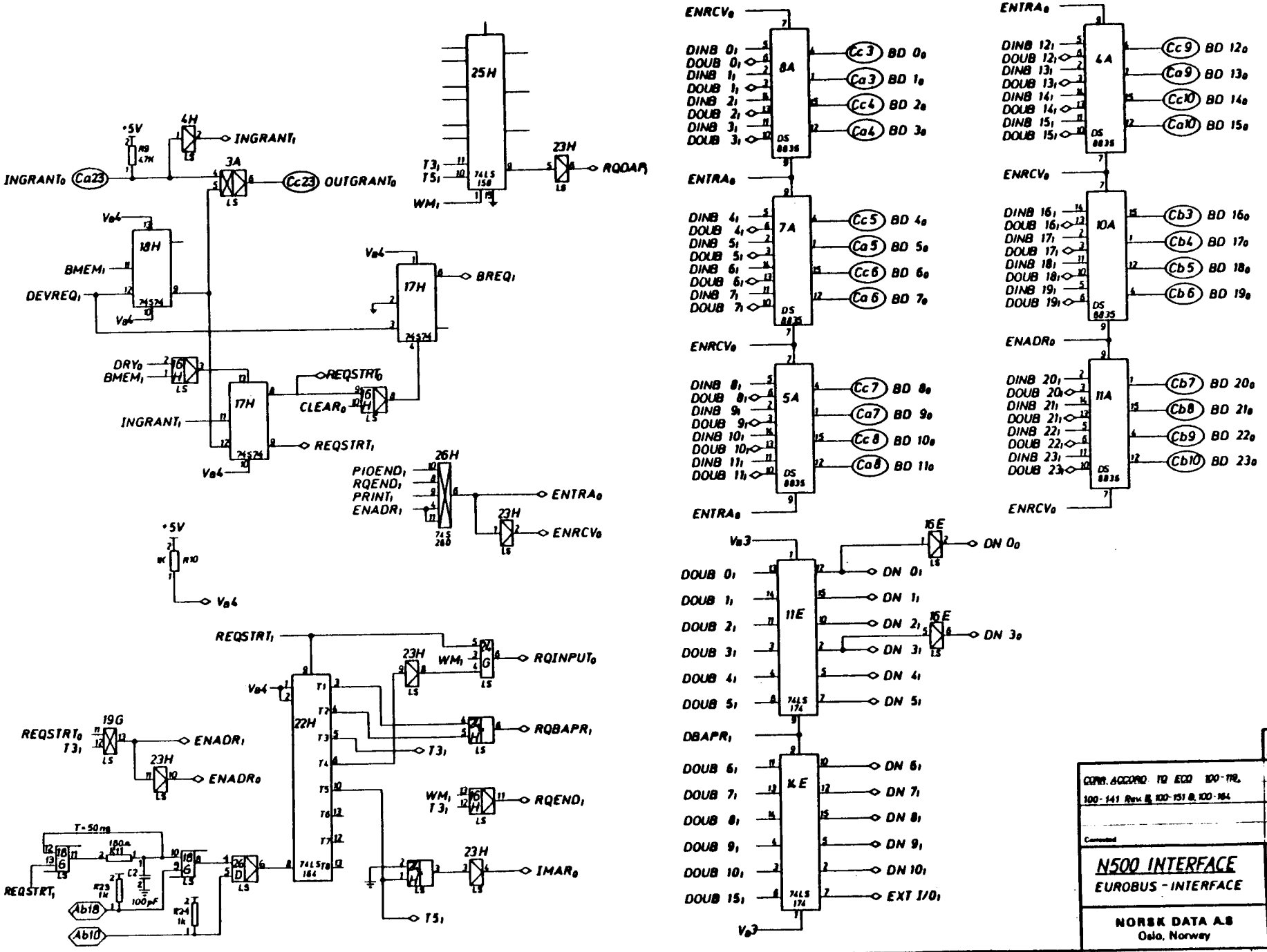


ID NO. 322622	CARD PRINT G C,F,G
CORR. ACCORD TO ECO 100-119	02.10.80 AL
100-141 Rev B, 100-151 Rev B, 100-164	31/08/81 BW
Corrected	Date Sign
N500 INTERFACE	Print no. 3022
BUS MULTIPLEXERS	Drawn Checked Conn TS 26/06/80
	Page 2 of 6
	Replacement for
NORSK DATA A.S Oslo, Norway	5A71
	Replaced by

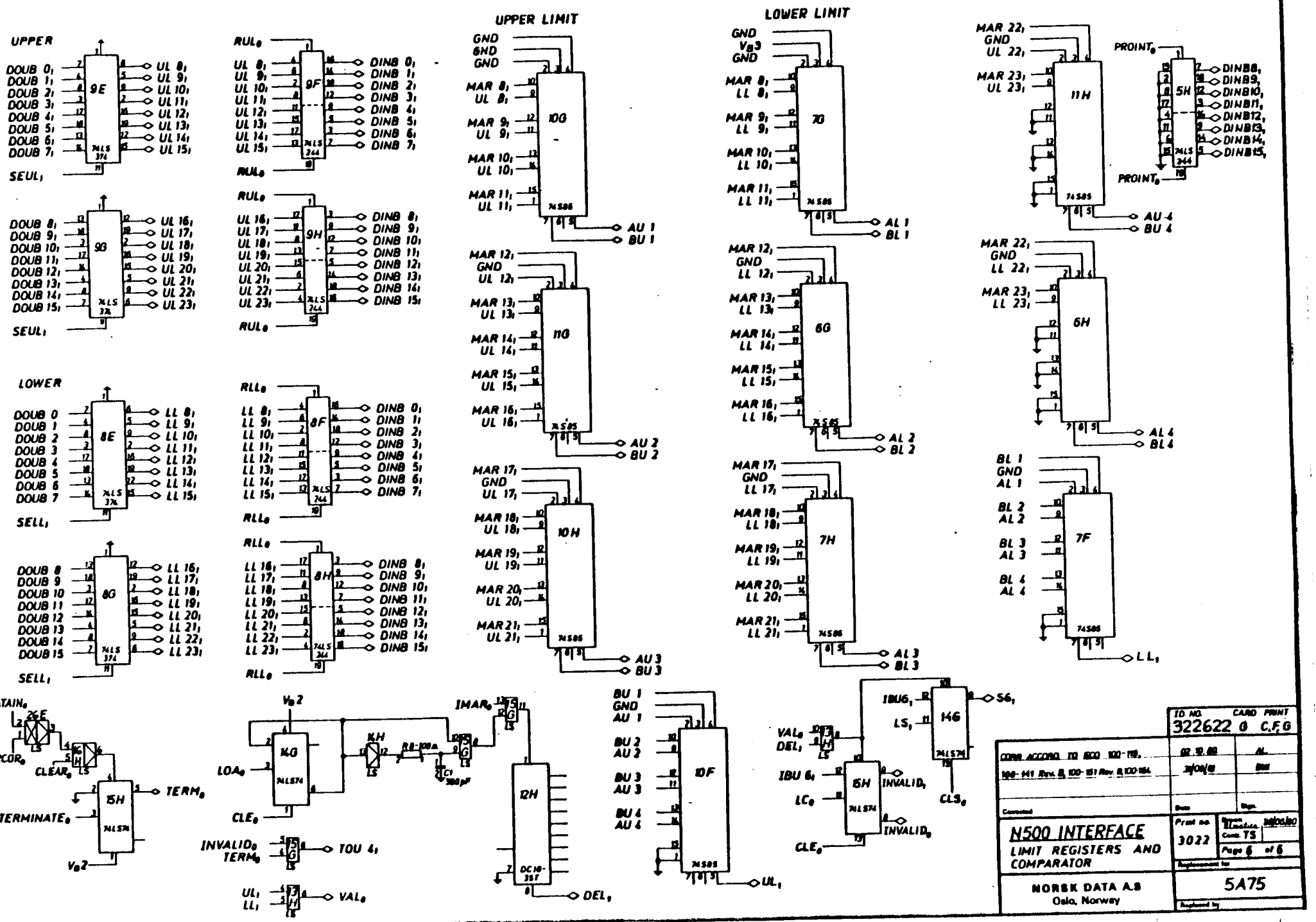

CORE ADDRESS REGISTER
CONTROL REGISTER
7C
7B
4C
4B
13B
13A
10C
10B
8B
5B
11B
12C
4D
18F
19F
19E
17F
18E
17E
18A
21F
20E
22F
24E
26E
16E
N500 INTERFACE
CORE ADDRESS, DECODES
NORSK DATA A.S
Oslo, Norway
322622
5A72
3022
Page 3 of 6



TD. NO. 322622	CARD PRINT G	C.F.G	
CORR. ACCORD. TO ECO 100-118	02.10.80	AL	
100-141 Rev. B, 100-151 Rev. B	31/08/81	BM	
Comment	Date	Sign.	
N500 INTERFACE IDENT REGS	Print no. 3022	Drawn Y.Lund Corr. TS	2810/80
		Page 4 of 6	
		Replacement for	
NORSK DATA A.S Oslo, Norway	5A73		
		Replaced by	



ID NO 322622	CARD PRINT G C.F.G		
CORR. ACCORD TO ECO 100-119, 100-141 Rev. B, 100-151 B, 100-164	02.10.80	AL	
	31/08/81	BW	
Corrected	Date	Sign.	
N500 INTERFACE EUROBUS - INTERFACE	Print no. 3022	Drawn Eliasson 26/08/80 Code TS 1	
		Page 5 of 6	
	Replacement for		
NORSK DATA A.S Oslo, Norway	5A74		
	Replaced by		



TD NO. 322622 0	CARD PRINT C.F.G	
Code according to 800 100-119, 140-141 Rev. B, 100-151 Rev. B, 100-164	82.12.08	AL
	26/04/83	BM
Corrected	Date	Sign.
N500 INTERFACE LIMIT REGISTERS AND COMPARATOR	Print no. 3022	Date 26/04/83 Code TS Page 6 of 6
NORSK DATA A.S Oslo, Norway	Registered by 5A75	

NORSK DATA A.S Oslo, Norway	Title 5205, CACHE TERMINATION WIRING LIST	Drawing no. Page 1 of 3

CONNECTOR PIN (ROW A AND C OPPOSITE OF BACKWIRING)	RESISTOR NETWORK PIN	SIGNAL INSTR: CACHE (POS. 1-4) B-CONNECTOR AI (0-15)	SIGNAL DATA CACHE (POS. 6-9) A-CONNECTOR AD (0-15)
a5	8A6	0	3
c5	8A5	2	2
a6	8A4	9	1
c6	8A3	11	0
a7	8A2	10	8
c7	8A1	8	9
a8	8A8	1	10
c8	8A9	3	11
a9	8A10	15	15
c9	8A11	14	14
a10	8A12	13	13
c10	8A13	12	12
a11	6A6	7	7
c11	6A5	6	6
a12	6A4	5	5
c12	6A3	4	4

DRAWN BY BS/AL	Remarks	Replacement for	Date 16.06.80
APPROVED BY		Replaced by	Date
DATE			

NORSK DATA A.S Oslo, Norway	Title 5205, CACHE TERMINATION BOARD WIRING LIST	Drawing no. Page 2 of 3

CONNECTOR PIN (ROW A AND C OPPOSITE OF BACKWIRING)	RESISTOR NETWORK PIN	SIGNAL INSTR: CACHE (POS. 1-4) B-CONNECTOR ID (16-31)	SIGNAL DATA CACHE (POS. 6-9) D (16-31)
a15	6A2	30	30
c15	6A1	31	31
a16	6A8	28	28
c16	6A9	29	29
a17	6A10	26	26
c17	6A13	27	27
a18	6A12	24	24
c18	6A11	25	25
a19	4A6	23	23
c19	4A5	22	22
a20	4A1	21	21
c20	4A2	20	20
a21	4A3	19	19
c21	4A4	18	18
a22	4A8	17	17
c22	4A9	16	16

DRAWN BY BS/AL	Remarks	Replacement for	Date 16.06.80
APPROVED BY		Replaced by	Date
DATE			

NORSK DATA A.S Oslo, Norway	Title 5205, CACHE TERMINATION BOARD WIRING LIST	Drawing no. Page 3 of 3

CONNECTOR PIN (ROW A AND C OPPOSITE OF BACKWIRING)	RESISTOR NETWORK PIN	SIGNAL INSTR: CACHE (POS. 1-4) B-CONNECTOR ID (0-15)	SIGNAL DATA CACHE (POS. 6-9) A-CONNECTOR D (0-15)
a23	4A13	15	15
c23	4A12	14	14
a24	4A11	13	13
c24	4A10	12	12
a25	2A6	11	11
c25	2A5	10	10
a26	2A1	9	9
c26	2A2	8	8
a27	2A3	7	7
c27	2A4	6	6
a28	2A8	5	5
c28	2A9	4	4
a29	2A13	3	3
c29	2A12	2	2
a30	2A11	1	1
c30	2A10	0	0

DRAWN BY BS/AL	Remarks	Replacement for	Date
APPROVED BY			16.06.80
DATE		Replaced by	Date

NORSK DATA A.S

Title: INTERNAL - EXTERNAL CABLE ND 500 - ND 100 1/0

Drawing No.: 3 - 9387 B

WIRE NO.	SIGNAL	POLARITY	EUROPLUG IN N - 500 RACK PIN NO.	PLUGPANEL 2x37 PIN D. CON.IN N - 500 PIN. NO.	PLUGPANEL 2x37 PIN D. CON. IN N - 100 PIN. NO.	EUROPLUG IN N - 100 BackWIRING
01	GROUND		Cc 1	1	1	Ac 1
02	GROUND		Ca 1	20	20	Aa 1
03	DBU 0	0	Cc 2	2	2	Ac 2
04	DBU 0	1	Ca 2	21	21	Aa 2
05	DBU 1	0	Cc 3	3	3	Ac 3
06	DBU 1	1	Ca 3	22	22	Aa 3
07	DBU 2	0	Cc 4	4	4	Ac 4
08	DBU 2	1	Ca 4	23	23	Aa 4
09	DBU 3	0	Cc 5	5	5	Ac 5
10	DBU 3	1	Ca 5	24	24	Aa 5
11	DBU 4	0	Cc 6	6	6	Ac 6
12	DBU 4	1	Ca 6	25	25	Aa 6
13	DBU 5	0	Cc 7	7	7	Ac 7
14	DBU 5	1	Ca 7	26	26	Aa 7
15	DBU 6	0	Cc 8	8	8	Ac 8
16	DBU 6	1	Ca 8	27	27	1 Aa 8
17	DBU 7	0	Cc 9	9	9	Ac 9
18	DBU 7	1	Ca 9	28	28	Aa 9
19	DBU 8	0	Cc 10	10	10	Ac 10
20	DBU 8	1	Ca 10	29	29	Aa 10
21	DBU 9	0	Cc 11	11	11	Ac 11
22	DBU 9	1	Ca 11	30	30	Aa 11
23	DBU 10	0	Cc 12	12	12	Ac 12
24	DBU 10	1	Ca 12	31	31	Aa 12
25	DBU 11	0	Cc 13	13	13	Ac 13
26	DBU 11	1	Ca 13	32	32	Aa 13
27	DBU 12	0	Cc 14	14	14	Ac 14
28	DBU 12	1	Ca 14	33	33	Aa 14
29	DBU 13	0	Cc 15	15	15	Ac 15
30	DBU 13	1	Ca 15	34	34	Aa 15
31	DBU 14	0	Cc 16	16	16	Ac 16
32	DBU 14	1	Ca 16	35	35	Aa 16
33	DBU 15	0	Cc 17	1	1	Ac 17
34	DBU 15	1	Ca 17	20	20	Aa 17
35	TIN 0	0	Cc 18	2	2	Ac 18
36	TIN 0	1	Ca 18	21	21	Aa 18
37	TIN 1	0	Cc 19	3	3	Ac 19
38	TIN 1	1	Ca 19	22	22	Aa 19
39	TIN 2	0	Cc 20	4	4	Ac 20
40	TIN 2	1	Ca 20	23	23	Aa 20
41	TIN 3	0	Cc 21	5	5	Ac 21
42	TIN 3	1	Ca 21	24	24	Aa 21
43	TIN 4	0	Cc 22	6	6	Ac 22
44	TIN 4	1	Ca 22	25	25	Aa 22
45	UNLOCK	0	Cc 23	7	7	Ac 23
46	UNLOCK	1	Ca 23	26	26	Aa 23
47	PWR. FAIL	0	Cc 24	8	8	Ac 24
48	PWR. FAIL	1	Ca 24	27	27	2 Aa 24
49	MSTR. CL	0	Cc 25	9	9	Ac 25
50	MSTR. CL	1	Ca 25	28	28	Aa 25
51	RETAG	0	Cc 26	10	10	Ac 26
52	RETAG	1	Ca 26	29	29	Aa 26
53	DATA IN	0	Cc 27	11	11	Ac 27
54	DATA IN	1	Ca 27	30	30	Aa 27
55	SPARE		Cc 28	12	12	Ac 28
56	SPARE		Ca 28	31	31	Aa 28
57	ACTIVATE	0	Cc 29	13	13	Ac 29
58	ACTIVATE	1	Ca 29	32	32	Aa 29
59	STOP	0	Cc 30	14	14	Ac 30
60	STOP	1	Ca 30	33	33	Aa 30
61	DATA OUT	0	Cc 31	15	15	Ac 31
62	DATA OUT	1	Ca 31	34	34	Aa 31
63	GROUND		Cc 32	16	16	Ac 32
64	GROUND		Ca 32	35	35	Aa 32

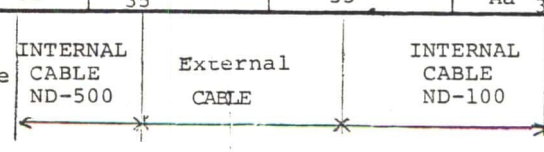
INTERNAL CABLE TYPE: 64 wire flat cable

EXTERNAL CABLE TYPE 1: 64 Wire flat cable

EXTERNAL CABLE TYPE 2:

EXTERNAL CABLE TYPE 3:

EXTERNAL CABLE TYPE 4:



Drawn by: HO/ma	Remarks	Replacement for	Date
Approved			
Date: 21.8.80		Replaced by	Date

NORSK DATA A.S

Title: ND-500

INTERNAL CABLE DATA INST. ADDRESS AND 5204 PCB ADAPTER

MEM 2

Drawing No. 3 - 9513

WIRE NO.	SIGNAL	POLARITY	ND-500 POS. EUROPLUG PIN NO	ADDRESS IN ON 5204 PCB ON PLUG PANEL EUROPLUG PIN NO	5204 PCB ADAPTER OUT 1/1 CACHE EUROPLUG PIN NO	5204 PCB ADAPTER OUT ½ CACHE EUROPLUG PIN NO	5204 PCB ADAPTER OUT ¼ CACHE EUROPLUG PIN NO
01	GROUND		C c1	c1	NOT USED	NOT USED	NOT USED
02	GROUND		C a1	a1	NOT USED	NOT USED	NOT USED
03	LMA 2	0	C c2	c2	NOT USED	NOT USED	c17
04	LMA 2	1	C a2	a2	NOT USED	NOT USED	a17
05	LMA 3	0	C c3	c3	NOT USED	c17	c18
06	LMA 3	1	C a3	a3	NOT USED	a17	a18
07	LMA 4	0	C c4	c4	c17	c18	c19
08	LMA 4	1	C a4	a4	a17	a18	a19
09	LMA 5	0	C c5	c5	c18	c19	c20
10	LMA 5	1	C a5	a5	a18	a19	a20
11	LMA 6	0	C c6	c6	c19	c20	c21
12	LMA 6	1	C a6	a6	a19	a20	a21
13	LMA 7	0	C c7	c7	c20	c21	c22
14	LMA 7	1	C a7	a7	a20	a21	a22
15	LMA 8	0	C c8	c8	c21	c22	c23
16	LMA 8	1	C a8	a8	a21	a22	a23
17	LMA 9	0	C c9	c9	c22	c23	c24
18	LMA 9	1	C a9	a9	a22	a23	a24
19	LMA 10	0	C c10	c10	c23	c24	c25
20	LMA 10	1	C a10	a10	a23	a24	a25
21	LMA 11	0	C c_{11}	c_{11}	c24	c25	c26
22	LMA 11	1	C a_{11}	a_{11}	a24	a25	a26
23	LMA 12	0	C c_{12}	c_{12}	c25	c26	c27
24	LMA 12	1	C a_{12}	a_{12}	a25	a26	a27
25	LMA 13	0	C c_{13}	c_{13}	c26	c27	c28
26	LMA 13	1	C a_{13}	a_{13}	a26	a27	a28
27	LMA 14	0	C c_{14}	c_{14}	c27	c28	c29
28	LMA 14	1	C a_{14}	a_{14}	a27	a28	a29
29	LMA 15	0	C c_{15}	c_{15}	c28	c29	c30
30	LMA 15	1	C a_{15}	a_{15}	a28	a29	a30
31	LMA 16	0	C c_{16}	c_{16}	c29	c30	c31
32	LMA 16	1	C a_{16}	a_{16}	a29	a30	a31
33	LMA 17	0	C c_{17}	c_{17}	c30	c31	c32
34	LMA 17	1	C a_{17}	a_{17}	a30	a31	a32
35	LMA 18	0	C c_{18}	c_{18}	c31	c32	c15
36	LMA 18	1	C a_{18}	a_{18}	a31	a32	a15
37	LRA 19	0	C c_{19}	c_{19}	c32	c15	c16
38	LRA 19	1	C a_{19}	a_{19}	a32	a15	a16
39	LRA 20	0	C c_{20}	c_{20}	c15	c16	NOT USED
40	LRA 20	1	C a_{20}	a_{20}	a15	a16	NOT USED
41	LRA 21	0	C c_{21}	c_{21}	c16	NOT USED	NOT USED
42	LRA 21	1	C a_{21}	a_{21}	a16	NOT USED	NOT USED
43		0	C c_{22}	c_{22}			
44		1	C a_{22}	a_{22}			
45		0	C c_{23}	c_{23}			
46		1	C a_{23}	a_{23}			
47		0	C c_{24}	c_{24}			
48		1	C a_{24}	a_{24}			
49		0	C c_{25}	c_{25}			
50		1	C a_{25}	a_{25}			
51		0	C c_{26}	c_{26}			
52		1	C a_{26}	a_{26}			
53		0	C c_{27}	c_{27}			
54		1	C a_{27}	a_{27}			
55		0	C c_{28}	c_{28}			
56		1	C a_{28}	a_{28}			
57		0	C c_{29}	c_{29}			
58		1	C a_{29}	a_{29}			
59		0	C c_{30}	c_{30}			
60		1	C a_{30}	a_{30}			
61		0	C c_{31}	c_{31}			
62		1	C a_{31}	a_{31}			
63	GROUND		C c_{32}	c_{32}			
64	GROUND		C a_{32}	a_{32}			

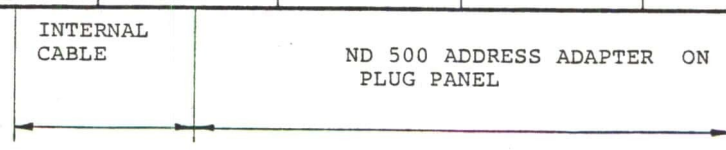
INTERNAL CABLE TYPE: 64 WIRE

EXTERNAL CABLE TYPE 1: FLAT CABLE

EXTERNAL CABLE TYPE 2:

EXTERNAL CABLE TYPE 3:

EXTERNAL CABLE TYPE 4:



Drawn by: HO/ma

Approved:

Date: 27.5.81

Remarks: CONNECTED FROM RACK POS C11 AND C12 TO PCB 5204 ON PLUG PANEL

Replacement for: Date:

Replaced by: Date:

NORSK DATA A.S

Title: ND-500

INTERNAL CABLE DATA - INST. DATA AND 5203 PCB ADAPTER MEM 2

Drawing No. 3 - 9514

WIRE NO.	SIGNAL	POLARITY	EUROPLUG IN IN ND 500 RACK PIN NO	DATA ND500 ON 5203 PCB ON PLUG EUROPLUG PIN NO	5203 PCB ADAPTER DATA LEAST PIN NO	5203 PCB ADAPTER DATA MOST PIN NO	
01	B0L	0	C c1	c1	c17		
02	B0L	1	C a1	a1	a17		
03	B1L	0	C c2	c2	c18		
04	B1L	1	C a2	a2	a18		
05	B2L	0	C c3	c3	c19		
06	B2L	1	C a3	a3	a19		
07	B3L	0	C c4	c4	c20		
08	B3L	1	C a4	a4	a20		
09	B4L	0	C c5	c5	c21		
10	B4L	1	C a5	a5	a21		
11	B5L	0	C c6	c6	c22		
12	B5L	1	C a6	a6	a22		
13	B6L	0	C c7	c7	c23		
14	B6L	1	C a7	a7	a23		
15	B7L	0	C c8	c8	c24		
16	B7L	1	C a8	a8	a24		
17	B8L	0	C c9	c9	c25		
18	B8L	1	C a9	a9	a25		
19	B9L	0	C c10	c10	c26		
20	B9L	1	C a10	a10	a26		
21	B10L	0	C c11	c11	c27		
22	B10L	1	C a11	a11	a27		
23	B11L	0	C c12	c12	c28		
24	B11L	1	C a12	a12	a28		
25	B12L	0	C c13	c13	c29		
26	B12L	1	C a13	a13	a29		
27	B13L	0	C c14	c14	c30		
28	B13L	1	C a14	a14	a30		
29	B14L	0	C c15	c15	c31		
30	B14L	1	C a15	a15	a31		
31	B15L	0	C c16	c16	c32		
32	B15L	1	C a16	a16	a32		
33	B16L	0	C c17	c17		c17	
34	B16L	1	C a17	a17		a17	
35	B17L	0	C c18	c18		c18	
36	B17L	1	C a18	a18		a18	
37	B18L	0	C c19	c19		c19	
38	B18L	1	C a19	a19		a19	
39	B19L	0	C c20	c20		c20	
40	B19L	1	C a20	a20		a20	
41	B20L	0	C c21	c21		c21	
42	B20L	1	C a21	a21		a21	
43	B21L	0	C c22	c22		c22	
44	B21L	1	C a22	a22		a22	
45	B22L	0	C c23	c23		c23	
46	B22L	1	C a23	a23		a23	
47	B23L	0	C c24	c24		c24	
48	B23L	1	C a24	a24		a24	
49	B24L	0	C c25	c25		c25	
50	B24L	1	C a25	a25		a25	
51	B25L	0	C c26	c26		c26	
52	B25L	1	C a26	a26		a26	
53	B26L	0	C c27	c27		c27	
54	B26L	1	C a27	a27		a27	
55	B27L	0	C c28	c28		c28	
56	B27L	1	C a28	a28		a28	
57	B28L	0	C c29	c29		c29	
58	B28L	1	C a29	a29		a29	
59	B29L	0	C c30	c30		c30	
60	B29L	1	C a30	a30		a30	
61	B30L	0	C c31	c31		c31	
62	B30L	1	C a31	a31		a31	
63	B31L	0	C c32	c32		c32	
64	B31L	1	C a32	a32		a32	

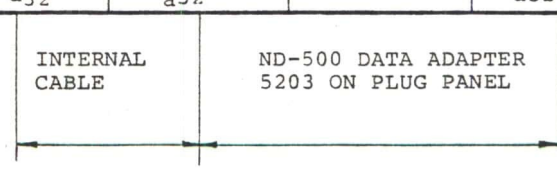
INTERNAL CABLE TYPE: 64 WIRE

EXTERNAL CABLE TYPE 1: FLAT CABLE

EXTERNAL CABLE TYPE 2:

EXTERNAL CABLE TYPE 3:

EXTERNAL CABLE TYPE 4:



NB! See drawing 3-9515

Drawn by: HO/ma

Approved:

Date: 27.5.81

Remarks: CONNECTED FROM RACK POS. C9,C8,C7, C6 and C4,C3,C2,C1 TO PLUG ND-500 DATA ON 5203 PCB ON PLUG PANEL

Replacement for | Date

Replaced by | Date

NORSK DATA A.S

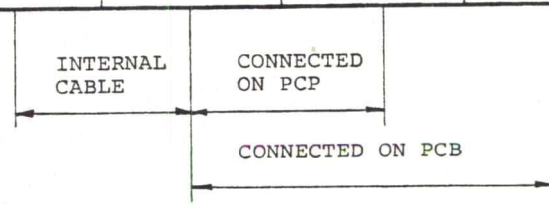
Title: ND-500

INTERNAL CABLE DATA - INST. CONTROL AND 5203 PCB ADAPTER OUTPUT FOR MEMORY 2

Drawing No. 3-9515

WIRE NO.	SIGNAL	POLARITY	EUROPLUG IN ND-500 RACK PIN NO	CONT. PLUG IN 5203 PCB ON PLUG PANEL EUROPLUG PIN NO	5203 PCB ADAPTER OUTPUT DATA LEAST PIN NO	5203 PCB ADAPTER OUTPUT DATA MOST PIN NO
01	GROUND		D c1	c1		
02	GROUND		D a1	a1		
03	+5V		D c2	c2		
04	+5V		D a2	a2		
05	MPL0	0	D c3	c3	c15	
06	MPL0	1	D a3	a3	a15	
07	MPL1	0	D c4	c4	c16	
08	MPL1	1	D a4	a4	a16	
09	REQ1	0	D c5	c5	c11	
10	REQ1	1	D a5	a5	a11	
11	WM 1	0	D c6	c6	c12	
12	WM 1	1	D a6	a6	a12	
13	DR 1	0	D c7	c7	c13	
14	DR 1	1	D a7	a7	a13	
15	MAR1 (NOT USED)	0	D c8	c8	c14	
16	MAR1 (NOT USED)	1	D a8	a8	a14	
17			D c9	c9		
18			D a9	a9		
19	MPL2	0	D c10	c10		c15
20	MPL2	1	D a10	a10		a15
21	MPL3	0	D c11	c11		c16
22	MPL3	1	D a11	a11		a16
23	REQ0	0	D c12	c12		c11
24	REQ0	1	D a12	a12		a11
25	WM 0	0	D c13	c13		c12
26	WM 0	1	D a13	a13		a12
27	DR 0	0	D c14	c14		c13
28	DR 0	1	D a14	a14		a13
29	MAR0 (NOT USED)		D c15	c15		c14
30	MAR0 (NOT USED)		D a15	a15		a14
31			D c16	c16		
32			D a16	a16		
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						
47						
48						
49						
50						
51						
52						
53						
54						
55						
56						
57						
58						
59						
60						
61						
62						
63						
64						

INTERNAL CABLE TYPE: 32 WIRE
EXTERNAL CABLE TYPE 1: FLAT CABLE
EXTERNAL CABLE TYPE 2:
EXTERNAL CABLE TYPE 3:
EXTERNAL CABLE TYPE 4:



Drawn by: HO/ma
Approved:
Date: 27.5.81

Remarks: CONNECTED FROM RACK POS D9,D8,D7,D6 AND D4,D3,D2,D1, TO PLUG CONTROL ON PCB 5203 ON PLUG PANEL

Replacement for | Date
Replaced by | Date

NORSK DATA A.S

Title: BMPM CONN - ND 500
INTERNAL CABLE (DATA-INSTR).
ADDR. VIA 1976 PCB BMPM N-500
MEM.2

Drawing No. 3 - 9516

WIRE NO.	SIGNAL	POLARITY	BMPM POS EUROPLUG PIN NO.	PLUG ADDRESS TO 1976 PCB SOLDRING SIDE PIN NO.	1976 PCB PLUG ADDRESS IN/OUT PLUG SIDE PIN NO.	1976 PCB PLUG DATA DATA TERM PLUG SIDE PIN NO.	PLUG ON EXT. PLUG PANEL (EP) PIN NO.
01	BA 15	0	95	1	2		2
02	BA 15	1	94	2	1		1
03	BA 14	0	93	3	4		4
04	BA 14	1	92	4	3		3
05	BA 13	0	91	5	6		6
06	BA 13	1	90	6	5		5
07	BA 12	0	89	7	8		8
08	BA 12	1	88	8	7		7
09	BA 11	0	87	9	10		10
10	BA 11	1	86	10	9		9
11	BA 10	0	85	11	12		12
12	BA 10	1	84	12	11		11
13	BA 9	0	83	13	14		14
14	BA 9	1	82	14	13		13
15	BA 8	0	81	15	16		16
16	BA 8	1	80	16	15		15
17	BA 7	0	79	17	18		18
18	BA 7	1	78	18	17		17
19	BA 6	0	77	19	20		20
20	BA 6	1	76	20	19		19
21	BA 5	0	75	21	22		22
22	BA 5	1	74	22	21		21
23	BA 4	0	73	23	24		24
24	BA 4	1	72	24	23		23
25	BA 3	0	71	25	26		26
26	BA 3	1	70	26	25		25
27	BA 2	0	69	27	28		28
28	BA 2	1	68	28	27		27
29	BA 1	0	67	29	30		30
30	BA 1	1	66	30	29		29
31	BA 0	0	65	31	32		32
32	BA 0	1	64	32	31		31
33	BA 17	0	63	33	34		34
34	BA 17	1	62	34	33		33
35	BA 16	0	61	35	36		36
36	BA 16	1	60	36	35		35
37	WR	0	59	37	38 CONN.	42	38
38	WR	1	58	38	37 ONLY	41	37
39	REQ	0	57	39	40 IN	44	40
40	REQ	1	56	40	39 PLUG	43	39
41							42
42							41
43							44
44							43
45							46
46							45
47							48
48							47
49							50
50							49
51							
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
64							

50 PIN PLUG 3M3307

50 PIN PLUG ANSLEY MALE ON 1976 PCB

50 PIN PLUG MALE ON 1976 PCB

50 PIN PLUG MALE ON 1976 PCB

50 PIN MALE ON PLUG PANEL

INTERNAL CABLE TYPE 1: 46 WIRE
INTERNAL CABLE TYPE 2: 50 WIRE
EXTERNAL CABLE TYPE
EXTERNAL CABLE TYPE
EXTERNAL CABLE TYPE

INTERNAL CABLE FROM LOCAL PANEL TO BACKWIRING

CABLE TYPE 1

SAME PLUG ON 1976 PCB

CONNECTION ON 1976 PCB

INTERNAL CABLE BETWEEN 1976 PCB AND Ext. PLUG PANEL. CABLE TYPE 2

Drawn by HO/ma	Remarks	Replacement for	Date
Approved			
Date 3.6.81		Replaced by	Date

NORSK DATA A.S

Title: BMPM CONN. - ND 500
INTERNAL CABLE (DATA - INSTR).
DATA LEAST - DATA MOST VIA
1976 PCB BMPM N-500 MEM 2

Drawing No. 3 - 9517

WIRE NO.	SIGNAL	POLARITY	BMPM POS EUROPLUG PIN NO.	PLUG DATA TO 1976 PCB SOLDRING SIDE PIN NO.	1976 PCB PLUG ADDR. IN/OUT PIN NO.	1976 PCB PLUG DATA DATA TERM PIN NO.	PLUG ON EXT. PLUG PANEL (EP) PIN NO.
01	BD 15	0	95	1		2	2
02	BD 15	1	94	2		1	1
03	BD 14	0	93	3		4	4
04	BD 14	1	92	4		3	3
05	BD 13	0	91	5		6	6
06	BD 13	1	90	6		5	5
07	BD 12	0	89	7		8	8
08	BD 12	1	88	8		7	7
09	BD 11	0	87	9		10	10
10	BD 11	1	86	10		9	9
11	BD 10	0	85	11		12	12
12	BD 10	1	84	12		11	11
13	BD 9	0	83	13		14	14
14	BD 9	1	82	14		13	13
15	BD 8	0	81	15		16	16
16	BD 8	1	80	16		15	15
17	BD 7	0	79	17		18	18
18	BD 7	1	78	18		17	17
19	BD 6	0	77	19		20	20
20	BD 6	1	76	20		19	19
21	BD 5	0	75	21		22	22
22	BD 5	1	74	22		21	21
23	BD 4	0	73	23		24	24
24	BD 4	1	72	24		23	23
25	BD 3	0	71	25		26	26
26	BD 3	1	70	26		25	25
27	BD 2	0	69	27		28	28
28	BD 2	1	68	28		27	27
29	BD 1	0	67	29		30	30
30	BD 1	1	66	30		29	29
31	BD 0	0	65	31		32	32
32	BD 0	1	64	32		31	31
33	BD 17	0	63	33		34	34
34	BD 17	1	62	34		33	33
35	BD 16	0	61	35		36	36
36	BD 16	1	60	36		35	35
37	AR	0	59	37		38	38
38	AR	1	58	38		37	37
39	DR	0	57	39		40	40
40	DR	1	56	40		39	39
41	WR } IN	0			38 } CONN.	42	42
42	WR } ADDR.	1			37 } ONLY	41	41
43	REQ } PLUG	0			40 } IN	44	44
44	REQ }	1			39 } PLUG	43	43
45						46	46
46						45	45
47							48
48							47
49							50
50							49
51							
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
64							

50 PIN PLUG 3M3307

50 PIN PLUG MALE PLUG ON 1976 PCB

50 PIN PLUG MALE PLUG ON 1976 PCB

50 PIN PLUG MALE PLUG ON 1976 PCB

50 PIN PLUG MALE ON PLUG PANEL

INTERNAL CABLE TYPE: 1:40 WIRE
INTERNAL CABLE TYPE 2:50 WIRE

INTERNAL CABLE LOCAL PANEL TO BACKWIRING

CABLE TYPE 1

DATA PLUG IS SAME PLUG ON 1976 PCB

CONNECTION ON 1976 PCB

INTERNAL CABLE BETWEEN 1976 PCB AND EXT. PLUG PANEL
CABLE TYPE 2

Drawn by	HO/ma	Remarks	Replacement for	Date
Approved			Replaced by	Date
Date	3.6.81			

NORSK DATA A.S

Title: BMPM CONN - ND 500
EXT. CABLE (DATA - INSTR).
ADDRESS AND (DATA - INSTR). DATA

Drawing No. 3 - 9518

WIRE NO.	SIGNAL	POLARITY	ND 500 PLUG PANEL EUROPLUG PIN NO	DUAL BMPM EXT.PLUG PANEL PIN NO			
01			a 32	1			
02			c 32	2			
03			a 31	3			
04			c 31	4			
05			a 30	5			
06			c 30	6			
07			a 29	7			
08			c 29	8			
09			a 28	9			
10			c 28	10			
11			a 27	11			
12			c 27	12			
13			a 26	13			
14			c 26	14			
15			a 25	15			
16			c 25	16			
17			a 24	17			
18			c 24	18			
19			a 23	19			
20			c 23	20			
21			a 22	21			
22			c 22	22			
23			a 21	23			
24			c 21	24			
25			a 20	25			
26			c 20	26			
27			a 19	27			
28			c 19	28			
29			a 18	29			
30			c 18	30			
31			a 17	31			
32			c 17	32			
33			a 16	33			
34			c 16	34			
35			a 15	35			
36			c 15	36			
37			a 14	37			
38			c 14	38			
39			a 13	39			
40			c 13	40			
41			a 12	41			
42			c 12	42			
43			a 11	43			
44			c 11	44			
45			a 10	45			
46			c 10	46			
47			a 9	47			
48			c 9	48			
49			a 8	49			
50			c 8	50			
51			EUROPLUG 64 PIN FEMALE	50 PIN PLUG FEMALE			
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
64							

INTERNAL CABLE TYPE:
EXTERNAL CABLE TYPE 1: 50 WIRE FLAT
EXTERNAL CABLE TYPE 2:
EXTERNAL CABLE TYPE 3:
EXTERNAL CABLE TYPE 4:

Drawn by HO/ma	Remarks FOR ND 500 PLUG PANEL/ 3M33320000 FOR BMPM EXT. PLUG PANEL ANSLEY/609-5001	Replacement for	Date
Approved		Replaced by	Date
Date 4.6.81			

NORSK DATA A.S

Title: BMPM CONN. ND-100
INTERNAL CABLE ND-100 OR DMA
INTERLEAVE ADDRESS VIA 1988 PCB
MEM 2

Drawing No. 3 - 9519

WIRE NO.	SIGNAL FROM ND 100 TO EXT. PLUG PANEL BMPM IN ON 1988 PCB	POLARITY	PLUG ADDRESS 1988 PCB ON EXT. PLUG PANEL PLUG IN PIN NO	0 WAY INTERLEAVE		2 WAY INTERLEAVE		4 WAY INTERLEAVE		8 WAY INTERLEAVE	
				PLUG 1988 PCB	BMPM POS	PLUG 1988 PCB	BMPM POS	PLUG 1988 PCB	BMPM POS	PLUG 1988 PCB	
01	BAL 15	1	1	1	95	3	93	5	91	7	89
02	BAL 15	0	2	2	94	4	92	6	90	8	88
03	BAL 14	1	3	3	93	5	91	7	89	9	87
04	BAL 14	0	4	4	92	6	90	8	88	10	86
05	BAL 13	1	5	5	91	7	89	9	87	11	85
06	BAL 13	0	6	6	90	8	88	10	86	12	84
07	BAL 12	1	7	7	89	9	87	11	85	13	83
08	BAL 12	0	8	8	88	10	86	12	84	14	82
09	BAL 11	1	9	9	87	11	85	13	83	15	81
10	BAL 11	0	10	10	86	12	84	14	82	16	80
11	BAL 10	1	11	11	85	13	83	15	81	17	79
12	BAL 10	0	12	12	84	14	82	16	80	18	78
13	BAL 9	1	13	13	83	15	81	17	79	19	77
14	BAL 9	0	14	14	82	16	80	18	78	20	76
15	BAL 8	1	15	15	81	17	79	19	77	21	75
16	BAL 8	0	16	16	80	18	78	20	76	22	74
17	BAL 7	1	17	17	79	19	77	21	75	23	73
18	BAL 7	0	18	18	78	20	76	22	74	24	72
19	BAL 6	1	19	19	77	21	75	23	73	25	71
20	BAL 6	0	20	20	76	22	74	24	72	26	70
21	BAL 5	1	21	21	75	23	73	25	71	27	69
22	BAL 5	0	22	22	74	24	72	26	70	28	68
23	BAL 4	1	23	23	73	25	71	27	69	29	67
24	BAL 4	0	24	24	72	26	70	28	68	30	66
25	BAL 3	1	25	25	71	27	69	29	67	31	65
26	BAL 3	0	26	26	70	28	68	30	66	32	64
27	BAL 2	1	27	27	69	29	67	31	65	45	51
28	BAL 2	0	28	28	68	30	66	32	64	46	50
29	BAL 1	1	29	29	67	31	65	45	51	43	53
30	BAL 1	0	30	30	66	32	64	46	50	44	52
31	BAL 0	1	31	31	65	45	51	35	53	41	55
32	BAL 0	0	32	32	64	46	50	34	52	42	54
33	BAL 17	1	33	33	63	35	61	1	95	3	93
34	BAL 17	0	34	34	62	36	60	2	94	4	92
35	BAL 16	1	35	35	61	37	95	3	93	5	91
36	BAL 16	0	36	36	60	38	94	4	92	6	90
37	WR	1	37	37	59	39	59	37	59	37	59
38	WR	0	38	38	58	40	58	38	58	38	58
39	REQ	1	39	39	57	41	57	39	57	39	57
40	REQ	0	40	40	56	42	56	40	56	40	56
41	BAL 18	1	41	41	55	33	63	35	61	1	95
42	BAL 18	0	42	42	54	34	62	36	60	2	94
43	BAL 19	1	43	43	53	41	55	33	63	33	61
44	BAL 19	0	44	44	52	42	54	34	62	34	60
45	BAL 20	1	45	45	51	43	53	41	55	35	63
46	BAL 20	0	46	46	50	44	52	42	54	36	62
47	BAL 21	1	NC	NC	NC	NC	NC	NC	NC	NC	NC
48	BAL 21	0	NC	NC	NC	NC	NC	NC	NC	NC	NC
49											
50											
51											
52											
53											
54											
55											
56											
57											
58											
59											
60											
61											
62											
63											
64											

INTERNAL CABLE TYPE:1; 50 WIRE FLAT CABLE BETWEEN EXTERNAL PLUG PANEL AND LOCAL PANEL 1:1
INTERNAL CABLE TYPE 2: 46 WIRE FLAT CABLE BETWEEN LOCAL PLUG PANEL AND BACKWIRING 1:1

Drawn by: HO/ma
Approved:
Date: 4.6.81

Remarks:
ALL BMPM POS. AS A SAME BMPM POS.
50 PIN 3M3307

Replacement for | Date
Replaced by | Date

NORSK DATA A.S	Title BMPM CONN. ND-100 INTERNAL CABLE ND-100 AND DMA DATA MEM 2.	Drawing No. 3 - 9520

WIRE NO.	SIGNAL FROM ND-100 TO EXT. PLUG PANEL BMPM	POLARITY	PLUG DATA ON EXT. PLUG PANEL ON BMPM PIN NO	PLUG DATA ON LOCAL PLUG PANEL ON BMPM PIN NO	BMPM POS PIN NO
01	BDL 15	0	1	1	95
02	BDL 15	1	2	2	94
03	BDL 14	0	3	3	93
04	BDL 14	1	4	4	92
05	BDL 13	0	5	5	91
06	BDL 13	1	6	6	90
07	BDL 12	0	7	7	89
08	BDL 12	1	8	8	88
09	BDL 11	0	9	9	87
10	BDL 11	1	10	10	86
11	BDL 10	0	11	11	85
12	BDL 10	1	12	12	84
13	BDL 9	0	13	13	83
14	BDL 9	1	14	14	82
15	BDL 8	0	15	15	81
16	BDL 8	1	16	16	80
17	BDL 7	0	17	17	79
18	BDL 7	1	18	18	78
19	BDL 6	0	19	19	77
20	BDL 6	1	20	20	76
21	BDL 5	0	21	21	75
22	BDL 5	1	22	22	74
23	BDL 4	0	23	23	73
24	BDL 4	1	24	24	72
25	BDL 3	0	25	25	71
26	BDL 3	1	26	26	70
27	BDL 2	0	27	27	69
28	BDL 2	1	28	28	68
29	BDL 1	0	29	29	67
30	BDL 1	1	30	30	66
31	BDL 0	0	31	31	65
32	BDL 0	1	32	32	64
33	BDL 17	0	33	33	63
34	BDL 17	1	34	34	62
35	BDL 16	0	35	35	61
36	BDL 16	1	36	36	60
37	ARL	0	37	37	59
38	ARL	1	38	38	58
39	DRL	0	39	39	57
40	DRL	1	40	40	56
41			41	41	
42			42	42	
43			43	43	
44			44	44	
45			45	45	
46			46	46	
47			47	47	
48			48	48	
49			49	49	
50			50	50	
51					
52					
53			50 PIN PLUG MALE ON PLUG PANEL	50 PIN PLUG MALE ON PLUG PANEL	50 PIN PLUG 3M3307
54					
55					
56					
57					
58					
59					
60					
61					
62					
63					
64					

INTERNAL CABLE TYPE: 1: 50 WIRE FLAT CABLE
INTERNAL CABLE TYPE 2: 40 WIRE FLAT CABLE

INTERNAL CABLE TYPE 1 | INTERNAL CABLE TYPE 2

Drawn by HO/ma	Remarks	Replacement for	Date
Approved			
Date 4.6.81		Replaced by	Date

NORSK DATA A.S

Title: BMPM CONN. ND - 100
INTERNAL CABLE ERROR LOG
BMPM

Drawing No. 3 - 9521

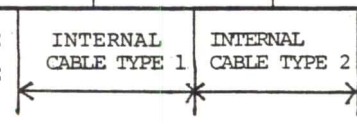
WIRE NO.	SIGNAL	POLARITY	BMPM POS PIN NO	LOCAL PLUG PANEL ON BMPM PIN NO	EXT. PLUG PANEL ON BMPM PIN NO		
01	B 15 L	0	95	1	1		
02	B 15 L	1	94	2	2		
03	B 14 L	0	93	3	3		
04	B 14 L	1	92	4	4		
05	B 13 L	0	91	5	5		
06	B 13 L	1	90	6	6		
07	B 12 L	0	89	7	7		
08	B 12 L	1	88	8	8		
09	B 11 L	0	87	9	9		
10	B 11 L	1	86	10	10		
11	B 10 L	0	85	11	11		
12	B 10 L	1	84	12	12		
13	B 9 L	0	83	13	13		
14	B 9 L	1	82	14	14		
15	B 8 L	0	81	15	15		
16	B 8 L	1	80	16	16		
17	B 7 L	0	79	17	17		
18	B 7 L	1	78	18	18		
19	B 6 L	0	77	19	19		
20	B 6 L	1	76	20	20		
21	B 5 L	0	75	21	21		
22	B 5 L	1	74	22	22		
23	B 4 L	0	73	23	23		
24	B 4 L	1	72	24	24		
25	B 3 L	0	71	25	25		
26	B 3 L	1	70	26	26		
27	B 2 L	0	69	27	27		
28	B 2 L	1	68	28	28		
29	B 1 L	0	67	29	29		
30	B 1 L	1	66	30	30		
31	B 0 L	0	65	31	31		
32	B 0 L	1	64	32	32		
33	LINTL	0	63	33	33		
34	LINTL	1	62	34	34		
35	LDRYL	0	61	35	35		
36	LDRYL	1	60	36	36		
37	ACTL	0	59	37	37		
38	ACTL	1	58	38	38		
39	LIOXL	0	57	39	39		
40	LIOXL	1	56	40	40		
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
64							

50 PIN PLUG 3M3307

50 PIN PLUG MALE ON PLUG PANEL

50 PIN PLUG MALE ON PLUG PANEL

INTERNAL CABLE TYPE 1: 40 WIRE FLAT CABLE
INTERNAL CABLE TYPE 2: 50 WIRE FLAT CABLE
EXTERNAL CABLE TYPE 2:
EXTERNAL CABLE TYPE 3:
EXTERNAL CABLE TYPE 4:



Drawn by	Remarks	Replacement for	Date
HO/ma			
Approved	CARD 1145	Replaced by	Date
Date 4.6.81			

NORSK DATA A.S	Title BMPM CONN. ND-100 EXT. CABLE ERROR LOG	Drawing No. 3 - 9522

WIRE NO.	SIGNAL	POLARITY	ND 100 PLUG PANEL 2x37P PIN NO	EXT. PLUG PANEL ON DUAL BMPM PIN NO	DEVICE PLUG PIN NO		
01	B 15 L		1	1			
02	B 15 L		20	2			
03	B 14 L		2	3			
04	B 14 L		21	4			
05	B 13 L		3	5			
06	B 13 L		22	6			
07	B 12 L		4	7			
08	B 12 L		23	8			
09	B 11 L		5	9			
10	B 11 L		24	10			
11	B 10 L		6	11			
12	B 10 L		25	12			
13	B 9 L		7	13			
14	B 9 L		26	14			
15	B 8 L		8	15			
16	B 8 L		27	16			
17	B 7 L		9	17			
18	B 7 L		28	18			
19	B 6 L		10	19			
20	B 6 L		29	20			
21	B 5 L		11	21			
22	B 5 L		30	22			
23	B 4 L		12	23			
24	B 4 L		31	24			
25	B 3 L		13	25			
26	B 3 L		32	26			
27	B 2 L		14	27			
28	B 2 L		33	28			
29	B 1 L		15	29			
30	B 1 L		34	30			
31	B 0 L		16	31			
32	B 0 L		35	32			
33	LINTL		17	33			
34	LINTL		36	34			
35	LDRYL		18	35			
36	LDRYL		37	36			
37	ACTL		1	37			
38	ACTL		20	38			
39	LIOXL		2	39			
40	LIOXL		21	40			
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							
55							
56							
57							
58							
59							
60							
61							
62							
63							
64							

2x37P ANSLEY 609 - 37P

50 PIN PLUG (ANSLEY 609 - 5001

INTERNAL CABLE TYPE:
EXTERNAL CABLE TYPE 1: 40 WIRE FLAT CABLE
EXTERNAL CABLE TYPE 2:
EXTERNAL CABLE TYPE 3:
EXTERNAL CABLE TYPE 4:

Drawn by HO/ma	Remarks	Replacement for	Date
Approved			
Date 5.6.81		Replaced by	Date

NORSK DATA A.S Oslo, Norway	Title ND - 100 ERROR LOG CARD 1146 USED ON CARD 3009	Drawing no. 4 - 9458

NO.	SIGNAL	POLARITY	PLUG BERG	EUROPLUG NORD-100	PLUG PANEL 2x37 pin plug connection		
1	B 15 L	0	BERG 95	a20	1		
	B 15 L	1	BERG 94	c20	20		
2	B 14 L	0	BERG 93	a19	2		
	B 14 L	1	BERG 92	c19	21		
3	B 13 L	0	BERG 91	a18	3		
	B 13 L	1	BERG 90	c18	22		
4	B 12 L	0	BERG 89	a17	4		
	B 12 L	1	BERG 88	c17	23		
5	B 11 L	0	BERG 87	a16	5		
	B 11 L	1	BERG 86	c16	24		
6	B 10 L	0	BERG 85	a15	6		
	B 10 L	1	BERG 84	c15	25		
7	B 9 L	0	BERG 83	a14	7		
	B 9 L	1	BERG 82	c14	26		
8	B 8 L	0	BERG 81	a13	8		
	B 8 L	1	BERG 80	c13	27		
9	B 7 L	0	BERG 79	a12	9		
	B 7 L	1	BERG 78	c12	28		
10	B 6 L	0	BERG 77	a11	10		
	B 6 L	1	BERG 76	c11	29		
11	B 5 L	0	BERG 75	a10	11		
	B 5 L	1	BBRG 74	c10	30		
12	B 4 L	0	BERG 73	a 9	12		
	B 4 L	1	BERG 72	c 9	31		
13	B 3 L	0	BERG 71	a 8	13		
	B 3 L	1	BERG 70	c 8	32		
14	B 2 L	0	BERG 69	a 7	14		
	B 2 L	1	BERG 68	c 7	33		
15	B 1 L	0	BERG 67	a 6	15		
	B 1 L	1	BERG 66	c 6	34		
16	B 0 L	0	BERG 65	a 5	16		
	B 0 L	1	BERG 64	c 5	35		
17	LINTL	0	BERG 63	a 4	17		
	LINTL	1	BERG 62	c 4	36		
18	LDRYL	0	BERG 61	a 3	18		
	LDRYL	1	BERG 60	c 3	37		
19	ACTL	0	BERG 59	a 2	1		
	ACTL	1	BERG 58	c 2	20		
20	LIOXL	0	BERG 57	a 1	2		
	LIOXL	1	BERG 56	c 1	21		
21		0	BERG 55		3		
		1	BERG 54		22		

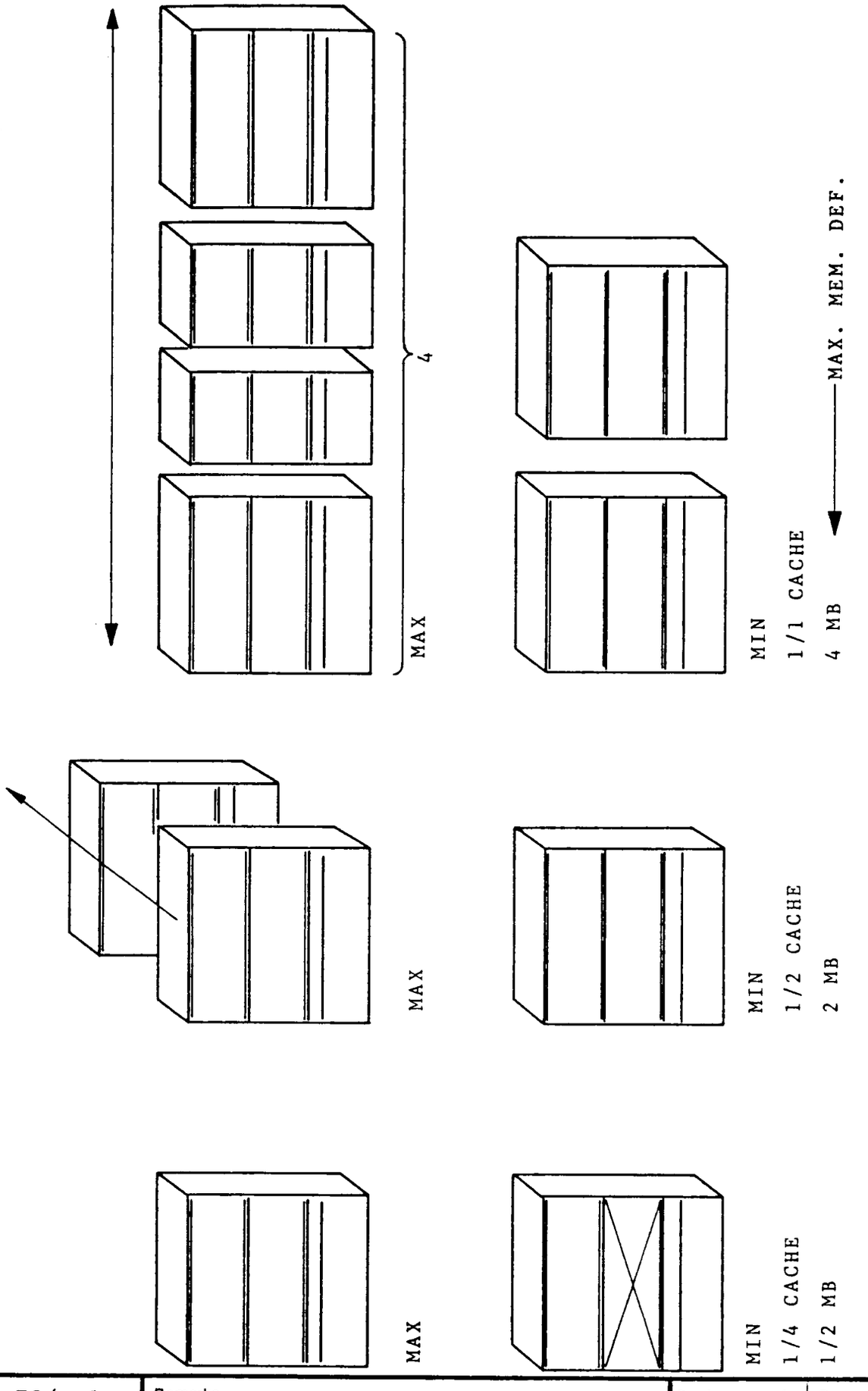
DRAWN BY HO/ma	Remarks	Replacement for	Date
APPROVED BY		Replaced by	Date
DATE 5.6.81			

MEMORY & CACHE SIZE

COMBINATIONS ND-100 - ND-500

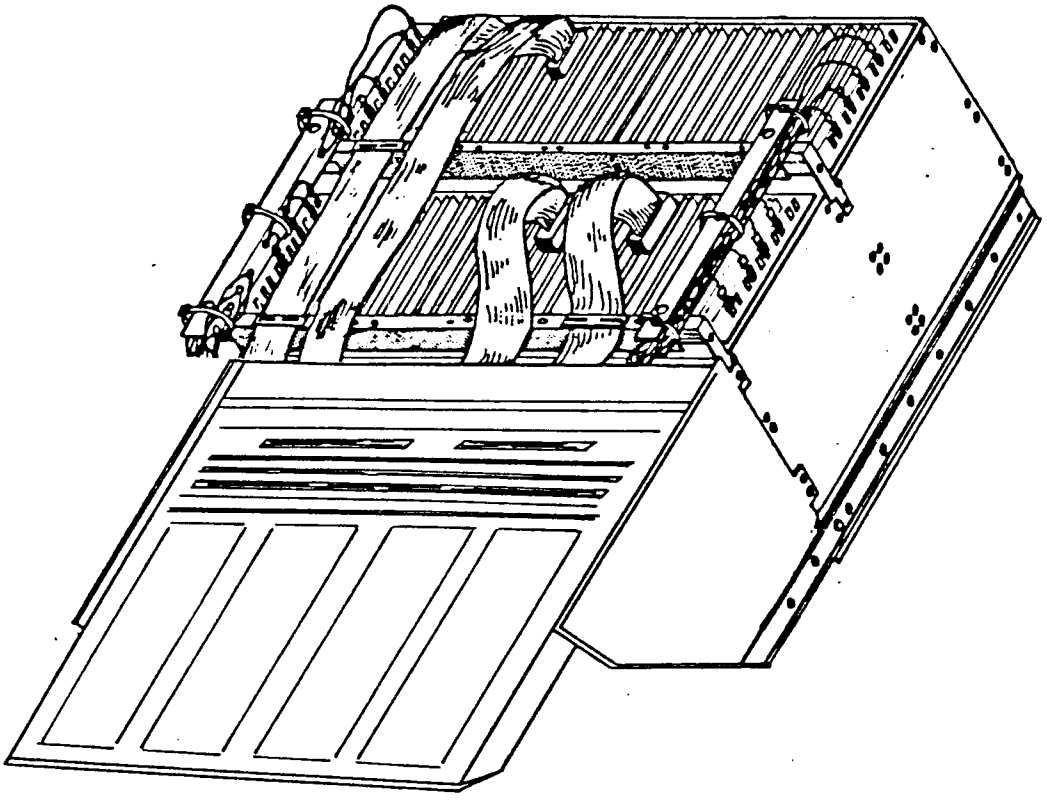
DEFINED CONFIGURATIONS					MPM CRATE SIZE	MAX-MIN MPM SIZE	INTERLEAVE	
MPM OTHER	MPM ND CAB	MPM ND-100	MPM ND-500	CACHE SIZE			BANK	BANK
LOCAL	-	-	YES	32 KB 1/4	SINGLE	MIN 128 KB MAX 512 KB	OK	
LOCAL	-	-	YES	32 KB 1/4	DOUBLE	MIN 128 KB MAX 1 MB		OK
LOCAL	-	-	YES	64 KB 1/2	DOUBLE	MIN 256 KB MAX 1 MB	OK	
LOCAL	-	YES	YES	64 KB 1/2	DOUBLE	MIN 256 KB MAX 2 MB		OK
LOCAL	-	YES	YES	128 KB 1/1	DOUBLE	MIN 512 KB MAX 2 MB	OK	
LOCAL	YES	YES	YES	128 KB 1/1	DOUBLE	MIN 1 MB MAX 4 MB		OK

NORSK DATA A.S Oslo, Norway	Title BMPM CONFIGURATION	Drawing no.



DRAWN BY TS/eml	Remarks	Replacement for	Date
APPROVED BY		Replaced by	Date
DATE 26/05/81			

NORSK DATA A.S Oslo, Norway	Title DUAL BMPM LAYOUT	Drawing no.



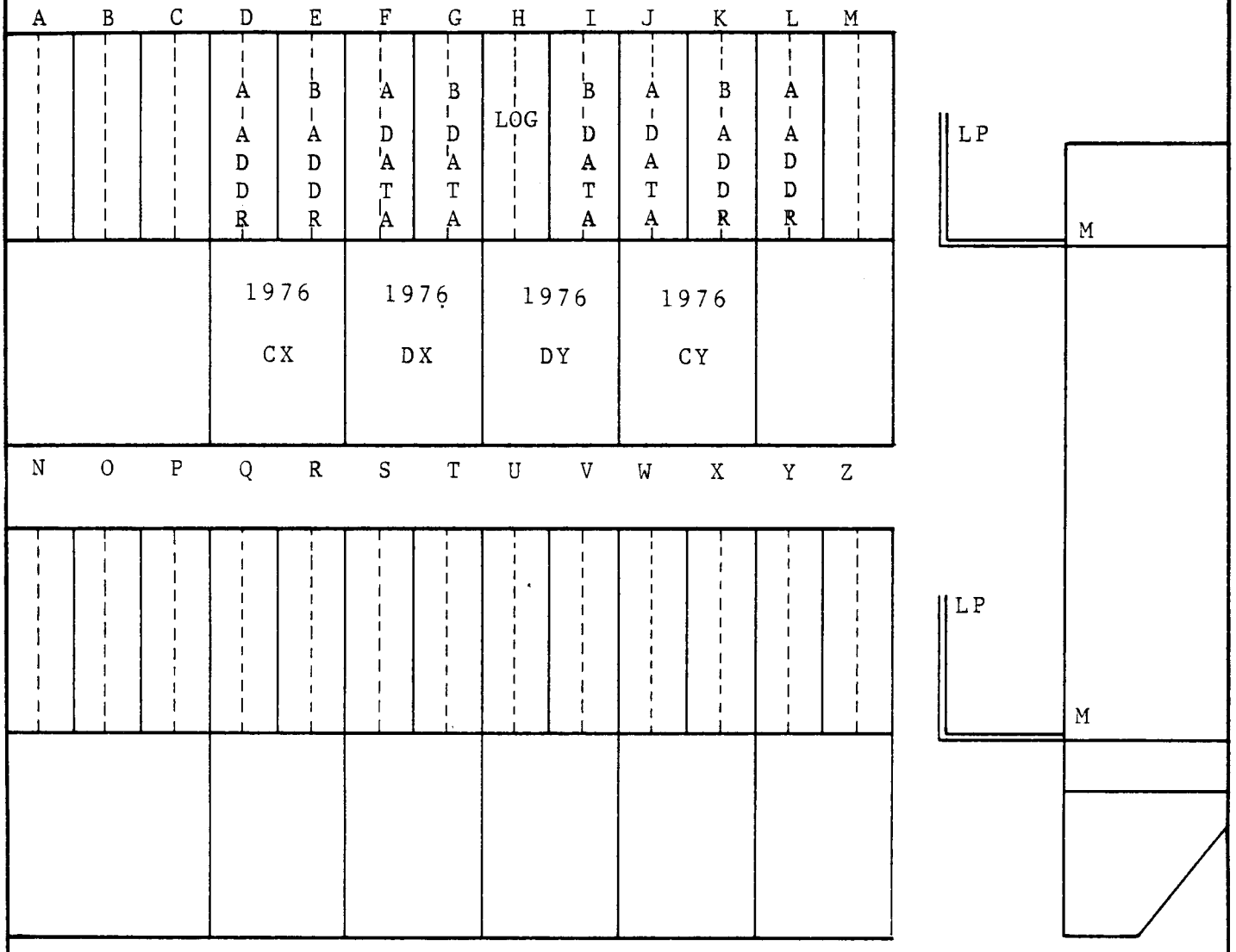
POWER DISTR.

PLUG PANEL

A	B	C	D
	L.LEAVE 8W	IADD IN	DADD IN
	4W	IADD OUT	DADD OUT
	2W	IDATA 0	DDATA 0
	0W	IDATA 1	DDATA 1
	N100ADD IN	IDATA 2	DDATA 2
	N100A OUT	IDATA 3	DDATA 3
	N100D IN		
	N100D OUT		
	ERR LOG IN		
	ERR LOG OUT		

DRAWN BY	Remarks	Replacement for	Date
APPROVED BY			
DATE		Replaced by	Date

NORSK DATA A.S Oslo, Norway	Title DUAL BMPM INTERNAL WIRING	Drawing no.



Internal wiring from BMPM card rack M to local plug panel LP.
Same wiring beeween each rack M and panel LP.

M10 - LP:D	M12 - LP:R
M11 - LP:E	M13 - LP:T
M14 - LP:F	M16 - LP:Q
M15 - LP:G	M17 - LP:S
M18 - LP:H	M20 - LP:U
M22 - LP:I	M21 - LP:W
M23 - LP:J	M24 - LP:V
M26 - LP:K	M25 - LP:X
M27 - LP:L	

DRAWN BY TS/eml	Remarks	Replacement for Date
APPROVED BY		Replaced by Date
DATE 22/05/81		

NORSK DATA A.S Oslo, Norway	Title DUAL BMPM WIRING LOCAL PANELS TO EXTERNAL PANELS	Drawing no.

Local plug panel LP

A	B	C	D	E	F	G	H	I	J	K	L	M
			A ADDR	B ADDR	A DATA	B DATA	LOG	B DATA	A DATA	B ADDR	A ADDR	
			1976 CX		1976 DX		1976 DY		1976 DX			

N	O	P	Q	R	S	T	U	V	W	X	Y	Z

LOG

	Ext.cable
EP:B2 -	LOG
EP:B2 -	LP1:G1
LP1:G2-	LP2:G2
LP2:G1-	EP:B1

Port A, allocated for DMA, is not wired.

PORT B:

		Ext.cable
	EP:B6	B-ADDR
EP:B7/10-	LP1:D1	
LP1:D2 -	LP2:D2	
LP2:D1 -	LP2:J2	
LP2:J1 -	LP1:J1	
LP1:J2 -	EP:B5	
EP:B4 -	LP1:F1	B-DATA
LP1:F2 -	LP2:F2	
LP2:F1 -	LP2:H2	
LP2:H1 -	LP1:H1	
LP1:H2 -	EP:B3	

PORT C:

		Ext.cable
	EP:C10	C-ADDR
EP:C10 -	LP1:X1	
LP1:X2 -	LP2:X1	
LP2:X2 -	LP2:R1	
LP2:R2 -	LP1:R1	
LP1:R1 -	EP:C9	
EP:C8 -	LP1:Q1	C-DATA0
LP1:Q2 -	T	
EP:C7 -	LP1:W1	C-DATA1
LP1:W2 -	T	
EP:C6 -	LP2:Q1	C-DATA2
LP2:Q2 -	T	
EP:C5 -	LP2:W1	C-DATA3
LP2:W2 -	T	

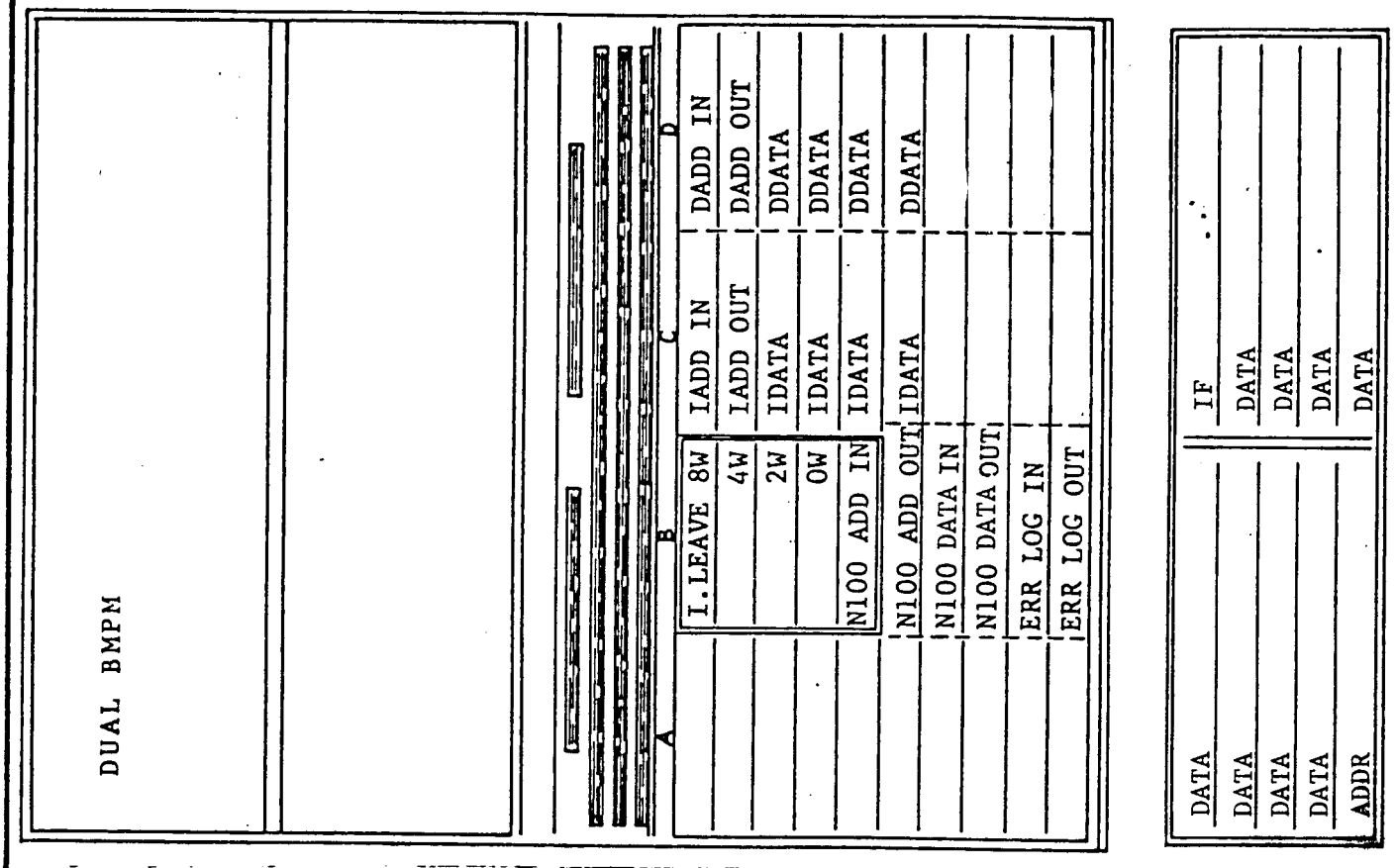
PORT D:

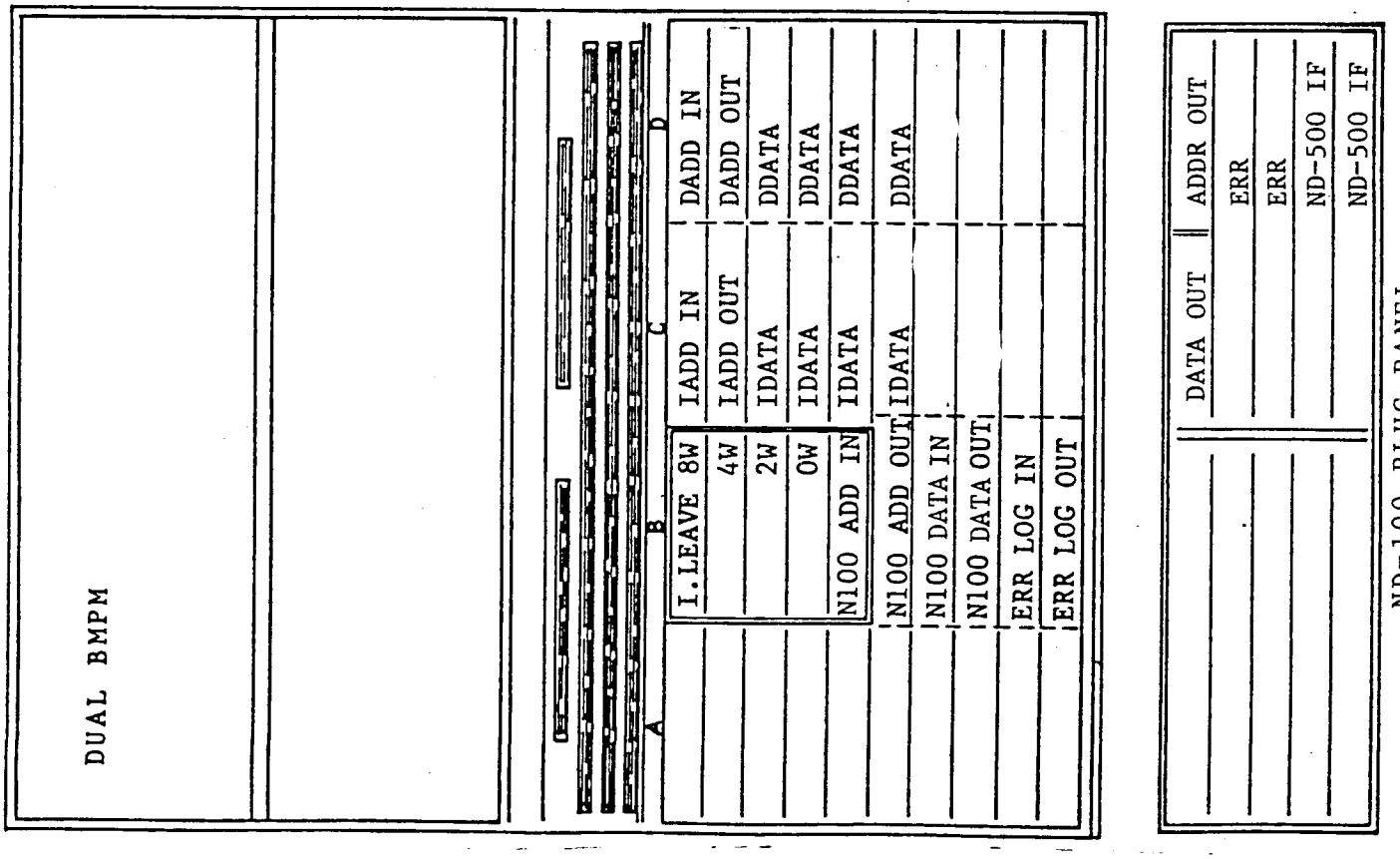
		Ext.cable
	EP:D10	D-ADDR
EP:D10 -	LP1:V1	
LP1:V2 -	LP2:V1	
LP2:V2 -	LP2:T1	
LP2:T2 -	LP1:T1	
LP1:T2 -	EP:D9	
EP:D8 -	LP1:S1	D-DATA0
LP1:S2 -	T	
EP:D7 -	LP1:U1	D-DATA1
LP1:U2 -	T	
EP:D6 -	LP2:S1	D-DATA2
LP2:S2 -	T	
EP:D5 -	LP2:U1	D-DATA3
LP2:U2 -	T	

A	B	C	D	
	I.LEAVE 8W	IADD IN	DADD IN	10
	I.LEAVE 4W	IADD OUT	DADD OUT	9
	I.LEAVE 2W	IDATA 0	DDATA 0	8
	I.LEAVE 0W	IDATA 1	DDATA 1	7
	N100 ADD IN	IDATA 2	DDATA 2	6
	N100 ADD OUT	IDATA 3	DDATA 3	5
	N100 DATA IN			4
	N100 DATA OUT			3
	ERR.LOG IN			2
	ERR.LOG OUT			1

DRAWN BY TS/eml	Remarks	Replacement for	Date
APPROVED BY			
DATE 25/05/81		Replaced by	Date

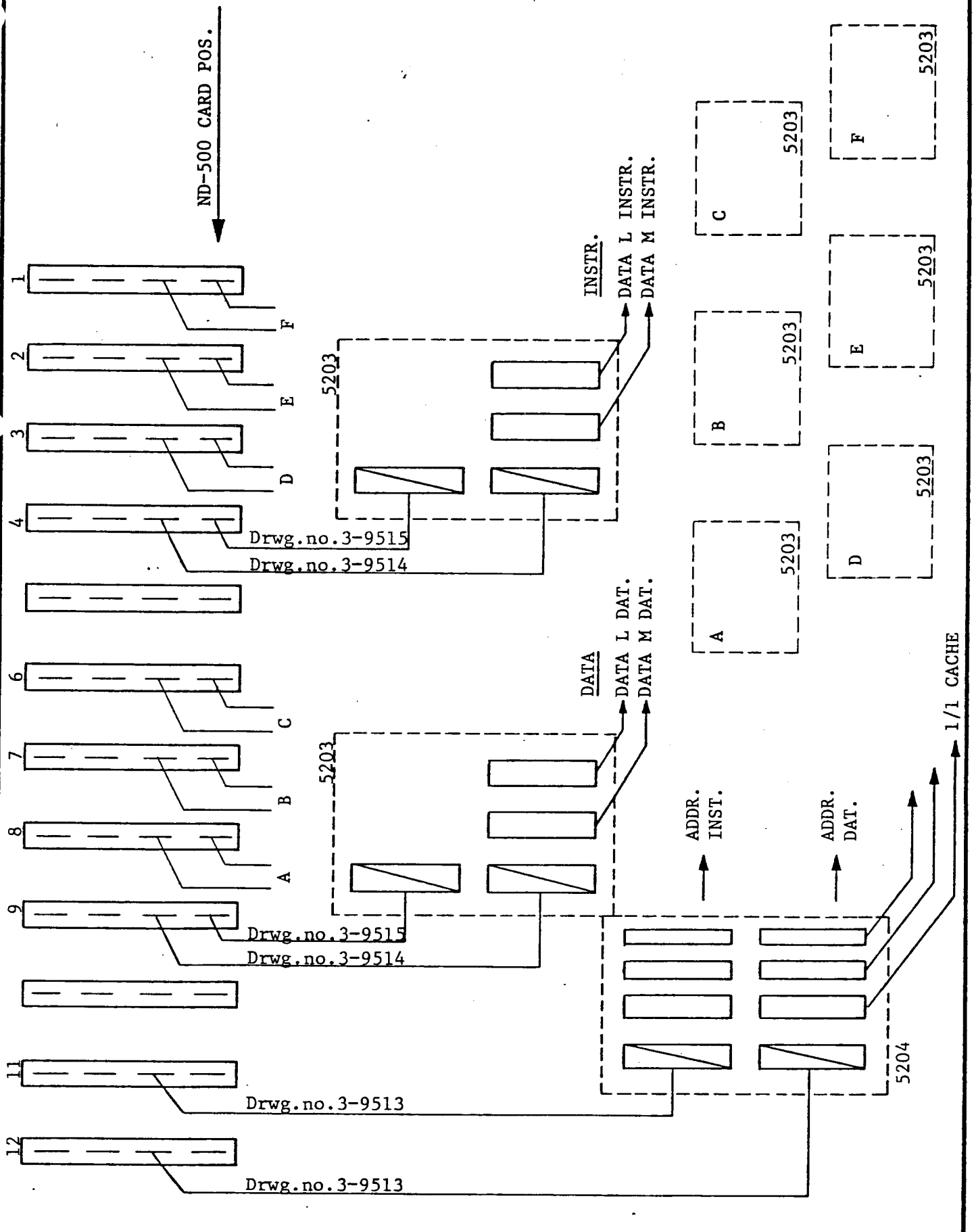
NORSK DATA A.S Oslo, Norway	Title ND-100 ND-500 BMPM INTERCONNECTION 1/1 CACHE	Drawing no.





DRAWN BY TS/eml	Remarks	Replacement for	Date
APPROVED BY			
DATE 26/05/81		Replaced by	Date

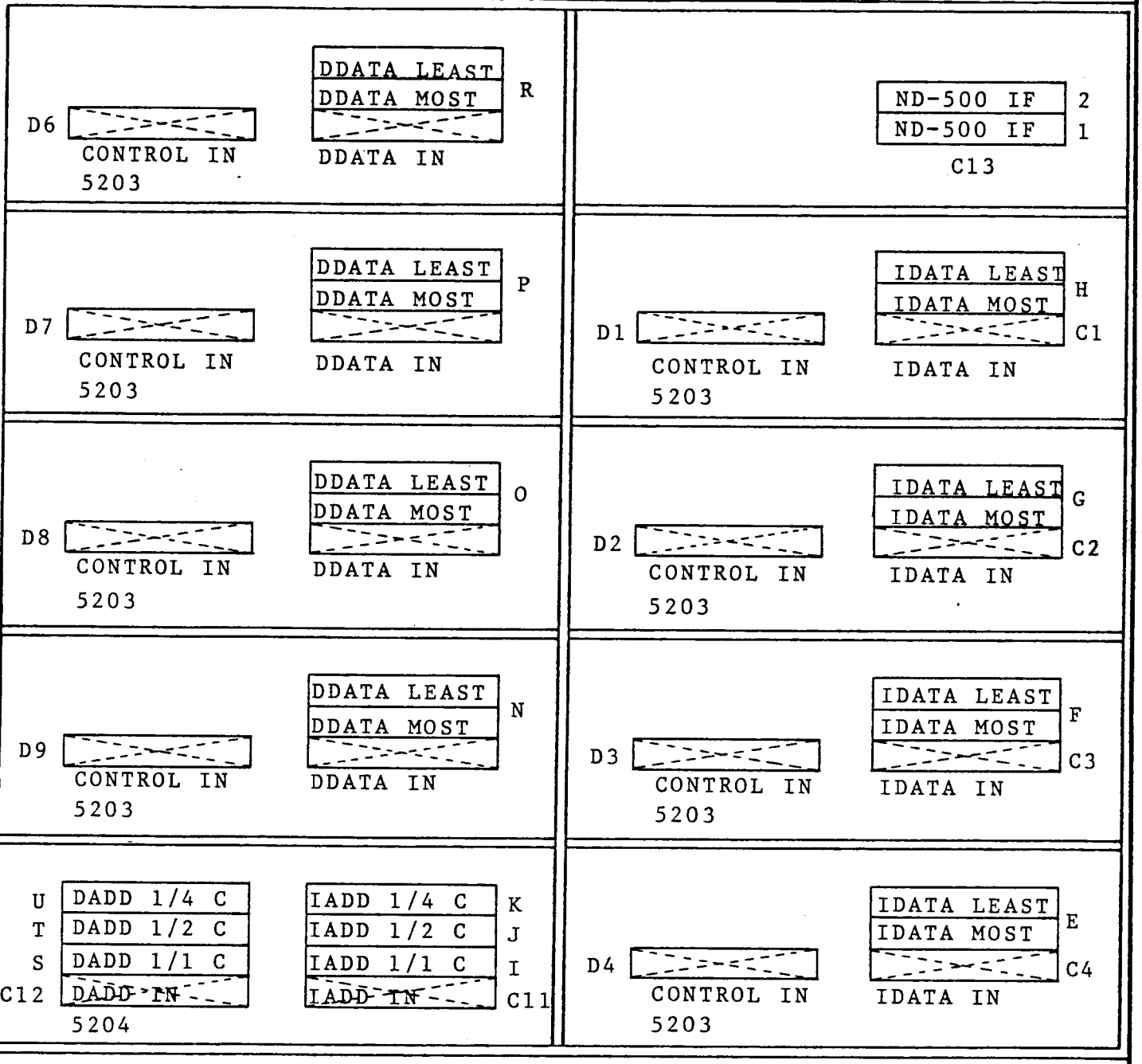
NORSK DATA A.S Oslo, Norway	Title ND-500 MEMORY CONNECTION 1/1 CACHE	Drawing no.



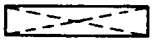
DRAWN BY TS/eml	Remarks	Replacement for	Date
APPROVED BY		Replaced by	Date
DATE 27/05/81			

NORSK DATA A.S Oslo, Norway	Title ND-500 PLUG PANEL 1/1 CACHE	Drawing no.

Plug panel as it will be viewed from the back side of the ND-500 cabinet.



All plugs mounted on PCB 5203 and 5204 are flat cable type, 2x32 pins.

Plugs marked  are mounted on the rear side of the print and connected to ND-500 backwiring, the other from the front and connected to BMPM plug panels.

DRAWN BY TS/eml	Remarks	Replacement for	Date
APPROVED BY			
DATE 25/05/81		Replaced by	Date

G.P. SELECT CUSTOMER CONFIGURATION BY X IN WINDOW

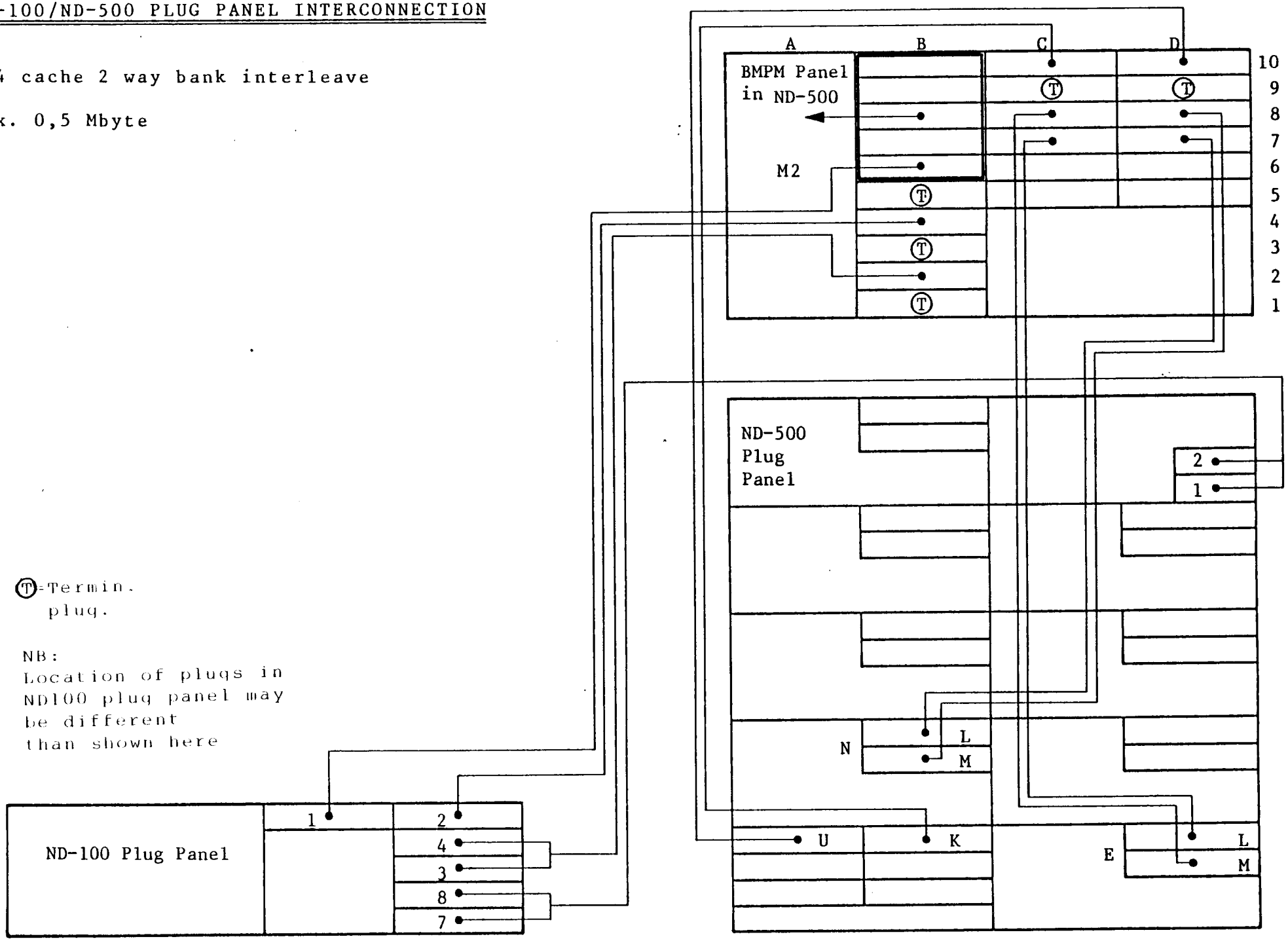
RIBBON CABLE CONFIGURATION LIST. PRINT NO. 5203

1/1 CACHE 1 + 2 + 1			1/1 CACHE 1 + 1			1/2 CACHE 1 + 1			1/2 CACHE 1			1/4 CACHE 1			1/4 CACHE 1/2			① CACHE DATA/INSTR. ② CACHE ADDR. ③ B-PORT MPM ND-100	CACHE MODULE #	MPM CODING	CACHE ADDR.	MPM B-PORT ND-100
M2.C08	8W	RACK INTERLEAVED	M2.C08	8W	BANK INTERLEAVED	M2.C08	4W	RACK INTERLEAVED	M2.C08	4W	BANK INTERLEAVED	M2.C08	2W	RACK INTERLEAVED	M2.C08	2W	BANK INTERLEAVED	EM - MOST INSTR. ①	# 1			
M2.C06			M2.C07			M2.C06			M2.C07			M2.C06			M2.C07			EL - LEAST INSTR.				
M2.D08			M2.D08			M2.D08			M2.D08			M2.D08			M2.D08			NM - MOST DATA				
M2.D06			M2.D07			M2.D06			M2.D07			M2.D06			M2.D07			NL - LEAST DATA				
M4.C08	0W		M2.C06	0W		M4.C08	0W		M2.C06									FM - MOST INSTR.	# 2			
M4.C06			M2.C05			M4.C06			M2.C05									FL - LEAST INSTR.				
M4.D08			M2.D06			M4.D08			M2.D06									OM - MOST DATA				
M4.D06			M2.D05			M4.D06			M2.D05									OL - LEAST DATA				
M6.C08	0W		M4.C08	0W														GM - MOST INSTR.	# 3			
M6.C06			M4.C07															GL - LEAST INSTR.				
M6.D08			M4.D08															PM - MOST DATA				
M6.D06			M4.D07															PL - LEAST DATA				
M8.C08	0W		M4.C06	0W														HM - MOST INSTR.	# 4			
M8.C06			M4.C05															HL - LEAST INSTR.				
M8.D08			M4.D06															RM - MOST DATA				
M8.D06			M4.D05															RL - LEAST DATA				
M2): ND-500 M4): MPM CAB M6): MPM CAB M8): ND-100			M2): ND-500 M4): ND-100			M2): ND-500 M4): ND-100			M2): ND-500			M2): ND-500			M2): ND-500				MULTIPORT ASSY CODING			
M2.C09 - M4.C10 M2.C10 - I M2.D09 - M4.D10 M2.D10 - S M4.C09 - M6.C10 M4.D09 - M6.D10 M6.C09 - M8.C10 M6.D09 - M8.D10 M8.C09 - Ⓣ M8.D09 - Ⓣ			M2.C05 - M4.C10 M2.C10 - I M2.D09 - M4.D10 M2.D10 - S M4.C09 - Ⓣ M4.D09 - Ⓣ			M2.C09 - M4.C10 M2.C10 - J M2.D09 - M4.D10 M2.D10 - T M4.C09 - Ⓣ M4.D09 - Ⓣ			M2.C09 - Ⓣ M2.C10 - J M2.D09 - Ⓣ M2.D10 - T			M2.C09 - Ⓣ M2.C10 - K M2.D09 - Ⓣ M2.D10 - U			M2.C09 - Ⓣ M2.C10 - K M2.D09 - Ⓣ M2.D10 - U			K - IADDR. 1/4 ② U - DADDR 1/4 J - IADDR 1/2 T - DADDR 1/2 I - IADDR 1/1 S - DADDR 1/1	DATA & INSTR. ADDRESS OUT PRINT 5204 ND-500 PANEL			
Same as 1/1 1+1 M4.B05-M6.B06 M6.B07-MPM CRATE M6.B05-M8.B06 M8.B05- Ⓣ M8.B07-MPM CRATE M4.B03-M6.B04 M6.B03-M8.B04 M8.B03- Ⓣ M4.B01-M6.B02 M6.B01-M8.B02 M8.B01- Ⓣ			M2.B10-MPM CRATE M2.B06-ND-100 ADDR M2.B05-M4.B06 M4.B07-MPM CRATE M4.B05- Ⓣ M2.B03-M4.B04 M4.B03- Ⓣ M2.B01-M4.B02 M4.B01- Ⓣ M2.B04-ND-100 DATA M2.B02-ND-100 LOG			M2.B09-MPM CRATE M2.B06-ND-100 ADDR M2.B05-M4.B06 M4.B07-MPM CRATE M4.B05- Ⓣ M2.B03-M4.B04 M4.B03- Ⓣ M2.B01-M4.B02 M4.B01- Ⓣ M2.B04-ND-100 DATA M2.B02-ND-100 LOG			M2.B09-MPM CRATE M2.B06-ND-100 ADDR M2.B05- Ⓣ M2.B04-ND-100 DATA M2.B03- Ⓣ M2.B02-ND-100 LOG M2.B01- Ⓣ			M2.B08-MPM CRATE M2.B06-ND-100 ADDR M2.B05- Ⓣ M2.B04-ND-100 DATA M2.B03- Ⓣ M2.B02-ND-100 LOG M2.B01- Ⓣ			M2.B08-MPM CRATE M2.B06-ND-100 ADDR M2.B05- Ⓣ M2.B04-ND-100 DATA M2.B03- Ⓣ M2.B02-ND-100 LOG M2.B01- Ⓣ			B10 - 8W ADDR ③ B09 - 4W ADDR B08 - 2W ADDR B07 - 0W ADDR B06 - ADDR IN B05 - ADDR OUT B04 - DATA IN B03 - DATA OUT B02 - LOG IN B01 - LOG OUT	B- PORT ND-100 MEMORY			

ND-100/ND-500 PLUG PANEL INTERCONNECTION

1/4 cache 2 way bank interleave

Max. 0,5 Mbyte



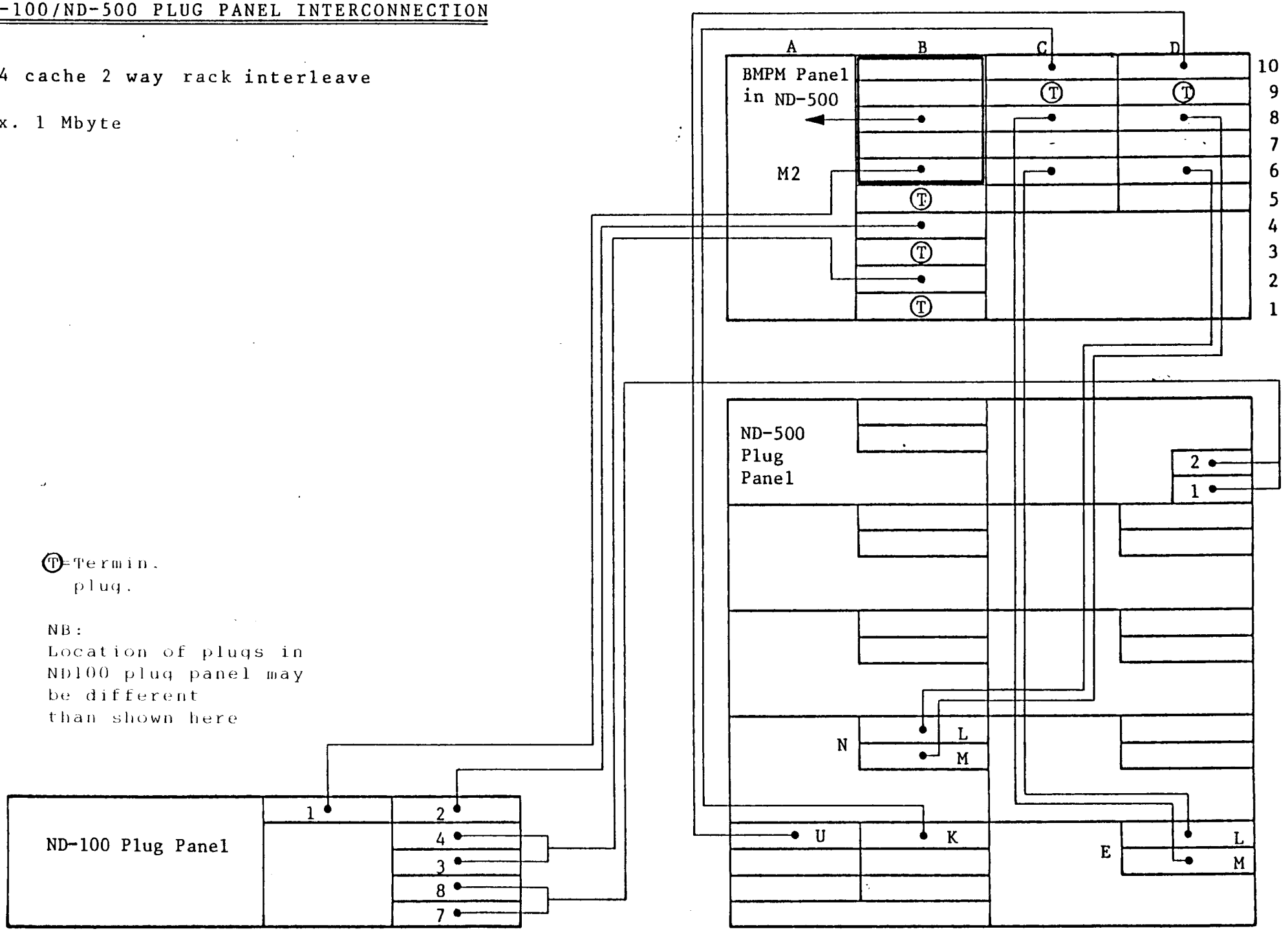
T=Termin.
plug.

NB:
Location of plugs in
ND100 plug panel may
be different
than shown here

ND-100/ND-500 PLUG PANEL INTERCONNECTION

1/4 cache 2 way rack interleave

Max. 1 Mbyte



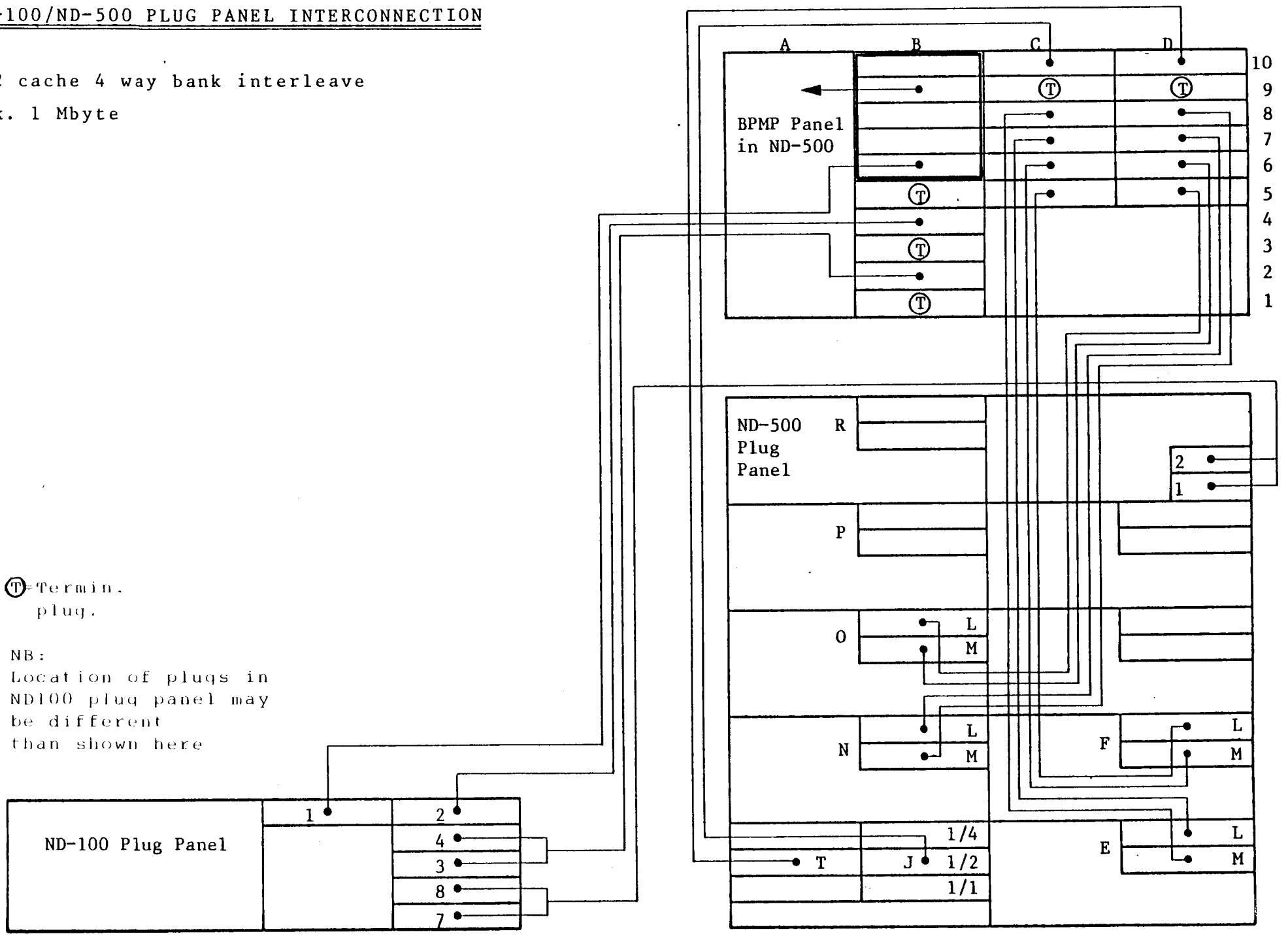
T=Termin.
plug.

NB:
Location of plugs in
ND100 plug panel may
be different
than shown here

ND-100/ND-500 PLUG PANEL INTERCONNECTION

1/2 cache 4 way bank interleave

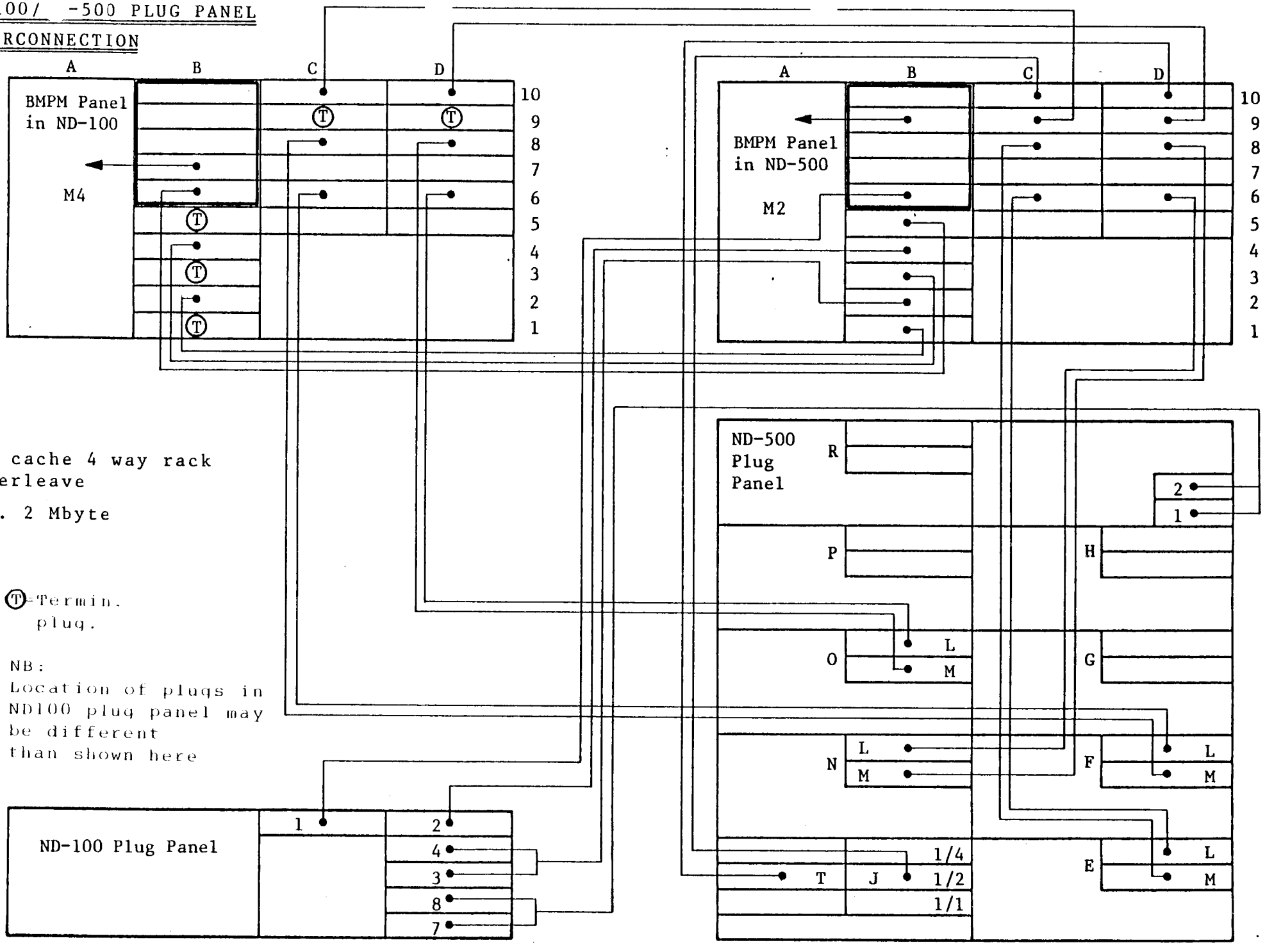
Max. 1 Mbyte



T=Termin.
plug.

NB:
Location of plugs in
ND100 plug panel may
be different
than shown here

ND-100/ -500 PLUG PANEL INTERCONNECTION



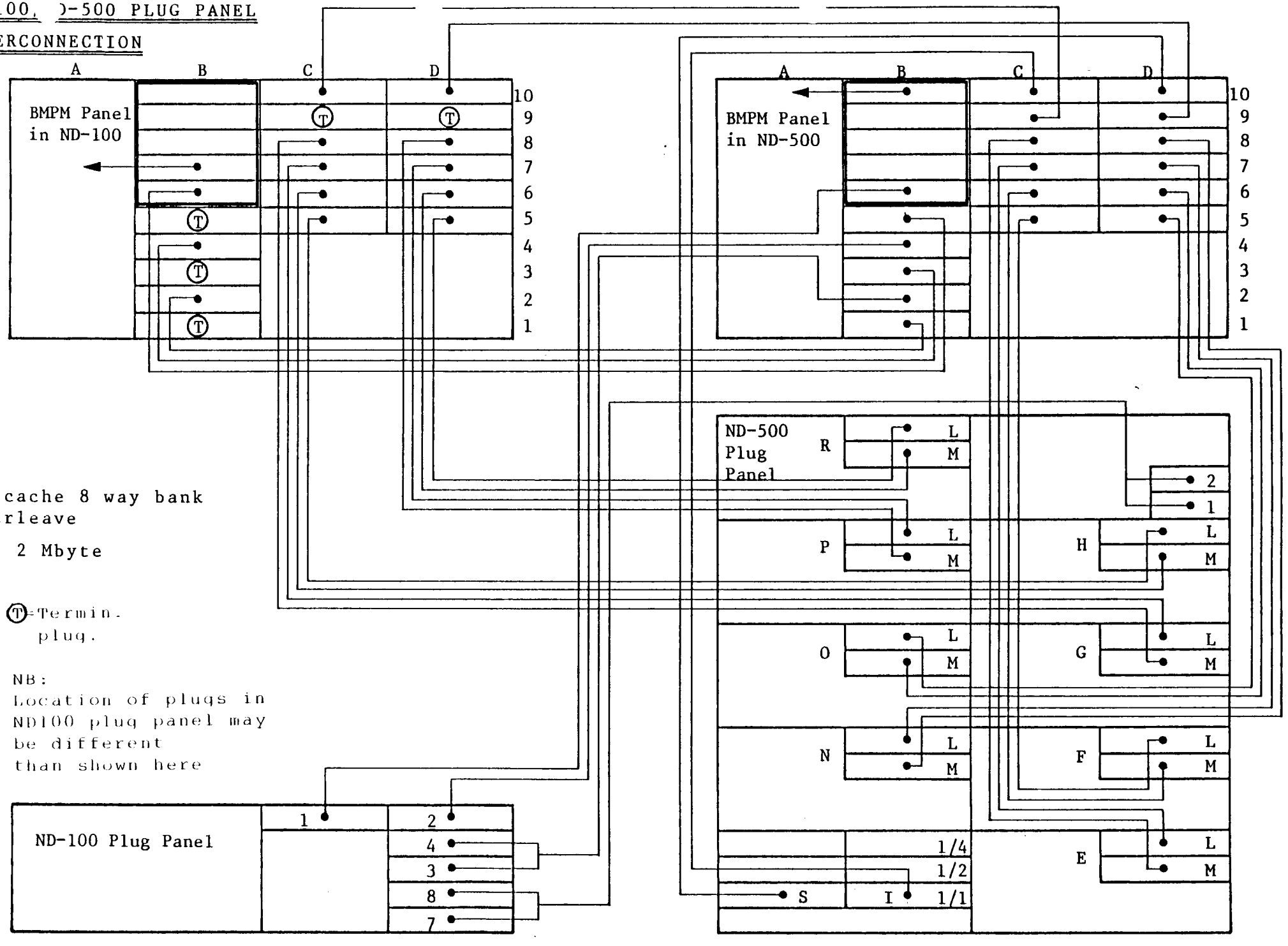
1/2 cache 4 way rack interleave

Max. 2 Mbyte

(T)=Termin. plug.

NB:
Location of plugs in ND100 plug panel may be different than shown here

ND-100, ND-500 PLUG PANEL INTERCONNECTION



1/1 cache 8 way bank interleave

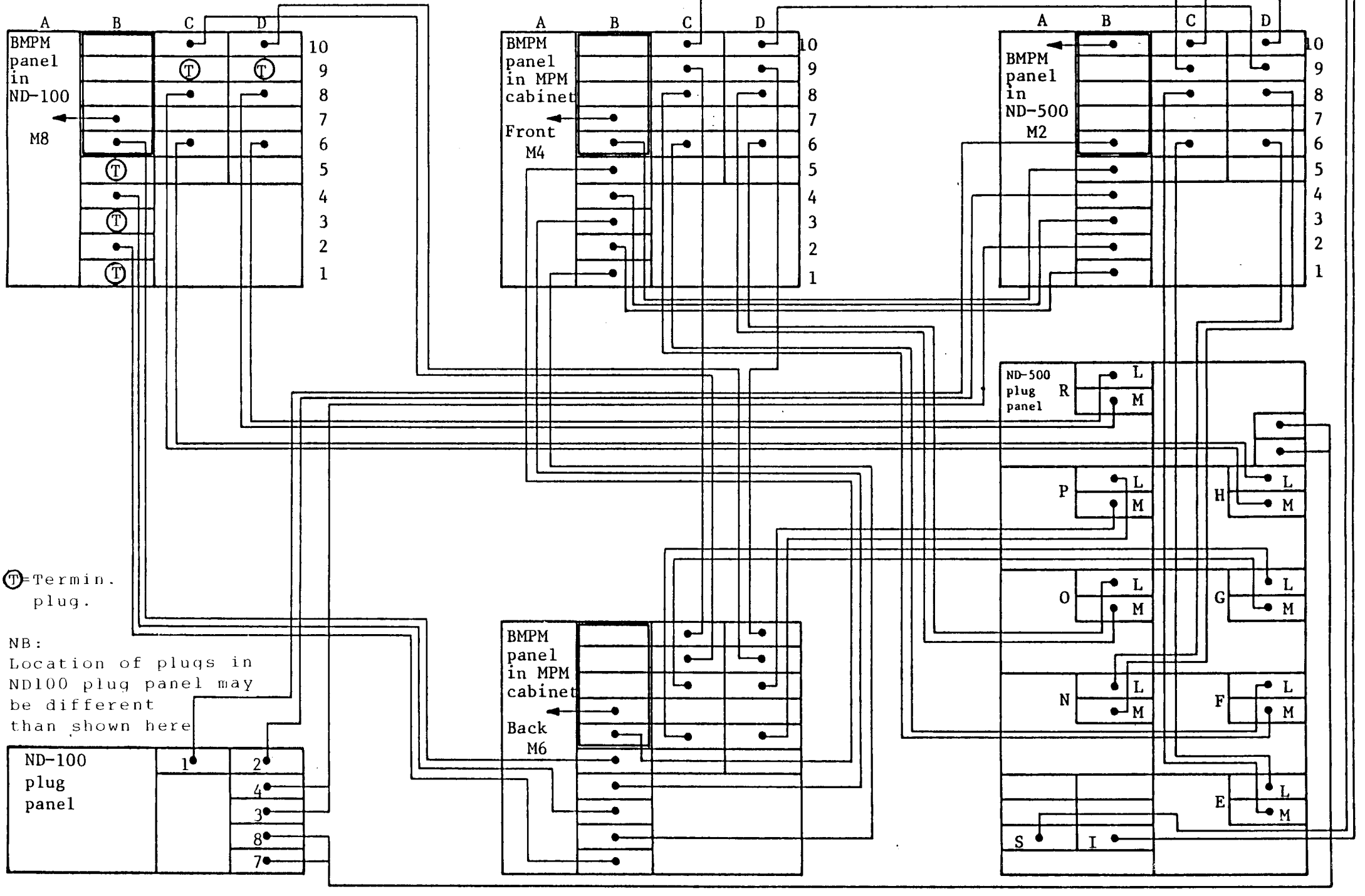
Max. 2 Mbyte

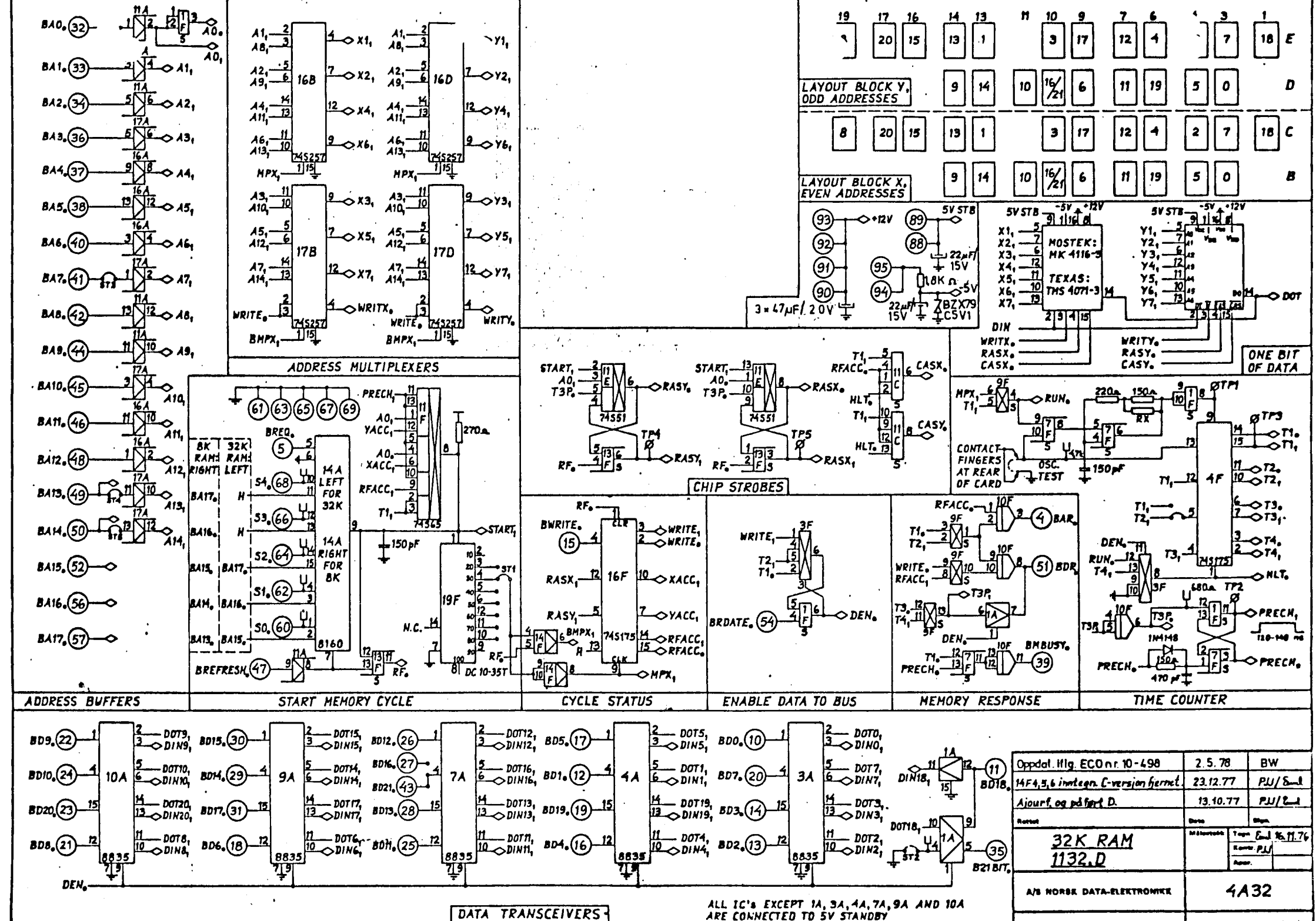
T=Termin. plug.

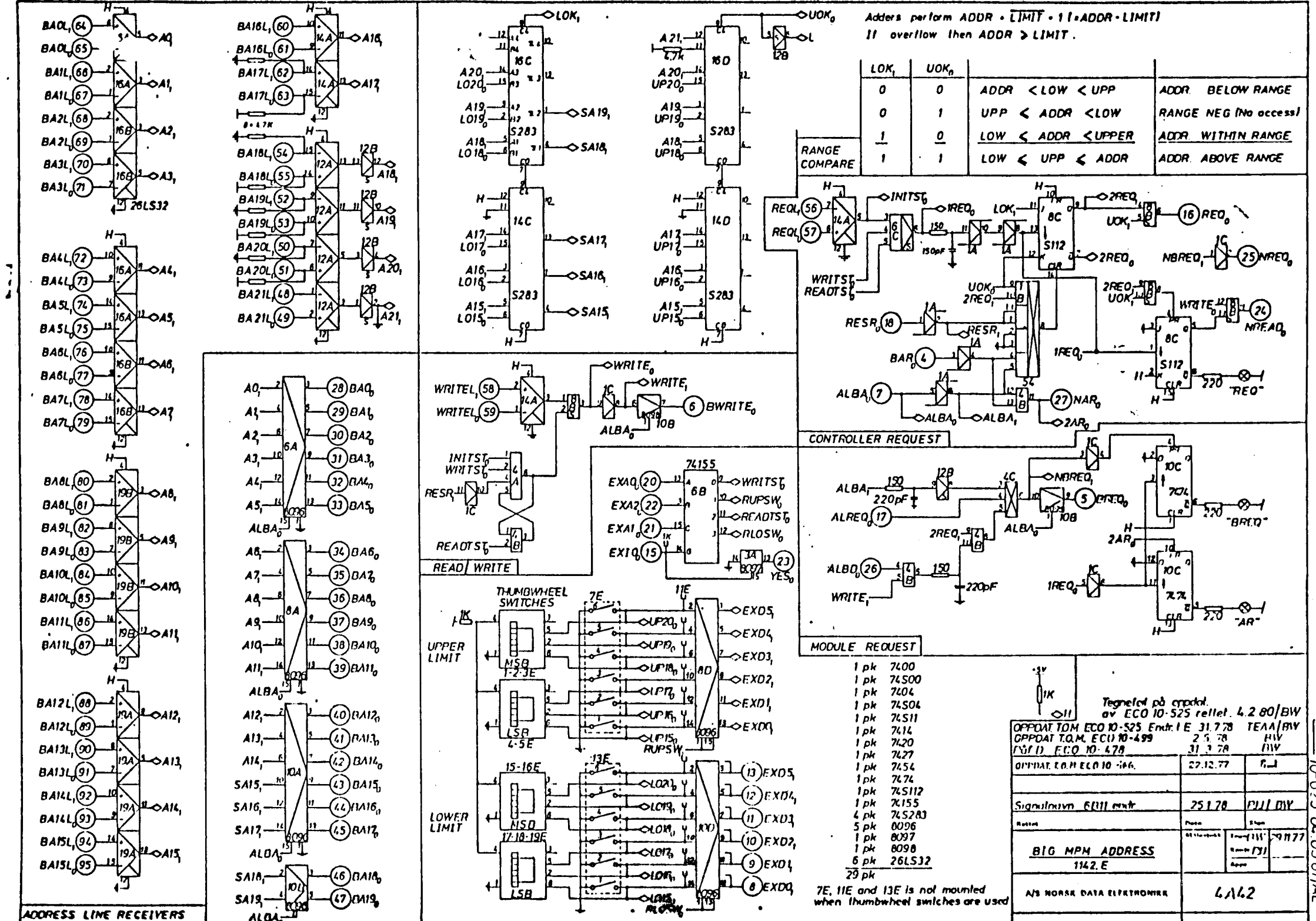
NB:
Location of plugs in ND100 plug panel may be different than shown here

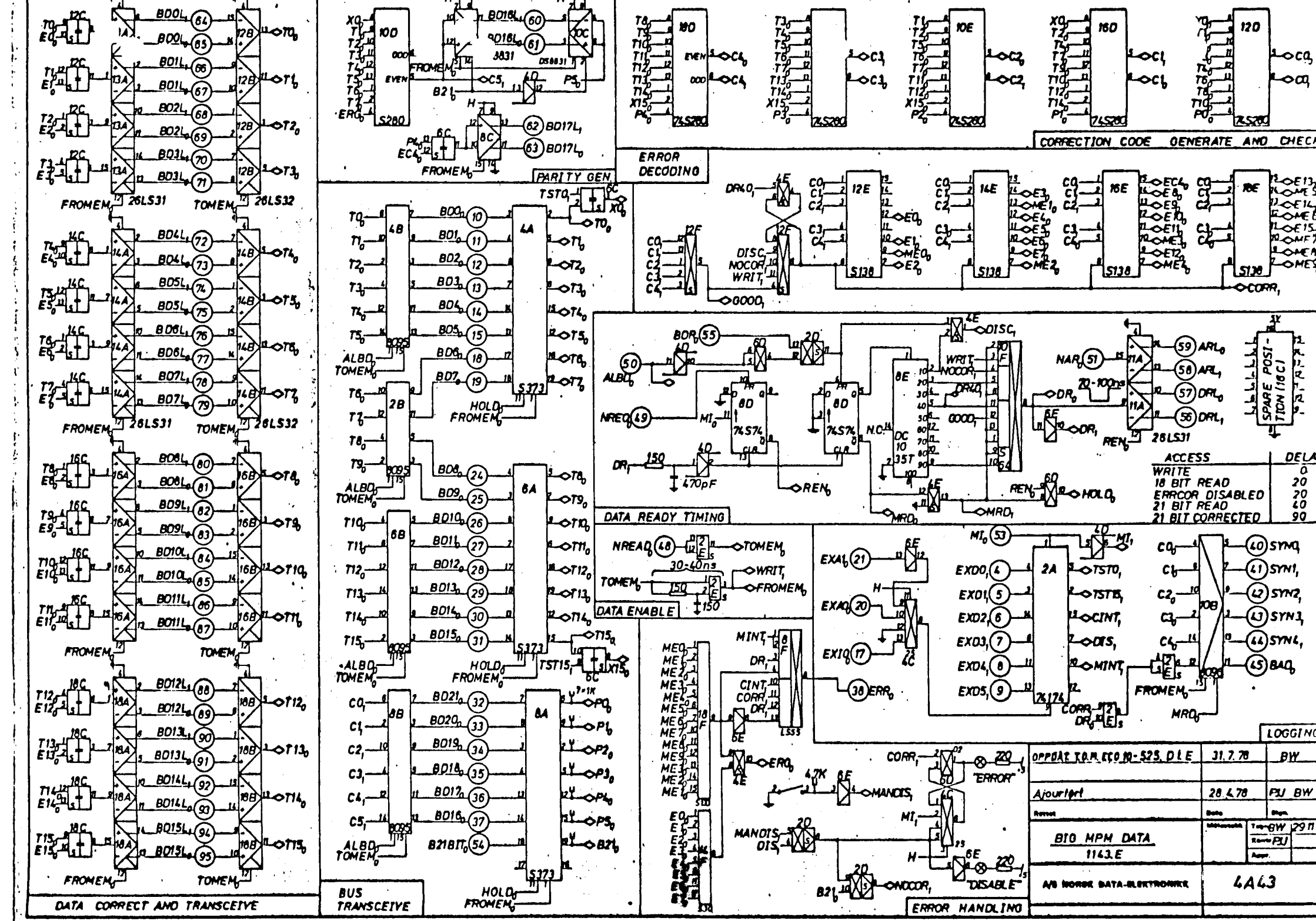
ND-100 ND-500 PLUG PANEL INTERCONNECTION

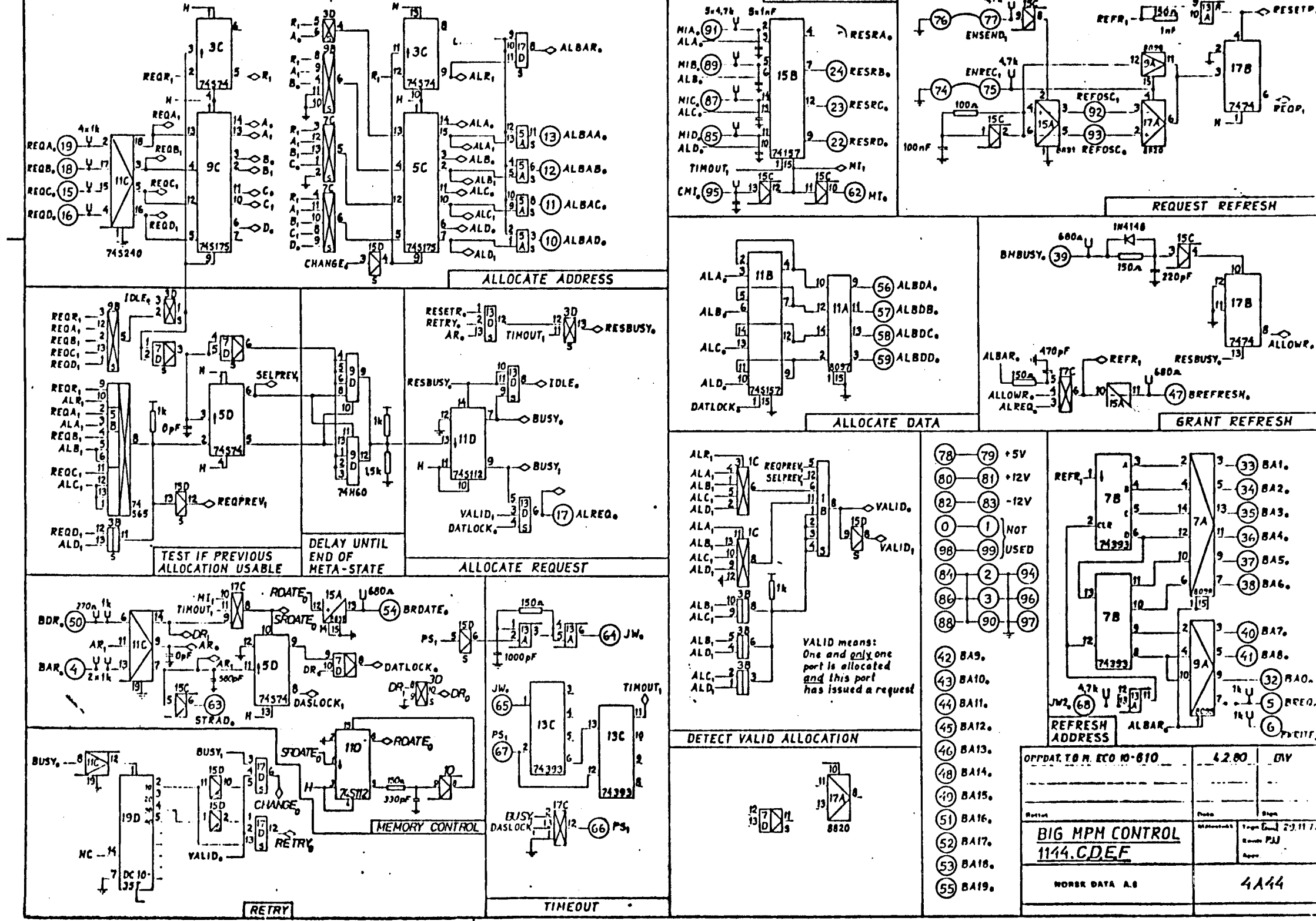
1/1 cache 8 w. rack interleave
Max. 4 Mbyte

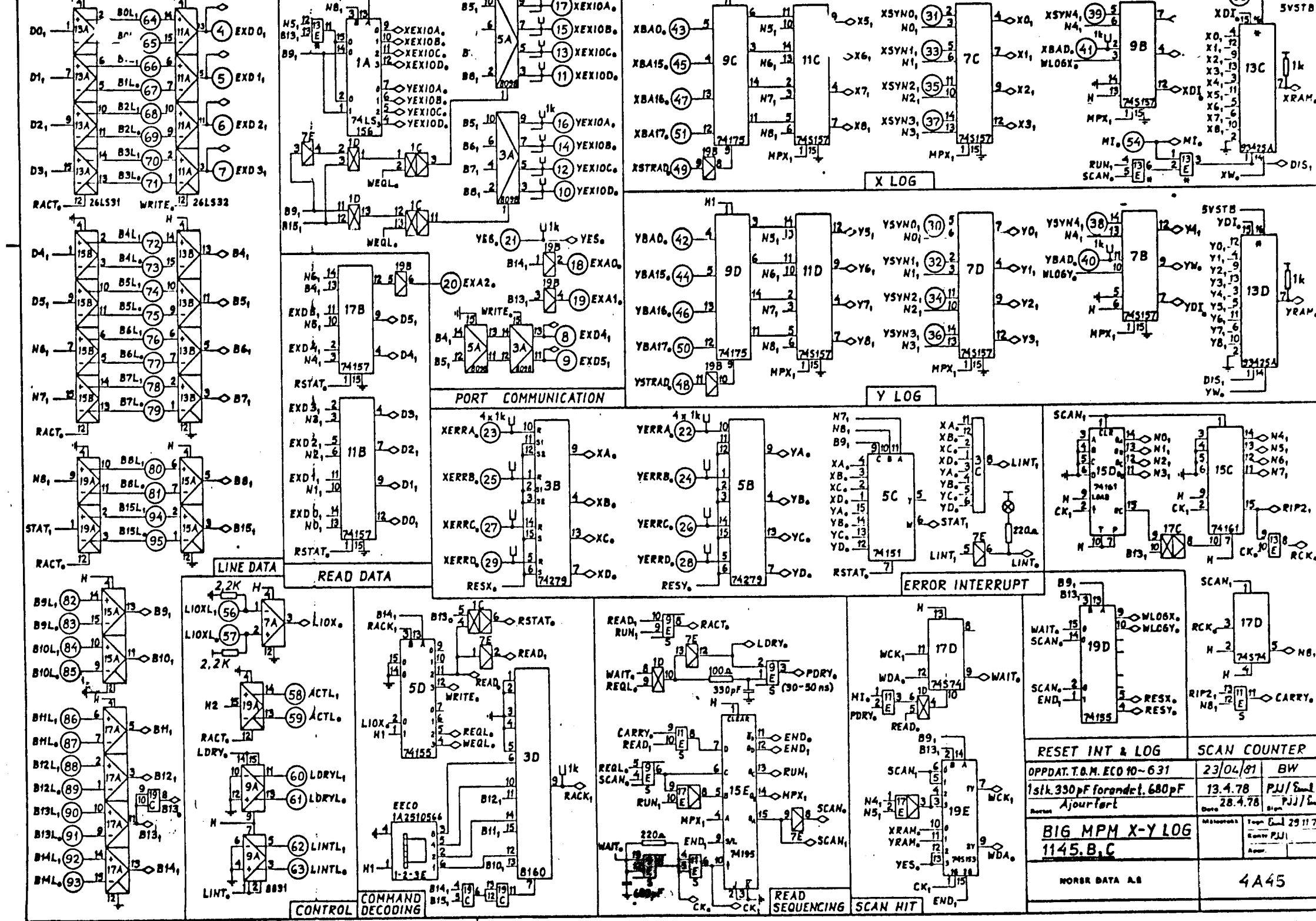


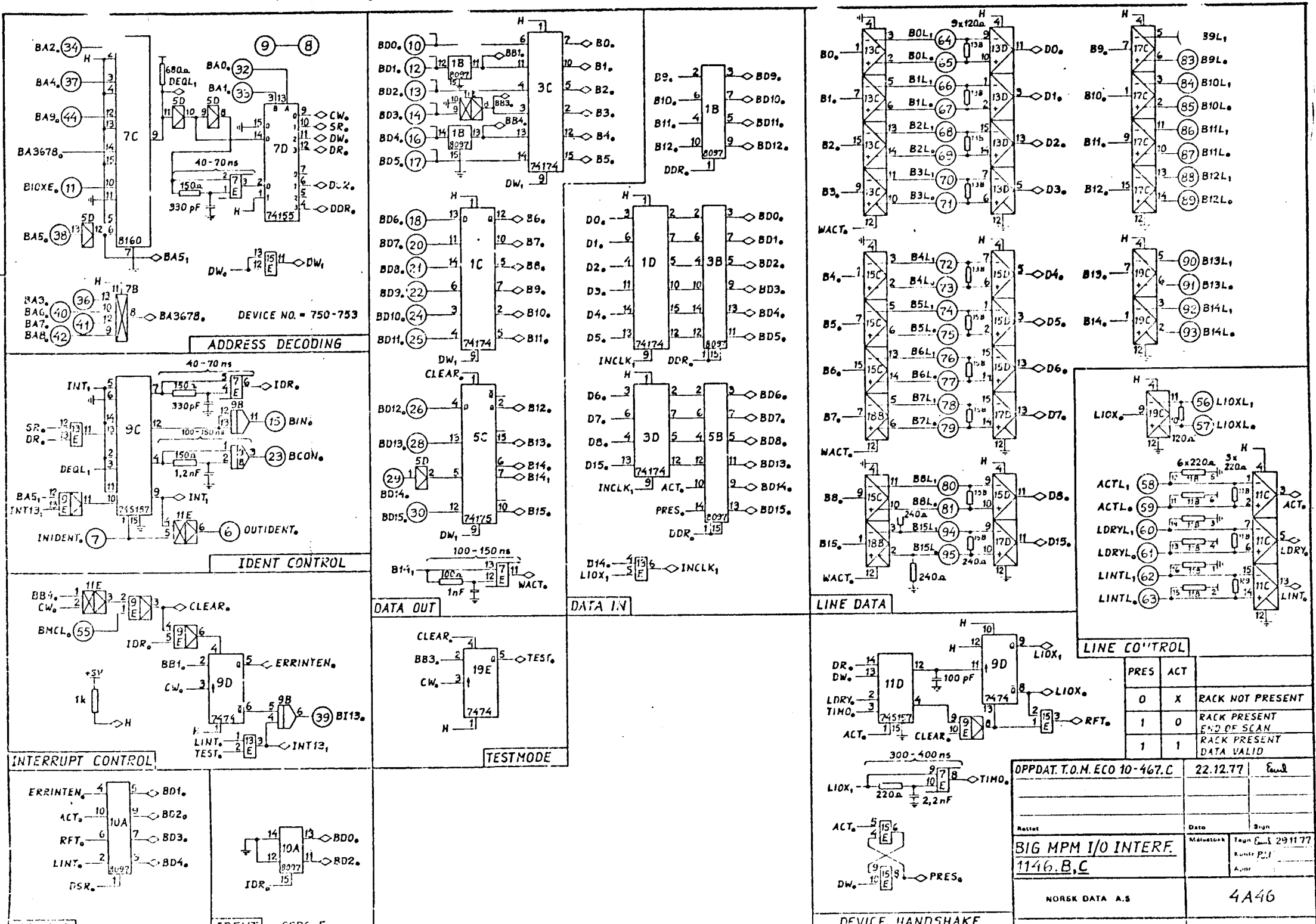

LAYOUT BLOCK Y, ODD ADDRESSES
LAYOUT BLOCK X, EVEN ADDRESSES
ADDRESS MULTIPLEXERS
CHIP STROBES
ONE BIT OF DATA
ADDRESS BUFFERS
START MEMORY CYCLE
CYCLE STATUS
ENABLE DATA TO BUS
MEMORY RESPONSE
TIME COUNTER
DATA TRANSCEIVERS
ALL IC's EXCEPT 1A, 3A, 4A, 7A, 9A AND 10A ARE CONNECTED TO 5V STANDBY
MOSTEK: MK 4116-3
TEXAS: TMS 4071-3
CONTACT FINGERS AT REAR OF CARD
32K RAM
1132.D
A/S NORSK DATA-ELEKTRONIKK
4A32
Oppdat. iflg. ECO nr. 10-498
14F4,5,6 innlegn. C-version fjernet
Ajourf. og påført D.
2.5.78
23.12.77
13.10.77
BW
PJJ/
PJJ/


ADDRESS LINE RECEIVERS
Adders perform ADDR + LIMIT + 1 = ADDR - LIMIT
If overflow then ADDR > LIMIT.
LOK1 UOK0
RANGE COMPARE
LOK1 UOK0
0 0 ADDR < LOW < UPP ADDR BELOW RANGE
0 1 UPP < ADDR < LOW RANGE NEG (No access)
1 0 LOW < ADDR < UPPER ADDR WITHIN RANGE
1 1 LOW < UPP < ADDR ADDR ABOVE RANGE
CONTROLLER REQUEST
MODULE REQUEST
READ/WRITE
THUMBWHEEL SWITCHES
UPPER LIMIT
LOWER LIMIT
1 pk 7400
1 pk 74S00
1 pk 7404
1 pk 74S04
1 pk 74S11
1 pk 7414
1 pk 7420
1 pk 7427
1 pk 7454
1 pk 7474
1 pk 74S112
1 pk 74155
4 pk 74S283
5 pk 8096
1 pk 8097
1 pk 8098
6 pk 26LS32
29 pk
7E, 11E and 13E is not mounted when thumbwheel switches are used
Tegnet på oppdat. av ECO 10-525 rettet. 4.2.80/BW
OPPDAT TOM ECO 10-525 Endr: I E 31.7.78 TEAA/BW
OPPDAT T.O.M. ECO 10-499 2.5.78 BW
Rett i ECO 10-478 31.3.78 BW
OPPDAT. T.O.M ECO 10-466. 27.12.77
Signalnavn 6111 endr 25.1.78 BW
BIG MPM ADDRESS
1142.E
A/S NORSK DATA ELEKTRONIKK
4142


DATA CORRECT AND TRANSCEIVE
BUS TRANSCEIVE
PARITY GEN.
ERROR DECODING
CORRECTION CODE GENERATE AND CHECK
DATA READY TIMING
DATA ENABLE
ERROR HANDLING
ACCESS
WRITE
18 BIT READ
ERRCOR DISABLED
21 BIT READ
21 BIT CORRECTED
SPARE POSITION (18C)
OPPDAT T.O.M. ECO Nr. 525, D.L.E
31.7.78
BW
Ajourført
28.6.78
PU BW
BIO MPM DATA
1143.E
A/S NORSK DATA-ELEKTRONIKK
4A43

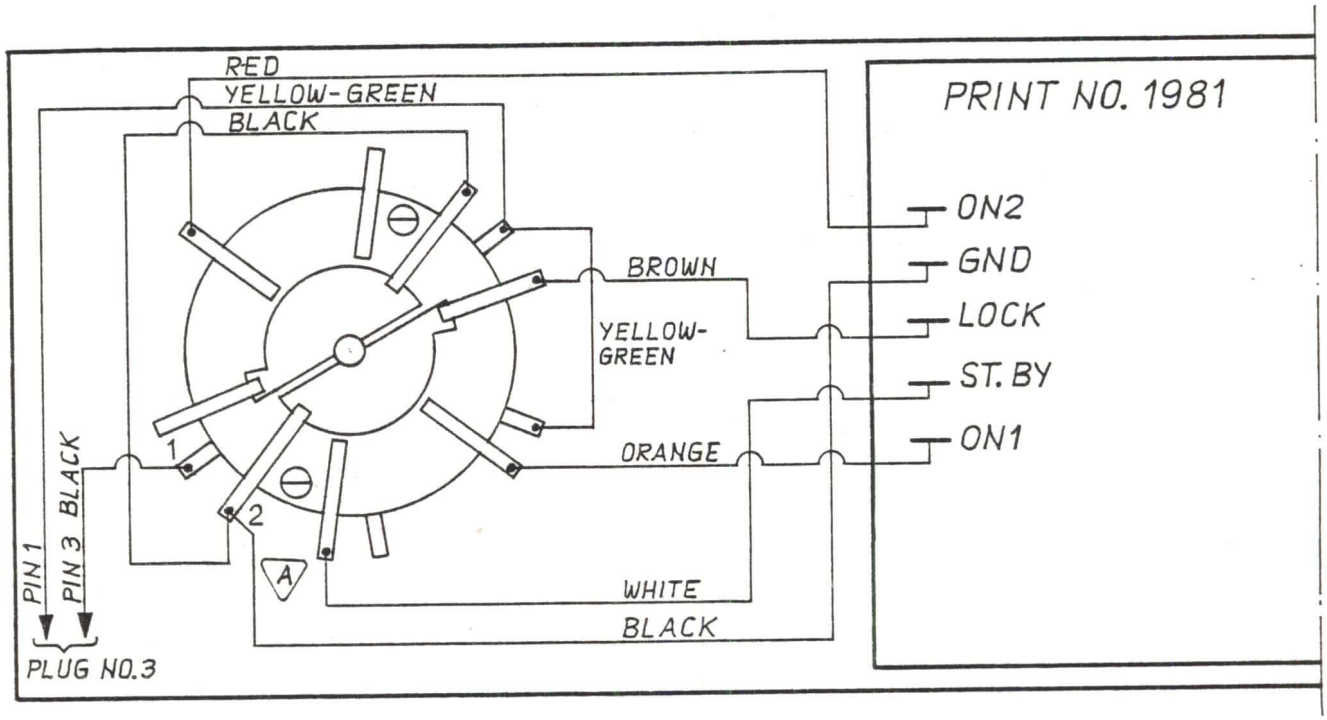

ALLOCATE ADDRESS
REQUEST REFRESH
ALLOCATE DATA
GRANT REFRESH
TEST IF PREVIOUS ALLOCATION USABLE
DELAY UNTIL END OF META-STATE
ALLOCATE REQUEST
DETECT VALID ALLOCATION
REFRESH ADDRESS
MEMORY CONTROL
RETRY
TIMEOUT
VALID means: One and only one port is allocated and this port has issued a request
BIG MPM CONTROL
1144.CDEF
NORSK DATA A.S
4A44


LINE DATA
READ DATA
PORT COMMUNICATION
X LOG
Y LOG
ERROR INTERRUPT
CONTROL
COMMAND DECODING
READ SEQUENCING
SCAN HIT
RESET INT & LOG
SCAN COUNTER
BIG MPM X-Y LOG
1145.B.C
NORSK DATA A.S
4A45
OPPDAT. T.B.M. ECO 10-631
1stk. 330pF forandet. 680pF
Ajourført
23/04/81
13.4.78
28.4.78
BW
PJJ/
PJJ/


ADDRESS DECODING
DEVICE NO. = 750-753
IDENT CONTROL
INTERRUPT CONTROL
DATA OUT
TESTMODE
DATA IN
LINE DATA
LINE CONTROL
DEVICE HANDSHAKE
PRES ACT
0 X RACK NOT PRESENT
1 0 RACK PRESENT END OF SCAN
1 1 RACK PRESENT DATA VALID
OPPDAT. T.O.M. ECO 10-467.C 22.12.77
BIG MPM I/O INTERF.
1146.B,C
NORSK DATA A.S
4A46

NORSK DATA A.S Oslo, Norway	Title NORD-100-500 (A) KEY SWITCH CONNECTION	Drawing no. 4 - 9456

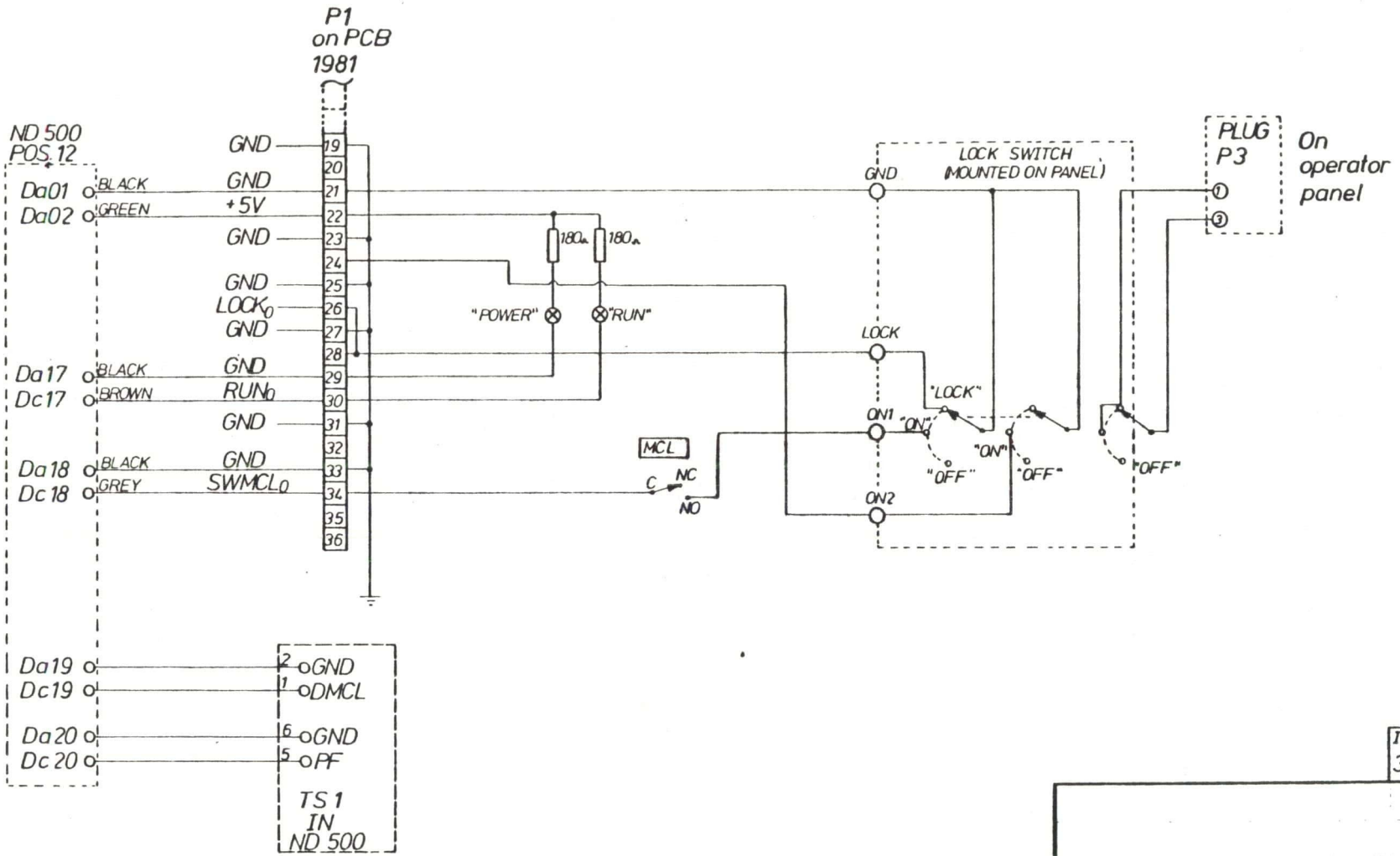
CABLE DIMENSION 0,3 mm^2



OPERATOR PANEL, REAR VIEW

(A)2 corrected 12.02.81 . H.O.

DRAWN BY HO/Eml	Remarks RERLACES DRAWING NO. 4-9455 FOR BOTH VERSION OF NORD-100	Replacement for	Date
APPROVED BY		Replaced by	Date
DATE 09.10.80			



ID.NO.	CARD	PRINT
322571	A	A

Corrected | Date | Sign.

PANEL CONTROL
ND 500

Print no. 1981

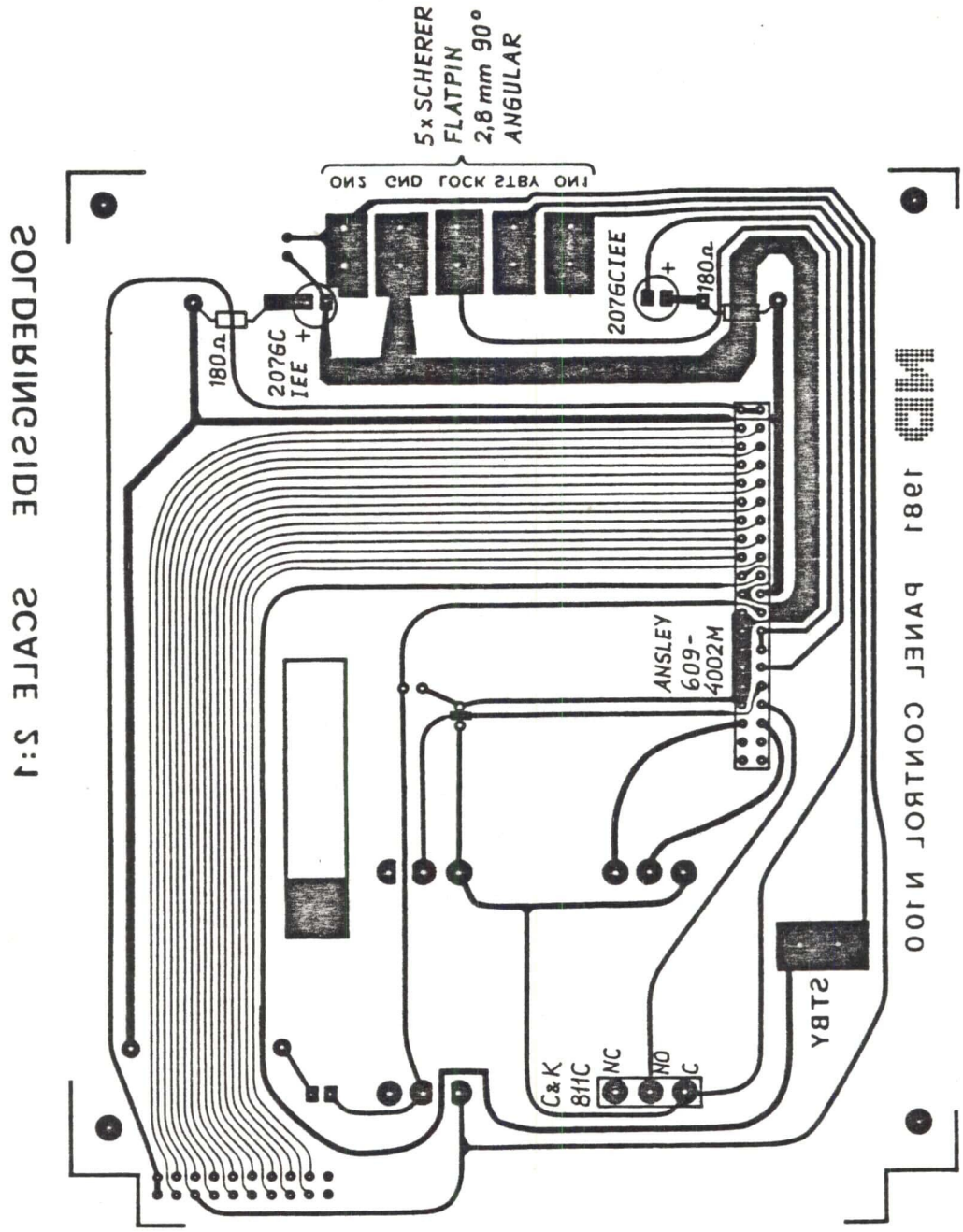
Drawn AL 10/04/81
Contr. TS.
Page 1 of 1

Replacement for

NORSK DATA A.S
Oslo, Norway

Replaced by

NORSK DATA A S Oslo Norway	Title PANEL CONTROL N-500	ID. NO. 322571	CARD PRINT A A
		PRINT NO. 1981	



DRAWN BY Eml	Remarks SAME PRINT FOR PANEL CONTROL N-100 AND PANEL CONTROL N-500	Replacement for Date
APPROVED BY TS/SEH		Replaced by Date
DATE 18.12.80		

NORSK DATA A.S

Title: 1981 PCB OP.PANEL CABLE FOR NORD - 500

Drawing No.: 3 - 9502

WIRE NO.	SIGNAL	POLARITY	N-500 FRAME P12 D-CONNECTOR FOR CABLE TRIPPEL BERG CONNECTOR PIN NO.	PLUG ON 1981 PCB IN OP.PANEL. FOR CABLE DOUBLE BERG CONNECTOR PIN NO.	PLUG PL 8 ON N-500 POWER CONTROL PANEL PIN NO.	TERMINAL STRIP BEHIND N-500 FRAME	COLOUR CODE	WIRE GAUGE
01			DC 1					
02	GND		DA 1	21			BLACK	0,20
03			DC 2					
04	+5V		DA 2	22			GREEN	0,20
05			DC 3					
06			DA 3					
07			DC 4					
08			DA 4					
09			DC 5					
10			DA 5					
11			DC 6					
12			DA 6					
13			DC 7					
14			DA 7					
15			DC 8					
16			DA 8					
17			DC 9					
18			DA 9					
19			DC 10					
20			DA 10					
21			DC 11					
22			DA 11					
23			DC 12					
24			DA 12					
25			DC 13					
26			DA 13					
27			DC 14					
28			DA 14					
29			DC 15					
30			DA 15					
31			DC 16					
32			DA 16					
33	RUNNING		DC 17	30	NC		BROWN	0,20
34	GND		DA 17	29	NC		BLACK	0,20
35	SWMCL		DC 18	34	NC		GREY	0,20
36	GND		DA 18	33	NC		BLACK	0,20
37	DMCL		DC 19	NC	8	1 MI	GREY	0,75
38	GND		DA 19	NC	10	2 GND	BLACK	0,75
39						3 MI	GREY	0,75
40						4 GND	BLACK	0,75
41	POWER FAIL		DC 20	NC	9	5 PFINT	WHITE	0,75
42	GND		DA 20	NC	10	6 GND	BLACK	0,75
43					9	7 PFINT	WHITE	0,75
44					10	8 GND	BLACK	0,75
45					12	9 EXT.PF	BROWN	0,75
46					10	10 GND	BLACK	0,75
47								
48								
49								
50								
51								
52								
53								
54								
55								
56								
57								
58								
59								
60								
61								
62								
63								
64								

INTERNAL CABLE TYPE: TWISTED PAIR IN PVC TUBING

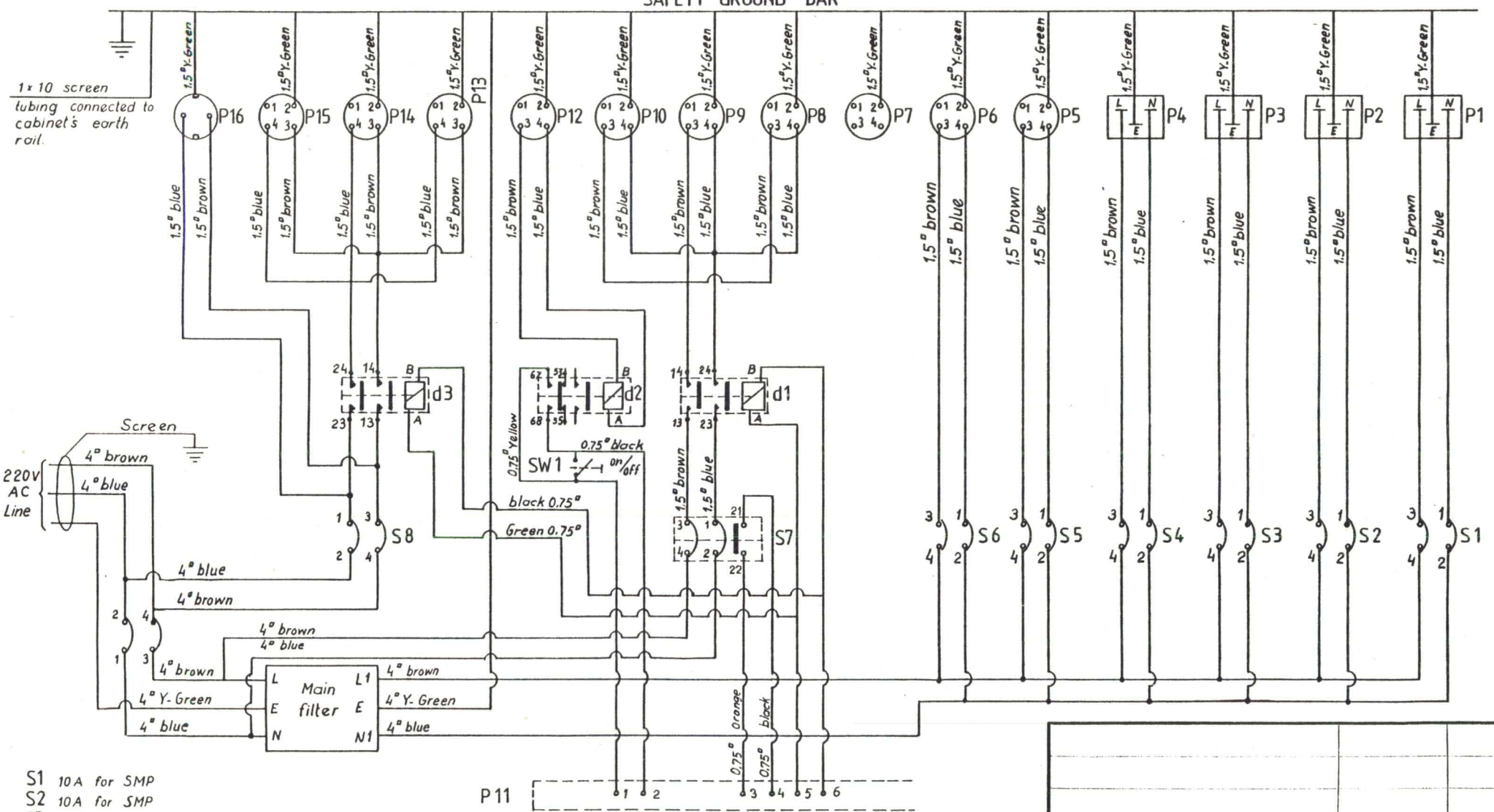
EXTERNAL CABLE TYPE 1:

EXTERNAL CABLE TYPE 2:

EXTERNAL CABLE TYPE 3:

EXTERNAL CABLE TYPE 4:

Drawn by: HO/ma	Remarks: NC - NO CONNECTION	Replacement for	Date
Approved		Replaced by	Date
Date: 25.2.81			



S1 10A for SMP
S2 10A for SMP
S3 10A for SMP
S4 10A for SMP
S5 4A for Control panel
S6 4A for Floppy
S7 4A with switch for control of fan.
S8 2A for control current out and service plug
S9 25A Main fuse
d1 12V DC Relay for fan
d2 220 V~ Relay with delay for on/off signal to power control.
d3 12V DC Relay control current output.

P1 for SMP1
P2 for SMP2
P3 for SMP3
P4 for SMP4
P5 for power control panel
P6 for floppy
P7 Spare
P8, P9, P10, for fans
P11 signal plug in/out.

P12 control current in
P13, P14, P15, control current out
P16 service plug
SW1 delay on/off for power control panel.

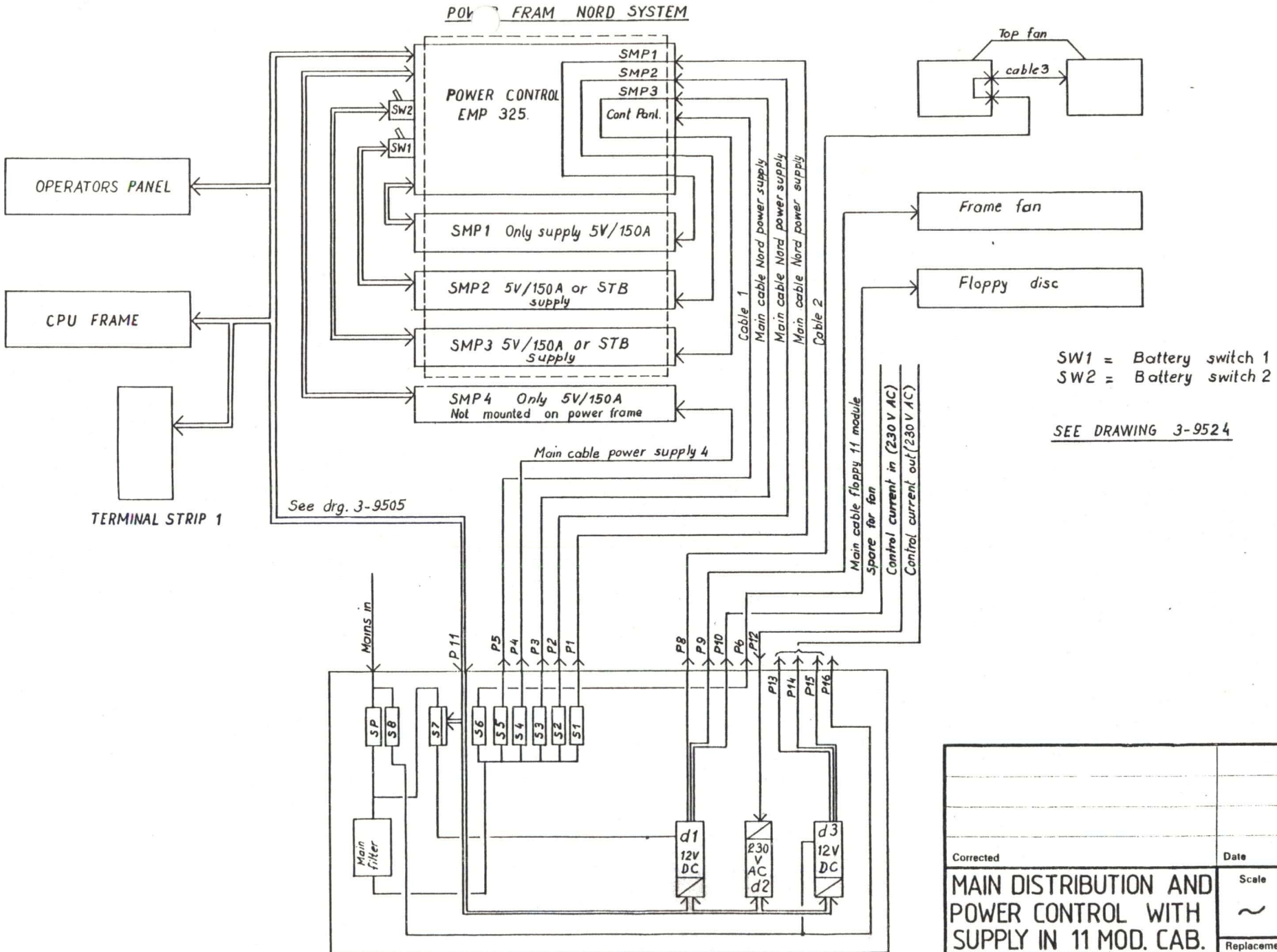
Corrected	Date	Sign.

WIRING DIAGRAM FOR 220V POWER PANEL ND 100-500. VERSION 4

NORSK DATA A.S
Oslo, Norway

Scale	Drawn HJM 29.4.81.
~	Contr.
	Appr.

Replacement for
3-9504
Replaced by



Corrected	Date	Sign.

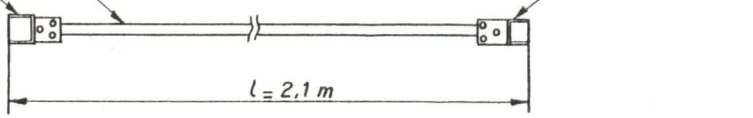
MAIN DISTRIBUTION AND POWER CONTROL WITH SUPPLY IN 11 MOD. CAB.	Scale ~	Drawn MJM 18.5.81
		Contr.
		Appr.
	Replacement for	
NORSK DATA A.S Oslo, Norway	3-9523	
	Replaced by	

Cable type: Ölflex 2 x 1.5° + Screen

CABLE MAINS NORD POWER SUPPLY
1 : 1

Plug Otto Hail 106

Plug Otto Hail 104



Brown = L
Blue = N
Screen = E (Earth)

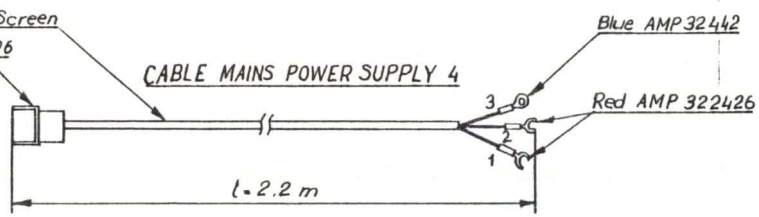
Cable type: Ölflex 2 x 1.5° + Screen

Plug Otto Hail 106

CABLE MAINS POWER SUPPLY 4

Blue AMP 32442

Red AMP 322426



Brown = L
Blue = N
Screen = E (Earth)

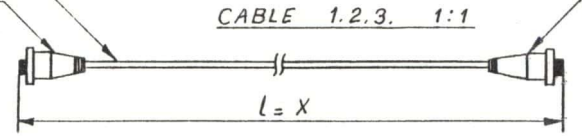
Brown = 1
Blue = 2
Green = 3

Cable type: 2 x 0,75° + Screen

AMP 206429-1
+ AMP 206358-1

CABLE 1.2.3. 1:1

AMP 206060-1
+ AMP 206358-1



Brown = Pin 3
Blue = Pin 4
Screen = Pin 2

Length

cable 1 = 1.6 m
cable 2 = 2.8 m
cable 3 = 0,3 m

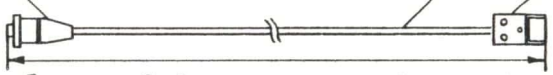
cable 1 = cable mains control panel 11 module cabinet
cable 2 = cable mains to top fan 11 modul cabinet
cable 2. Used for main control betwen master cabinet and slave cabinet.
cable 3 = coble mains top fan 30 cm 11 module cabinet.

AMP 206429-1
+ AMP 206358-1

MAIN CABLE FLOPPY 11 MOD.

cable type: Ölflex 2 x 0.75°
+ Screen

Otto Hail 4030



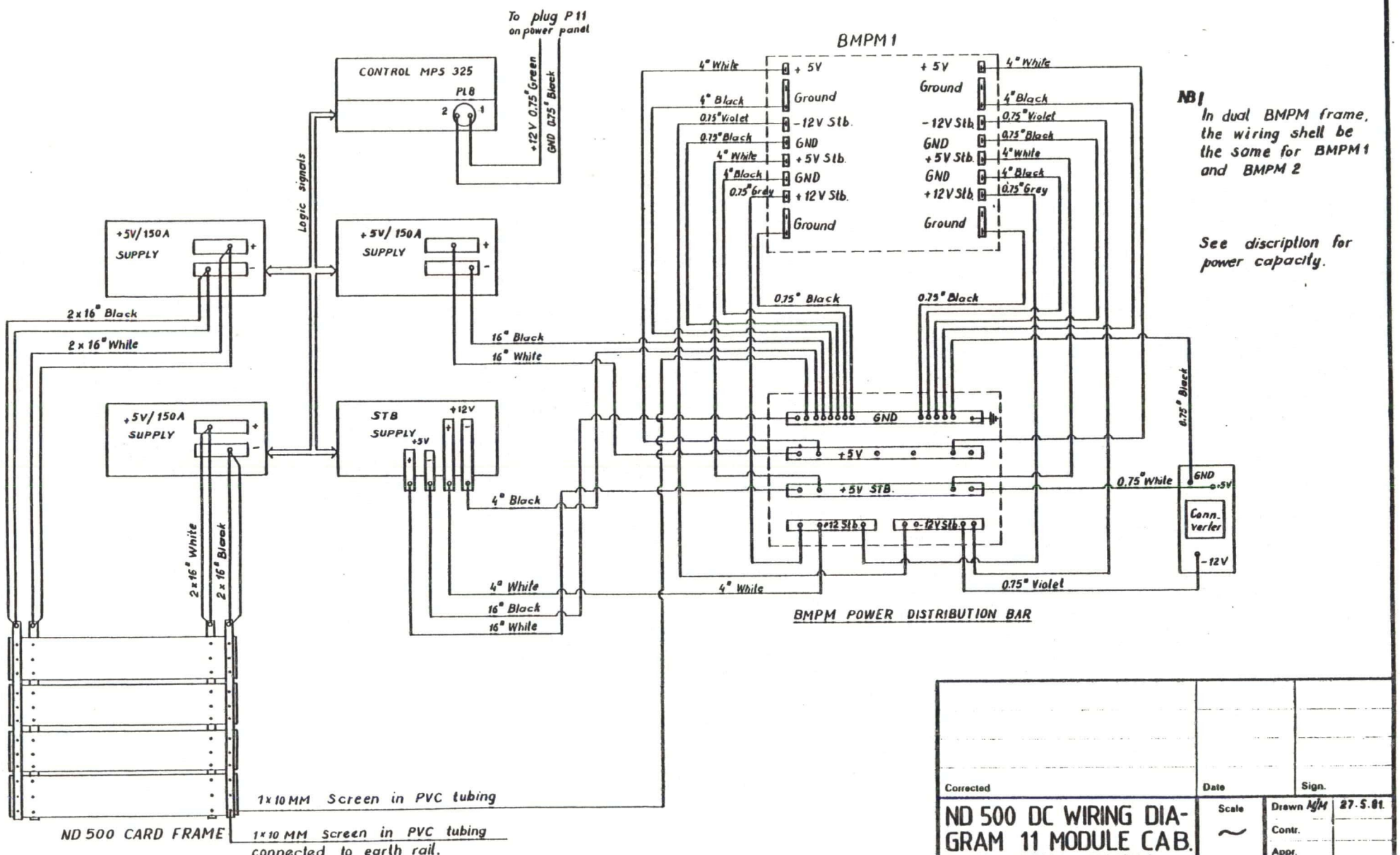
Brown = Pin 3
Blue = Pin 4
Screen = Pin 2

Brown = L
Blue = N
Screen = E (Earth)

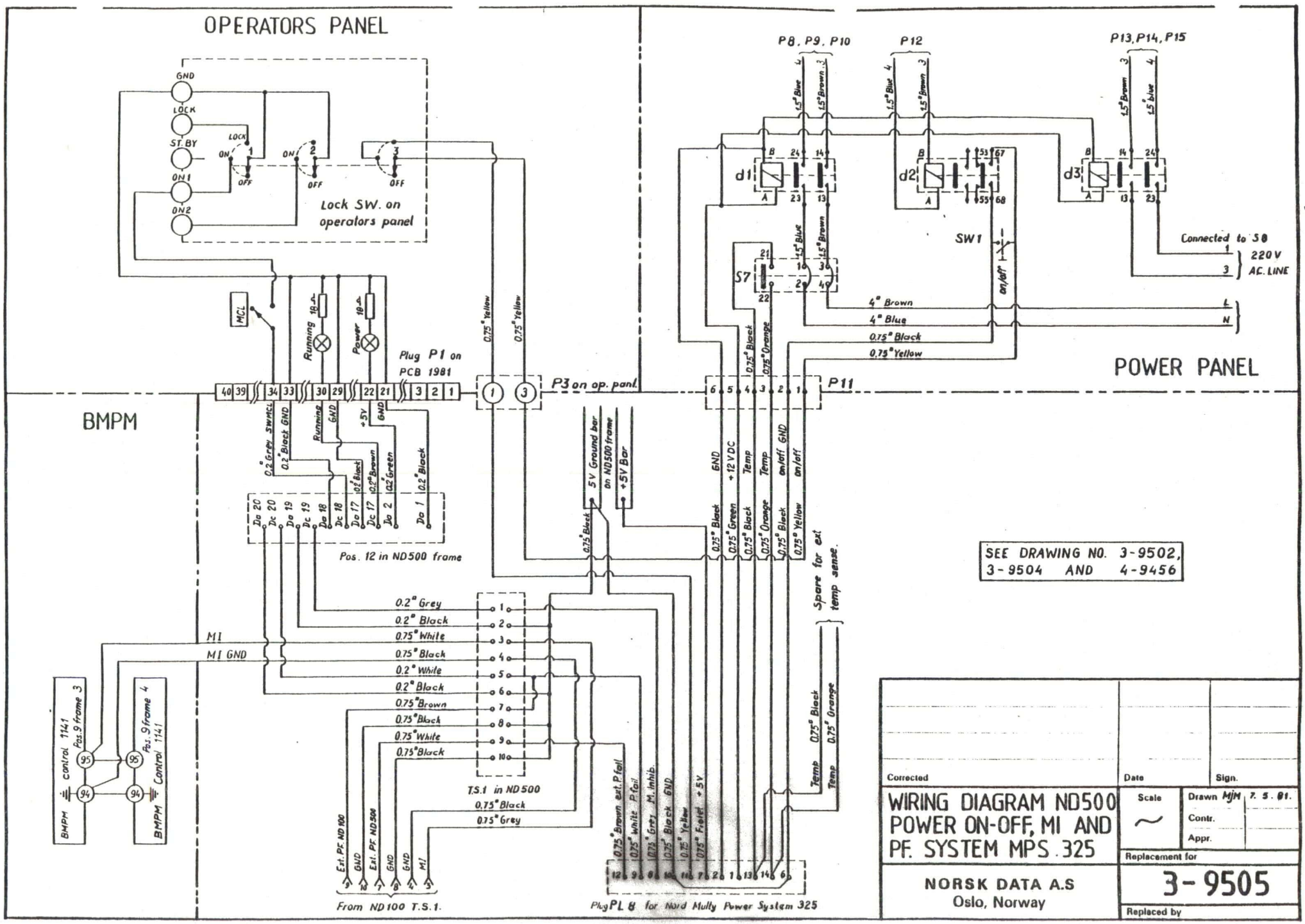
SEE DRAWING 3-9523

NB! screen on all these cables are of copper.

Corrected	Date	Sign.
MAINS CABLES USED IN 11-MODULE CAB.	Scale ~	Drawn MJM 26.5.81.
		Contr.
		Appr.
	Replacement for	
NORSK DATA A.S Oslo, Norway	3-9524	
	Replaced by	



Corrected	Date	Sign.
ND 500 DC WIRING DIAGRAM 11 MODULE CAB. WITH DUAL BMPM	Scale ~	Drawn Ajh 27.5.81 Contr. Appr.
	Replacement for	
NORSK DATA A.S Oslo, Norway	3-9526	
	Replaced by	


OPERATORS PANEL
GND
LOCK
ST. BY
ON1
ON2
Lock SW. on operators panel
MCL
Running 18
Power 18
Plug P1 on PCB 1981
P3 on op. panl
0.75° Yellow
0.75° Yellow
P8, P9, P10
P12
P13, P14, P15
d1
d2
d3
SW1
S7
Connected to S8
220 V AC. LINE
4° Brown
4° Blue
0.75° Black
0.75° Yellow
0.75° Orange
POWER PANEL
P11
BMPM
0.2° Grey SWMCL
0.2° Black GND
Running
GND
+5V
GND
Pos. 12 in ND500 frame
5 V Ground bar on ND500 frame
+5V Bar
GND
+12 VDC
Temp
Temp
on/off GND
on/off
Spare for ext temp sense.
SEE DRAWING NO. 3-9502, 3-9504 AND 4-9456
0.2° Grey
0.2° Black
0.75° White
0.75° Black
0.2° White
0.2° Black
0.75° Brown
0.75° Black
0.75° White
0.75° Black
MI
MI GND
BMPM control 114.1 Pos.9 frame 3
BMPM Control 114.1 Pos.9 frame 4
T.S.1 in ND500
0.75° Black
0.75° Grey
Ext. PF. ND100
Ext. PF. ND500
From ND100 T.S.1.
Plug PL 8 for Nord Multy Power System 325
Corrected
Date
Sign.
WIRING DIAGRAM ND500 POWER ON-OFF, MI AND PF. SYSTEM MPS 325
Scale
Drawn MJM 7. 5. 81.
Contr.
Appr.
Replacement for
NORSK DATA A.S
Oslo, Norway
3-9505
Replaced by