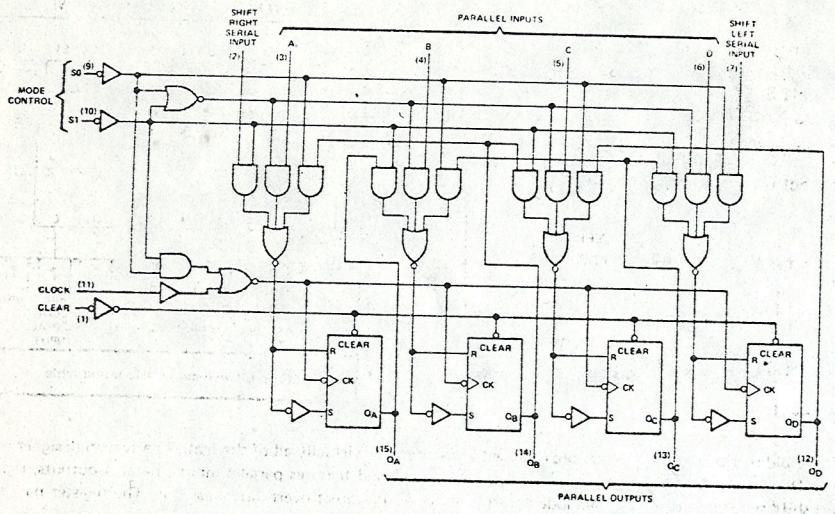
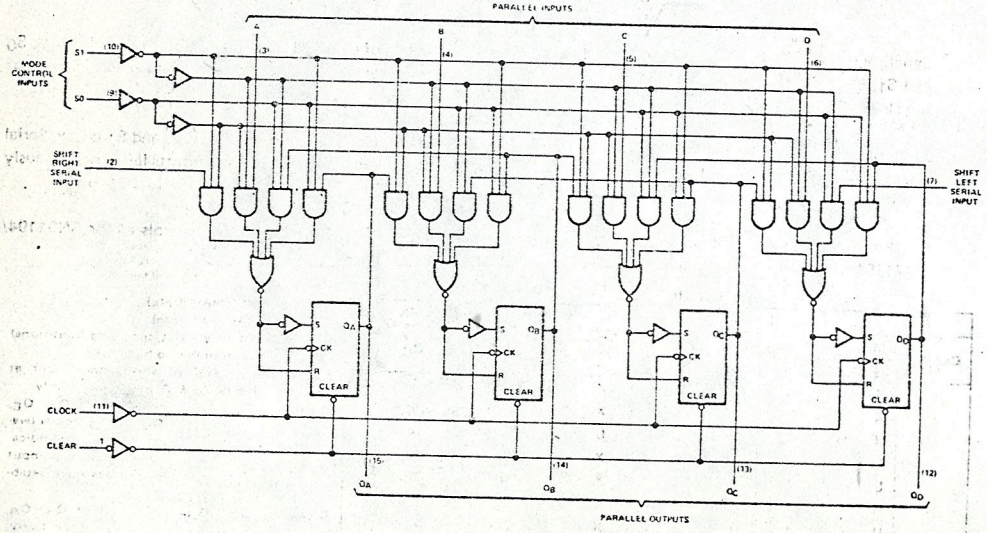
functional block diagrams

'194



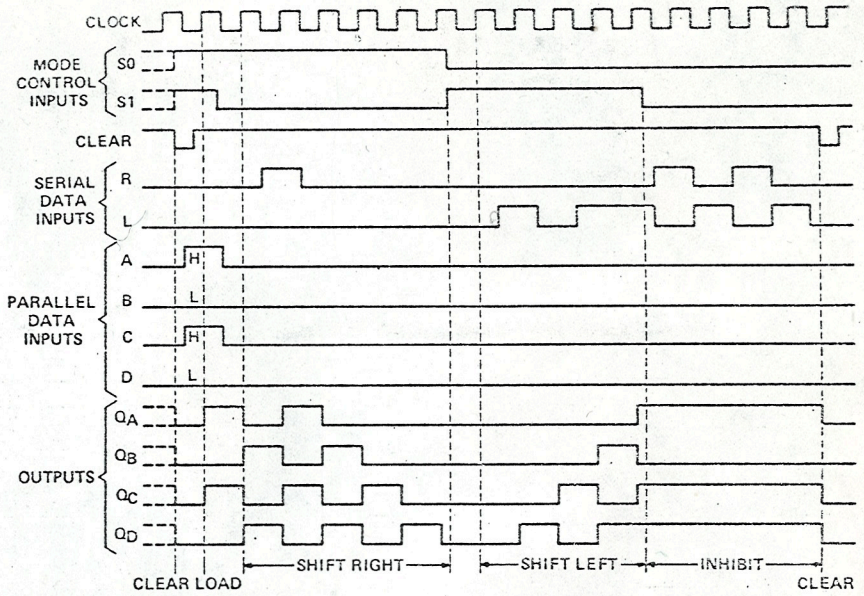
'LS194, 'S194



⊳ . . . . dynamic input activated by a transition from a high level to a low level.

TYPES SN54194, SN54LS194, SN54S194, SN74194, SN74LS194, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

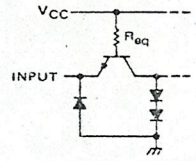
typical clear, load, right shift, left shift, inhibit, and clear sequences



schematics of inputs and outputs

'194

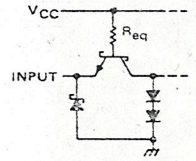
EQUIVALENT OF EACH INPUT



Clock: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 6 kΩ NOM

'LS194

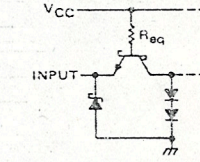
EQUIVALENT OF EACH INPUT



Clock: R_{eq} = 15 kΩ NOM
Other inputs: R_{eq} = 20 kΩ NOM

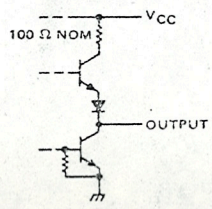
'S194

EQUIVALENT OF EACH INPUT

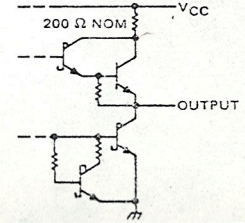


Clear, S0, S1: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 2.8 kΩ NOM

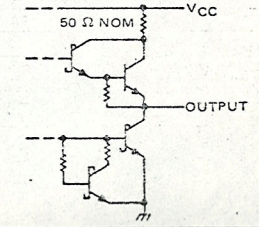
TYPICAL OF ALL OUTPUTS



TYPICAL OF ALL OUTPUTS

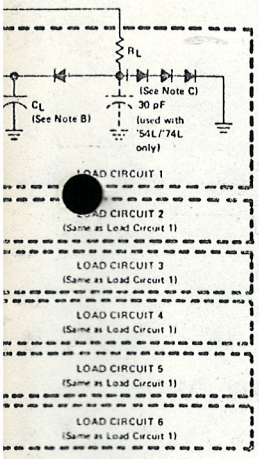


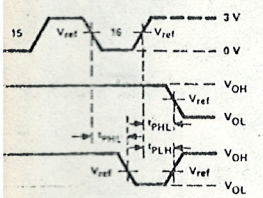
TYPICAL OF ALL OUTPUTS

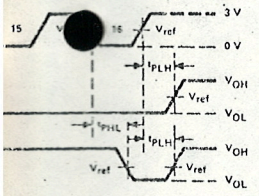


SN54LS192, SN54LS193,
92, SN74LS193
AL CLOCK WITH CLEAR)

MATION







0 Ω, duty cycle = 50%.

'L193.
193 binary counters. Count cycle for '192, 'L

193.
L193.

ES

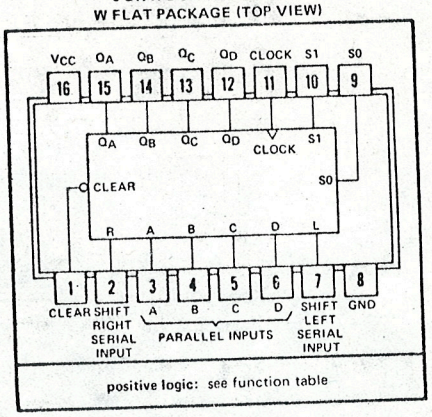
TTL
MSI

TYPES SN54194, SN54LS194, SN54S194, SN74194, SN74LS194, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194	28 MHz	60 mW
'S194	105 MHz	425 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_D)
Shift Left (In the direction Q_D toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

FUNCTION TABLE

INPUTS									OUTPUTS			
CLEAR	MODE S_1	MODE S_0	CLOCK	SERIAL LEFT	SERIAL RIGHT	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

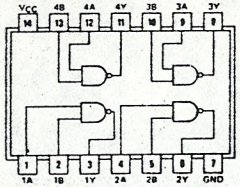
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, Q_D, respectively, before the most-recent ↑ transition of the clock.

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

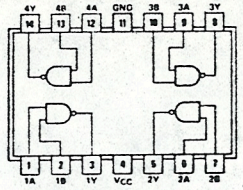
00
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 86



SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)

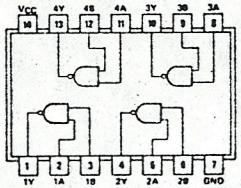


SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

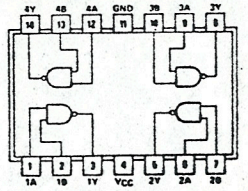
01
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

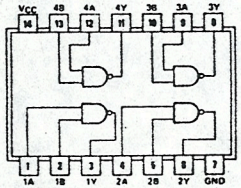
See page 88



SN5401/SN7401(J, N)
SN54LS01/SN74LS01(J, N, W)



SN5401/SN7401(W)
SN54H01/SN74H01(W)
SN54L01/SN74L01(T)

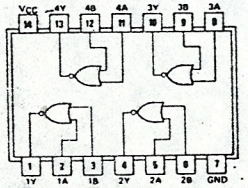


SN54H01/SN74H01(J, N)

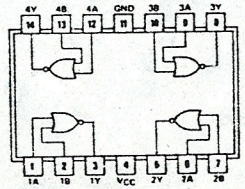
02
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

See page 92



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



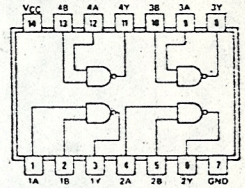
SN5402/SN7402(W)
SN54L02/SN74L02(T)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

03
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 88

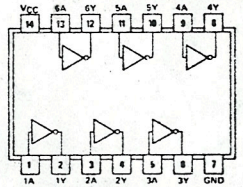


SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

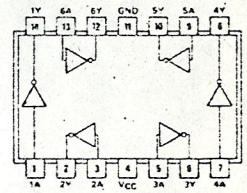
04
HEX INVERTERS

positive logic:
$Y = \overline{A}$

See page 86



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)

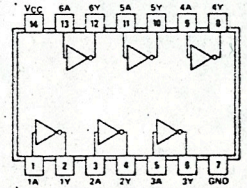


SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

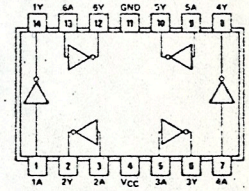
05
HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A}$

See page 88



SN5405/SN7405(J, N)
SN54H05/SN74H05(J, N)
SN54LS05/SN74LS05(J, N, W)
SN54S05/SN74S05(J, N, W)

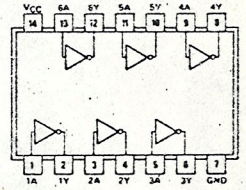


SN5405/SN7405(W)
SN54H05/SN74H05(W)

06
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106



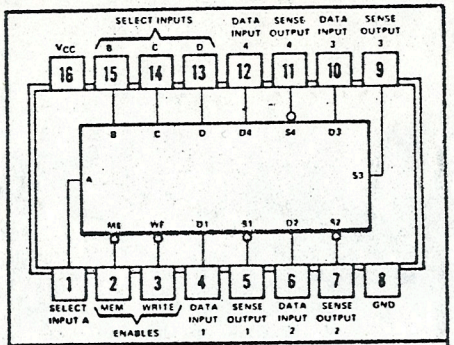
SN5406/SN7406(J, N, W)

TYPE SN7489
64-BIT READ/WRITE MEMORY

BULLETIN NO. DL-S 7211386, FEBRUARY 1971 – REVISED DECEMBER 1972

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see description

†Pin assignments for these circuits are the same for all packages.

description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. The open-collector outputs may be utilized to drive external loads directly; however, dynamic reponse of an output can, in most cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

FUNCTION TABLE

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

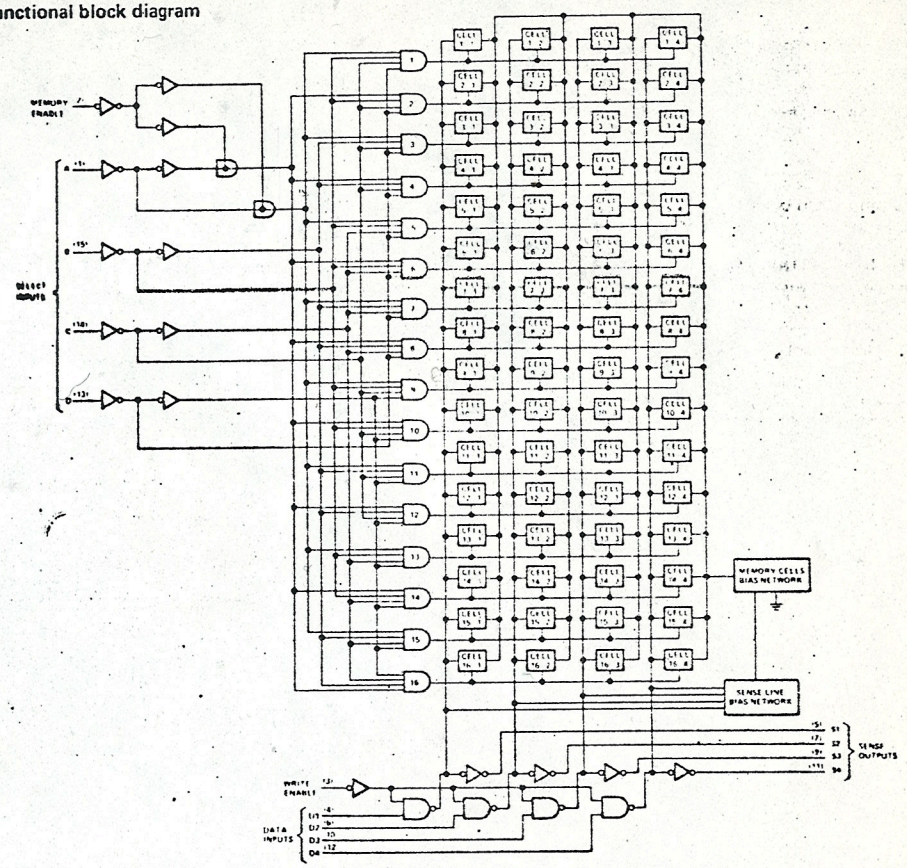
write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

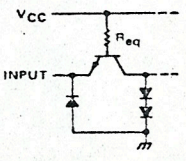
The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

functional block diagram



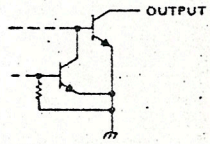
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



D1, D2, D3, D4: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



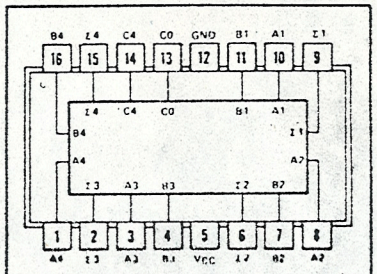
TYPES SN5483A, SN54LS83, SN7483A, SN74LS83
4-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211853, DECEMBER 1972

- For applications in:
  Digital Computer Systems
  Data-Handling Systems
  Control Systems
- SN54283/SN74283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout

TYPE	TYPICAL ADD TIMES: TWO 8-BIT WORDS	TYPICAL ADD TIMES: TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
'83A	23 ns	43 ns	310 mW
'LS83	89 ns	165 ns	75 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion. Designed for medium-to-high-speed, the circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) but are compatible with both DTL and TTL families.

The '83A circuits feature full look ahead across four bits to generate the carry term in typically 10 nanoseconds to achieve partial look-ahead performance with the economy of ripple carry.

The 'LS83 can reduce power requirements to less than 20 mW/bit for power-sensitive applications. These circuits are implemented with single-inversion, high-speed, Darlington-connected serial-carry circuits within each bit.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS are characterized for 0°C to 70°C operation.

FUNCTION TABLE

INPUT							OUTPUT: WHEN C0 = L				WHEN C0 = H		
									WHEN C2 = L				WHEN C2 = H
A1	B1	A2	B2	C0	C2	C4	Σ1	Σ2	Σ3	Σ4	Σ1	Σ2	Σ3	Σ4
A3	B3	A4	B4											
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
H	L	L	L	L	L	L	H	L	L	L	L	H	L	L
L	H	L	L	L	L	L	H	L	L	L	L	H	L	L
H	H	L	L	L	L	L	L	H	L	L	H	H	L	L
L	L	H	L	L	L	L	H	L	L	L	H	H	L	L
H	L	H	L	L	L	L	L	H	L	L	L	L	H	L
L	H	H	L	L	L	L	L	H	L	L	L	L	H	L
H	H	H	L	L	L	L	H	L	L	L	H	L	H	L
L	L	L	H	L	L	L	H	L	L	L	H	H	L	L
H	L	L	H	L	L	L	L	H	L	L	L	L	H	L
L	H	L	H	L	L	L	L	H	L	L	L	L	H	L
H	H	L	H	L	L	L	H	L	L	L	H	L	H	L
L	L	H	H	L	L	L	H	L	L	L	H	H	L	L
H	L	H	H	L	L	L	L	H	L	L	L	L	H	L
L	H	H	H	L	L	L	L	H	L	L	L	L	H	L
H	H	H	H	L	L	L	H	L	L	L	H	L	H	L
L	L	L	L	H	H	H	H	L	H	H	H	L	H	H
H	L	L	L	H	H	H	L	H	H	H	L	H	H	H
L	H	L	L	H	H	H	L	H	H	H	L	H	H	H
H	H	L	L	H	H	H	H	L	H	H	H	L	H	H
L	L	H	L	H	H	H	H	L	H	H	H	L	H	H
H	L	H	L	H	H	H	L	H	H	H	L	H	H	H
L	H	H	L	H	H	H	L	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	L	H	H	H	L	H	H
L	L	L	H	H	H	H	H	L	H	H	H	L	H	H
H	L	L	H	H	H	H	L	H	H	H	L	H	H	H
L	H	L	H	H	H	H	L	H	H	H	L	H	H	H
H	H	L	H	H	H	H	H	L	H	H	H	L	H	H
L	L	H	H	H	H	H	H	L	H	H	H	L	H	H
H	L	H	H	H	H	H	L	H	H	H	L	H	H	H
L	H	H	H	H	H	H	L	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	L	H	H

H = high level, L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54LS' Circuits	−55°C to 125°C
SN74', SN74LS' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the '83A, this rating applies between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4. For the 'LS83, this rating applies between the following pairs: A1 and B1, A1 and C0, B1 and C0, A3 and B3.

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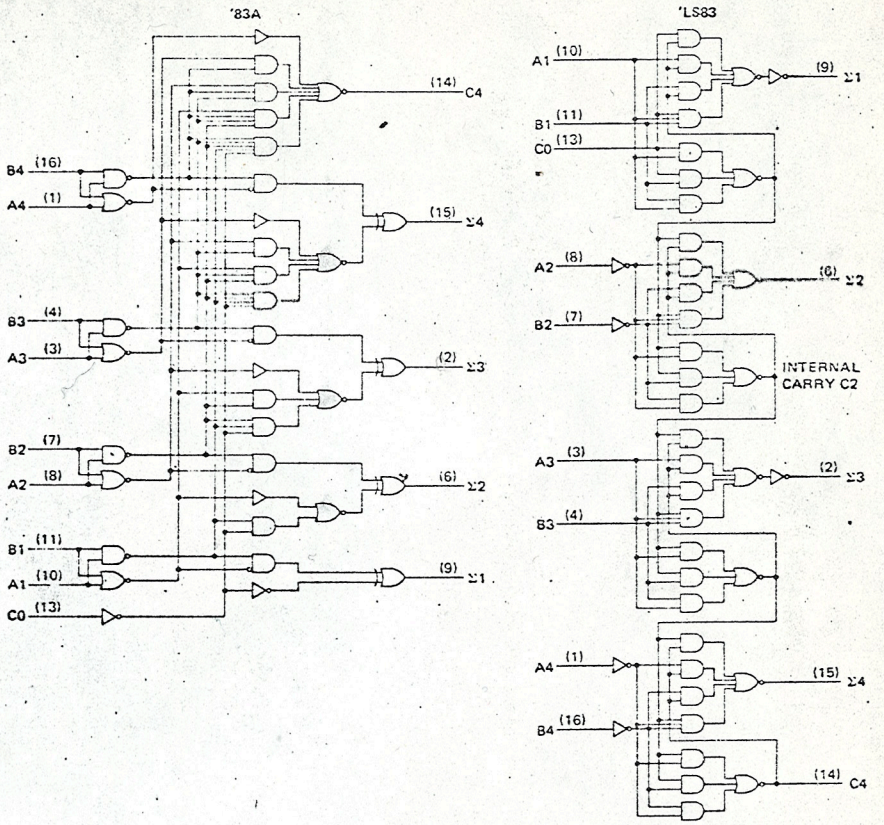
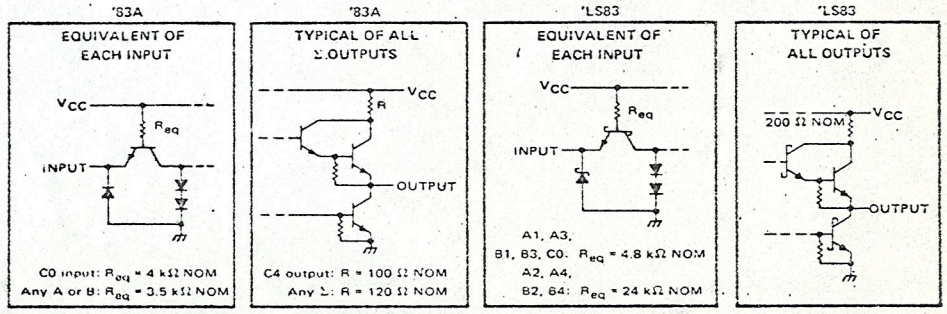
functional block diagrams



schematics of inputs and outputs



TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211812, DECEMBER 1972

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS
for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

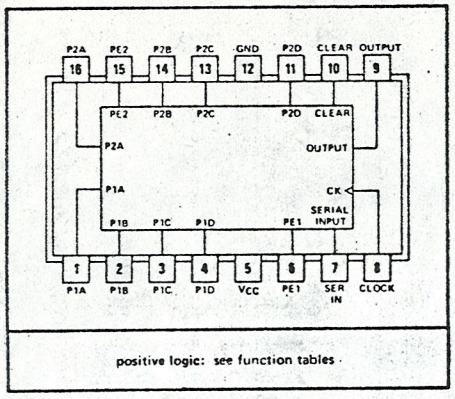
description

These monolithic shift registers which utilize transistor-transistor logic (TTL) circuits in the familiar Series 54/74 configuration, are composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to a low output level by applying a high-level voltage to the clear input while the internal presets are inactive (high). See the preset function table below. Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to either the P1 or P2 inputs of each register stage (A, B, C, and D) with the corresponding preset enable input, PE1 or PE2, high. Presetting, like clearing, is independent of the level of the clock input.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function tables

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be setup at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a low level and the internal presets must be inactive (high) when clocking occurs.

PRESET FUNCTION TABLE
(BIT A, TYPICAL OF ALL)

PRESET INPUTS				INTERNAL
PE1	P1A	PE2	P2A	PRESET A
L	X	L	X	H (inactive)
L	X	X	L	H (inactive)
X	L	L	X	H (inactive)
X	L	X	L	H (inactive)
H	H	X	X	L (active)
X	X	H	H	L (active)

REGISTER FUNCTION TABLE

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

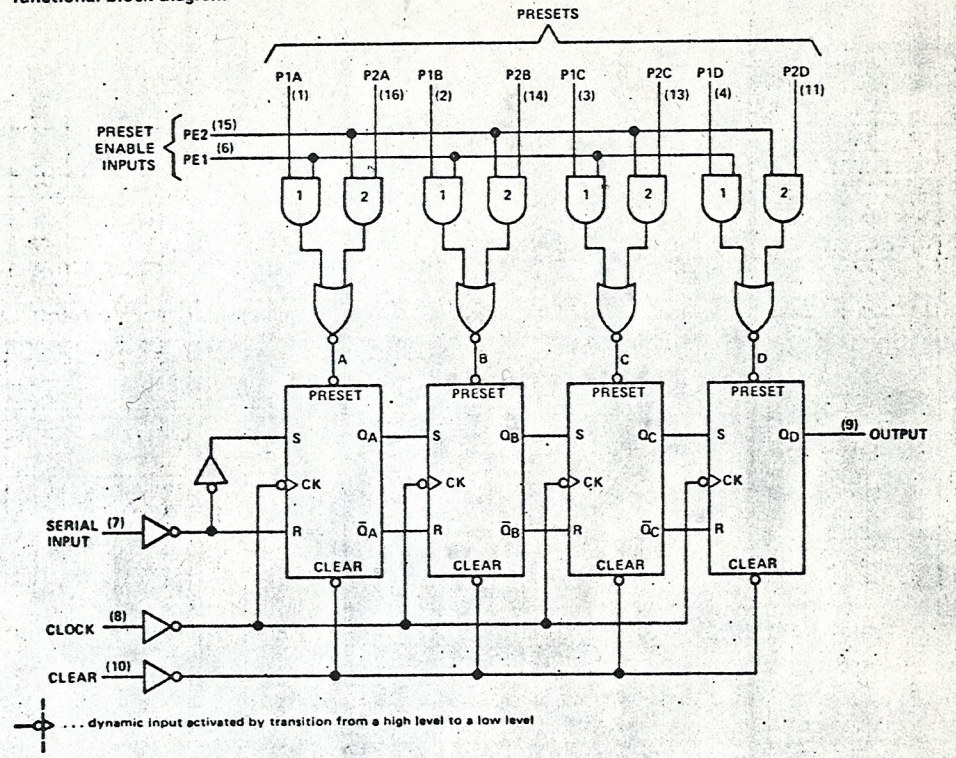
H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5494 Circuits	−55°C to 125°C
SN7494 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

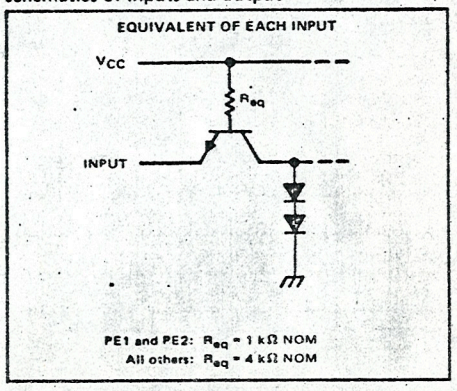
NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

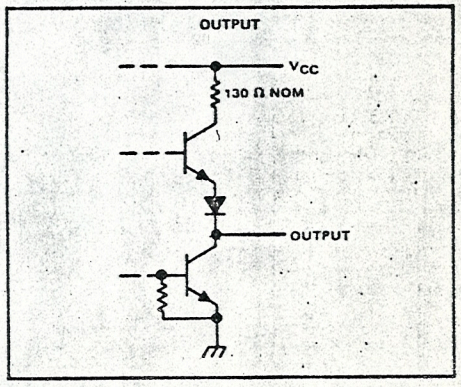
functional block diagram



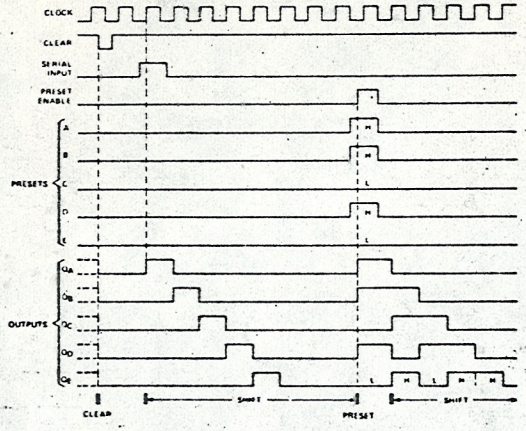
... dynamic input activated by transition from a high level to a low level

schematics of inputs and output

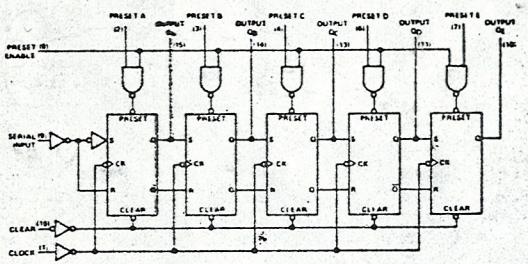




typical clear, shift, preset, and shift sequences



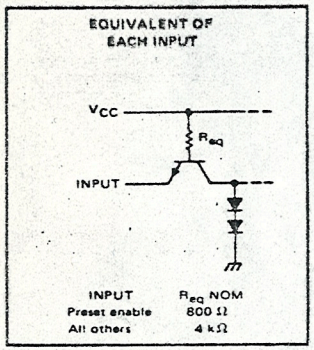
functional block diagram



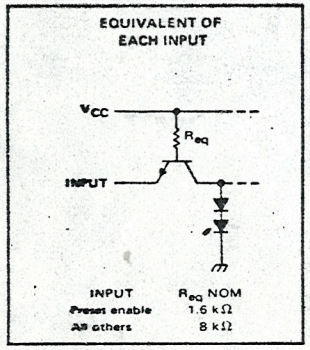
⊣ . . . dynamic input activated by transition from a high level to a low level.

schematics of inputs and outputs

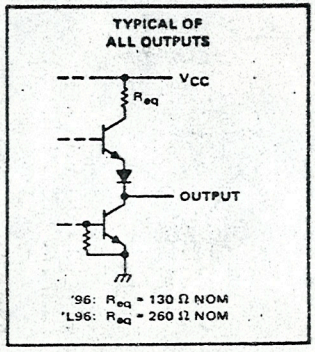
'96



'L96



'96, 'L96

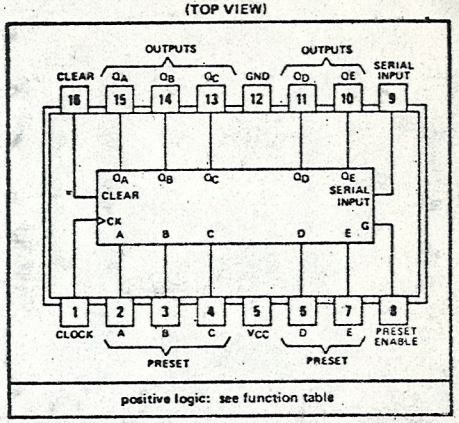


BULLETIN NO. DL-S 7211821, DECEMBER 1972

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW

'96 . . . J, N, OR W PACKAGE
'L96 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

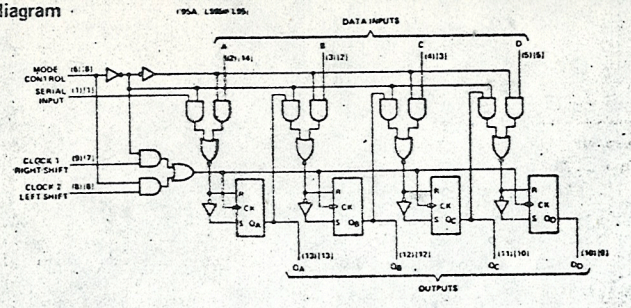
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

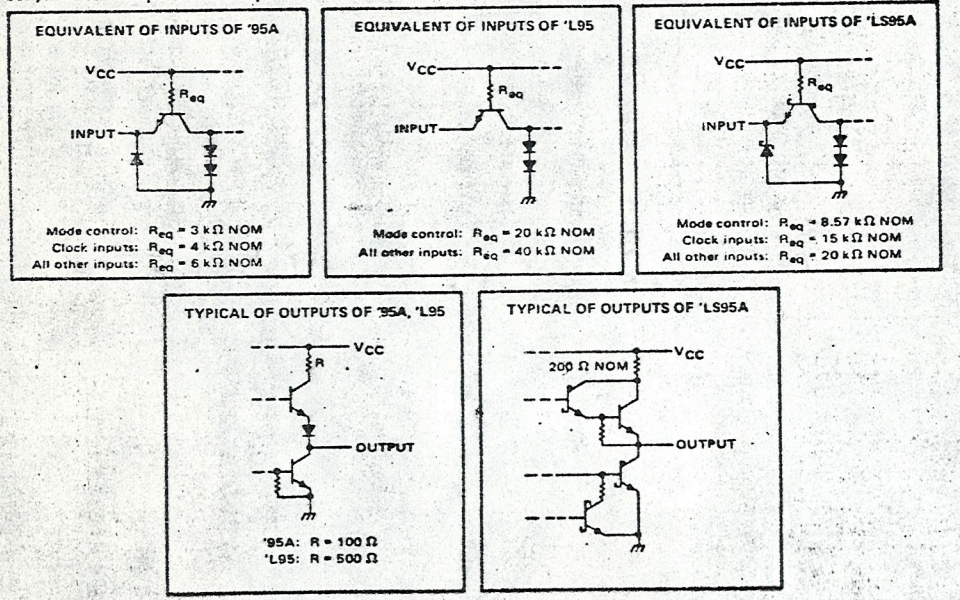
INPUTS								OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	PRESET B	PRESET C	PRESET D	PRESET E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most-recent ↑ transition of the clock.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '95A, 'LS95A . . . . . 7 V
'L95 . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Interemitter voltage (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54L', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. For the 'L95, input voltages must be zero or positive with respect to network ground terminal.
3. This is the voltage between two emitters of a multiple-emitter input transistor. For these devices, this ratings applies between the clock-2 input and the mode control input.

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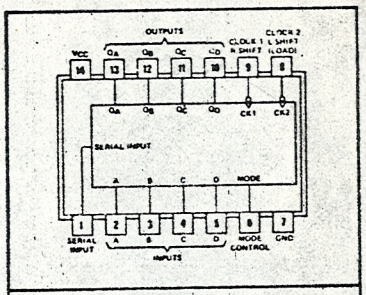
BULLETIN NO. DL-S 7211872, DECEMBER 1972

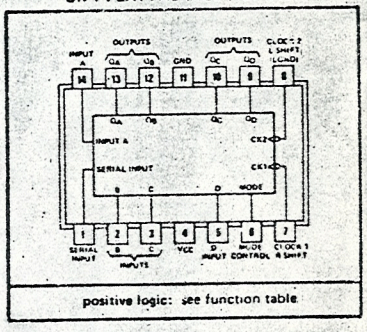
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'L95	5 MHz	19 mW
'LS95A	28 MHz	50 mW

'95A and 'LS95A
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

'L95
J OR N DUAL-IN-LINE
OR T FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (Broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock 2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low, however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

FUNCTION TABLE

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_{Bn}†	Q_{Cn}†	Q_{Dn}†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

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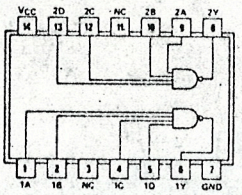
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

40

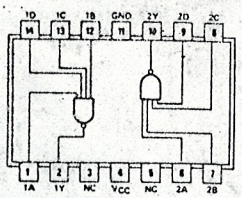
DUAL 4-INPUT
POSITIVE-NAND BUFFERS

positive logic:
$Y = \overline{ABCD}$

See page 102



SN5440/SN7440(J, N)
SN54H40/SN74H40(J, N)
SN54LS40/SN74LS40(J, N, W)
SN54S40/SN74S40(J, N, W)



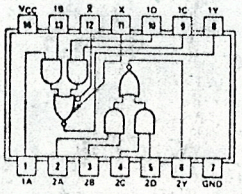
SN5440/SN7440(W)
SN54H40/SN74H40(W)

NC—No internal connection

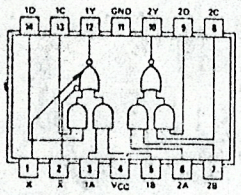
50

DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES
(ONE GATE EXPANDABLE)
positive logic:
$Y = \overline{AB+CD+X}$
'50: X = output of SN5460/SN7460
'H50: X = output of SN54H60/SN74H60
or SN54H62/SN74H62

See page 113 side 70



SN5450/SN7450(J, N)
SN54H50/SN74H50(J, N)

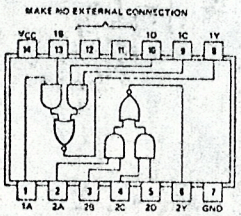


SN5450/SN7450(W)
SN54H50/SN74H50(W)

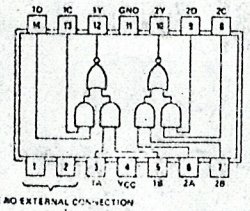
51

DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES

'51, 'H51, 'S51
positive logic:
$Y = \overline{AB+CD}$



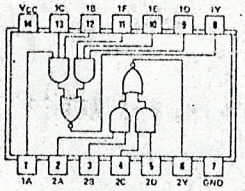
SN5451/SN7451(J, N)
SN54H51/SN74H51(J, N)
SN54S51/SN74S51(J, N, W)



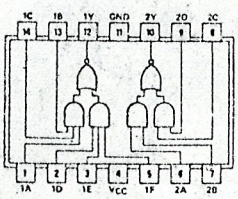
SN5451/SN7451(W)
SN54H51/SN74H51(W)

'L51, 'LS51
positive logic:
$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$
$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

See page 110



SN54L51/SN74L51(J, N)
SN54LS51/SN74LS51(J, N, W)



SN54L51/SN74L51(T)

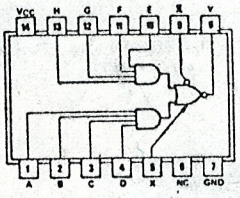
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

55

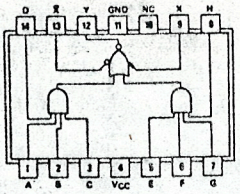
2-WIDE 4-INPUT AND-OR-INVERT GATES

'H55 (EXPANDABLE)
positive logic:
$Y = \overline{ABCD+EFGH+X}$
X = output of SN54H60/SN74H60 or SN54H62/SN74H62

See page 113



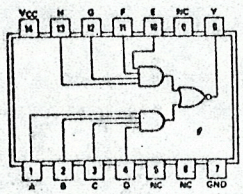
SN54H55/SN74H55(J, N)



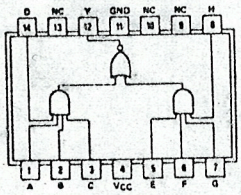
SN54H55/SN74H55(W)

'L55, 'LS55
positive logic:
$Y = \overline{ABCD+EFGH}$

See page 110



SN54L55/SN74L55(J, N)
SN54LS55/SN74LS55(J, N, W)



SN54L55/SN74L55(T)
NC—No internal connection

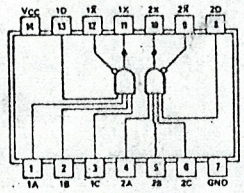
60

DUAL 4-INPUT EXPANDERS

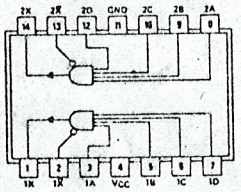
'60
positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453

'H60
positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

See pages 117 and 118



SN5460/SN7460(J, N)
SN54H60/SN74H60(J, N)



SN5460/SN7460(W)
SN54H60/SN74H60(W)

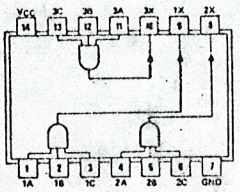
NC—No internal connection

61

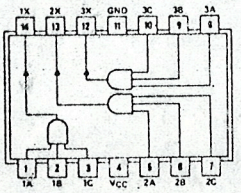
TRIPLE 3-INPUT EXPANDERS

positive logic:
X = ABC when connected to X input of SN54H52/SN74H52

See page 119



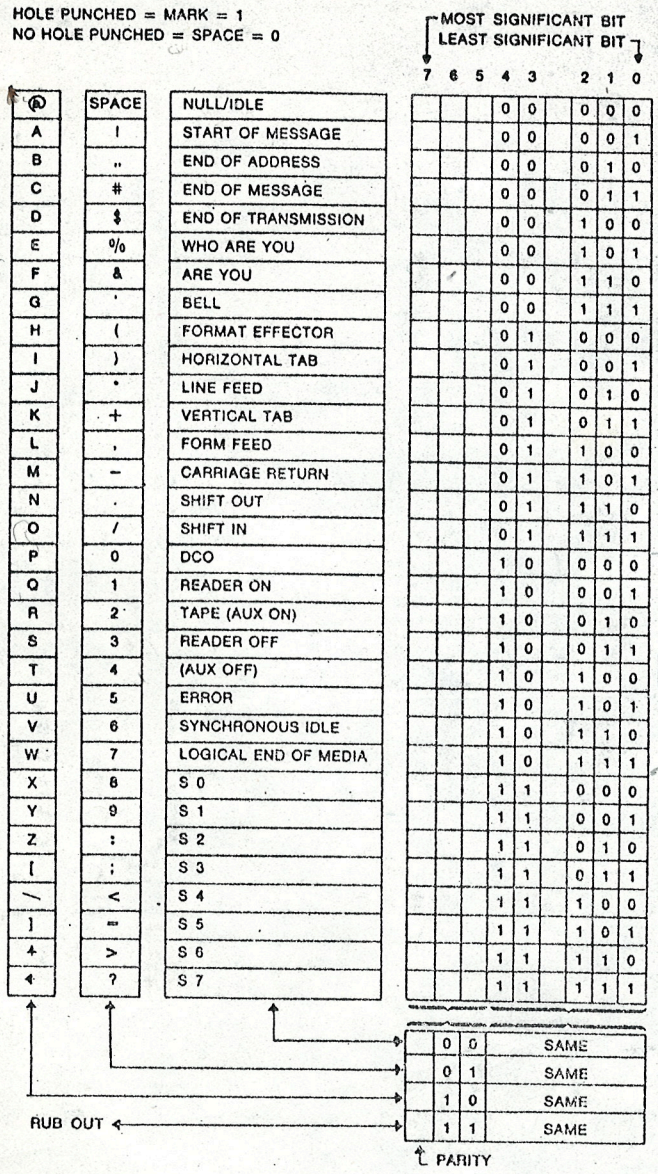
SN54H61/SN74H61(J, N)



SN54H61/SN74H61(W)

APPENDIX C

ASCII Codes



			7	6	5	4	3	2	1	0
@	SPACE	NULL/IDLE				0	0	0	0	0
A	!	START OF MESSAGE				0	0	0	0	1
B	"	END OF ADDRESS				0	0	0	1	0
C	#	END OF MESSAGE				0	0	0	1	1
D	$	END OF TRANSMISSION				0	0	1	0	0
E	%	WHO ARE YOU				0	0	1	0	1
F	&	ARE YOU				0	0	1	1	0
G	'	BELL				0	0	1	1	1
H	(	FORMAT EFFECTOR				0	1	0	0	0
I	)	HORIZONTAL TAB				0	1	0	0	1
J	*	LINE FEED				0	1	0	1	0
K	+	VERTICAL TAB				0	1	0	1	1
L	,	FORM FEED				0	1	1	0	0
M	-	CARRIAGE RETURN				0	1	1	0	1
N	.	SHIFT OUT				0	1	1	1	0
O	/	SHIFT IN				0	1	1	1	1
P	0	DCO				1	0	0	0	0
Q	1	READER ON				1	0	0	0	1
R	2	TAPE (AUX ON)				1	0	0	1	0
S	3	READER OFF				1	0	0	1	1
T	4	(AUX OFF)				1	0	1	0	0
U	5	ERROR				1	0	1	0	1
V	6	SYNCHRONOUS IDLE				1	0	1	1	0
W	7	LOGICAL END OF MEDIA				1	0	1	1	1
X	8	S 0				1	1	0	0	0
Y	9	S 1				1	1	0	0	1
Z	:	S 2				1	1	0	1	0
[	;	S 3				1	1	0	1	1
\	<	S 4				1	1	1	0	0
]	=	S 5				1	1	1	0	1
↑	>	S 6				1	1	1	1	0
←	?	S 7				1	1	1	1	1

0	0	SAME
0	1	SAME
1	0	SAME
1	1	SAME

description (continued)

ALU Signal Designations

The '181, 'LS181, and 'S181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

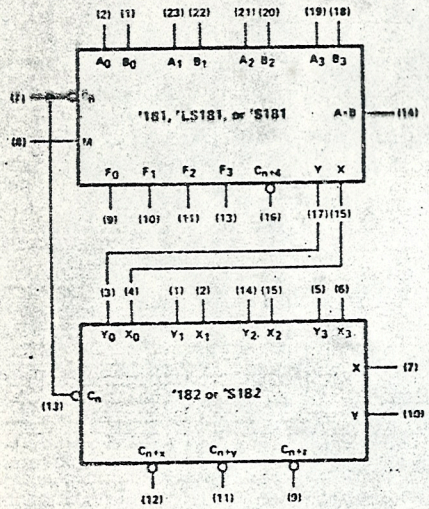


FIGURE 1
(FOR TABLE 1)

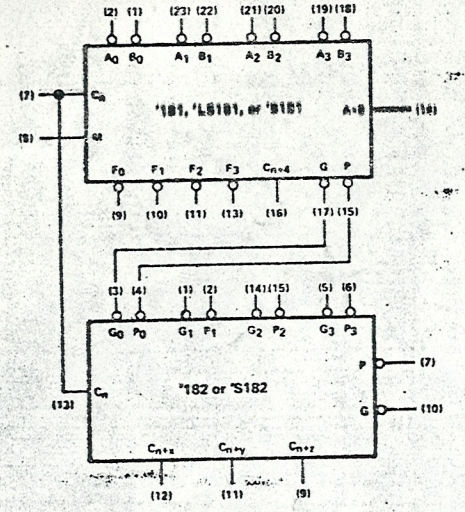


FIGURE 2
(FOR TABLE 2)

TABLE 1

SELECTION	ACTIVE HIGH DATA		
	M = H	M = L, ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $A\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE 2

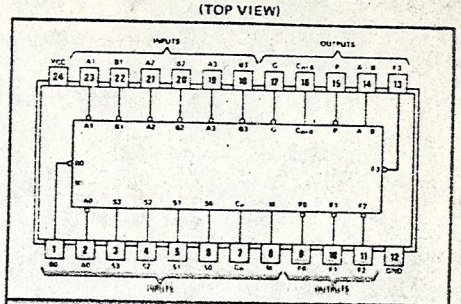
SELECTION	ACTIVE LOW DATA		
	M = H	M = L, ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = A $\oplus$ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + B) PLUS 1
H L L L	F = $\overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A $\oplus$ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

'181, 'LS181 . . . J, N, OR W PACKAGE
SN54S181 . . . J OR W PACKAGE
SN74S181 . . . J, N, OR W PACKAGE
(TOP VIEW)



logic: see tables 1 and 2

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

TYPICAL ADDITION TIMES

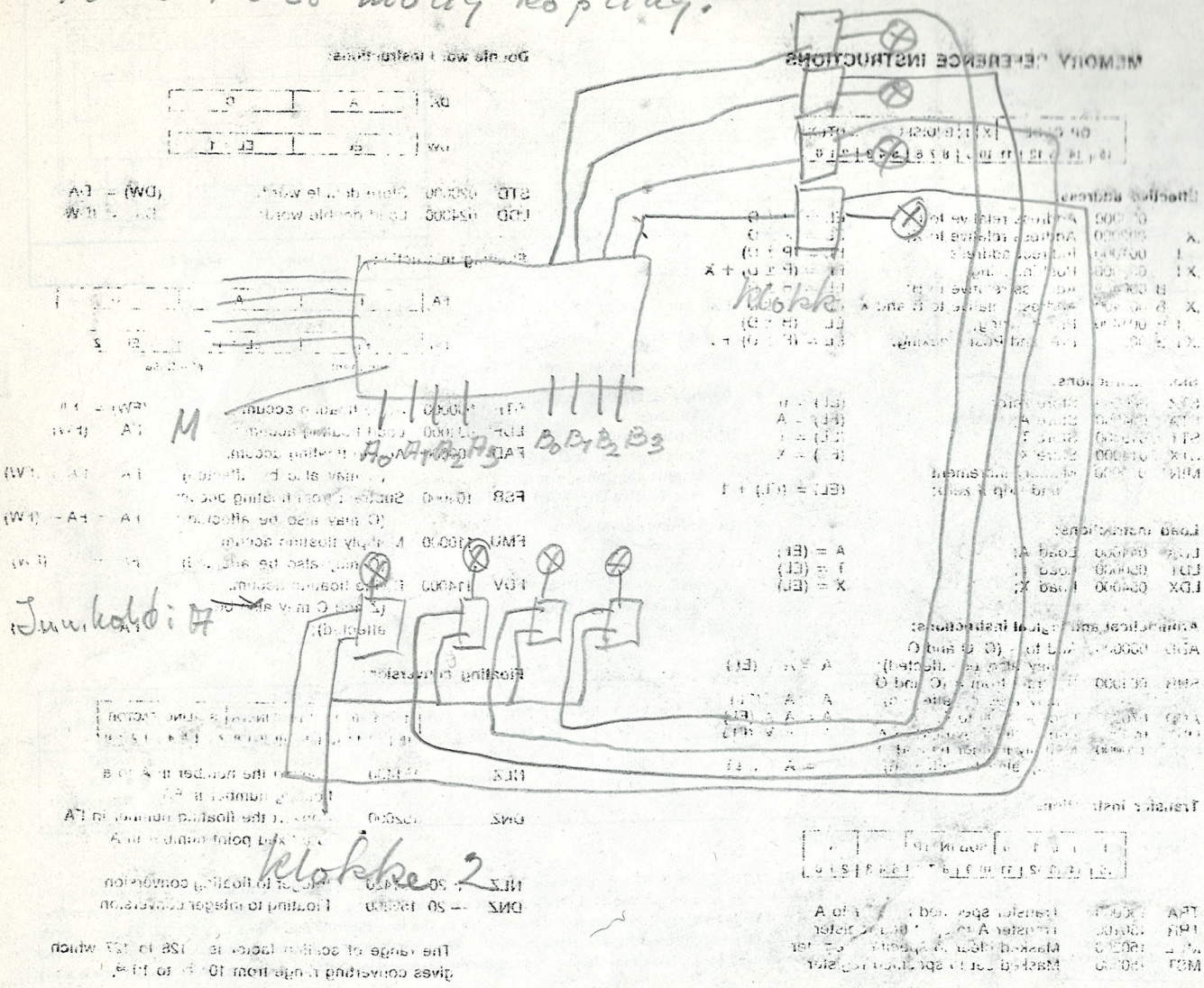
NUMBER OF BITS	ADDITION TIMES			PACKAGE COUNT		CARRY METHOD BETWEEN ALU's
	USING '181 AND '182	USING 'LS181 AND '182	USING 'S181 AND 'S182	ARITHMETIC/ LOGIC UNITS	LOOK-AHEAD CARRY GENERATORS	
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2	1	RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	2 to 5	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16		FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made

1 Sjekker dette bladet om nyttig før du setter spenning på brikken.

2 Tenk ut en måte du kan prøve brikken på i en enklest mulig kopling.



① sett 0101 i B

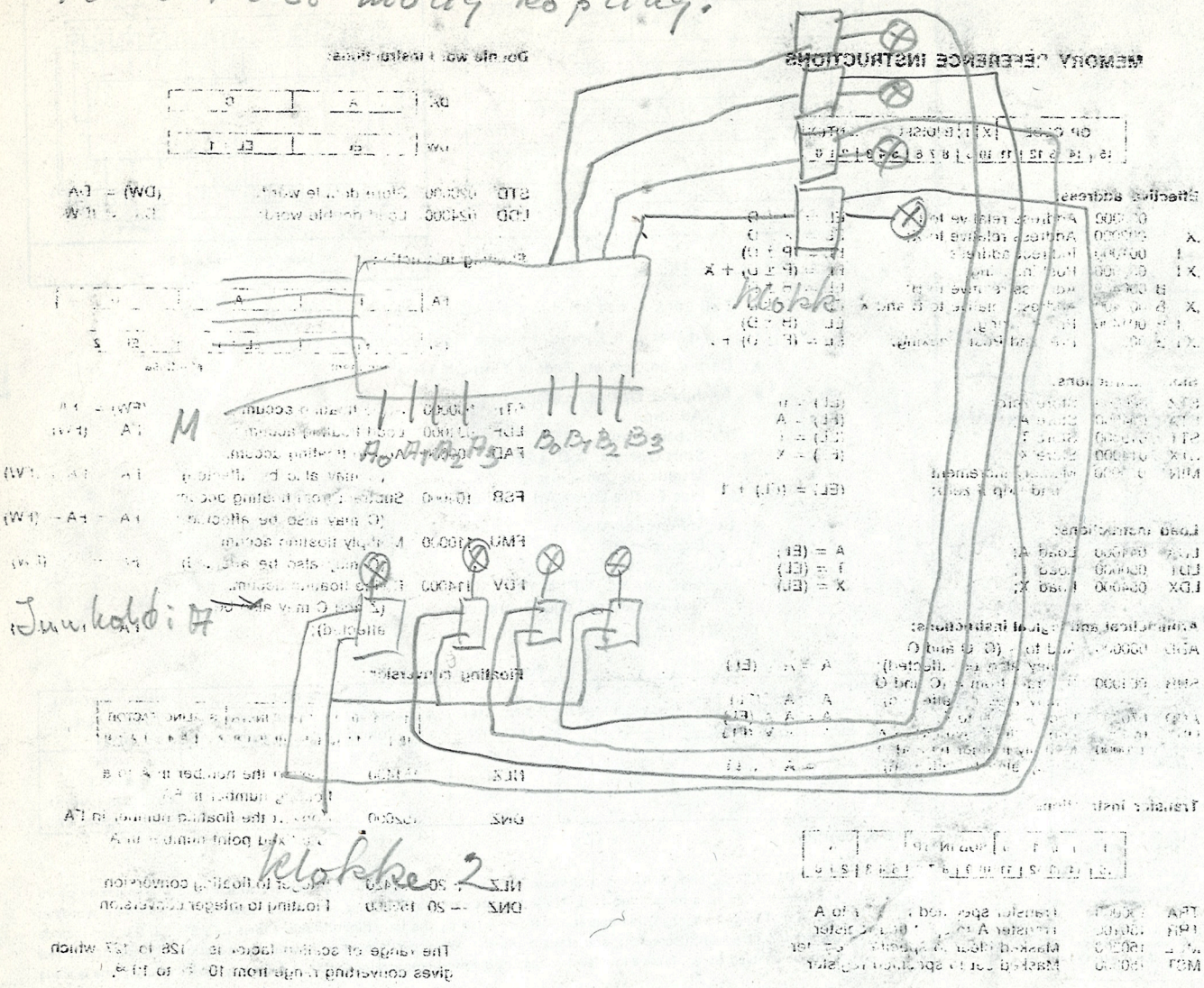
② kjør dette bitet

③ sett 0011 i B

④ Ta logisk AND mellom Reg B og A og få resultatet som ønsket svar.

1 Sjekker da bladet om hensiktsmessig før du setter spenning på brikken.

2 Tenk ut en måte du kan prøve brikken på i en enklest mulig kopling.



① sett 0101 i B

② kjör dette tall til A

③ sett 0011 i B

④ Ta logisk AND mellom Reg B AND B og få resultatet som utslag.

DEFINITION

Registers:

A Accumulator, Main register

D Extension register

T Temporary register

L Link register

X Index register (post-index)

B Base register (pre-index)

P Program counter

STS (F) Status word contains C, Q, O, Z, K, M and PIL

PID Priority interrupt detect register

PIE Priority interrupt enable register

MPR Memory protect register

OPR Operator panel register

Status word:

Bit no.

K 2 One bit accumulator

Z 3 Floating point overflow

Q 4 Dynamic overflow

O 5 Static overflow

C 6 Carry indicator

M 7 Multishift

PIL 8–11 Interrupt level indicator

Abbreviations:

EL Effective location

EW Effective word

DA Double accumulator

FA Floating accumulator

DW Double word

FW Floating word

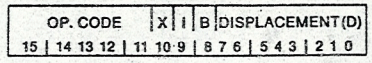
∧ Logical AND

V Logical inclusive OR

⊻ Logical exclusive OR

( ) The content of

MEMORY REFERENCE INSTRUCTIONS



Effective address:

	000000	Address relative to P;	EL = P ± D
,X	002000	Address relative to X;	EL = X ± D
I	001000	Indirect address;	EL = (P ± D)
,X I	003000	Post-indexing;	EL = (P ± D) + X
,B	000400	Address relative to B;	EL = B ± D
,X ,B	002400	Address relative to B and X;	EL = B ± D + X
I ,B	001400	Pre-indexing;	EL = (B ± D)
,X I ,B	003400	Pre- and Post-indexing;	EL = (B ± D) + X

Store instructions:

STZ	000000	Store zero;	(EL) = 0
STA	004000	Store A;	(EL) = A
STT	010000	Store T;	(EL) = T
STX	014000	Store X;	(EL) = X
MIN	040000	Memory increment and skip if zero;	(EL) = (EL) + 1

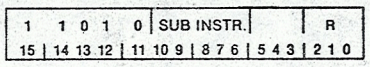
Load instructions:

LDA	044000	Load A;	A = (EL)
LDT	050000	Load T;	T = (EL)
LDX	054000	Load X;	X = (EL)

Arithmetical and logical instructions:

ADD	060000	Add to A (C, O and Q may also be affected);	A = A + (EL)
SUB	064000	Subtract from A (C and Q may also be affected);	A = A − (EL)
AND	070000	Logical AND to A;	A = A ∧ (EL)
ORA	074000	Logical inclusive OR to A;	A = A V (EL)
MPY	120000	Multiply integer (O and Q may also be affected);	A = A * (EL)

Transfer instructions:

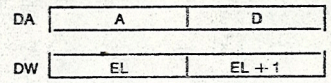


TRA	150000	Transfer specified register to A
TRR	150100	Transfer A to specified register
MCL	150200	Masked clear to specified register
MST	150300	Masked set to specified register

Specify register R:

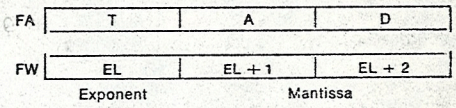
STS	000001	Status word. (PIL will not be affected by any instruction)
OPR	000002	Operator panel register
MPR	000003	Memory protection register
PID	000006	Priority interrupt detect register
PIE	000007	Priority interrupt enable register

Double word instructions:



STD	020000	Store double word;	(DW) = DA
LDD	024000	Load double word;	DA = (DW)

Floating instructions:



STF	030000	Store floating accum.;	(FW) = FA
LDF	034000	Load floating accum.;	FA = (FW)
FAD	100000	Add to floating accum. (C may also be affected);	FA = FA + (FW)
FSB	104000	Subtract from floating accum. (C may also be affected);	FA = FA − (FW)
FMU	110000	Multiply floating accum. (C may also be affected);	FA = FA * (FW)
FDV	114000	Divide floating accum. (Z and C may also be affected);	FA = FA / (FW)

Floating conversion:

NLZ	151400	Convert the number in A to a floating number in FA
DNZ	152000	Convert the floating number in FA to a fixed point number in A
NLZ + 20	151420	Integer to floating conversion
DNZ − 20	152360	Floating to integer conversion

The range of scaling factor is −128 to 127 which gives converting range from 10^{-39} to 10^{39}.

UENCING INSTRUCTIONS

Unconditional jump:

For instruction word format and effective address, see section for memory reference instructions.

JMP	124000	Jump;	P = EL
JPL	134000	Jump to subroutine;	L = P; P = EL

Conditional jump:

1	0 1 1	0	COND.	DISPLACEMENT (D)
15	14 13 12	11	10 9	8 7 6 | 5 4 3 | 2 1 0

JAP	130000	Jump if: A is positive;	P = P ± D if: A ≥ 0
JAN	130400	A is negative;	A < 0
JAZ	131000	A is zero;	A = 0
JAF	131400	A is nonzero;	A ≠ 0
JXN	133400	X is negative;	X < 0
JXZ	133000	X is zero;	X = 0
JPC	132000	Increment X and jump if positive; X = X + 1; P = P ± D if X ≥ 0	
JNC	132400	Increment X and jump if negative; X = X + 1; P = P ± D if X < 0	

SHIFT INSTRUCTIONS

1	1 0 1	1	LIN ZIN	ROT	SAD SHA	SHD	SHIFT COUNTER
15	14 13 12	11	10	9	8	7	6 | 5 4 3 | 2 1 0

SHT	154000	Shift T-register
SHD	154200	Shift D-register
SHA	154400	Shift A-register
SAD	154600	Shift A- and D-register connected
	000000	Arithmetic shift. During right shift bit 15 is extended. During left shift zeros are shifted in from right
ROT	001000	Rotational shift. Most and least significant bits are connected together
ZIN	002000	Zero end input
LIN	003000	Link end input. The last vacated bit is fed to M after every shift instruction
SHR		Shift right; gives negative shift counter

INPUT - OUTPUT CONTROL

1	1 1 0	0	PIN	SKA	ACT	DEVICE NO.
15	14 13 12	11	10	9	8	7 6 | 5 4 3 | 2 1 0

IOT 160000 Operate specified device according to function

Function:

ACT	000400	Activate the specified device
SKA	001000	Skip next instruction if device is ready
PIN	002000	Enable interrupt of specified device
SNI	000000	Skip next instruction if no interrupt

Interrupt control:

1	1 0 1	0	SUB INSTR.		GRP
15	14 13 12	11	10 9	8 7 6 | 5 4 3	2 1 0

ION	150500	Turn on interrupt system
IOF	150400	Turn off interrupt system
INTEN	150540	Enable interrupt
INTDS	150440	Disable interrupt

Specify Group:

GRP1	000001	Group one
GRP2	000002	Group two
GRP3	000004	Group three
GRP4	000010	Group four

Device no. for group one:	Input	Output
Teletype I	RKE; 2	PNT; 3
Teletype II	4	5
Teletype III	10	11
20 mS real time clock	6	
High speed punch		PFA; 7
High speed reader	REA; 22	
Card reader	42	

Halt Instruction:

1	1 0 1	0	SUB INSTR.	WAIT NUMBER
15	14 13 12	11	10 9	8 7 6 | 5 4 3 | 2 1 0

WAIT 151000

I Interrupt off:
Halt the program. The program will continue by depressing continue button.

II Interrupt on:
Give up priority. If there are no interrupt requests on any level, the program on level zero is entered.

It is legal to specify a WAIT NUMBER less than 377.

MODEL 33 ASR/KSR TELETYPE C E (ASCII) IN BINARY FORM

HOLE PUNCHED = MARK = 1
NO HOLE PUNCHED = SPACE = 0

MOST SIGNIFICANT BIT
LEAST SIGNIFICANT BIT

			7	6	5	4	3	2	1	0
@	SPACE	NULL/IDLE				0	0	0	0	0
A	!	START OF MESSAGE				0	0	0	0	1
B	"	END OF ADDRESS				0	0	0	1	0
C	#	END OF MESSAGE				0	0	0	1	1
D	$	END OF TRANSMISSION				0	0	1	0	0
E	%	WHO ARE YOU				0	0	1	0	1
F	&	ARE YOU				0	0	1	1	0
G	'	BELL				0	0	1	1	1
H	(	FORMAT EFFECTOR				0	1	0	0	0
I	)	HORIZONTAL TAB				0	1	0	0	1
J	*	LINE FEED				0	1	0	1	0
K	+	VERTICAL TAB				0	1	0	1	1
L	,	FORM FEED				0	1	1	0	0
M	-	CARRIAGE RETURN				0	1	1	0	1
N	.	SHIFT OUT				0	1	1	1	0
O	/	SHIFT IN				0	1	1	1	1
P	0	DCO				1	0	0	0	0
Q	1	READER ON				1	0	0	0	1
R	2	TAPE (AUX ON)				1	0	0	1	0
S	3	READER OFF				1	0	0	1	1
T	4	(AUX OFF)				1	0	1	0	0
U	5	ERROR				1	0	1	0	1
V	6	SYNCHRONOUS IDLE				1	0	1	1	0
W	7	LOGICAL END OF MEDIA				1	0	1	1	1
X	8	S 0				1	1	0	0	0
Y	9	S 1				1	1	0	0	1
Z	:	S 2				1	1	0	1	0
[	;	S 3				1	1	0	1	1
\	<	S 4				1	1	1	0	0
]	=	S 5				1	1	1	0	1
↑	>	S 6				1	1	1	1	0
←	?	S 7				1	1	1	1	1

	0 0	SAME
	0 1	SAME
	1 0	SAME
	1 1	SAME

RUB OUT

PARITY

GISTER OPERATION

1	1 0 0	1	RAD	C	I	CM1	CLD	SOURCE	DESTIN.
15	14 13 12	11	10	9	8	7	6	5 4 3	2 1 0

Arithmetic operations, RAD 1:

C, O and Q may be affected by following instructions

RADD	146000	Add source to destination;	(D) = (D) + (S)
RSUB	146600	Subtract source from destination;	(D) = (D) — (S)
COPY	146100	Register transfer;	(D) = (S)
AD1	000400	Also add one to destination;	(D) = (D) + 1
ADC	001000	Also add old carry to destination;	(D) = (D) + C

Logical operations, RAD = 0:

SWAP	141000	Register exchange;	(S) = (D); (D) = (S)
RAND	144400	Logical AND to destination;	(D) = (D) ∧ (S)
REXO	145000	Logical exclusive OR;	(D) = (D) ∨ (S)
RORA	145400	Logical inclusive OR;	(D) = (D) V (S)
CLD	000100	Clear destination before op.;	(D) = 0
CM1	000200	Use one's complement of source;	(S) = (S)o

Combined instructions:

EXIT	146142	= COPY SL DP,	Return from subroutine
RCLR	146100	= COPY.	Register clear
RINC	146400	= RADD AD1,	Register increment
RDCR	146200	= RADD CM1,	Register decrement
SMIL	146302	= COPY CM1 DP,	Starting address of MAC

Specify source register S:

SD	000010	D-register as source
SP	000020	P-register as source
SB	000030	B-register as source
SL	000040	L-register as source
SA	000050	A-register as source
ST	000060	T-register as source
SX	000070	X-register as source
	000000	Source value equals zero

Specify destination register D:

DD	000001	D-register as destination
DP	000002	P-register as destination
DB	000003	B-register as destination
DL	000004	L-register as destination
DA	000005	A-register as destination
DT	000006	T-register as destination
DX	000007	X-register as destination
	000000	No operation

BIT OPERATION INSTRUCTIONS

1	1 1 1	1	FUNCTION	BIT NO.	DESTIN.
15	14 13 12	11	10 9 8 7 6	5 4 3	2 1 0

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Operation instruction:

BSKP	175000	Skip next location if specified condition is true;	P = P+1
BSET	174000	Set specified bit equal to specified condition.	
BSTA	176200	Store and clear K;	(B) = K; K = 0
BSTC	176000	Store complement and set K;	(B) = K_o ; K = 1
BLDA	176600	Load K;	K = (B)
BLDC	176400	Load bit complement to K;	K = $(B)_o$
BANC	177000	Logical AND with bit complement;	K = K ∧ (B)o
BORC	177400	Logical OR with bit complement;	K = K V (B)o
BAND	177200	Logical AND to K;	K = K ∧ (B)
BORA	177600	Logical OR to K;	K = K V (B)

Specify condition:

ZRO	000000	Specified bit equals zero;	(B) = 0
ONE	000200	one;	(B) = 1
BAC	000600	K;	(B) = K
BCM	000400	Complement specified bit;	(B) = $(B)_o$

Specify bit no:

0	000000	Specifies bit in dest. reg.;	B = 0
10	000010		B = 1
20	000020		B = 2
⋮	⋮		⋮
170	000170		B = 15

For destination (D) mnemonics see section for register operations. D = 0 specifies STS-register.

Specify control flip-flop:

SSK	000020	Specifies; one bit accum.;	B = K
SSZ	000030	floating point ov.fl.;	B = Z
SSQ	000040	dynamic ov.fl.;	B = Q
SSO	000050	static ov.fl.;	B = O
SSC	000060	carry;	B = C
SSM	000070	multishift link;	B = M

SKIP INSTRUCTIONS

1	1 0 0	0	COND.		SOURCE(S)	DESTIN. (D)	
15	14 13 12	11	10 9	8 7 6	5 4 3	2 1 0	4 2 1

SKP	140000	Skip next location if specified condition is true; P = P + 1

Specified condition:

EQL	000000	Equal to
UEQ	002000	Unequal to
GRE	001000	Greater or equal to
LST	003000	Less than
IF	000000	May be used freely to obtain
0	000000	easy readability

For Source and Destination mnemonics see section for Register operations.
The destination register (D) should be specified before the source register (S).

ARGUMENT INSTRUCTION

1	1 1 1	0	FUNCT.	ARGUMENT		
15	14 13 12	11	10 9	8 7 6	5 4 3	2 1 0

Function:

SAA	170400	Set argument to A;	A = ARG
AAA	172400	Add argument to A;	A = A + ARG
SAX	171400	Set argument to X;	X = ARG
AAX	173400	Add argument to X;	X = X + ARG
SAT	171000	Set argument to T;	T = ARG
AAT	173000	Add argument to T;	T = T + ARG
SAB	170000	Set argument to B;	B = ARG
AAB	172000	Add argument to B;	B = B + ARG

Argument is a signed number ranging from −128 to +127.

MAC COMMANDS

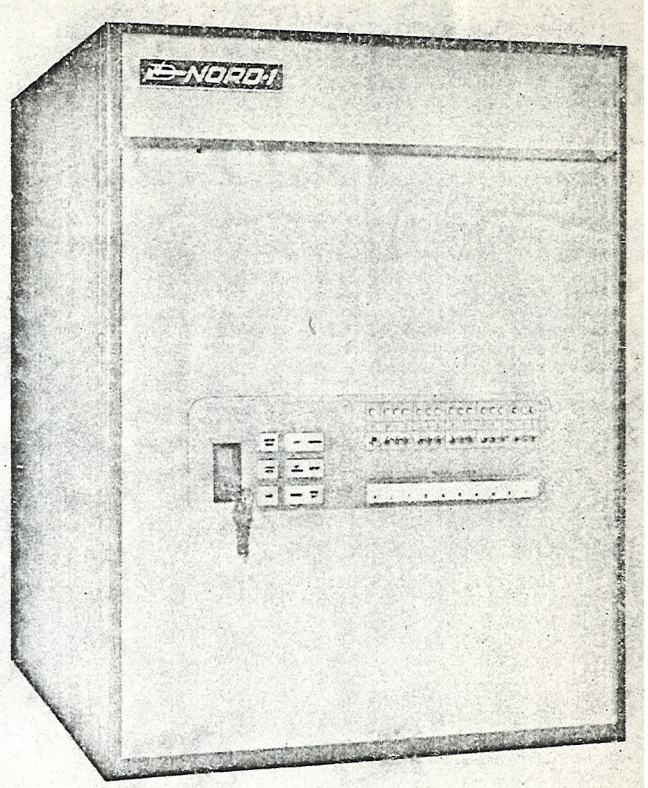
:	Following immediately after a symbol causes the value of the last symbol to be printed out
:	Following after a space or an octal number causes the value of the whole expression to be printed out
"	Set MAC in library mode
#	Form a 16 bit number equal to the 8 bit teletype codes of the following two characters
# #	Form a 16 bit number where bits 0–7 are equal to the following 8 bit teletype code. Bits 8–15 equal zero
# # # #	Form a 32 bit word containing up to 5 letters
%	Demarcation between instruction and comment
)LINE @	Set MAC in on-line mode
)TAPE $	Set MAC in off-line mode
!	Start execution of assembled program. The starting address must precede the command
◂	Preceded by a symbol, will delete the reference to this symbol in the symbol table. If no reference is found, symbol in the US-table is deleted
)WRUS ?	Write undefined symbols
)FILL &	The value of expressions following a (, will automatically be stored in locations following current location
)CLEAR	Reset MAC tables
)PUNCH	Punch the content of the locations between lower and upper boundary, defined by two numbers, separated by the character <. Output on high speed punch
)PRINT	Same as)PUNCH, but output is on teletype
)BPUN	Binary dump of locations between lower and upper boundary must be followed by a symbol specifying the starting address. The program will automatically start after it has been read in
)ZERO	Clear locations between lower and upper boundary

)WMNE	Write the mnemonics allowed in MAC
)WLOC	Write the symbols in symbol table
)OUTM	Set MAC to outmode
)INMO	Set MAC to inmode
)WRITE	Followed by a string of symbols on the same line will cause the symbols and their octal values to be printed out during assembly-time, when in write mode
)NWRT	Reset the)WRTM command
)WRTM	Set MAC to write mode
)KILL	Followed by a string of symbols on the same line will delete the corresponding references in the symbol table. If a symbol is undefined, the last reference in the US-table is deleted
)PCL	Followed by a symbol, will cause all symbol references after this reference to be deleted
)DEC	Set MAC to decimal mode
)OCT	Set MAC to octal mode
)CORE	Print upper and lower boundary of available core
)LIST	List all defined symbols and their values
)CHANGE	Change all instructions or part of instruction between lower and upper boundary in this way: OLD / Old content NEW / New content MASK / Ones in bits to be changed a < b ; upper and lower boundary)CHANGE Only masked bits will be searched for and changed

BREAKPOINT

. .	Set breakpoint in location specified before this command
!	Start execution in location specified before this command
1 !	Step one forward in program sequence
0 !	Continue without more breakpoints
)RBP	Reset breakpoint

REFERENCE DATA:



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