TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
	OPERATOR PANEL
START switch	Energizes (when pressed to light) spindle drive motor and begins First Seek sequence provided the following conditions are met: 1. Disk Pack is in place and canister removed. 2. Pack cover is closed. 3. Circuit breakers are on. Causes a power off sequence (when pressed to extinguish).
START indicator	Lights when switch is on.
FAULT switch	Clears the fault circuitry and extinguishes the FAULT indicator. (Does not clear Maintenance Fault register.)
UNIT MAINTENANCE switch	Prevents drive from activating Unit Selected signal, thus preventing the controller from selecting drive. This switch should not be used during normal on line operation.
FAULT indicator	Lights in response to one or more of the following conditions: 1. Read and write are selected at the same time. 2. No ac write current when Write Gate is present. 3. More than one head is selected. 4. Read or Write is selected while off cylinder. 5. Low voltage condition sensed for ±5v, ±20v, ±42v. 6. Loss of dibit signal for 350 ms with heads loaded.
LOGIC PLUG	Completes circuitry to permit selection of the unit through a binary code. CAUTION Unit select logic plug should not be changed or removed unless unit is shut off with heads unloaded.
READY indicator	Lights when the unit is up to speed, the heads are loaded, and no fault condition exists.
	REAR PANEL
AC POWER circuit breaker	Controls application of ac power.
POWER SUPPLY circuit breaker	Controls application of dc power to the logic chassis.
Elapsed Time Meter	Active when ac power and dc power are applied by circuit breakers. Records accumulated ac power-on time.

TABLE 2-1. CONTROLS AND INDICATORS (Cont'd)

MAINTENANCE PANEL (BACK OF OP PNL)	
Control or Indicator	Function
WRITE FAULT indicator	Indicates a write was attempted and no ac write current and/or dc current was sensed.
HEAD SELECT FAULT indicator	Indicates more than one head selected.
W.R. FAULT indicator	Read or write were selected at same time.
ON CYLINDER FAULT indicator	Read or write was selected while off cylinder.
VOLTAGE FAULT indicator	Low voltage condition existed for ±5v, ±20v, ±42v.

3. Disengage bottom dust cover from disk pack by turning canister handle counterclockwise. Set cover aside in an uncontaminated area.

CAUTION

Avoid abusive contact between the disk pack and the spindle. The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place disk pack onto spindle.

NOTE

A spindle lock mechanism is actuated when the disk pack canister cover is on the spindle. The mechanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist canister handle clockwise to lock disk pack in place.

NOTE

A click may be heard as the spindle lock mechanism engages.

6. Lift canister clear of disk pack, place bottom dust cover on canister, and set aside in an uncontaminated area.

7. Close pack access immediately to prevent entry of dust and contamination of disk surfaces.

DISK PACK REMOVAL

1. Press operator panel START switch to extinguish the START indicator.
2. Check that disk pack rotation has stopped. (Stopping time is approximately 1.5 minutes without brake and 20 seconds with brake.)
3. Raise front cover.

CAUTION

The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place plastic canister over mounted disk pack so that post protruding from center of disk pack is received into canister handle.
5. Twist canister handle counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly.

6. Lift canister and disk pack clear of spindle.
7. Close front cover.
8. Place bottom dust cover in position on disk pack and lock it.

FIELD TEST EXERCISER

The Field Test Exerciser permits full control of the drive seek and read/write logic without computer intervention. Refer to the Field Test Exerciser manual for a complete description of operation.

Description

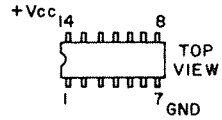
The 149 circuit is a quad 2-input Exclusive OR gate that performs the function $Y=A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the high level.

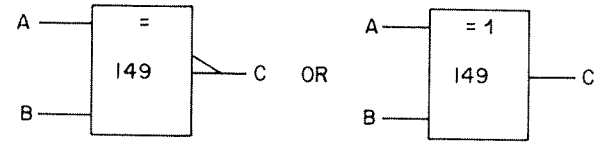
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

Element	Vendor Number
149	7486
149H	3021
149L	74L86
149LS	74LS86
149S	74S86

3. Package pin configuration.

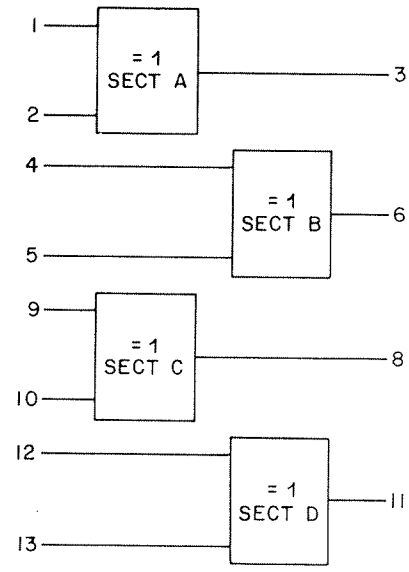




LOGIC SYMBOL

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

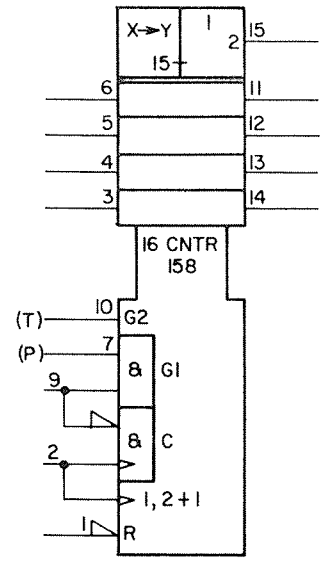
149
Rev B
Sheet 1 of 1

Description

The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.

In order for the counter to count, the load (pin 9), clear (R), and P and T enable inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

When P is low, the clock input is disabled so that the counter can not count. When T is low, the clock input and carry output are both disabled.



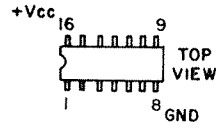
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
158	74161,9316
158A	74161
158LS	74LS161

2. Package pin configuration.



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Rev B
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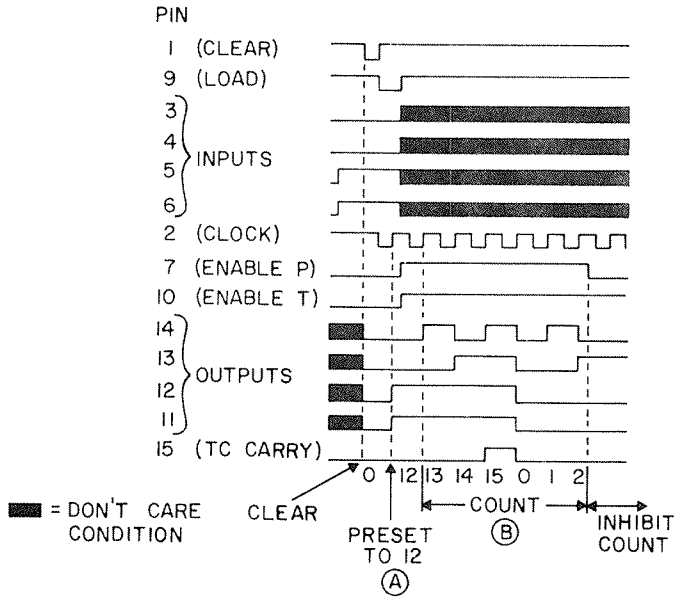


NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

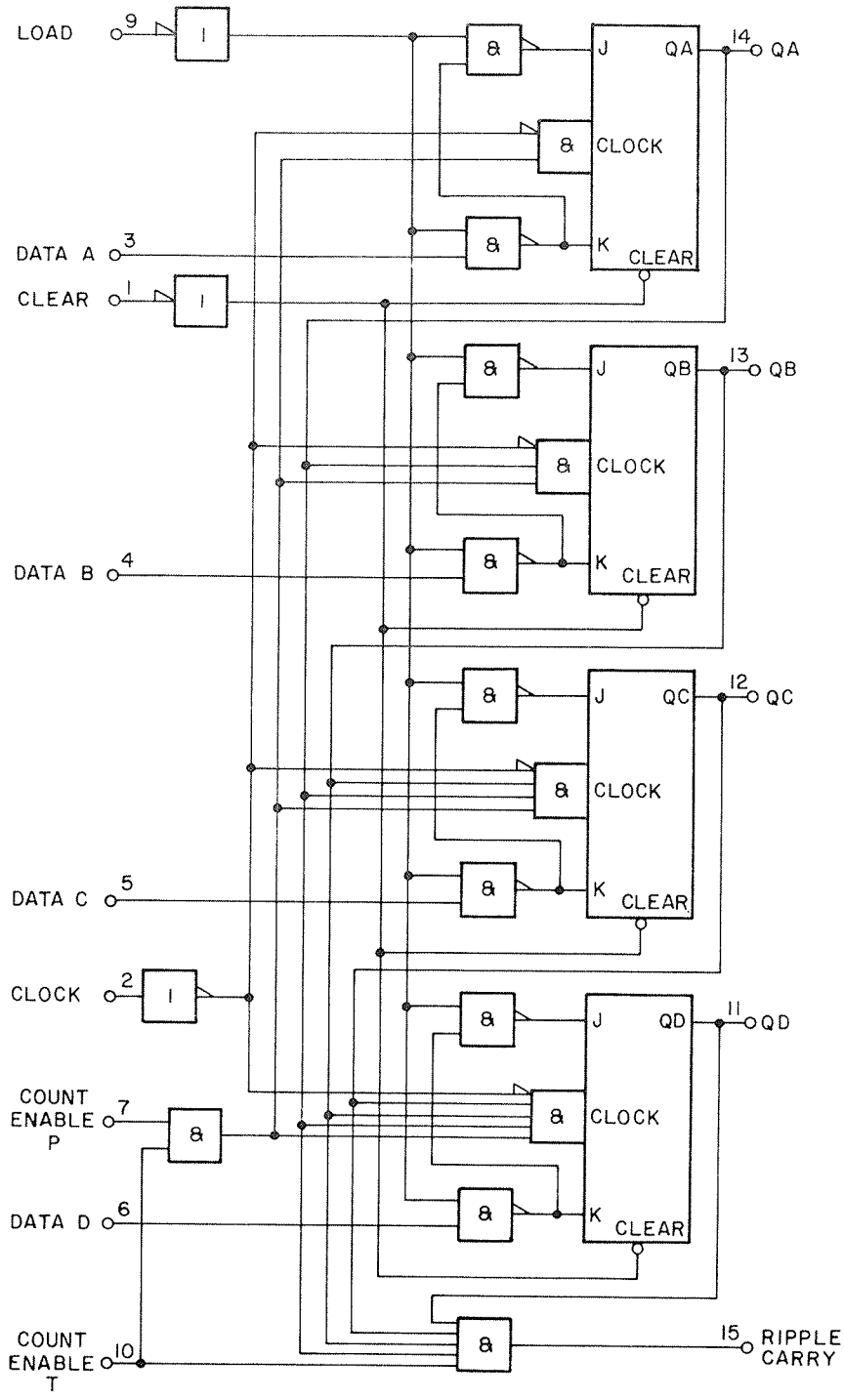
Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE

158
Rev B
Sheet 2 of 3



FUNCTION DIAGRAM

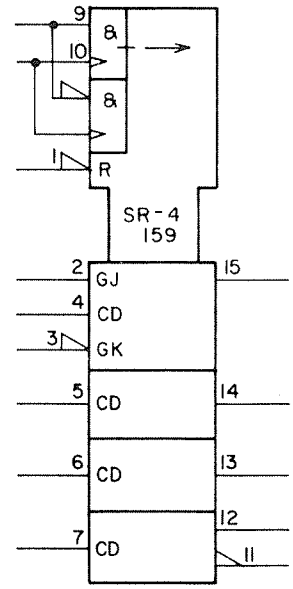
158
Rev B
Sheet 3 of 3

Description

The 159 circuit is a synchronous 4-bit shift register capable of shifting, counting, storage, and serial code conversion.

Data entry is synchronous; the outputs change state after each low to high transition of the clock. When the load/shift input is low, the parallel inputs determine the next condition of the shift register. When the load/shift input is high, the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through the J-K (serial) inputs. By tying the J and K inputs together, D-type entry is obtained.

A low level to the clear input will clear the outputs to a low level regardless of the levels to any input.



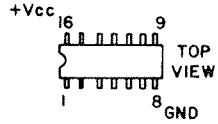
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
159	74195,9300
159LS	74LS195

2. Package pin configuration.



Pin	Function
1	Master Reset (clear)
2	First stage J input
3	First stage K input
4,5,6,7	Parallel data inputs
9	Load/Shift control
10	Clock
12,13,14,15	Parallel outputs
11	Complementary output ($\overline{12}$) for last stage

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Rev B
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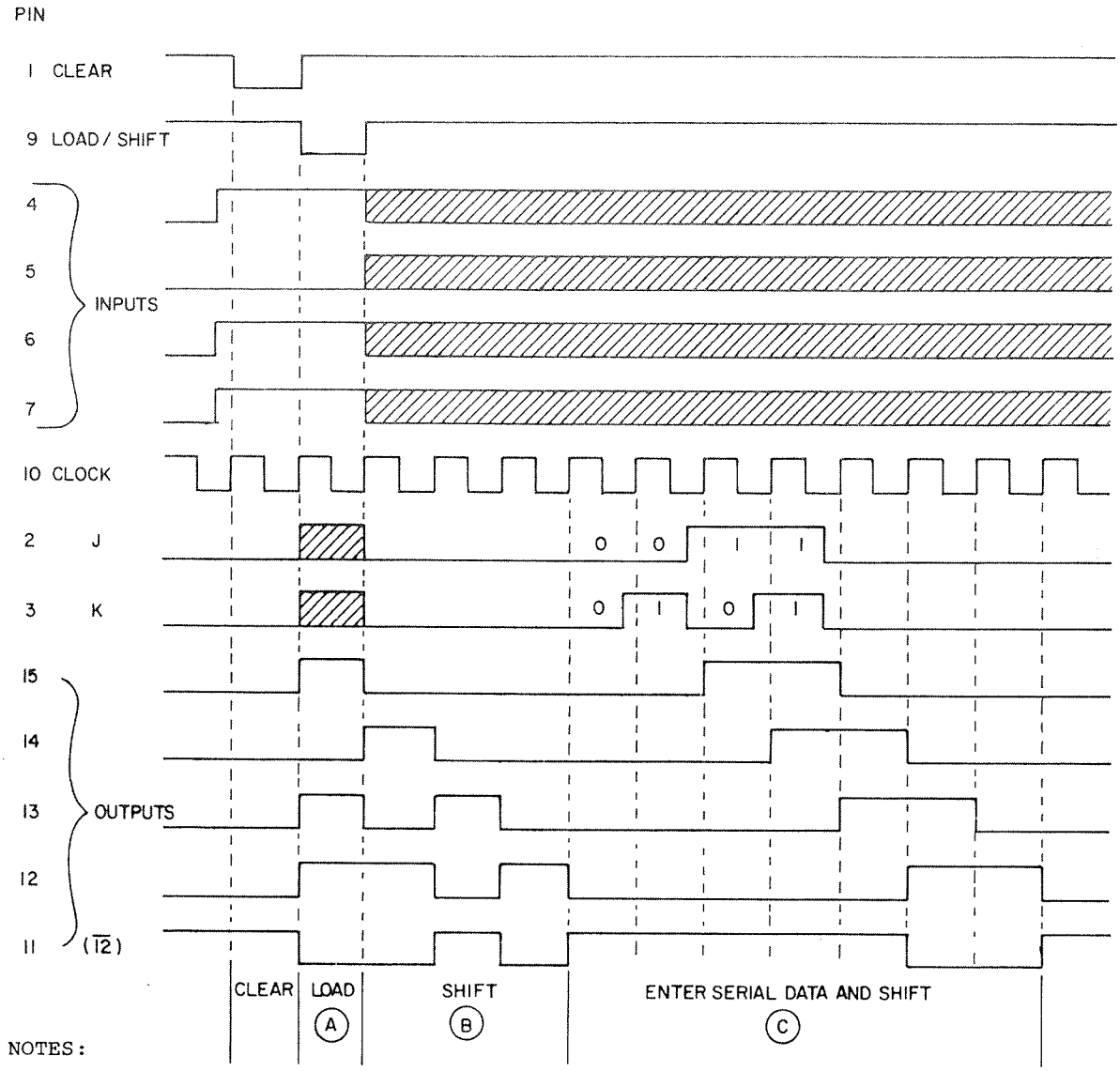


NOTES:

(A) Parallel data entered via CD inputs by pin 9 low and positive-going signal on pin 10.

(B) Data shifts down (Pin 15→Pin 14, etc.) with clock.

(C) Serial data entered into J-K inputs by pin 9 high and positive-going clock. Pin 4 input inhibited because pin 9 is high. Outputs follow Truth Table shown below. (Were J and K tied together, output at pin 15 would track the J input with no deviation from the Truth Table.)

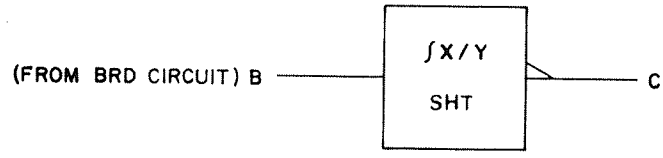
INPUT PINS		OUTPUT PIN
2	3	15
0	0	0
0	1	0(NO CHANGE)
1	0	1(TOGGLES)
1	1	1

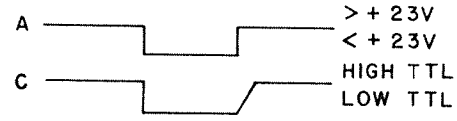
159
Rev B
Sheet 2 of 3

LEVEL TRANSLATOR (OUTPUT SECTION) - SHT

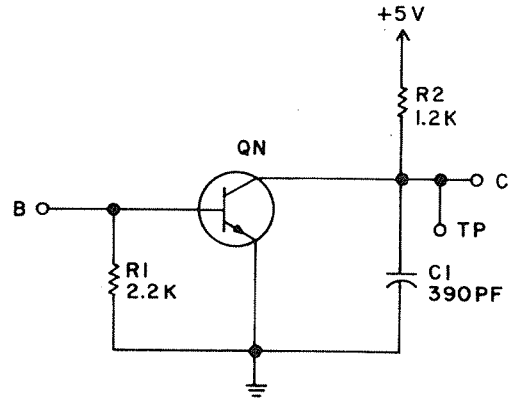
The SHT circuit provides a TTL compatible output for the comparator section of a level translator.

The SHT circuit functions in conjunction with the BRD circuit to indicate whether or not the write current is below a minimum value. (See BRD circuit description.) The output of the BRD circuit provides bias for transistor QN to turn it on or off. When the write current falls below +23V, QN is turned on to provide a low level TTL output. When the write current is above +23V, QN is turned off to provide a high level TTL output.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



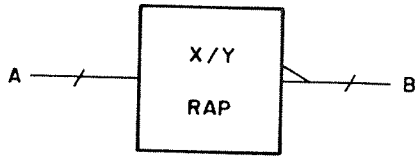
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

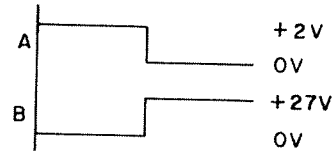
SHT
Rev B
Sheet 1 of 1

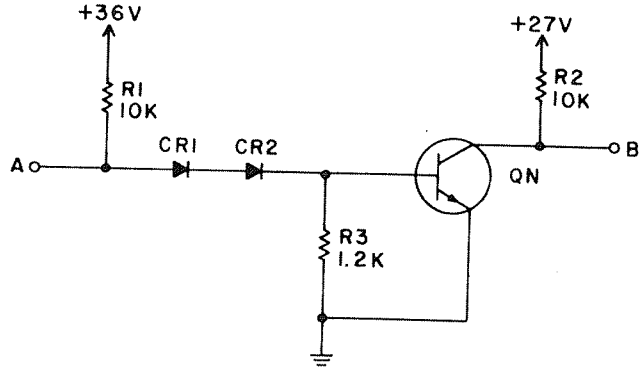
WRITE PROTECT CLAMP - RAP

The RAP circuit acts as a clamp, changing its output impedance path from high to low when the input is switched high.

When the input at A is low (TTL) Q1 is turned off, and the impedance from B to ground is high. When A is switched high (TTL) Q1 is turned on, providing a low impedance path between output B and ground for the write current.





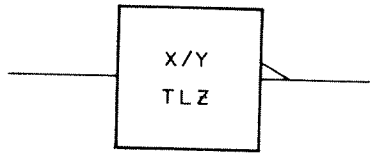


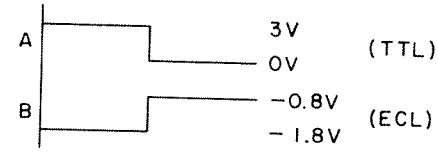
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

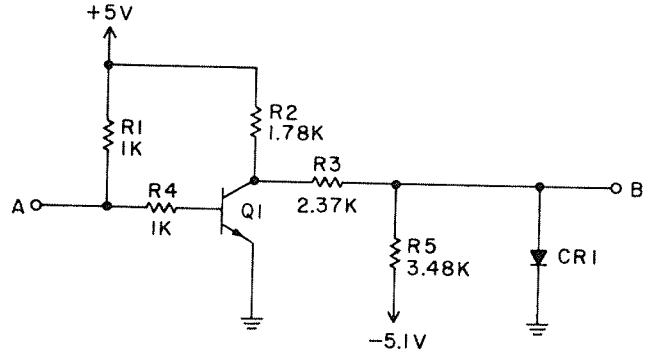
RAP
Rev B
Sheet 1 of 1

INVERTING TRANSLATOR (TTL TO ECL) - TLZ

The first part, consisting of R_1, R_4 and Q_1 form a simple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

TLZ
Rev A
Sheet 1 of 1

DELAY - UB-

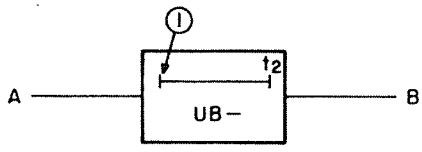
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

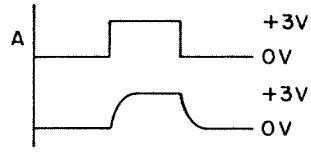
Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

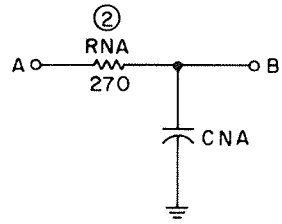
If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time	CNA	RNA
UBR	40 NS	2200 PF	None
UBS	25 NS	680 PF	None







NOTES:

① COMPONENT VALUES VARY.

② USED ON UBR AND UBS ONLY.

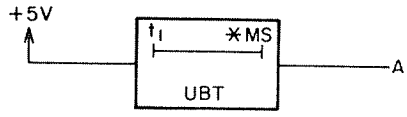
3 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

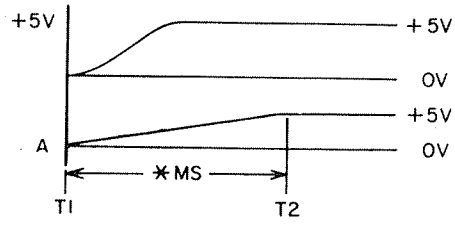
UB-
Rev A
Sheet 1 of 1

DELAY - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

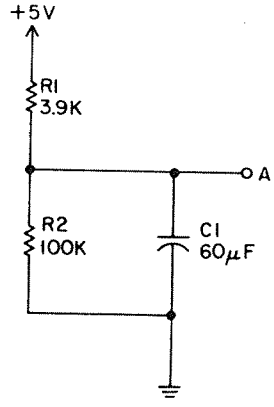
Applying +5v (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UBT
Rev A
Sheet 1 of 1

DELAY - UC-

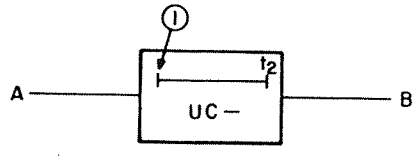
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

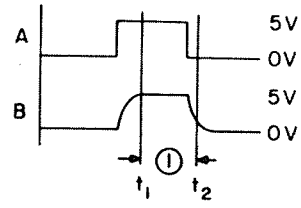
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

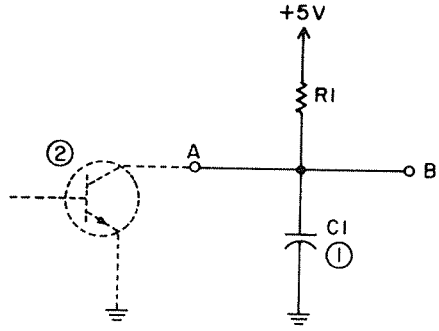
If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS







NOTES:

① DELAY TIME DEPENDENT ON CIRCUIT TYPE.

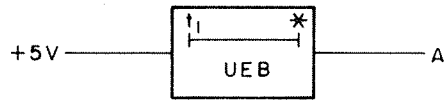
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

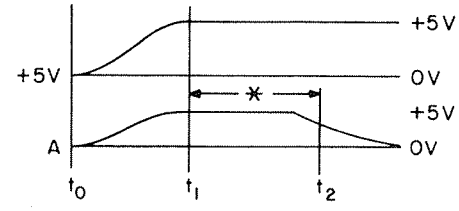
UC-
Rev B
Sheet 1 of 1

DELAY - UEB

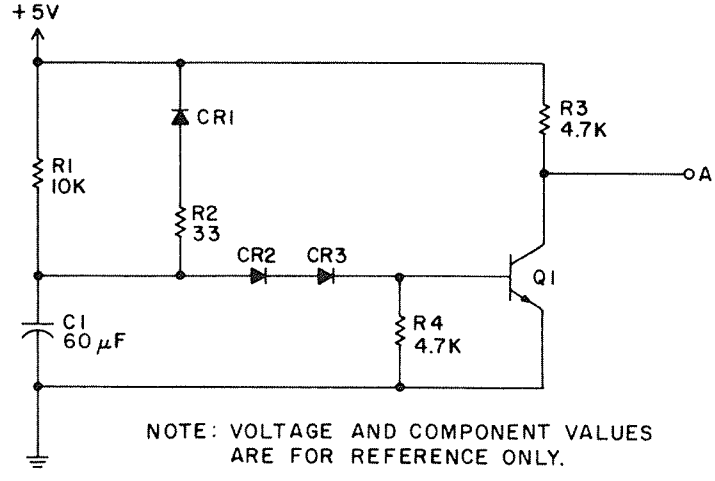
The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharged by R4, CR2, and CR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.





* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UEB
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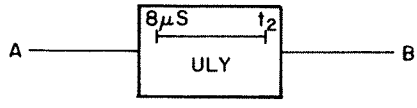
Sheet 1 of 1

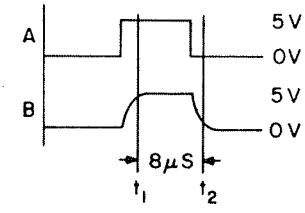
DELAY - ULY

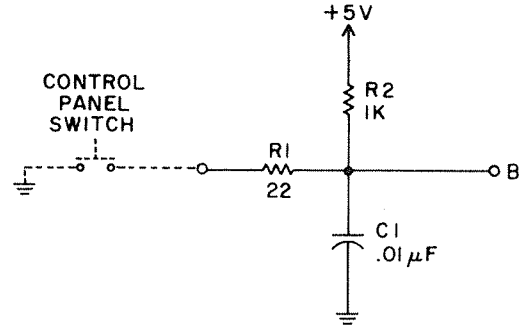
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.







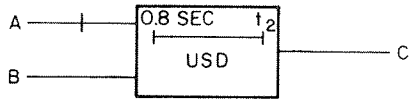
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

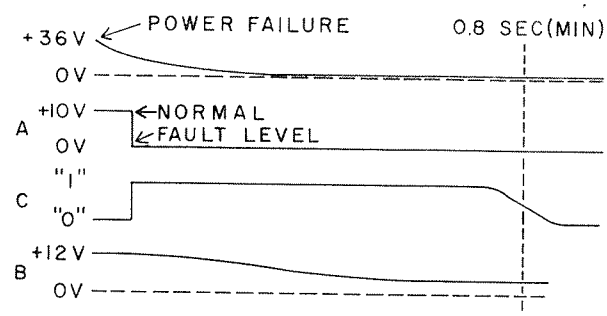
ULY
Rev A
Sheet 1 of 1

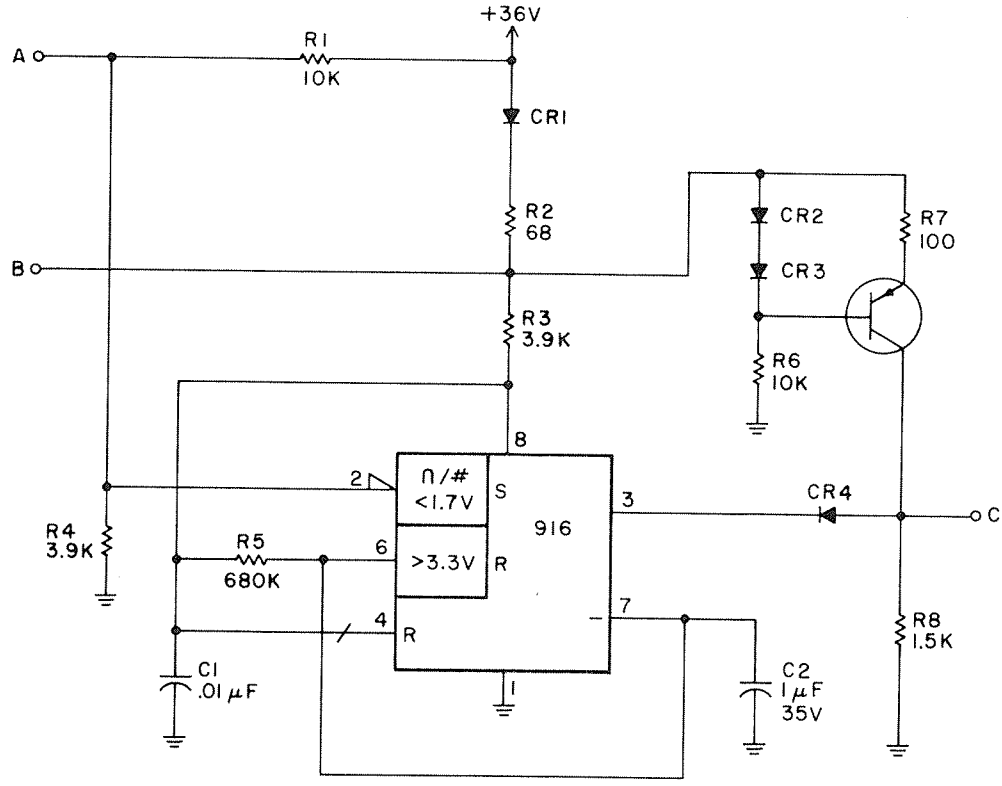
DELAY - USD

The USD circuit maintains a TTL high level output for 0.8 sec during the time that the power supply voltage is dropping.

The USD circuit functions as the delay portion of a write fault clamp circuit which prevents write current from reaching the head during a +36 V supply voltage fault condition. The switching action of transistor QN is initiated by the fault trigger at input A. QN is turned on when input A goes to 0 V, causing output C to go high. Resistor R5 and capacitor C2 provide the time-out constant to keep output C high for 0.8 sec. Stored energy is supplied at input B to maintain QN in the on state for the 0.8 sec duration. The high output at C is used to switch on a write clamp circuit.







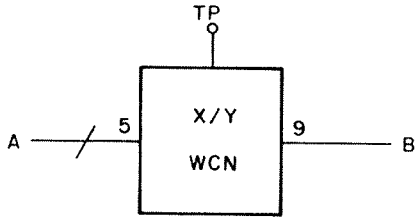
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

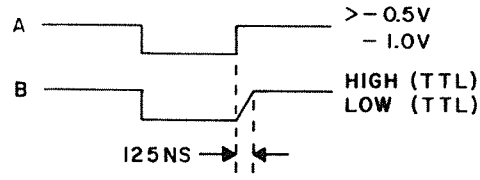
USD
Rev B
Sheet 1 of 1

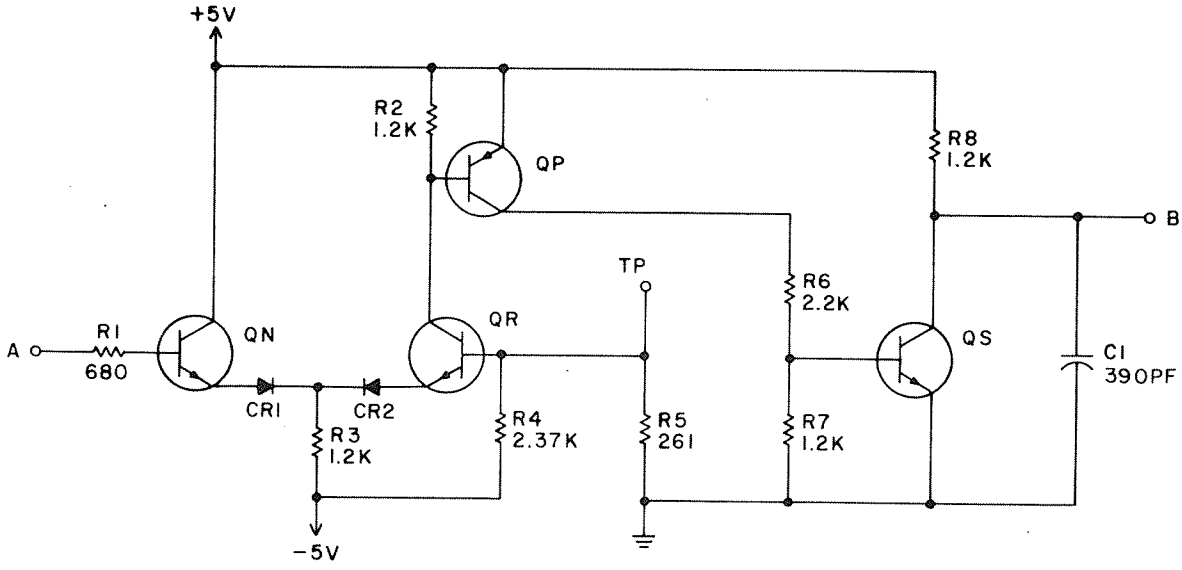
LEVEL TRANSLATOR - WCN

The WCN circuit translates input signal levels of below -0.5 V to a low TTL level output and input signal levels of above -0.5 V to a high TTL level output.

The WCN circuit has a differential voltage comparator circuit to indicate whether the write driver is on or off. A voltage reference of -0.5 V is applied to the base of transistor QR. When the write driver is off, the voltage at the base of transistor QN is -1 V, turning off QN. Therefore, transistor QR is turned on and its collector voltage goes low, turning on transistor QP. Transistor QS is then forward biased providing a low TTL output. If the write driver is on, the voltage to the base of QN goes above -0.5 V (less negative) and QN is turned on. As a result QR, QP, and QS are turned off, providing a high TTL output. Capacitor C1 delays the low to high transition by 125 ns.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

WCN
Rev B
Sheet 1 of 1

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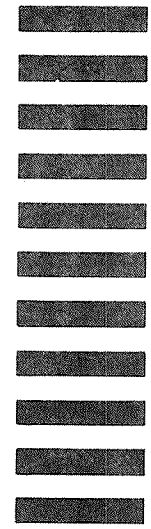

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