83308500

CONTROL DATA CORPORATION

CONTROL DATA®
STORAGE MODULE DRIVE
BJ7XX

GENERAL DESCRIPTION
OPERATION
THEORY OF OPERATION
KEY TO LOGIC
INTEGRATED CIRCUITS
DISCRETE COMPONENT CIRCUITS

HARDWARE REFERENCE MANUAL

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REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(1-15-75)	
B	Update with Engineering Change Order 37725A. Technical and editorial changes.
(3-4-76)	
C	Update with Engineering Change Orders 37825A. Editorial changes.
(6-17-76)	
D	Manual rewrite. Technical and editorial changes. This edition obsoletes all
(9-30-76)	previous editions.
E	Update manual with technical and editorial changes.
(3-29-77)	
F	Update with Engineering change order 55290 and additional technical and
(12-18-78)	editorial changes.
G	Manual updated to include Technical and Editorial changes.
(6-15-79)	
H	
(4-03-80)	Manual updated to include Technical and Editorial Changes.
J	Manual updated to include Tchnical and Editorial Changes.
(8-01-80)	
Publication No. 83308500	

Printed in the United States of America

Address comments concerning this manual to:

Control Data Corporation
Technical Publications Dept.
7801 Computer Avenue
Minneapolis MN 55435

or use Comment Sheet in the back of this manual.

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PREFACE

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the storage module drive (SMD). Shown in the configuration chart.

Reference information is provided in six sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification.

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Section 4 - Introduction to logic symbology and card construction.

Section 5 - Description of integrated circuits used in the drive. Includes pin assignments along with truth tables and/or typical waveforms.

Section 6 - Description of descrete components and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ) explains these functions and illustrates the actual discrete elements.

Manuals applicable to the SMD are as follows:

Publication No.	Title
83308400	Maintenance
83308500	Reference
83308600	Parts Data

A guide for the Disk Drive Operator, Publication number 83323770, is also available. The guide may be ordered through Literature Distribution Services at the following address:

Control Data Corporation
Literature Distribution Services
308 North Dale St.
St. Paul, MN 55103

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FIGURES

TABLES

STORAGE MODULE DRIVE CONFIGURATION

EQUIP. IDENT. NUMBER	FINAL ASSY P/N	POWER		CABINET FEATURES							ELEC FEATURES				
		HZ	VOLT	ACST	NON ACST	IX	2X	DESK	RACK	CAB-INET	DAISY CHAIN	HYST. BRAKE	NRZ/ MFM	PLO	VAR. SECT.
BJ7A1-A	76420002	60	120		X					X		X	X	X	
BJ7A2-A	76420003	60	120		X					X	X	X	X	X	X
BJ7A2-B	76420009	50	220		X					X	X	X	X	X	X
BJ7A2-C	76420011	60	100		X					X	X		X	X	
BJ7A2-D	76420010	50	100		X					X	X	X	X	X	X
BJ7A2-E	76420015	60	120		X				X		X	X	X	X	X
BJ7A2-F	76420016	50	220		X				X		X	X	X	X	X
BJ7A2-G	76420037	60	120	X			X				X	X	X	X	X
BJ7A2-H	76420038	50	220	X			X				X	X	X	X	X
BJ7A2-J	76420046	60	120		X			X			X	X	X	X	X
BJ7A2-K	76420048	50	220		X					X	X	X	X	X	X
BJ7A2-L	76420049	60	100		X				X		X	X	X	X	X
BJ7A2-M	76420050	50	100		X				X		X	X	X	X	X
BJ7A2-N	76420052	60	120		X					X	X	X	X	X	X
BJ7A2-P	76420051	50	220		X					X	X	X	X	X	X
BJ7A2-R	76420066	60	120		X				X		X	X	X	X	X
BJ7A2-S	76420053	50	220		X					X	X	X	X	X	X
BJ7A2-T	76420056	60	120		X					X	X	X	X	X	X
BJ7A2-U	76420057	50	220		X					X	X	X	X	X	X
BJ7A2-V	76420070	50	220	X		X				X	X	X	X	X	X
BJ7A2-T	76420056	60	120		X					X	X	X	X	X	X
BJ7A2-U	76420057	50	220		X					X	X	X	X	X	X
BJ7A2-W	76420058	50	220		X			X			X	X	X	X	X
BJ7A2-Z	76420059	50	220		X					X	X	X	X	X	X
BJ7A3-A	76420004	60	120		X				X		X	X	X	X	
BJ7A3-B	76420008	50	220		X				X		X	X	X	X	X
BJ7A3-C	76420062	60	120	X			X				X	X	X	X	
BJ7A3-E	76420065	60	120	X			X				X	X	X	X	
BJ7A3-F	76420074	60	120		X					X	X	X	X	X	X
BJ7A3-G	76420075	50	220		X					X	X	X	X	X	X
BJ7A3-H	76420080	60	120	X			X				X	X	X	X	X
BJ7A3-K	76420082	60	120	X			X						X		
BJ7A4-A	76420005	60	120		X				X				X	X	
BJ7A5-A	76420006	60	120		X					X		X	X	X	
BJ7A5-B	76420007	50	220		X					X	X	X	X	X	
BJ7A6-A	76420012	60	120		X					X	X	X	X	X	
BJ7A7-A	76420013	60	120		X					X	X	X	X	X	X
BJ7A7-B	76420014	50	220		X					X	X	X	X	X	X
BJ7A7-C	76420031	60	120		X					X	X	X	X	X	X
BJ7A7-D	76420032	50	220		X					X	X	X	X	X	X
BJ7A7-E	76420076	60	120	X						X	X	X	X	X	X
BJ7A7-F	76420077	50	220	X						X	X	X	X	X	X
BJ7B2-A	76420029	60	120	X		X					X	X	X	X	X
BJ7B2-B	76420030	50	220	X		X					X	X	X	X	X
BJ7B2-C	76420033	60	120	X		X					X	X	X	X	X

(Contd) STORAGE MODULE DRIVE CONFIGURATION (Contd)

EQUIP. IDENT. NUMBER	FINAL ASSY P/N	POWER		CABINET FEATURES							ELEC FEATURES				
		HZ	VOLT	ACST	NON ACST	IX	2X	DESK	RACK	CAB-INET	DAISY CHAIN	HYST. BRAKE	NRZ/ MFM	PLO	VAR. SECT.
BJ7B2-D	76420034	50	220	X		X					X	X	X	X	X
BJ7B2-G	76420039	60	120	X		X					X	X	X	X	X
BJ7B2-H	76420040	50	220	X		X					X	X	X	X	X
BJ7B2-J	76420054	60	120	X		X					X	X	X	X	X
BJ7B2-K	76420055	50	220	X		X					X	X	X	X	X
BJ7B2-L	76420063	60	120	X		X					X	X	X	X	X
BJ7B2-M	76420074	50	220	X		X				X				X	
BJ7B2-N	76420064	60	120	X		X					X	X	X	X	X
BJ7B2-P	76420071	50	100	X		X				X	X	X	X	X	X
BJ7B2-R	76420078	50	220	X		X					X	X	X	X	X
BJ7B2-S	76420079	60	120	X		X					X	X	X	X	X
BJ7B2-U	76420081	60	120	X		X				X				X	
BJ7B4-A	76420041	60	120	X		X					X	X	X	X	X
BJ7B4-C	75420043	60	120	X			X				X	X	X	X	X
BJ7B4-E	76420044	60	120	X		X					X	X	X	X	X
BJ7B4-G	76420045	60	120	X			X				X	X	X	X	X
BJ7B5-A	76420069	60	120	X			X		X		X	X	X	X	X

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SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The CONTROL DATA® Storage Module Drive (SMD) is a high speed, random access, data storage device that interfaces with a central processor through a controller.

The electro-mechanical SMD positions its read/write heads to discrete tracks over spinning disk surfaces. Data, in the form of magnetized bits or spots, is written on or read from the disk surfaces by the read/write heads. Head positioning is performed by a closed loop proportional servo system. The carriage is driven by a voice coil linear actuator with position feedback provided from a servo surface on the disk pack.

The basic SMD consists of a disk pack spindle with associated drive motor, an actuator assembly, speed and position sensing devices, and logic circuitry for positioning, reading, writing, and interface. A hinged cover allows access to the spindle for normal pack installation and removal, while also providing a seal in the closed position to maintain cleanliness within the disk shroud.

Specifications for the storage module drive are listed in Table 1-1.

TABLE 1-1. DRIVE SPECIFICATIONS

Characteristic	Conditions	Specifications
PHYSICAL SPECIFICATIONS		
	Refer to SMD Maintenance Manual Publication No. 83308400.	
ENVIRONMENT		
Temperature	Operating	60°F (15.5°C) to 90°F (32°C)
	Gradient	12°F (6.6°C) per hour
	Transit (packed)	-30°F (-34°C) to +150°F (66°C)
Relative Humidity (no condensation)	Operating	20% to 80%
	Transit (packed)	5% to 95%
Altitude	Operating	-1000 ft (-305 m) to +6500 ft (3.05 km)
	Transit (packed)	-1000 ft (-305 m) to +15,000 ft (4.6 km)
POWER SPECIFICATIONS		
Refer to SMD Maintenance Manual Publication No. 83308400.		

TABLE 1-1. DRIVE SPECIFICATIONS (Cont'd)

Characteristic	Conditions	Specifications
DATA RECORDING SPECIFICATIONS		
Disk Pack	Packs/Drive	1
	Recording Surfaces/ Disk Pack	5
	Usable Cylinders/ Recording Surface	823 (0-822)
	Tracks/Cylinder	5
	Tracks/Inch	384
	Track Spacing	0.0026 inch (nominal)
	Rotational Speed	3600 rpm (16.7 ms/rev)
	Disk Pack	CDC 9877 or equivalent
	Disk Surface Diameter	14 inches (nominal)
	Disks/Disk Pack	5 (top and bottom disks are for protection only)
	Coating	Magnetic oxide
Seek Timing	Access Mechanism	Voice coil driven by servo loop
	822-Track Seek	55 ms (maximum)
	1-Track Seek	7 ms (maximum)
	Average Seek	30 ms

TABLE 1-1. DRIVE SPECIFICATIONS (Cont'd)

Characteristic	Conditions	Specifications
Latency Time	Average	8.33 ms (at 3600 rpm)
	Maximum	17.2 ms (at 3492 rpm)
Recording	Mode	Modified Frequency Modulation (MFM)
	Bit Density	4038 bits per inch (outer track, nominal)
		6038 bits per inch (inner track, nominal)
	Rate	9.677 MHz (nominal), 1,209,600 bytes/second
Heads	Recording	5
	Servo (positioning)	1
	Read/Write Width	0.002 inch (nominal)
Data Capacity	Nominal	80 MB
	Bits/Track	161,281 (unsectored)
	Bits/Cylinder	806; 400 (unsectored)
	Bits/Pack	651,571,200 (unsectored)
	Bits/Byte	8
	Bytes/Track	20,160
	Tracks/Cylinder	5
Controllers/Drive	Quantity	1
Drives/Controller	Quantity	16 (0-15) maximum
Interface Cables	Minimum Length	15 ft (4.6 meters)
	Maximum Total System Length	75 ft (22.8 meters)
	Type	Control: Twisted pair
		Signal: Twinax
	Connectors	2 per drive (star configuration)
	Pin Assignments	Refer to Maintenance Manual
	Signal Functions	Refer to Section 3 of this manual

ASSEMBLY LOCATIONS

Figure 1-1 illustrates the basic storage module drive. Detailed information on the construction and functions of these assemblies is provided in Section 3 of this manual.

TOP COVER ASSEMBLY

The top cover assembly protects the other drive assemblies during operation. The drive cover for pack loading is opened by means of a latch under the cover. An electrical switch senses that the cover is opened, disables the spindle motor power, and commands retract if the heads are loaded.

SPINDLE ASSEMBLY

The spindle assembly mounts and rotates the disk pack. Its associated drive motor runs continuously whenever a pack is installed, the pack cover is closed, and the START switch is on.

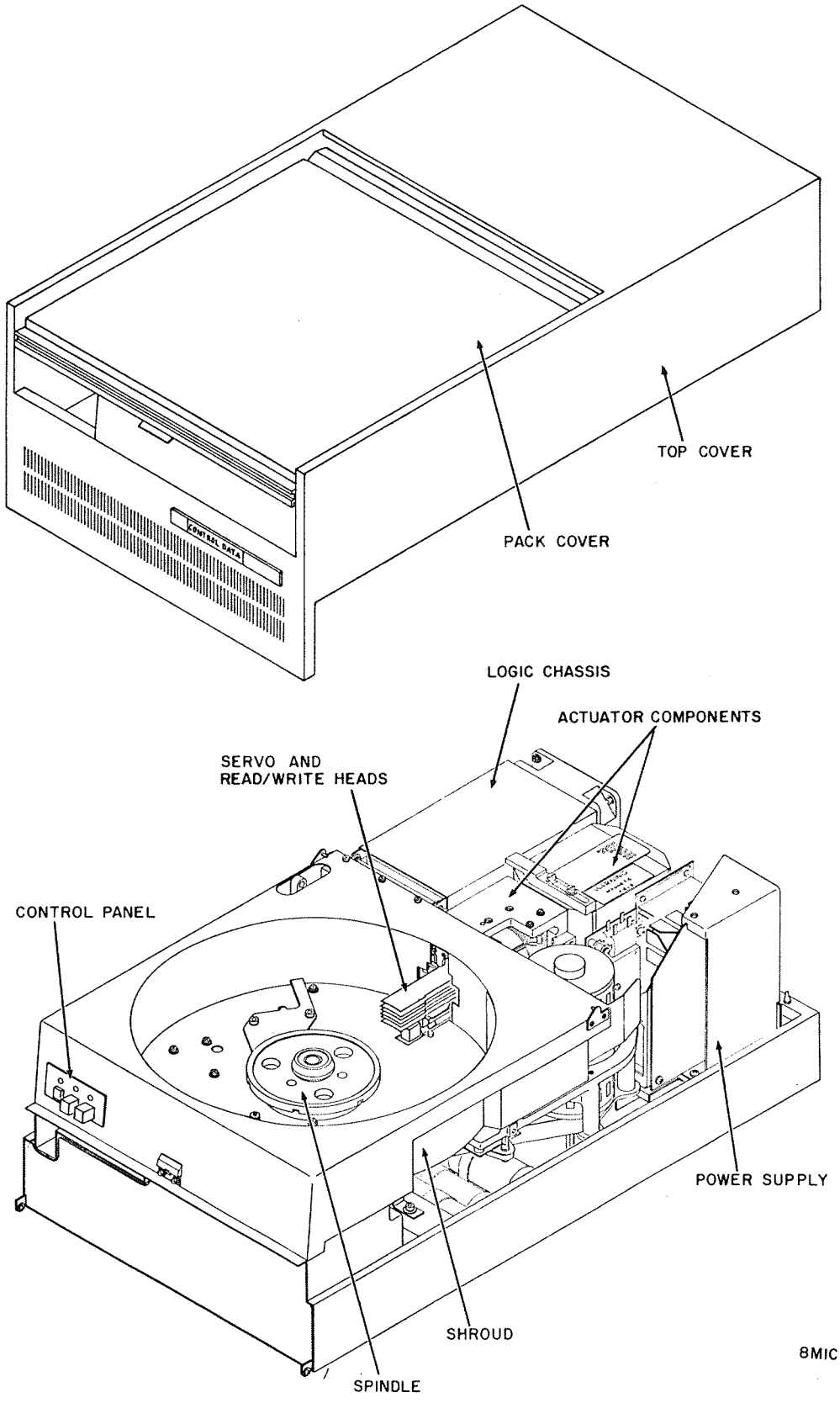


Figure 1-1. Assembly Locations

ACTUATOR ASSEMBLY

The actuator assembly mounts the read/write heads for processing data. The actuator contains a voice coil positioner controlled by a closed-loop, continuous-feedback servo system.

SHROUD

The shroud surrounds the disk pack. The shroud protects the pack, aids in directing air from the blower to the pack, and prevents the operator from damaging the read/write heads with the pack.

LOGIC CHASSIS

The logic chassis serves as the mounting point for the main complement of the logic cards. The chassis is mounted on the deck assembly. The backpanel terminals provide ready access to all signals entering and leaving each card. In addition, the cards have test points for monitoring critical signals within the cards.

Read/Write logic cards that contain logic directly affecting head selections and operation are mounted near the data head leads.

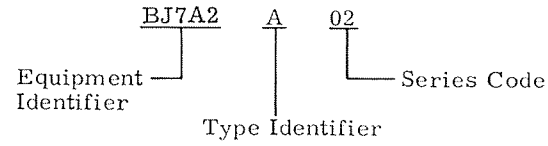
POWER SUPPLY

The power supply distributes the dc power required by the drive. Incoming power is filtered by a line filter and applied to a main ac power circuit breaker and a secondary ac power circuit breaker for the power supply.

EQUIPMENT IDENTIFICATION

An equipment number is assigned to each drive to identify its configuration. This provides a systematic method of identifying, accounting, and controlling changes that affect drive logic and mechanical components.

The equipment configuration is identified by a nameplate attached to the frame at the back of the drive. The Equipment Identification Number will be similar to the following:



The Equipment Identifier indicates the basic function of the unit. Refer to the equipment configuration listing in the preface.

The Type Identifier indicates a non-interchangeable difference in equipments that affects the interface. The term "Mod" is sometimes used interchangeably with "Type Identifier".

The Series Code changes with each non-interchangeable change within the equipment. Drives with different series codes are fully interchangeable at the system level; however, not all of their electrical or mechanical components may be interchangeable. Series codes are changed by Engineering Change Order (ECO) only at the factory.

Other changes are accomplished by Field Change Order (FCO). These changes may be installed either at the factory or by field personnel. FCO changes are indicated by an entry on the FCO Log that accompanies each machine. It is important that this log be kept current by the person installing each FCO.

Unless otherwise specified, all theory, procedures, and diagrams in these manuals apply to all units. Exceptions are noted where applicable.

Manuals accompanying unit shipments from the manufacturer match the configuration of those units. Subsequent manual changes are controlled by the Revision Record sheet behind the title page of every manual. This sheet identifies the Series Code and FCO effectivity of manual changes. If maintenance will be performed using a manual other than the manual supplied with each drive, verify that the manual and drive configurations match.

SECTION 2

OPERATION

INTRODUCTION

This section provides instructions and related information for operating the drive.

CONTROLS AND INDICATORS

The drive has a control panel located on the front of the machine, and power switches and a running time meter located at the rear. Figure 2-1 illustrates the controls and indicators, and table 2-1 provides functional descriptions.

OPERATING INSTRUCTIONS

POWER APPLICATION

1. Set AC POWER circuit breaker to ON. (If the pack is stored in the drive, the AC POWER breaker should be left on to maintain cleanliness of shroud and pack.)
2. Set POWER SUPPLY circuit breaker to ON.
3. Install a disk pack (refer to Disk Pack Installation procedure).
4. Press operator panel START switch.
5. Spindle motor energizes. Head loading sequence begins when spindle is up to speed.
6. Head loading sequence is complete when heads are positioned to track 0. Drive is now ready to receive a Read, Write, or Seek command from the control unit. READY indicator is on.

DISK PACK HANDLING

To ensure maximum disk pack life and reliability, observe the following precautions:

1. Store disk packs in machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).
2. If disk pack must be stored in different environment, allow two hours for adjustment to computer environment before use.
3. Never store disk pack in sunlight or in dirty environment.
4. Store disk packs flat, not on edge. They may be stacked with similar packs when stored.
5. Always be sure that both top and bottom plastic covers are on disk pack whenever it is not actually installed in a drive.
6. When marking packs, use pen or felt tip marker that does not produce loose residue. Never use a lead pencil. Write on label before it is applied to disk pack cannister.
7. Do not attach any label to the disk pack itself. Labels will not remain attached when the pack is spinning and catastrophic head crashes may result. All labels should be placed on the pack cannister if required.

DISK PACK INSTALLATION

Make certain that the disk pack to be installed has been maintained according to the Preventive Maintenance section.

1. Raise pack access cover. (AC POWER circuit breaker must be ON).
2. Lift disk pack by plastic canister handle.

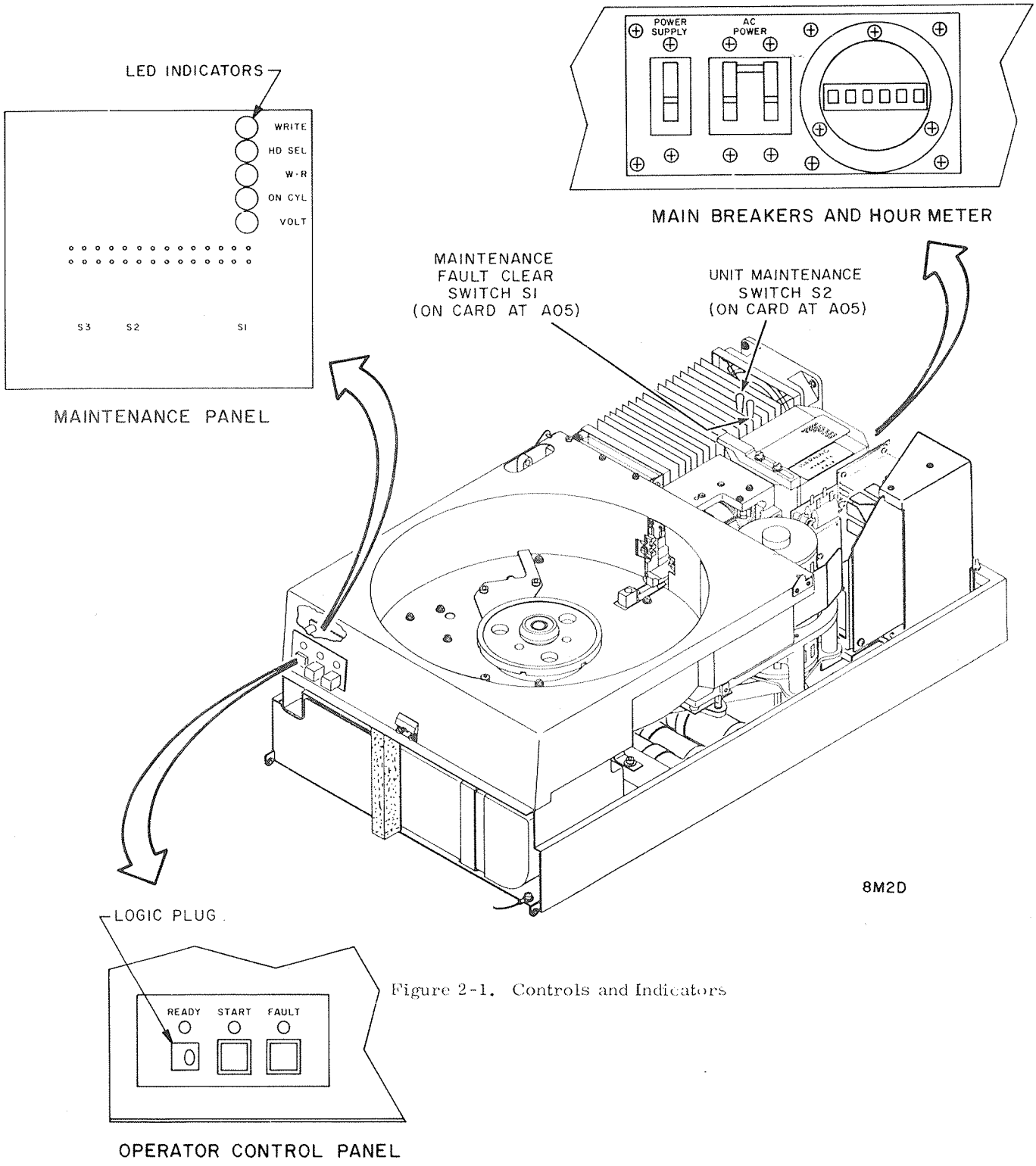


Figure 2-1. Controls and Indicators

TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
	OPERATOR PANEL
START switch	Energizes (when pressed to light) spindle drive motor and begins First Seek sequence provided the following conditions are met: 1. Disk Pack is in place and canister removed. 2. Pack cover is closed. 3. Circuit breakers are on. Causes a power off sequence (when pressed to extinguish).
START indicator	Lights when switch is on.
FAULT switch	Clears the fault circuitry and extinguishes the FAULT indicator. (Does not clear Maintenance Fault register.)
UNIT MAINTENANCE switch	Prevents drive from activating Unit Selected signal, thus preventing the controller from selecting drive. This switch should not be used during normal on line operation.
FAULT indicator	Lights in response to one or more of the following conditions: 1. Read and write are selected at the same time. 2. No ac write current when Write Gate is present. 3. More than one head is selected. 4. Read or Write is selected while off cylinder. 5. Low voltage condition sensed for ±5v, ±20v, ±42v. 6. Loss of dibit signal for 350 ms with heads loaded.
LOGIC PLUG	Completes circuitry to permit selection of the unit through a binary code. CAUTION Unit select logic plug should not be changed or removed unless unit is shut off with heads unloaded.
READY indicator	Lights when the unit is up to speed, the heads are loaded, and no fault condition exists.
	REAR PANEL
AC POWER circuit breaker	Controls application of ac power.
POWER SUPPLY circuit breaker	Controls application of dc power to the logic chassis.
Elapsed Time Meter	Active when ac power and dc power are applied by circuit breakers. Records accumulated ac power-on time.

TABLE 2-1. CONTROLS AND INDICATORS (Cont'd)

MAINTENANCE PANEL (BACK OF OP PNL)	
Control or Indicator	Function
WRITE FAULT indicator	Indicates a write was attempted and no ac write current and/or dc current was sensed.
HEAD SELECT FAULT indicator	Indicates more than one head selected.
W.R. FAULT indicator	Read or write were selected at same time.
ON CYLINDER FAULT indicator	Read or write was selected while off cylinder.
VOLTAGE FAULT indicator	Low voltage condition existed for ±5v, ±20v, ±42v.

3. Disengage bottom dust cover from disk pack by turning canister handle counterclockwise. Set cover aside in an uncontaminated area.

CAUTION

Avoid abusive contact between the disk pack and the spindle. The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place disk pack onto spindle.

NOTE

A spindle lock mechanism is actuated when the disk pack canister cover is on the spindle. The mechanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist canister handle clockwise to lock disk pack in place.

NOTE

A click may be heard as the spindle lock mechanism engages.

6. Lift canister clear of disk pack, place bottom dust cover on canister, and set aside in an uncontaminated area.

7. Close pack access immediately to prevent entry of dust and contamination of disk surfaces.

DISK PACK REMOVAL

1. Press operator panel START switch to extinguish the START indicator.
2. Check that disk pack rotation has stopped. (Stopping time is approximately 1.5 minutes without brake and 20 seconds with brake.)
3. Raise front cover.

CAUTION

The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

4. Place plastic canister over mounted disk pack so that post protruding from center of disk pack is received into canister handle.
5. Twist canister handle counterclockwise until disk pack is free of spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly.

6. Lift canister and disk pack clear of spindle.
7. Close front cover.
8. Place bottom dust cover in position on disk pack and lock it.

FIELD TEST EXERCISER

The Field Test Exerciser permits full control of the drive seek and read/write logic without computer intervention. Refer to the Field Test Exerciser manual for a complete description of operation.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

Theory of operation for the drive is organized into two parts. The first part describes the major mechanical assemblies. The second part describes the power functions, the logical functions, and the signals exchanged with the controller.

Functional descriptions are frequently accompanied by simplified diagrams. These diagrams are useful both for instructional purposes and as an aid in troubleshooting. The diagrams have been simplified to illustrate the principles of operation; therefore, some elements are omitted. The logic diagrams in the Maintenance Manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The descriptions are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals), and track format (i.e., data records and field organization).

ASSEMBLIES

Figure 3-1 illustrates the relation of the major assemblies comprising the SMD. The following paragraphs describe the operation of these assemblies.

POWER SUPPLY

Each drive has its own self-contained power supply. The power supply is located in the rear and cooled by air from a blower at the front of the drive cabinet. The power supply consists of a transformer and associated filter capacitors to supply ±5, ±12, ±20 and ±42 volts. The ±5 and ±12 V supplies are also internally regulated.

The power supply has the following outputs:

1. ±20 vdc for emergency retract relay, hysteresis brake, and the logic.
2. ±12 vdc for read amplifiers and track servo preamplifier.
3. ±5 vdc for the logic.
4. ±42 vdc for use by the voice coil positioner and by the writer circuitry.

Power is made available to the drive through a line filter and the closed contacts of the AC POWER and POWER SUPPLY circuit breakers. When the AC POWER circuit breaker is closed, the blower motor starts, logic fan, and running time meter operate. When the POWER SUPPLY circuit breaker is closed, all dc power is available, the logic fan starts. With both AC and DC circuit breakers closed, the running time meter operates. The ±5 vdc voltages are adjustable.

LOGIC CHASSIS

The logic chassis assembly consists of a wire wrap board, logic cards, and a blower motor. The logic cards are installed on the protruding pins of one side of the wire wrap board. Wiring between cards and to and from the logic chassis occurs at the protruding pins on the opposite side of the wire wrap board. Access to this wiring is gained by releasing two screws from the hinged support at the rear of the logic chassis and swinging the chassis upward. The chassis is held in this position by a sliding support mounted on the voice coil assembly.

The logic card chassis contains all the logic cards used in the drive except the writer and analog cards, which are located near the actuator assembly. The logic chassis cards are five by six inches and installed vertically in numerically identified positions.

DRIVE MOTOR ASSEMBLY

The drive motor drives the spindle assembly. The motor is a 1/2 hp unit of the induction type. The motor is secured to a mounting plate. The motor

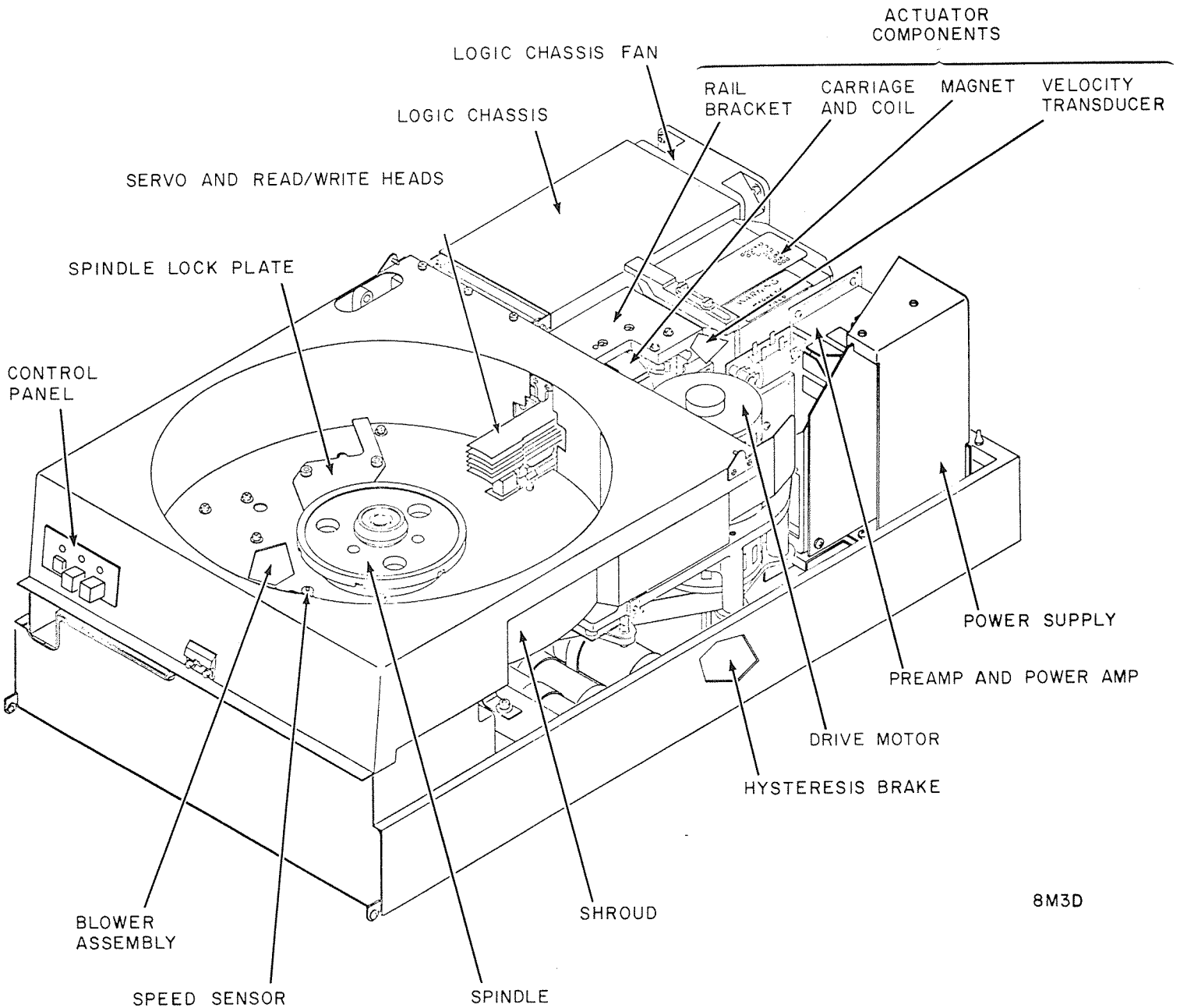


Figure 3-1. Deck Assemblies

mounting plate is secured to the underside of the deck plate. Power is transferred to the spindle via a flat, smooth-surfaced belt that threads over the pulleys of the spindle and drive motor. A motor tensioning spring maintains a constant tension on the motor mounting plate to keep the belt tight.

The temperature of the drive motor is monitored by an internal thermostat. If the motor overheats, the thermostat opens. The result is a speed loss and retraction of the heads. The drive motor thermal overload button is located on top of the motor; it is reset by pressing it.

HYSTERESIS BRAKE ASSEMBLY

The hysteresis brake decelerates the drive motor during a Power Off sequence (refer to Power Off sequence paragraph). The brake is energized whenever relay K4 is de-energized and the heads are unloaded. The brake mounts directly on the motor shaft, below the motor pulley. The brake consists of two concentric permeable bodies assembled with a uniform gap separating the outer diameter of one from the inner diameter of the other. These adjacent surfaces contain a series of pole faces. A permanent magnet, in the shape of a cup, fits in the gap to separate the cylinders. This cup is connected to the motor shaft by two setscrews. As long as spindle motor power is applied, brake power is not available and the cup is driven at the speed of the motor. When spindle motor power is removed and the heads unload, braking power is applied. A flux field is created between the inner and outer cylinder pole faces as braking voltage (+20v) is applied to the inner cylinder. The flux field sets up what is in effect magnetic friction between the inner cylinder and the cup, causing the cup (and motor shaft) to decelerate. Brake deceleration in turn causes spindle motor deceleration.

SPINDLE ASSEMBLY

The spindle assembly is the physical interface between a drive and a disk pack. The surface of the pack mounting plate (Figure 3-2) mates directly with the center of the disk pack.

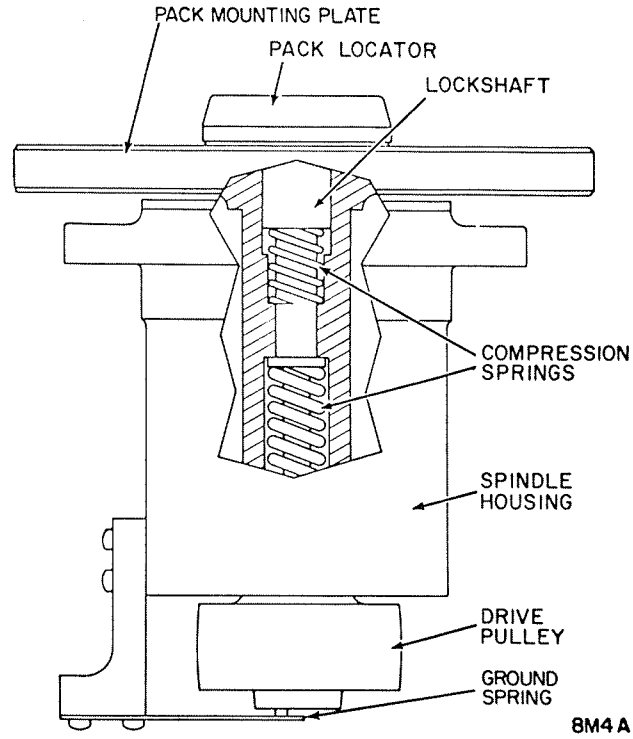


Figure 3-2. Spindle Assembly

The upper end of the spindle assembly contains internal threads that engage the external threads of a stud projecting from the disk pack. When the disk pack canister cover handle is rotated clockwise, the spring loaded lockshaft inside of the spindle is pulled upward and the disk pack is pulled down. As a result, the mating surfaces of the disk pack and spindle are engaged by a force of approximately 130 pounds. When the disk pack is fully engaged, a release mechanism in the canister handle frees the canister from the disk pack.

The spindle lock is actuated by the pack canister when installing or removing a disk pack. This makes it easier to install or remove a disk pack by preventing spindle rotation.

The spindle is driven by a flat belt linking the spindle drive pulley to the drive motor pulley.

A ground spring (Figure 3-2) is mounted at the lower end of the spindle assembly. The ground spring is

mounted so that it is always in contact with the shaft to bleed off any accumulation of static electricity on the spindle through a ground strap.

ACTUATOR

The actuator consists of the coil and carriage, rail bracket assembly, and magnet assembly. The actuator (Figure 3-3) is the device that supports and moves the read/write and track servo heads. The forward and reverse moves of the carriage on the carriage track are controlled by a servo signal. The basic signal is developed in the logic section and processed by a power amplifying stage. The power amplifier output is applied to the voice coil positioner (part of carriage). The signal causes a magnetic field about the voice coil positioner. This magnetic field reacts with the permanent magnetic field existing around the magnet assembly. The reaction either draws the voice coil into the permanent magnet field or forces it away. Signal polarity determines the direction of motion, while signal amplitude controls the acceleration of the motion.

The voice coil positioner is a bobbin-wound coil that is free to slide in and out of the forward face of the magnet assembly. Fastened to the positioner is a head/arm receiver which holds the 5 read/write heads and the single track servo head. The head/arm receiver mounts on the coil and carriage assembly that moves along the carriage rail on six anti-friction bearings. Movement of the positioner in or out of the magnet causes the same motion to be imparted to the entire carriage assembly. This linear motion is the basis for positioning the read/write and track servo heads to a particular track of data on the disk pack. (Refer to Head Loading paragraph for detailed information on read/write head loading and unloading.)

The positioning signal is derived in the logic chassis and power amplifier. The signal is applied to the voice coil positioner via two flexible, insulated, metal straps, the ends of which are secured to the carriage and bearing assembly.

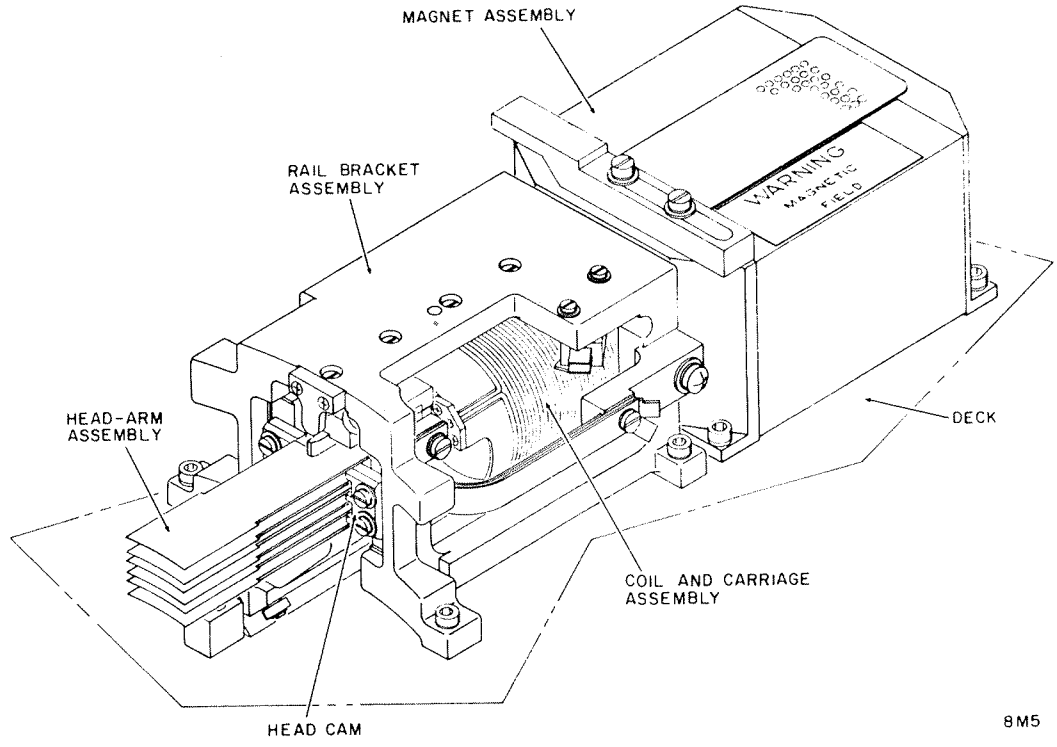


Figure 3-3. Actuator Elements (Heads Extended)

During any Seek operation, the logic must be informed of the current location and velocity of the carriage. This information is provided by the velocity transducer in the magnet assembly and the track servo head installed on the head/arm receiver.

The transducer is a two-piece device, one piece stationary and the other movable. Refer to the Transducer paragraph for a complete description.

The actuator contains a stop mechanism to limit extremes in forward and reverse movement. The forward stop assembly consists of two rubber bumpers located in the shroud vicinity. If the carriage moves too far toward the disk pack, the two bumpers contact the upper and lower front sides of the carriage. If the carriage is retracted far enough away from the disk pack, the rear of the head/arm receiver contacts a rear cylindrical bumper which protrudes out of the front face of the magnet core.

Head Loading

The read/write heads must be loaded to the disk surfaces before exchanging data with the controller. The heads must be removed (unloaded) from this position and driven clear of the disk pack either when power is removed from the unit or when the disk pack velocity falls below about 3000 rpm. The actuator components involved in these operations are identified in Figure 3-4.

Heads are loaded by moving the aerodynamically shaped head face toward the related disk surface. When the cushion of air that exists on the surface of the spinning disk is encountered, it resists any further approach by the head. Head load spring pressure is designed to just equal the opposing cushion pressure (function of disk pack rpm) at the required height. As a result, the head flies. However, if the head load spring pressure exceeds the cushion pressure (as would happen if the disk pack

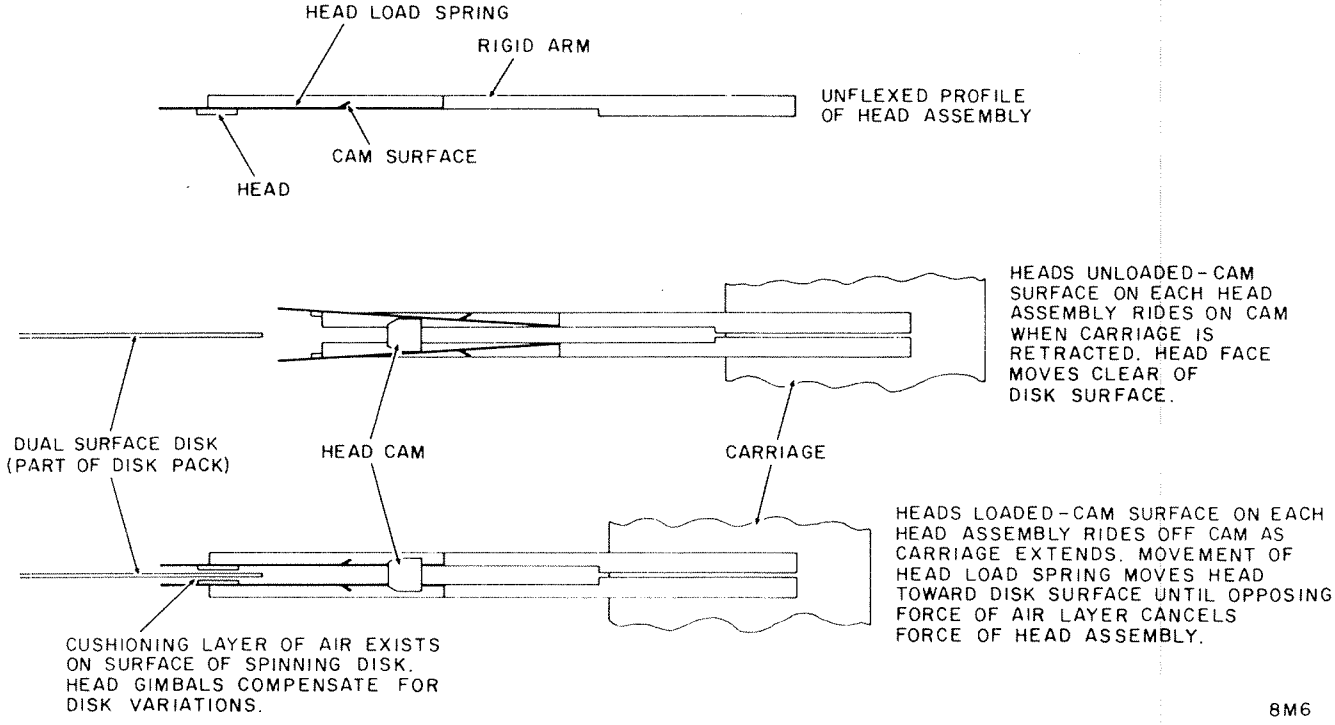


Figure 3-4. Head Loading

lost enough speed), the head stops flying and contacts the disk surface. This could cause damage to the head as well as the disk surface.

To prevent damage to the heads and/or the disk pack during automatic operation, loading occurs only after the disk pack is up to speed and the heads are over the disk surfaces. For the same reason, the heads unload automatically and are retracted if the disk pack rpm drops out of tolerance. During manual operations, heads should never be loaded on a disk pack that is not rotating. Head loading is a part of the Power On/Load function. Pressing the START switch initiates disk pack rotation and purge. Purge time is 15 to 30 seconds (30 sec max).

When the pack reaches 2800 rpm, the logic senses the Up to Speed condition. After up to speed and purge have been accomplished, the logic specifies a load command and the carriage moves forward toward track 0. Head loading occurs during this forward motion. The carriage continues to move toward the spindle until the servo detects track 0.

The head load spring (Figure 3-4) is designed to maintain a constant loading force. While the heads are retracted, head cams on the actuator housing bear against the head load spring cam surfaces. The cams support the loading force and hold the heads in unloaded position. As the carriage moves forward, the head load spring cam surface rides off the head cam just after the read/write heads move out over the disk surface. The loading force moves the head face toward the air layer on the surface of the spinning disk until the opposing forces balance.

The heads loaded switch status reflects the state of the read/write heads (loaded or unloaded). This status is used in the logic chassis and power supply. The switch mounts on the upper rail bracket and is transferred by carriage motion. Whenever the carriage is fully retracted, the switch state reflects the unloaded status of the heads. As the carriage moves forward during a Power On/Load, the switch transfers at a point within about 0.1 to 0.2 inch forward of the retracted stop. This switch status remains unchanged until the carriage is retracted to the same position and, as such, does not precisely indicate the loaded/unloaded status of the heads. Precise status is determined by the logic when the servo track head senses dibits. This switch is interlocked to the drive motor and will not allow spindle power to be removed until the heads are unloaded.

Head unloading occurs whenever power to the unit is removed or disk pack rpm drops below tolerance. Signals to the logic cause the voice coil to drive the carriage in reverse from its current location toward the retracted stop. (Either normal or emergency methods can be used. Refer to Power Off Sequence paragraph for additional information.) As the carriage retracts, the cam surfaces encounter the head load springs and each head rides vertically away from the related disk surface. The carriage continues back to the retracted position and stops.

Head/Arm Assemblies

Six head/arm assemblies are mounted on the carriage. A read/write head/arm assembly consists of a read/write head assembly mounted at the end of a supporting arm structure. A track servo head/arm assembly consists of a read coil head assembly mounted at the end of a supporting arm structure.

The head assembly (Figure 3-5), which includes a cable and plug, is mounted on a gimbal ring which, in turn, is mounted on a head load spring. This method of mounting allows the head assembly to pivot (independent of the arm) tangentially and radially relative to a data track on the disk surface. Such motion is required to compensate for possible irregularities in the disk surface.

The arm structure consists of a floating arm secured to a heavier fixed arm. The end of the fixed arm opposite the head mounts in the carriage receiver. The floating arm is the mounting point for the head and is necessarily flexible so that it can flex during load and unload motions, onto and off of the cam surfaces.

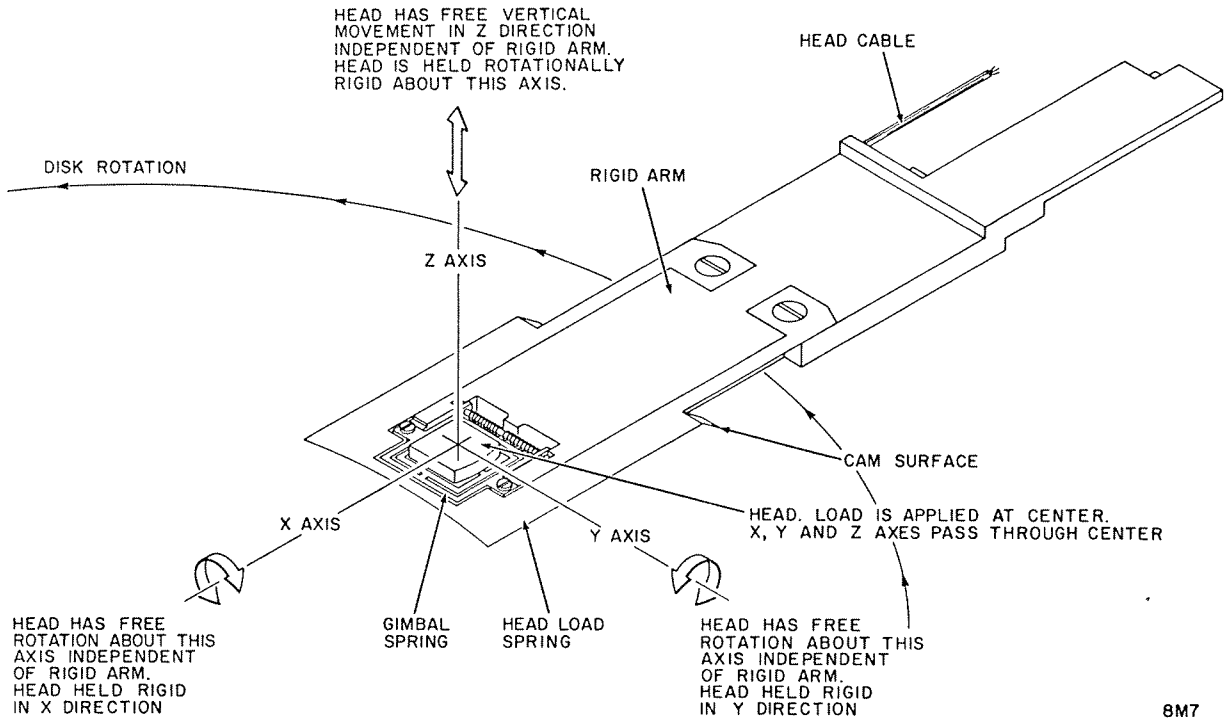


Figure 3-5. Head/Arm Assembly Motion

During head loading, each floating arm is driven off the related cam and unflexes to force a head toward the air cushion on the spinning disk surface. The force applied by the floating arm causes the heads to fly or float on the air cushion. Vertical motion by a disk surface (due to warpage or imperfection) is countered by a move in the opposite direction by the gimballed head and/or floating arm. As a result, flight height remains nearly constant.

TRANSDUCERS

The deck assembly contains two transducers: speed sensing transducer and velocity transducer. These transducers provide signals that are used by the logic chassis and the controller to generally control the progression of most machine operations.

Speed Sensing Transducer

The speed sensor (Figure 3-6) generates a voltage output whenever the two ferro-magnetic slugs enter the magnetic field surrounding the pole piece at the pickup end of the transducer. The pack hub is filled with two ferro-magnetic slugs. The speed sensor generates a signal each time the slug is detected by the transducer. The logic then shapes this signal into a 55-μsec pulse. As long as the speed exceeds

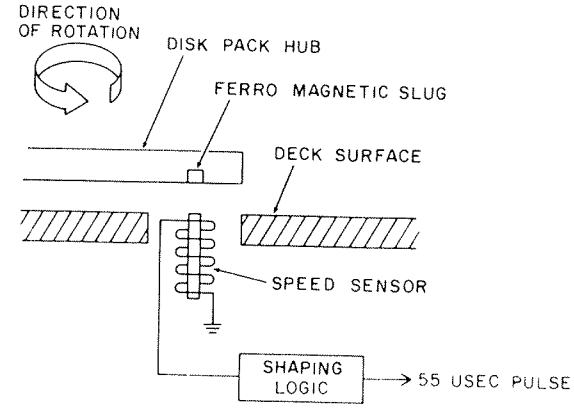


Figure 3-6. Speed Detection

2800 rpm, one of these pulses will be sensed at least once each 12.5 ms. A sensing circuit within the logic monitors the pulses and provides an enable to relay K2.

If speed is insufficient, the pulse repetition rate is reduced accordingly. This has either of two effects:

1. If the heads are not loaded, K2 cannot energize and the logic will not initiate the load sequence.
2. If the heads are already loaded, K2 opens, and the voice coil is disconnected from the logic power amplifier and connected to the emergency retract circuit. The heads immediately are unloaded to the retracted stop.

Velocity Transducer

The velocity transducer (Figure 3-7) is a two-piece device consisting of a stationary tubular coil/housing and a movable magnetic core.

The magnetic core is connected via the extension rod to the rear surface of the head/arm receiver. All motion of the carriage is therefore duplicated by the magnetic core. As the core moves, an emf is induced in the coil. The amplitude of this emf is directly related to the velocity of the core (and carriage). The polarity of the emf is an indication of the direction of movement by the core (and carriage). The transducer output drives an operational amplifier located in the logic chassis. This signal is used by the servo logic to control acceleration/deceleration of the carriage during Seek operations.

BLOWER SYSTEM

The blower system (figure 3-8) provides positive pressure in the pack area. The presence of this elevated pressure results in an outward dispersion of air preventing ingestion of contaminated air. This

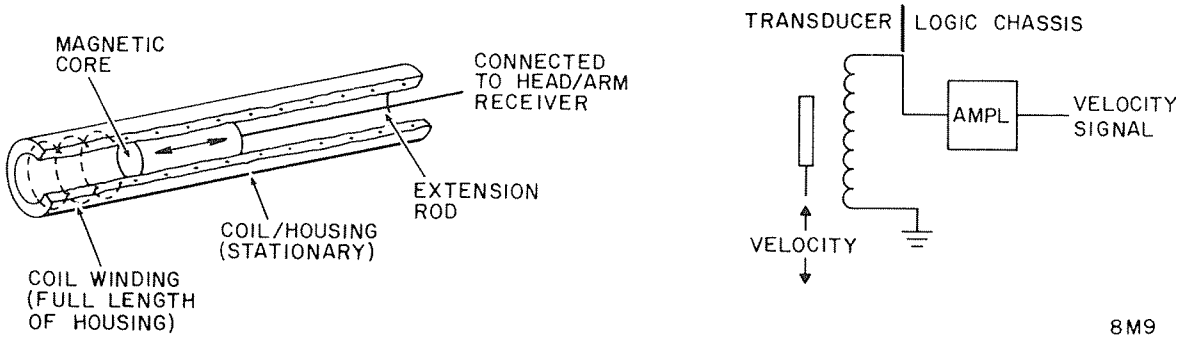


Figure 3-7. Velocity Detection

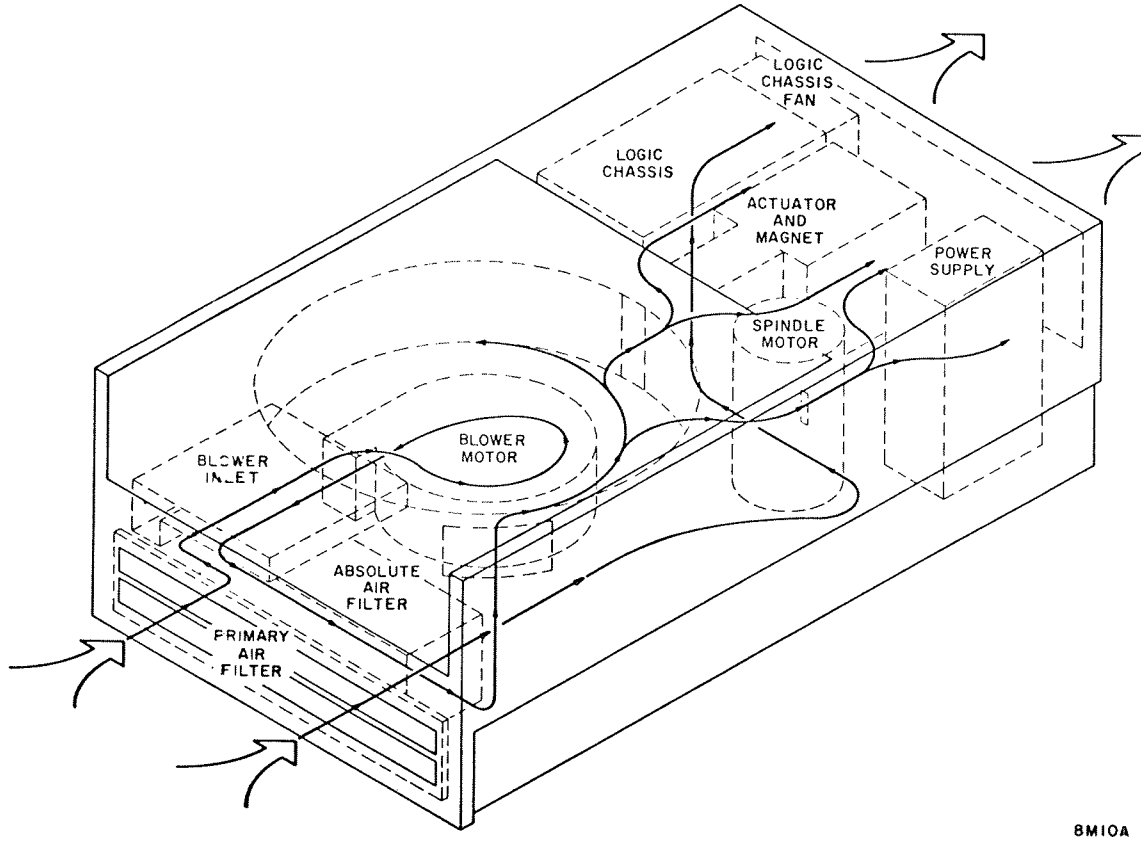


Figure 3-8. Blower System

air flow greatly reduces possible contamination and resulting damage to the disk surfaces and the read/write heads.

Power to the blower motor is available whenever the AC POWER circuit breaker is on.

DISK PACK

The disk pack is the recording medium for the drive. The disk pack consists of five 14-inch disks, center-mounted on a hub. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders and adhesives. The top and bottom disks are protective non-recording disks.

There are five recording surfaces and one track servo surface. The servo disk contains pre-recorded information that is used by the servo logic to position the heads to the desired track.

The 823 recording tracks are grouped in a 2-inch band near the outer edge of the disk. Track 822 has a diameter of approximately 9 inches; the diameter of track 0 is about 13 inches. The tracks are spaced about 0.0026-inch apart.

The disk pack has a two-piece container. The bottom cover can be removed simply by grasping and rotating the center hub. The top cover is designed so that it can be removed only by installing the disk pack on the spindle. The disk pack can be removed from the spindle only by using the top cover. This design protects the disk pack from physical damage and greatly reduces the possibility of contamination of the disk pack recording surfaces.

FUNCTIONS

I/O OPERATIONS

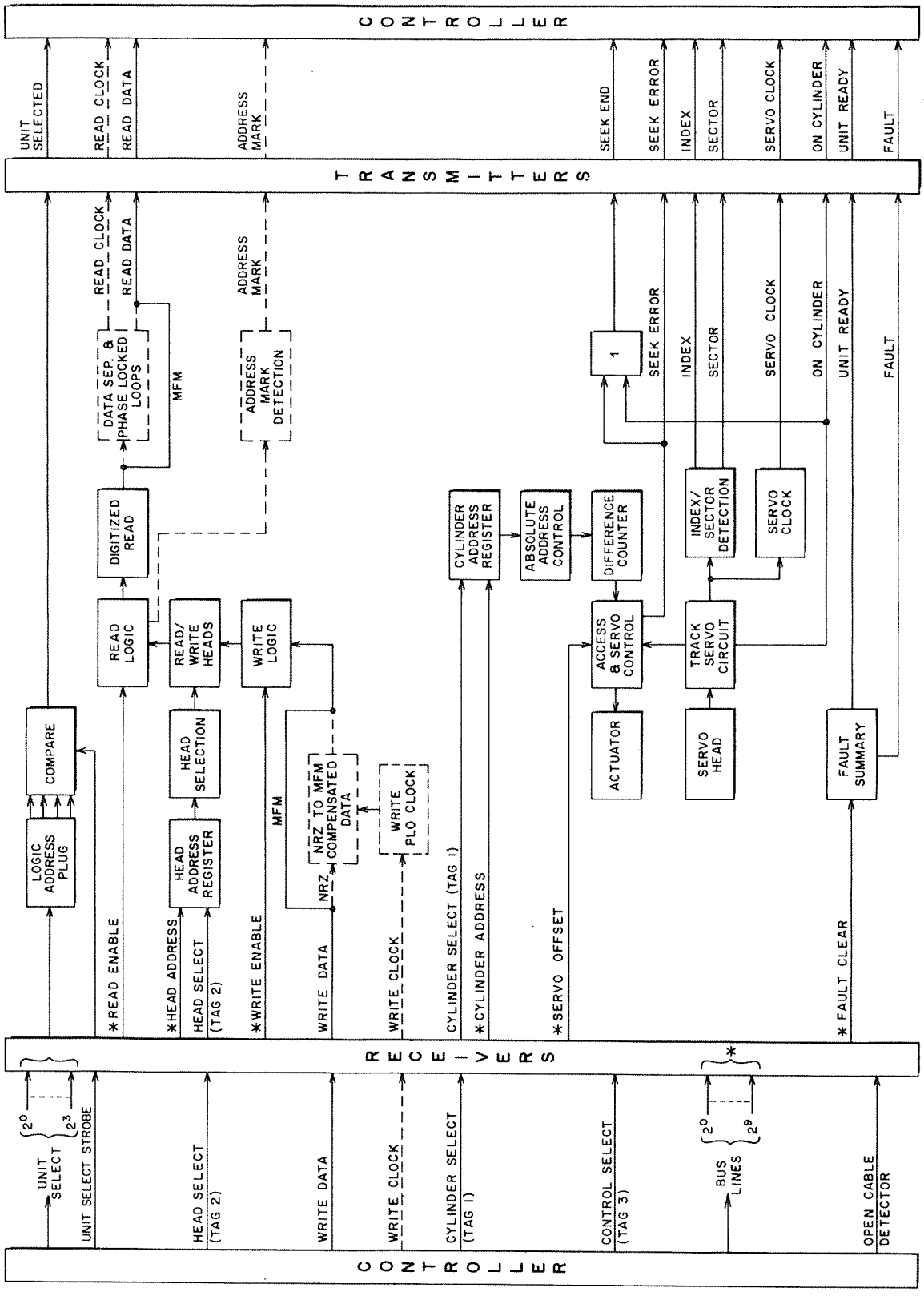
Figure 3-9 is a block diagram of the drive and its I/O lines. Table 3-1 defines the signals on the I/O lines. The block diagram shows only the main elements involved in the I/O dialog. More detailed diagrams that illustrate signal interchange between drive logic subsystems are provided in the applicable theory portions of this manual.

TABLE 3-1. I/O LINES

Signal Name	Function		
"A" CABLE (FROM CONTROLLER)			
Tag Bus Lines	Three lines that define the operation to be performed by the drive. Decoded in the drive to define tag functions: Tag 1 strobes in the cylinder address and initiates the seek. Tag 2 strobes in the head address and Tag 3 is the control select which enables the function to be performed.		
Bus In Lines	Tag 1	Tag 2	Tag 3
Bit 0	1	1	Write Gate - Enables write drivers.
Bit 1	2	2	Read Gate - Enables the digital read data lines. With PLO option, leading edge triggers read chain to sync on all-zeros pattern.
Bit 2	4	4	Servo Offset Plus - Offsets the actuator from the nominal or cylinder position toward the spindle.
Bit 3	8	-	Servo Offset Minus - Offsets the actuator from the nominal on cylinder position away from the spindle.
Bit 4	16	-	Fault Clear - Pulse sent to drive to clear the fault summary flip-flop.
Bit 5	32	-	Address Mark Enable (optional) - When combined with a Write Gate, Address Mark is written. When combined with a Read Gate, an Address Mark search is initiated.
Bit 6	64	-	RTZ - Pulse sent to drive to cause actuator to seek to track zero.
Bit 7	128	-	Data Strobe Early - Enables the PLO data separator (optional) to strobe the data at a time earlier than optimum.
Bit 8	256	-	Data Strobe Late - Enables the PLO data separator (optional) to strobe the data at a time later than optimum.
Bit 9	512	-	--
Unit Select Lines	Four lines used to select the drive. The binary code on the lines must match the code on the logic plug in the drive.		

TABLE 3-1. I/O LINES (Cont'd)

Signal Name	Function
	"A" CABLE (FROM DRIVE)
Sector Mark	Signal is derived from the servo track. There are a maximum of 128 sector marks available per revolution.
Fault	Indicates that one or more of these faults exist: DC power fault, head select fault, write fault, write or read while off cylinder, and Write Gate during a Read operation.
Seek Error	Indicates that the unit was unable to complete a move within 500 ms, or that carriage has moved to a position outside recording field. A seek error interrupt also occurs if an address greater than track 822 has been selected. In this case, the seek error interrupt drops, the counter clears, and the carriage does not move.
On Cylinder	Indicates that the servo has positioned the heads over a data track.
Index	The leading edge of this signal is coincident with the leading edge of the sector zero.
Unit Ready	Indicates that selected unit is up to speed, heads are loaded, and no fault exists.
Open Cable Detector	Inhibits Unit Selection and any unwanted command such as Write Gate when "A" cable is disconnected or controller power is lost.
Address Mark Found (Optional)	Indicates that an Address Mark has been found. Enabled by a combination of Read Gate and Address Mark Enable.
	"B" CABLE (FROM CONTROLLER)
Write Data	Carries data to be recorded on disk pack. Data is write compensated MFM or optional NRZ.
Write Clock (Optional)	Required for optional NRZ. MFM transmits the Write Clock signal which must be synchronized to the NRZ data.
	"B" CABLE (FROM DRIVE)
Servo Clock	Phase-locked 9.677 MHz clock generated from the servo track dibits. It is used to transfer data to the drive.
Read Data	Carries data recovered from the disk pack. Data is MFM or optional NRZ.
Read Clock (Optional)	Internally derived clock that is synchronous with the detected NRZ data.
Seek End	Seek End is a combination of ON CYL or SEEK ERROR indicating that a seek operation has terminated. If an address greater than 822 cylinders has been selected there will be no change in Seek End status.
Unit Selected	When the four unit select bit lines compare with the logic plug on the control panel, and when the unit select line is true, then the Unit Selected line is true.



NOTES: 1. SIGNALS TRANSMITTED VIA THE BUS LINES ARE INDICATED BY ASTERISKS.
2. DASHED LINES INDICATE OPTIONAL FEATURES.

Figure 3-9. Block Diagram

POWER SYSTEM FUNCTIONS

The drive power system receives its input from the site ac power source and uses it to produce all the ac and dc voltages necessary for drive operation. The remainder of this discussion describes the power system and contains the following major topics:

- Power Distribution
- Power On Sequence
- Power Off Sequence
- Emergency Retract and Data Protection

POWER DISTRIBUTION

Power distribution consists of routing power to the various elements in the power system and the rest of the drive. The distribution is controlled by the AC POWER and POWER SUPPLY circuit breakers. The power distribution circuits are shown on figure 3-10 and basic operation is explained in the following.

Site main ac power is input to the power supply via the AC POWER circuit breaker. When this breaker is closed, it applies power to the HOUR meter and blower motor. It also provides the input to the drive motor control triacs; however, the motor does not start until the power on sequence.

Closing the POWER SUPPLY circuit breaker applies power to the logic fan and dc power supply. The dc power supply converts the ac input into the dc voltages necessary for drive operation.

Power On Sequence

The power on sequence starts the drive motor and initiates loading of the heads. Figure 3-11 shows the circuits involved in this sequence and figures 3-11.1, 11.2, and 11.3 are flow charts of the operation.

The power on sequence begins when the operator presses the START switch. If all circuit breakers and interlocks are closed, pressing this switch deenergizes the hysteresis brake and energizes the Start and Run triacs. This causes the drive motor to start. The drive belt transfers drive motor motion to the spindle, thereby, causing the disk pack to rotate.

When pack speed reaches about 2800 r/min, the Up To Speed signal goes active and energizes the emergency retract relay (K2). Energizing this relay connects the voice coil to the power amplifier. This puts the voice coil under control of the servo system, thus allowing the heads load sequence to begin whenever the 25 second heads load delay (triggered when the START switch is pressed) times out. Details of the heads load sequence are given in the First Seek discussion.

Power Off Sequence

The power off sequence unloads the heads and stops the drive motor. Figure 3-11 shows the circuits involved in this sequence and figure 3-11.4 is a flow chart of the operation.

The power off sequence begins when the START switch is pressed. This enables the RTZ logic (see RTZ Seek discussion) and cause the heads to move in the reverse direction.

When the heads unloaded switch indicates the heads are unloaded, the following events occur:

- The RTZ logic is disabled.
- The run triac (K1) is deenergized to remove power from the drive motor run winding.
- The hysteresis brake is energized and applies a braking action to the drive motor.

Removing power from the run winding and energizing the brake cause the drive motor and therefore the disk pack to slow down. When pack speed is less than 2800 r/min the Emergency Retract relay (K2) deenergizes. This disconnects the voice coil from the power amplifier and connects it to the emergency retract circuit. The emergency retract circuit input pulls the heads back to the fully retracted position.

The drive motor continues to slow down and comes to a complete stop within 30 seconds of the start of the sequence. This leaves the drive in a standby condition with the blowers on and dc power active.

Emergency Retract and Data Protection

Certain emergency conditions could occur which require immediate disabling of the write cirucits and full retraction of the heads. These conditions are:

1. Loss of ac power.
2. Opening of the pack cover interlock.
3. Loss of spindle motor speed.
4. Loss of any of these dc voltages; ±5, ±12, ±20, or ±42.

Emergency Retract Circuit

The heads are retracted under emergency conditions to prevent damage to them if the disk speed is reduced. A velocity servo circuit (Figure 3-10) is used to retract the heads at approximately 20 ips. When relay K2 is deenergized as described in the following paragraphs, the voice coil is then connected to the emergency retract circuit. Input to the velocity circuit is received from the velocity transducer. If

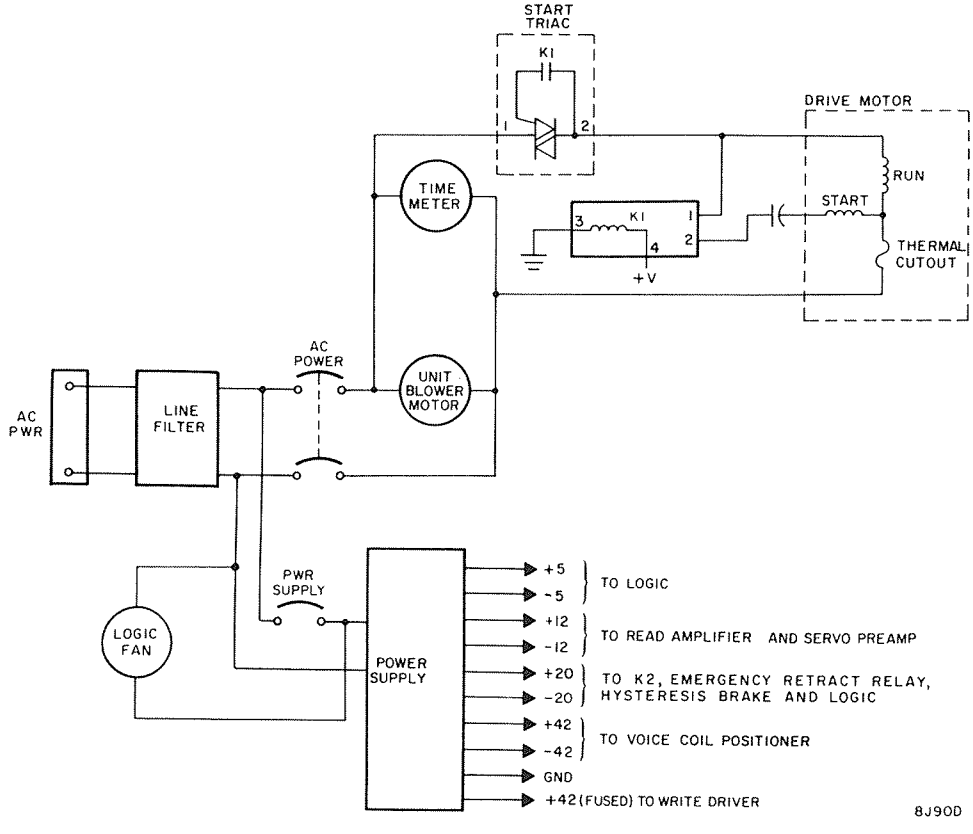


Figure 3-10. Power Distribution

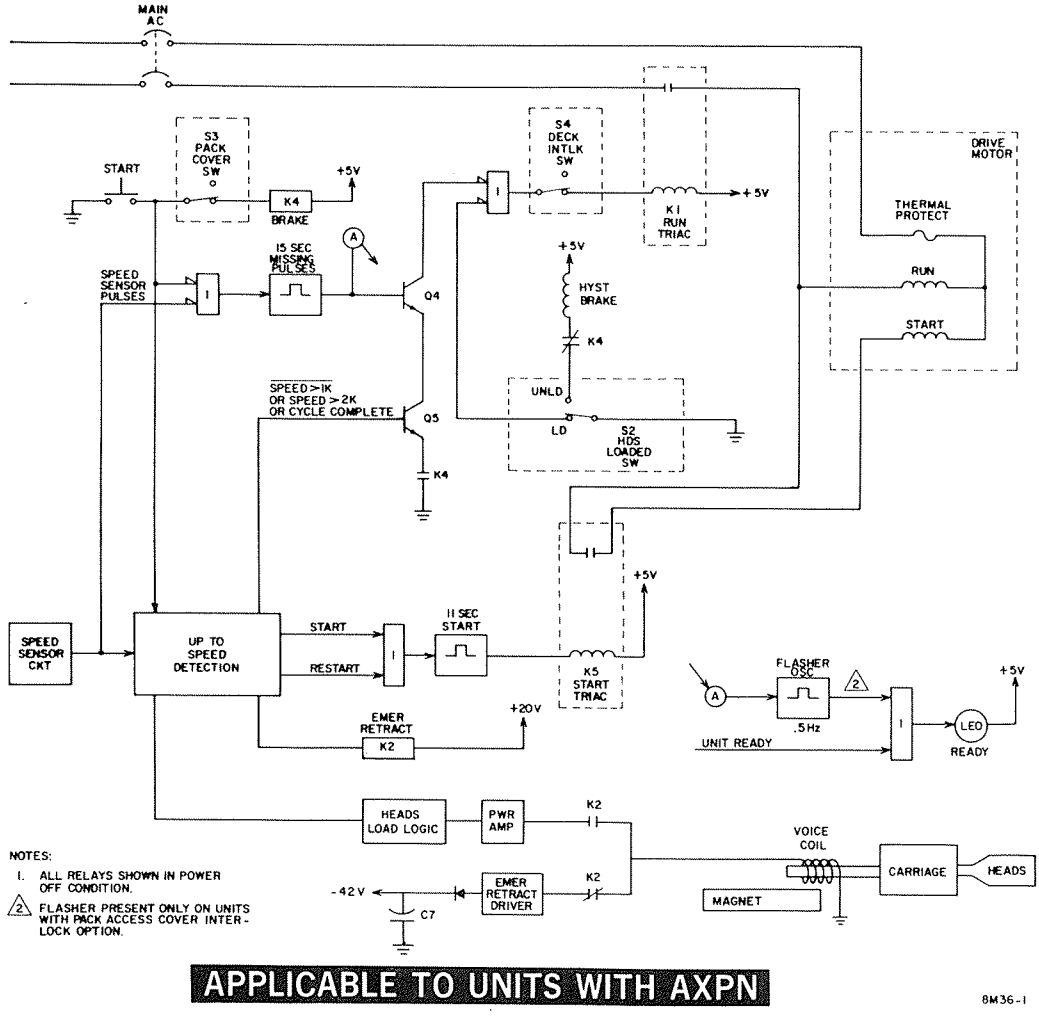


Figure 3-11. Power On Sequence Circuits (Sheet 1 of 3)

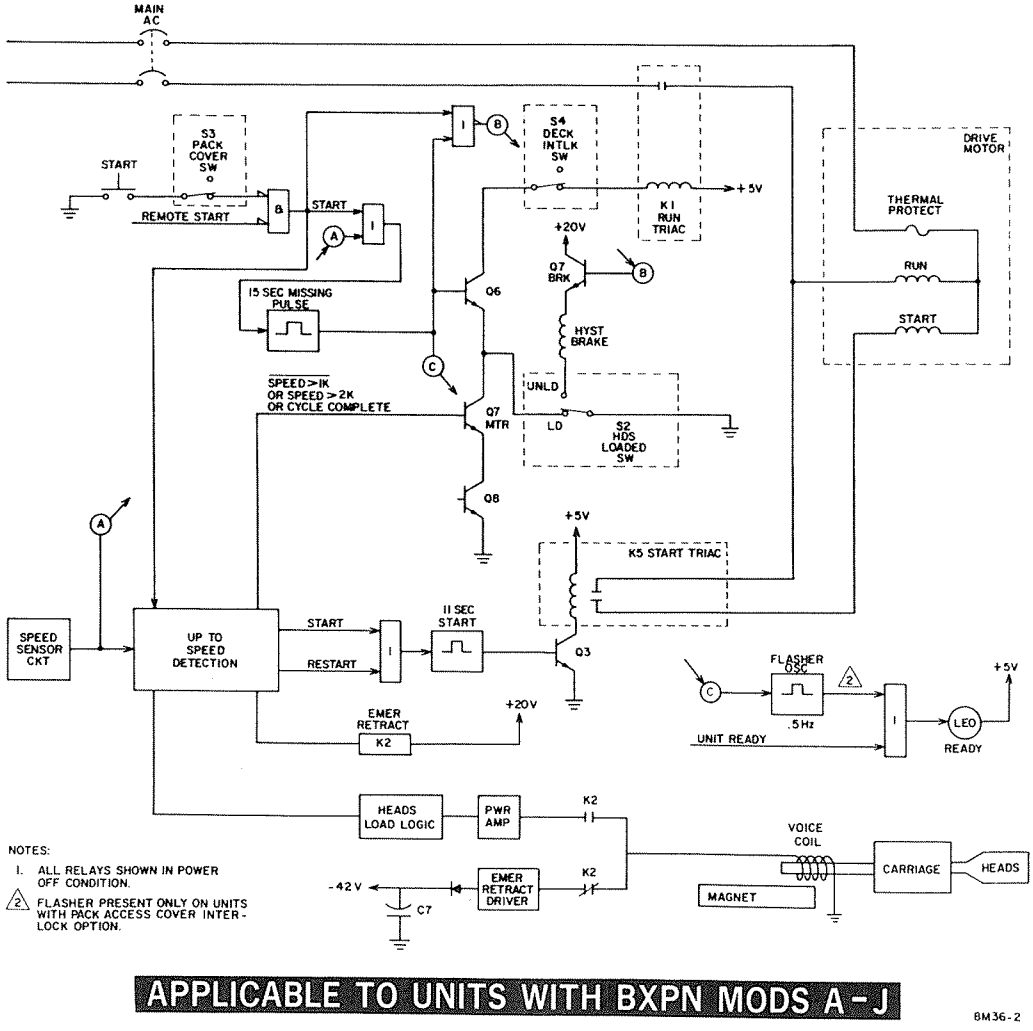


Figure 3-11. Power On Sequence Circuits (Sheet 2)

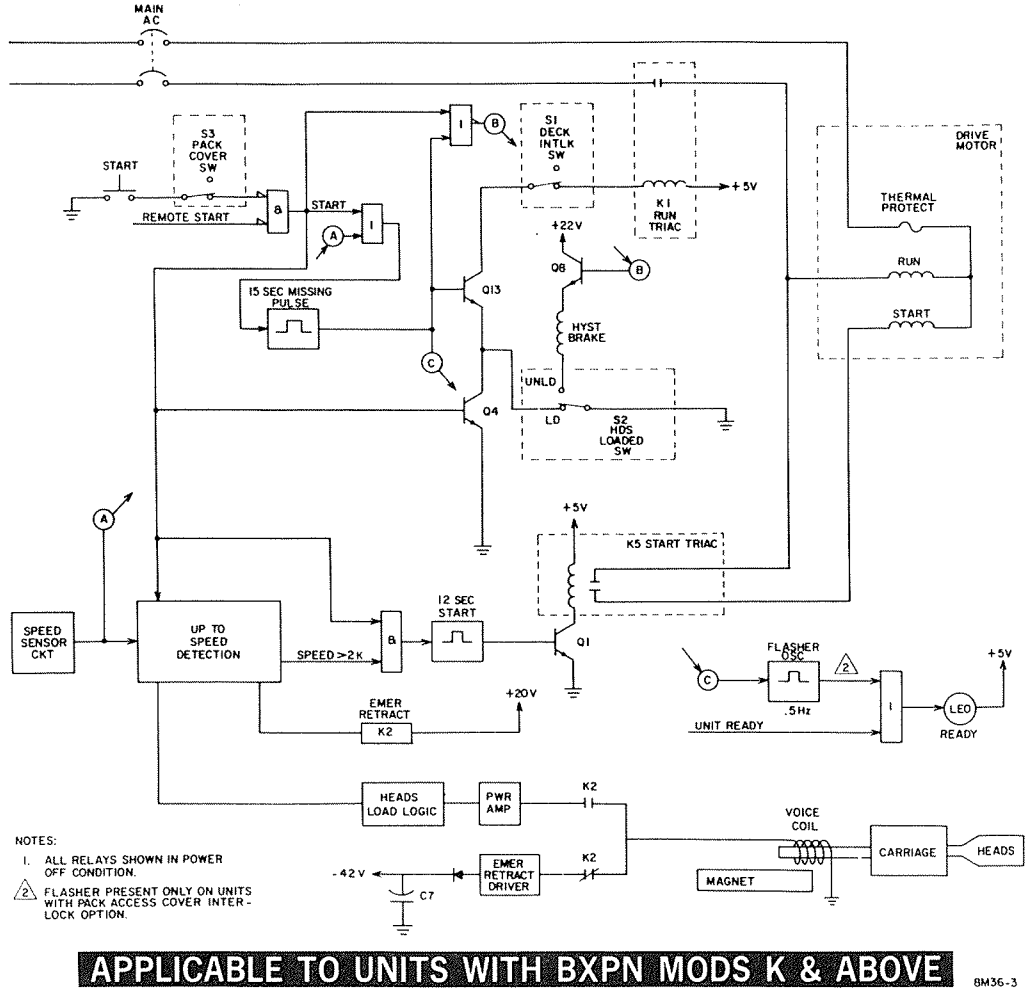


Figure 3-11. Power Sequence Circuits (Sheet 3)

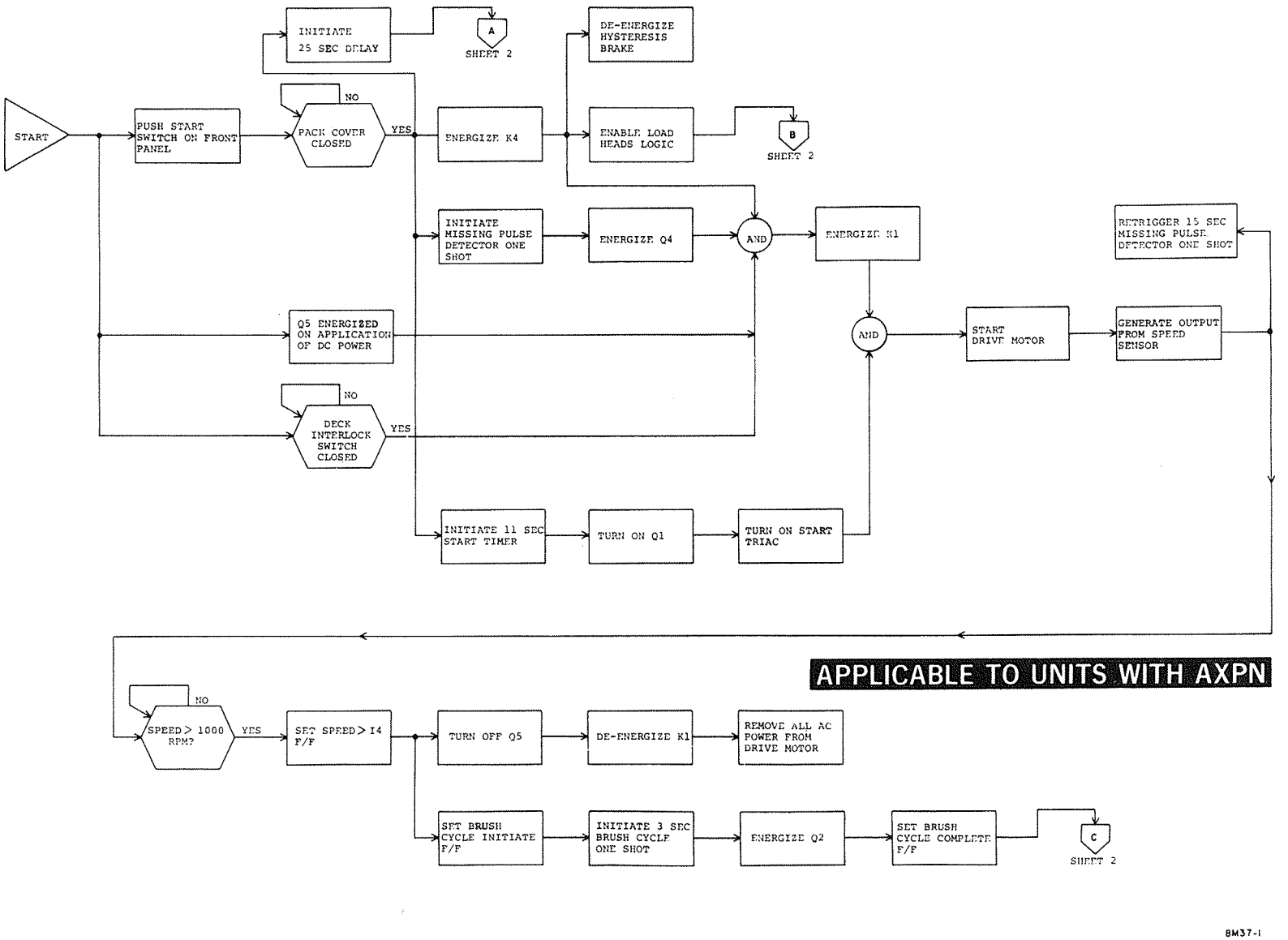


Figure 3-11.1 AXPN Power On Sequence Flow Chart (Sheet 1 of 2)

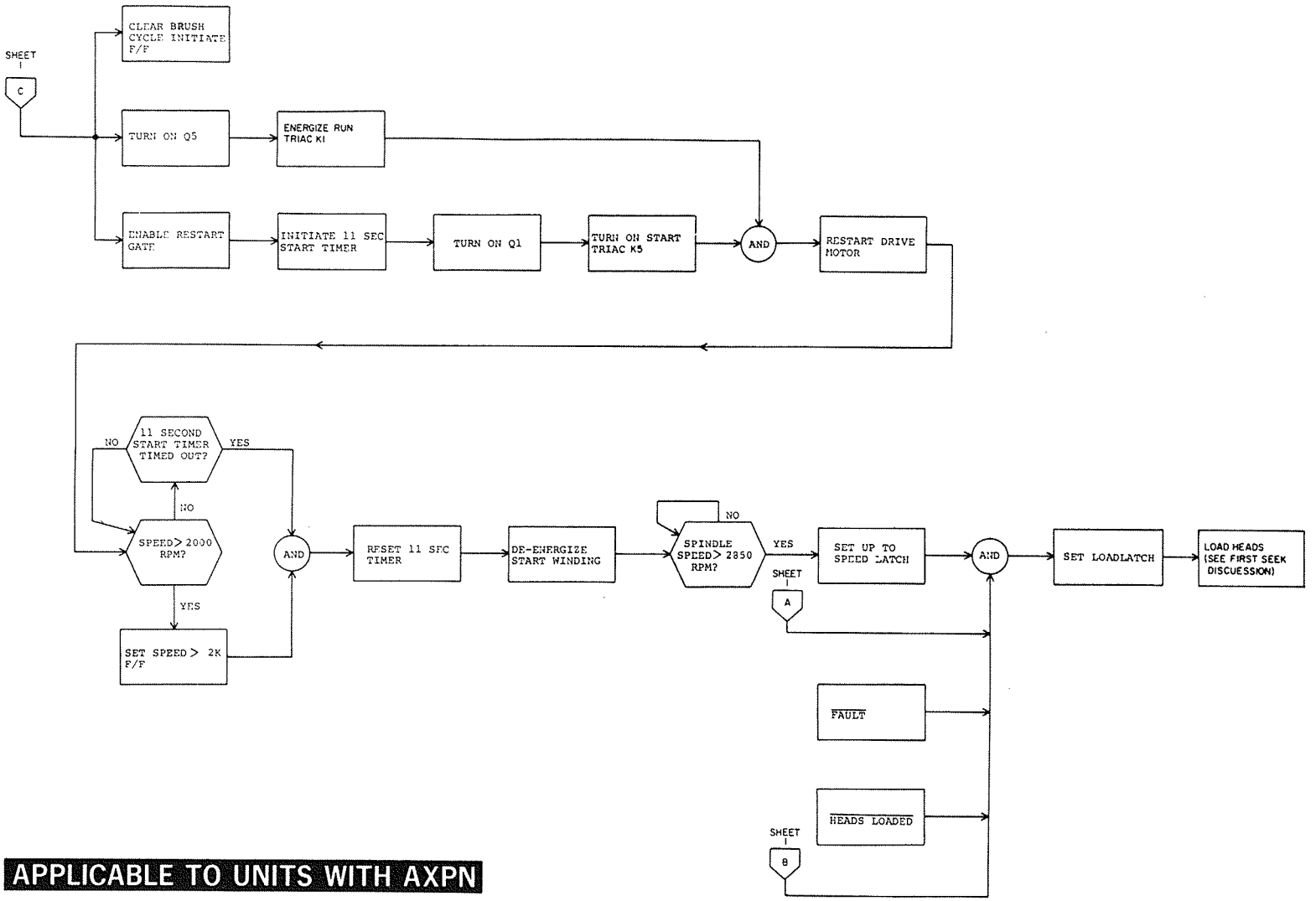


Figure 3-11.1 AXPN Power On Sequence Flow Chart (Sheet 2)

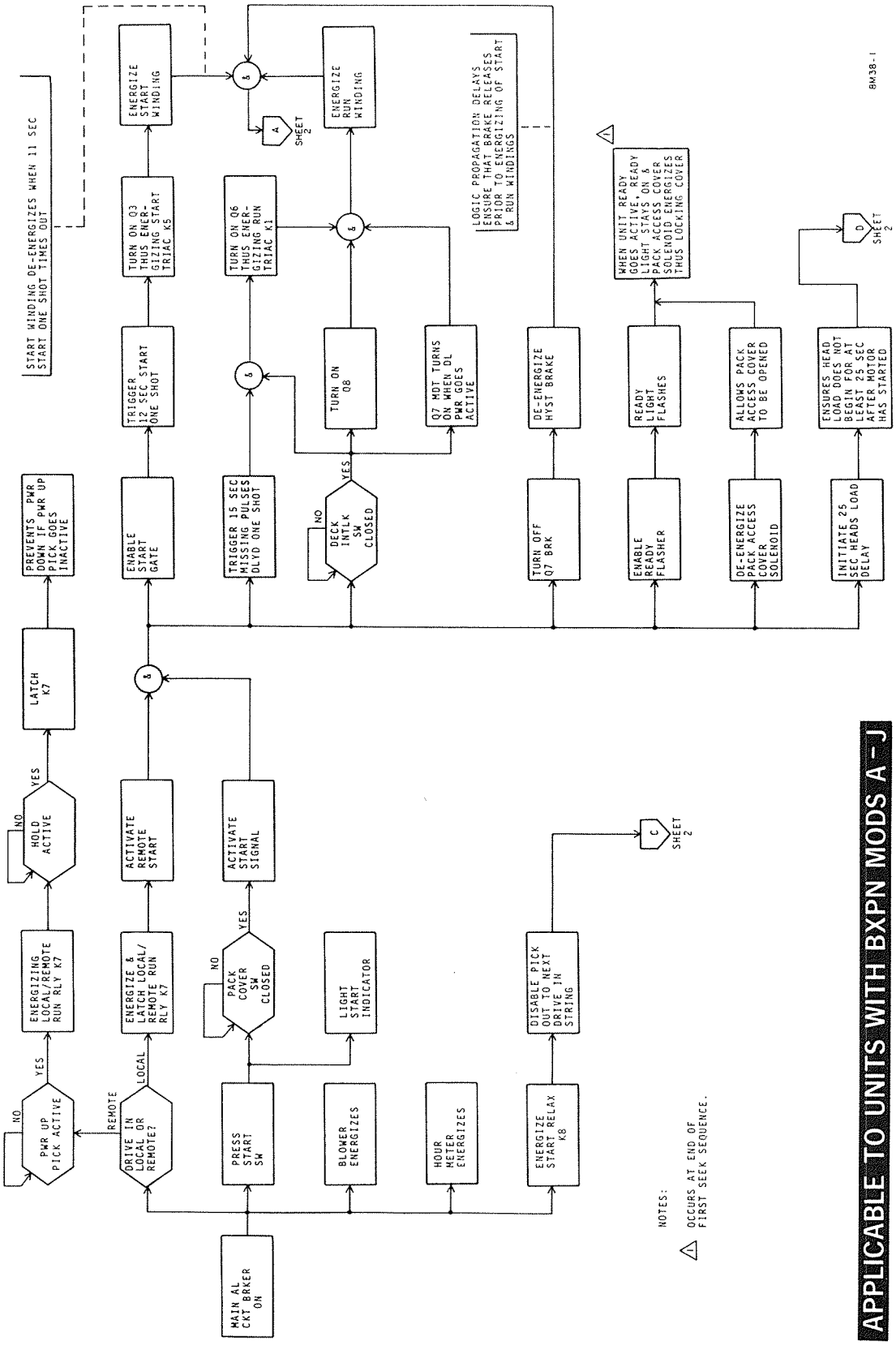
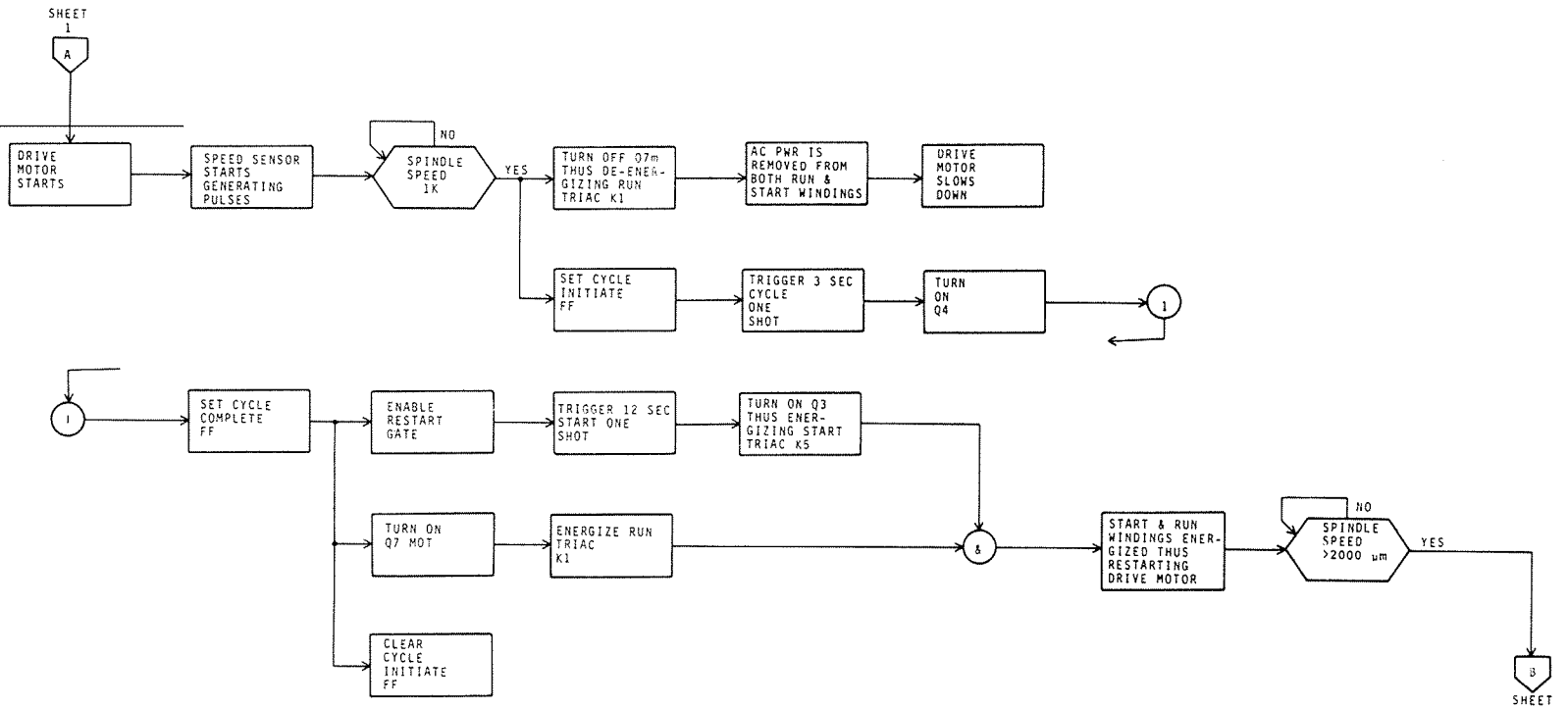


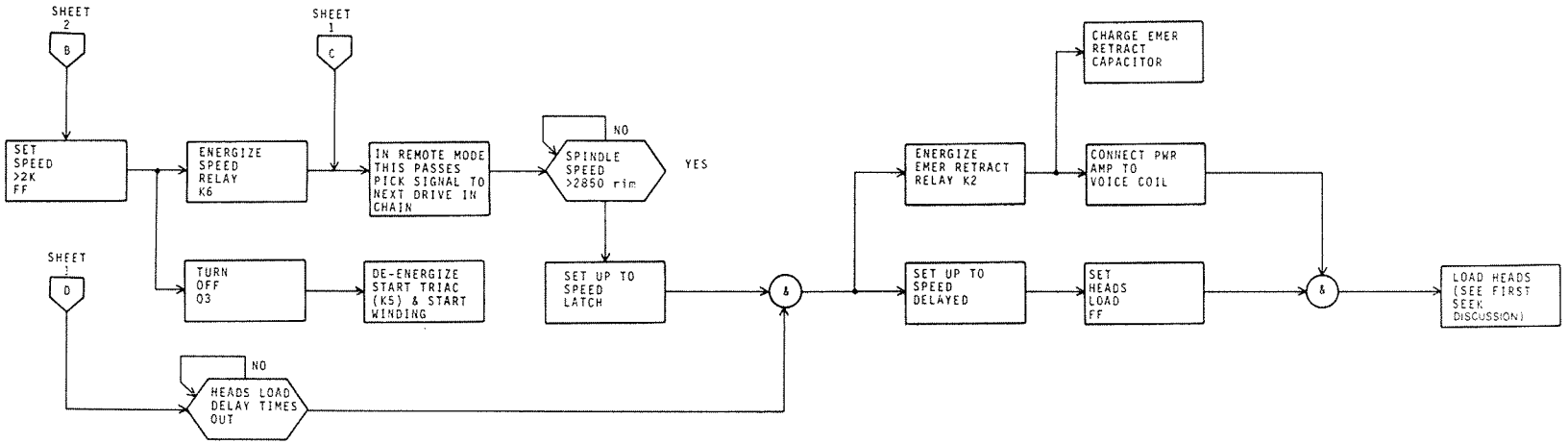
Figure 3-11.2. BXPN A-J Power On Sequence Flow Chart (Sheet 1 of 3)



APPLICABLE TO UNITS WITH BXPN MODS A - J

8M38-2

Figure 3-11.2. BXPN A-J Power On Sequence Flow Chart (Sheet 2)



APPLICABLE TO UNITS WITH BXPN MODS A-J

BM38-3

Figure 3-11.2. BXPN A-J Power On Sequence Flow Chart (Sheet 3)

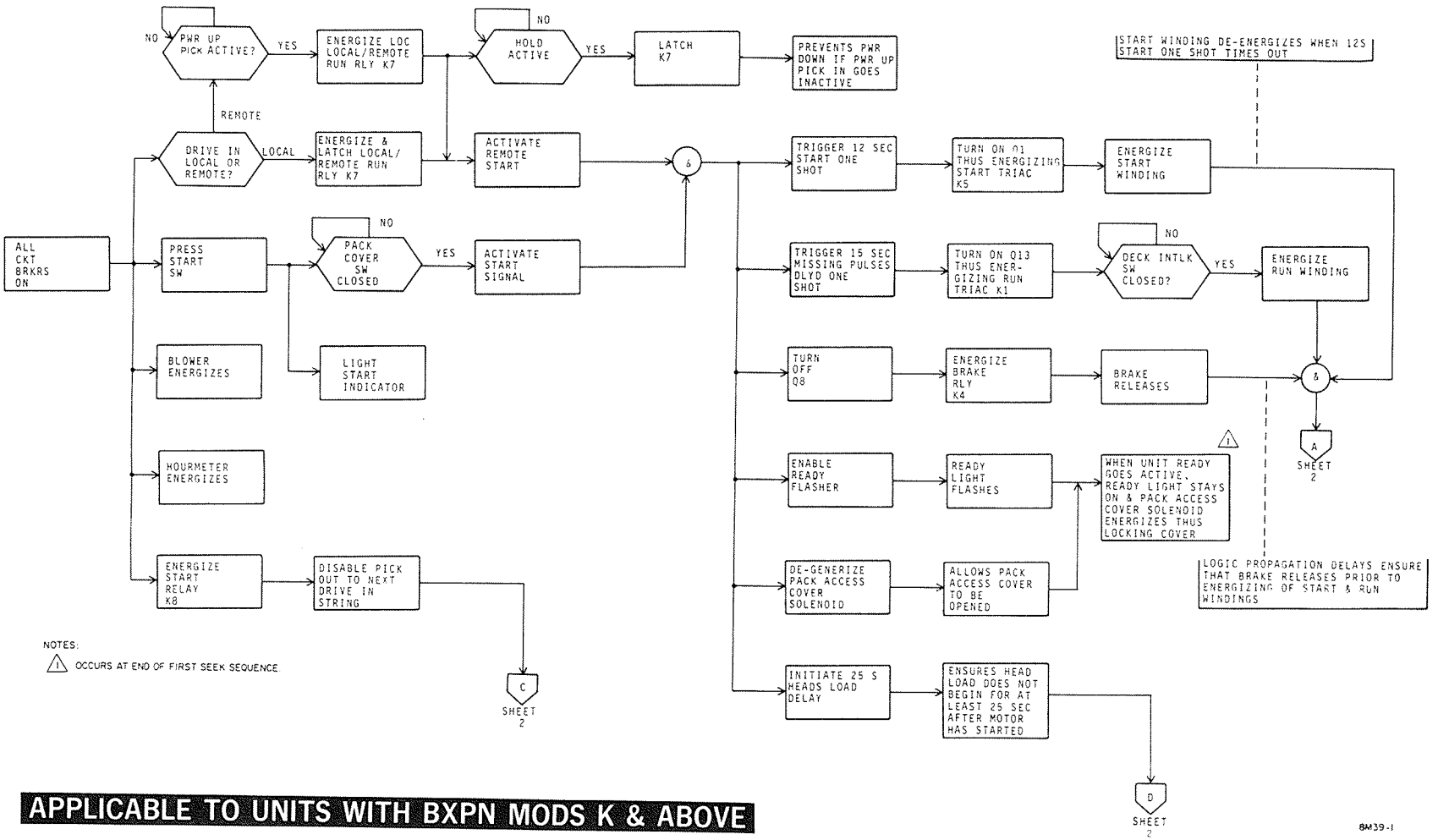


Figure 3-11.3. BXPN K & Above Power On Sequence Flow Chart (Sheet 1 of 2)

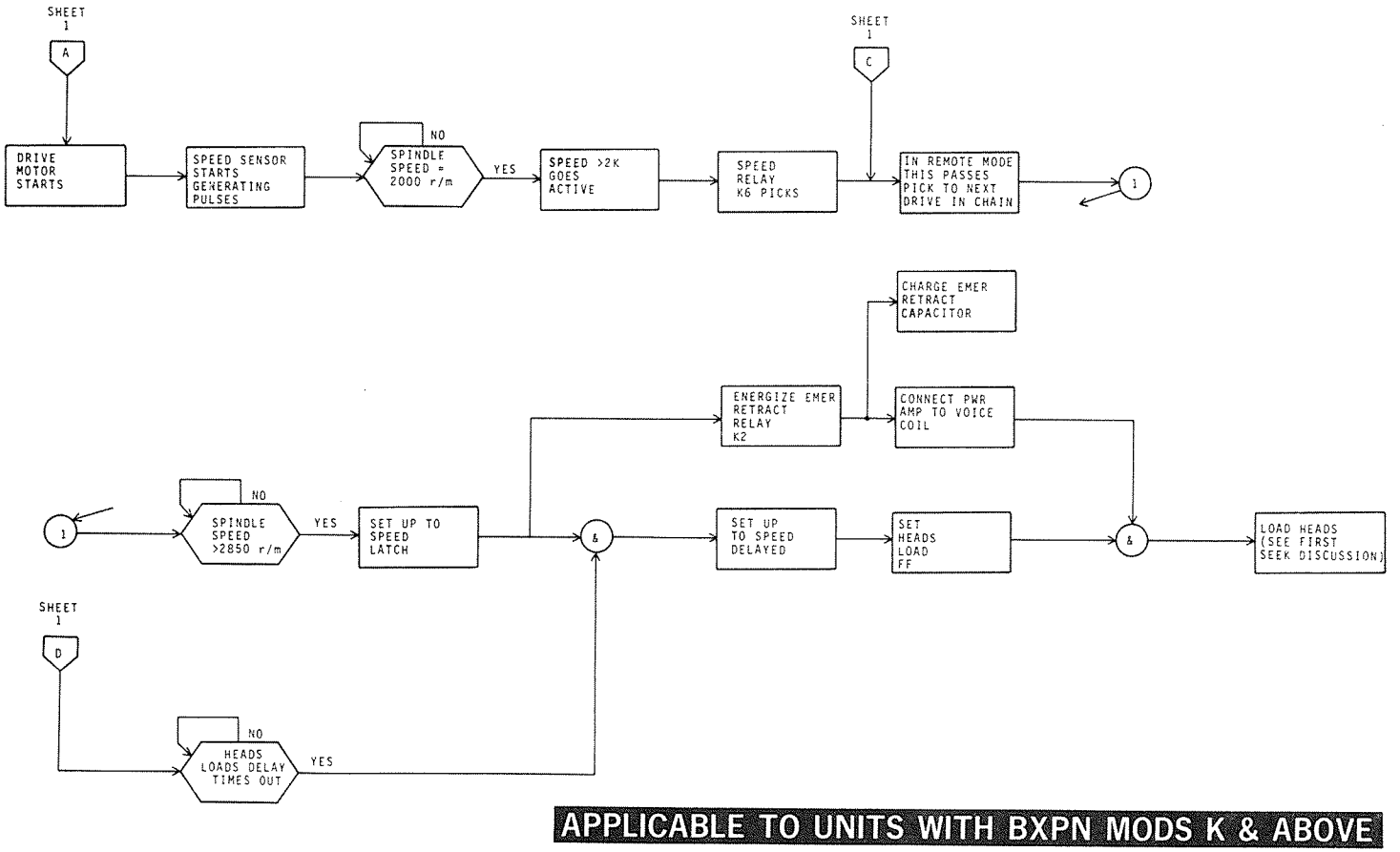


Figure 3-11.3. BXPN K & Above Power On Sequence Flow Chart (Sheet 2)

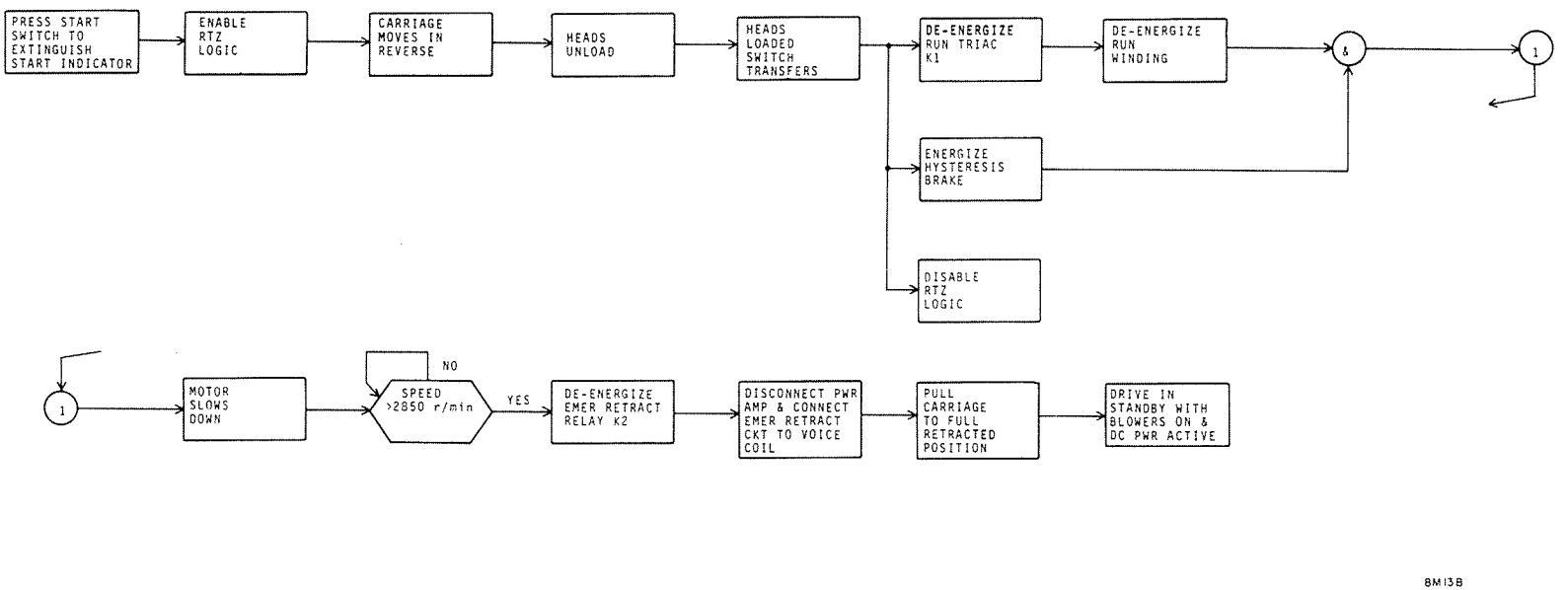


Figure 3-11.4. Power Off Sequence Flow Chart

the heads are positioned over a track or moving to any other track, the output of the transducer is respectively zero or a negative voltage. This voltage is applied to an operational amplifier, which controls the application of -42 vdc to the voice coil. The feedback loop controls the current to the voice coil while retracting to maintain a maximum velocity of 20 ips. When the heads loaded switch transfers, a FET switch turns off the operational amplifier, and the circuit removes the -42 vdc from the voice coil.

Loss of AC Power

Loss of site power results in:

1. The dc power supply outputs dropping to zero.
2. De-energizing all relays and disabling the logic.
3. Transferring the contacts of K2 to provide a path from the emergency retract circuit to the voice coil. This circuit pulls the carriage back to its retracted stop.

Loss of ac power at the AC POWER circuit breaker or within the unit results in the loss of spindle speed (see below).

Loss of Spindle Speed

If the spindle motor speed drops below 2500 rpm, the speed detection circuit in the logic detects the speed loss and opens relay K2. This connects the voice coil to the emergency retract circuit.

Loss of DC Power

Fault circuitry in the logic detects the loss of dc voltage outputs from the power supply. Relay K2 is then opened either by the logic or directly by the loss of +20 vdc, thus connecting the emergency retract circuit to the voice coil. If the +12v power is lost, servo dibits will not be detected and after approximately 350 ms the heads are unloaded. A Fault indication will appear on the control panel.

SEEK OPERATIONS

Seek operations are those drive functions that cause a repositioning of the read/write heads. The heads are attached to the actuator which, in turn, is moved by a voice coil positioner. The mechanical elements involved in the mechanism are described in the assembly portion of this section.

Two logic circuits are used to control the seek function:

1. The Servo Circuit, which controls the voice coil positioner.
2. The Track Servo Circuit, which generates signals relating to the position of the heads over the disk pack.

The general concepts of these two circuits are explained to provide the general background information needed to understand the specific types of seeks. Then more detailed explanations are provided for the three types of seeks: Load, Direct Seek, and Return to Zero Seek.

Servo Circuit

The servo circuit is a closed loop servomechanism used to position the read/write heads. Figure 3-12 is a simplified schematic of the servo circuit. Functions of the major elements of the system are explained in Table 3-2.

A servo loop sums all of the error voltages imposed on it. The loop always attempts to maintain itself at a null. If not nulled, the loop will adjust the correctable device (in this case, the voice coil positioner) to achieve this null. Signals applied to the loop are called error voltage. Two major error voltages are used:

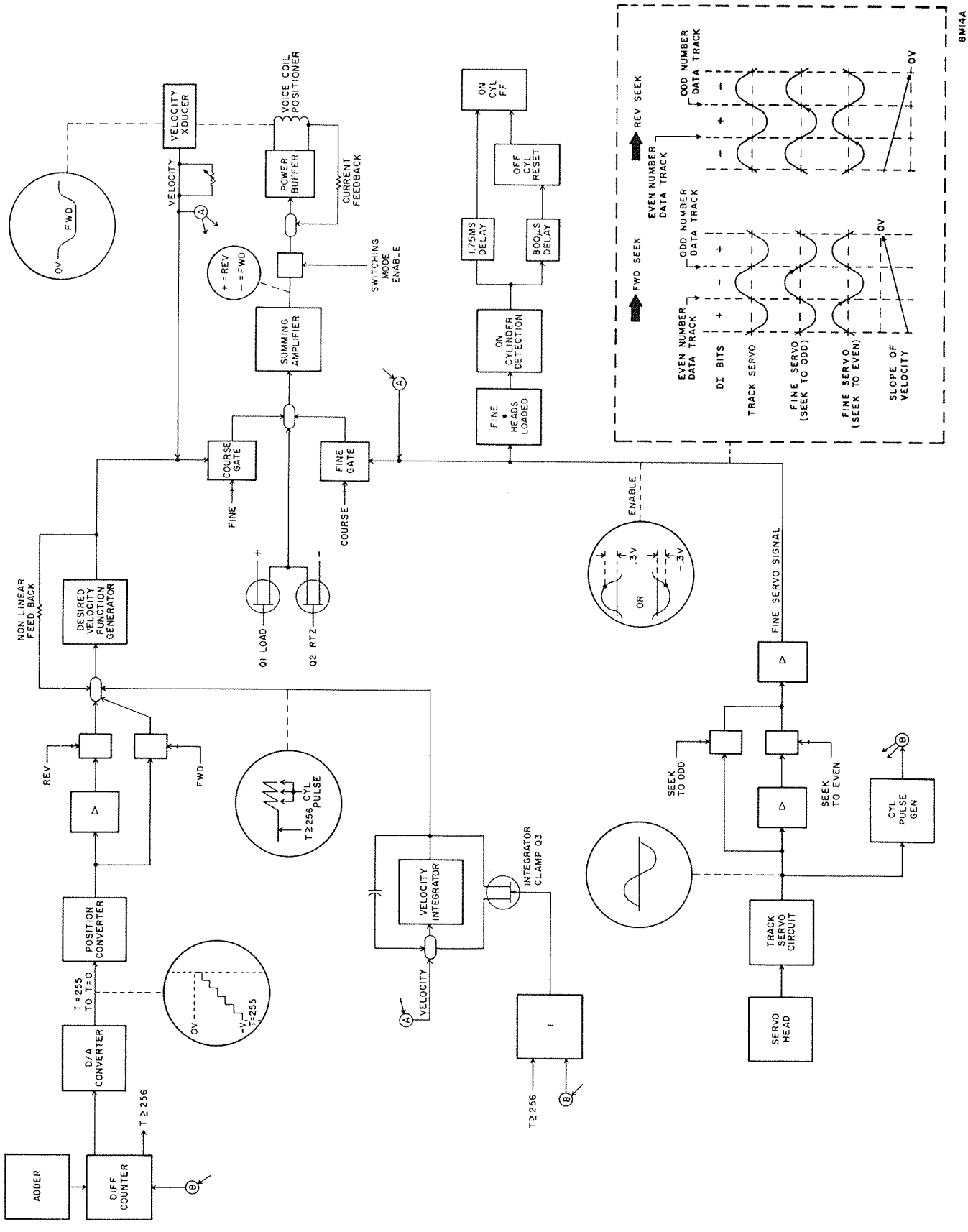


Figure 3-12. Track Servo Circuit

TABLE 3-2. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Cylinder Address Register	Holds the present cylinder address. It is updated to the new cylinder address when a seek is initiated.
Cylinder Address Adder	Combines the present cylinder address with the new cylinder address complement to arrive at the difference.
Difference Counter	Holds the number of tracks yet to be crossed before reaching the desired track or cylinder. Counter value is zero when on cylinder.
Digital-to-Analog Converter	Monitors the seven lowest order bits of difference counter to provide an analog indication of Position Error during the last 256 tracks (except last track) of all Seek operations.
Position Converter	Provides coarse Position Error signal, the amplitude of which is proportional to the number of tracks to go. Amplitude is clamped at negative saturation while tracks remaining are equal to, or greater than 256. Amplitude decreases in discrete steps (controlled by D/A converter) as last 256 tracks of a seek are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes Position Error signal at gain levels that vary as Position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control to deceleration. The parallel nonlinear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems. It also minimizes drift about null.
Summing Amplifier	Generates a control signal to drive the power amplifier. When Position Error exceeds Velocity Amplifier signal, control signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Switching Mode Control	Decelerates carriage from tracks equal 256 to tracks equal 7 by supplying pulses of maximum reverse current to the voice coil to follow Position Error deceleration curve.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity of 7 ips.
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity of 7 ips.
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.

TABLE 3-2. SERVO CIRCUIT FUNCTIONS (Cont'd)

Circuit Element	Function
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. Also receives a negative feedback from positioner which acts to cancel current coupling that occurs from the velocity transducer location within the magnetic field created when current is applied to the voice coil positioner. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retraction position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 256 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Fine Servo and Fine Latch	Fine servo monitors integrated velocity. When difference counter is 1 (T=1) and integrated velocity exceeds 1.4v, it indicates that there is one-half track to go. Fine latch sets to enable fine gate and disable coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine position (fine gate). Fine also has the following effects: a. Turns on integrator clamp to switch off velocity integrator. b. Enables on cylinder detection. During load or RTZ sequences, both outputs of Fine Latch are high. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Bit 0 Address Register and Slope FF	Used to select proper track servo signal phase for use as Fine Position Analog signal (signal controlling servo loop as last track is approached and carriage is stopped). If bit 0 is not set, the seek destination is an even numbered track and the track servo signal will not be inverted for use in stopping the carriage. If bit 0 is set, an odd track is identified and track servo is inverted. Register bit content is placed in Slope FF which performs actual gating.
On Cylinder Detector	Monitors fine position signal when $T \leq 1$. When signal is less than about 0.98v, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is returned to controller and to drive logic. If heads overshoot at end of seek so that voltage exceeds 1.61v,delay is re-initiated. Delay permits carriage to settle out before controller may attempt any read/write operations.

1. A position error: this is the departure of the positioner from the desired position.
2. A feedback signal to modify (or oppose) the position error to cause a smooth motion of the positioner.

The position error signal is provided by the position converter and its allied elements. The amplitude of the signal is proportional to the distance from the present position to the desired position (tracks-to-go). The major feedback signal is the output of the velocity transducer. The amplitude of this signal is proportional to the velocity of the positioner while the polarity indicates the direction of motion, forward or reverse.

The loop applies its position and feedback signals to one point, the summing amplifier. If the summation of these signals is not equal to zero, the summing amplifier outputs a signal proportional to the amplitude of the error voltage (which signifies the amount of displacement from the desired position) and the phase of the error voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the actuator drive amplifier assembly. The actuator contains a voice coil positioner that supports and moves the read/write heads. In turn, the voice coil is located within a powerful magnet. Whenever a current passes through the voice coil windings, the interaction of the induced emf and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.

Basic Seek Operation

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see Figure 3-13).

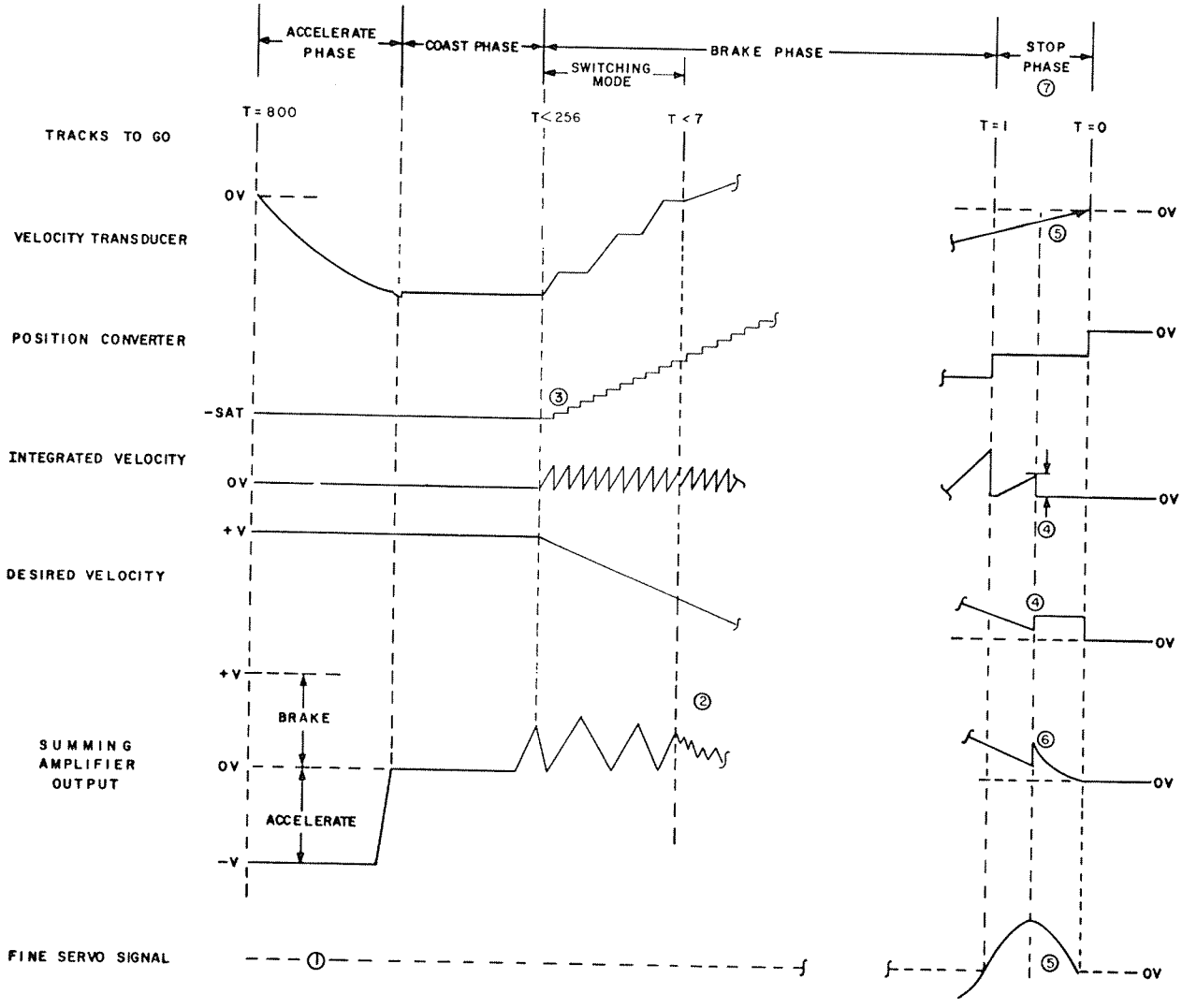
1. Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.
2. Coast Phase: velocity is at its maximum and the positioner velocity is constant.
3. Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.
4. Stop Phase: The positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Accelerate Phase: This phase is controlled largely by the position error signal. The controller sends the desired address to the cylinder address register and adder. The adder combines the new address complement with the present address to arrive at the difference. The difference is gated into the difference counter, which decrements until tracks-to-go equals zero.

The seven low-order bits of the difference counter are applied to the position converter. The value of these bits indicates the position error (or tracks-to-go) from 0 to 256, that is, the amplitude of the position converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 256 ($T \geq 256$), the position converter output is clamped at its maximum saturated value to cause a very large position error.

The input to the summing amplifier is now a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration.



NOTES:

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS.

② GAIN CHANGE CAUSED BY ADDITION OF INTEGRATED VELOCITY SIGNAL TO POSITION CONVERTER SIGNAL.

③ OUTPUT DECREASES WITH EACH CYLINDER PULSE.

④ FINE LATCH SETS WHEN $T \leq 1$ AND INTEGRATED VELOCITY > 1.4V. DESIRED VELOCITY HAS NO FURTHER EFFECT.

⑤ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER.

⑥ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑦ SCALE CHANGED AT T=1 FOR CLARITY.

8. DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

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Figure 3-13. Servo Circuit Signals

As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less. Acceleration continues.

Coast Phase: Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.

Deceleration Phase: Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each cylinder is passed. These pulses are used to decrement the difference counter.

When $T < 256$, the servo loop changes to the switching mode to maintain speed along desired velocity curve. This curve is the analog version of the number of tracks-to-go.

The velocity curve is generated by the desired velocity function generator. Its output is compared with velocity to achieve maximum deceleration under all conditions without overshoot. The deceleration curve permitting the best control is obtained by taking the square root of the position signal and comparing it with velocity. The position signal is the sum of the following:

1. The position error signal from the position converter. Its output, which is now unclamped, is a signal whose amplitude is proportional to the number of tracks-to-go.

2. Integrated velocity from the velocity integrator. Integrating a velocity signal provides a signal proportional to distance. This signal is a sawtooth waveform: it is pulled back to zero by each cylinder pulse and increases in proportion to velocity and time (distance). The combination of the stepping-down output from the position converter with the ramp integrated velocity signal results in a smooth curve of constantly-decreasing magnitude.

3. The square root function provided by the non-linear feedback around the desired velocity function generator.

When the desired velocity signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous desired velocity value. The current to the voice coil is then turned off and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the desired velocity signal). If the carriage velocity becomes too high for the existing desired velocity signal, a maximum reverse current is again applied until the velocity slows down below the instantaneous desired velocity value.

At $T \leq 7$ the switching mode logic is disabled and the total summing amplifier output is used to decelerate the carriage to keep the Velocity signal/Position Error signal difference to zero.

Stop Phase: Stop Phase begins when the difference counter indicates that there is one track-to-go. When $T=1$, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the fine gate. Desired velocity is disabled since the coarse gate is opened by Fine being set.

The last half-track of motion is controlled by the fine position analog signal from the track servo

circuit. Fine position and velocity are applied to the summing amplifier through the fine gate. The summing of these two signals controls the braking current.

At the start of the seek, the slope FF is set if the seek is to an odd-numbered cylinder. The slope signal controls the phase of the track servo signal applied to the fine position amplifier. This adjustment is required since track servo signal phasing is a function of the servo head position: the signal is positive when over negative dibits and negative when over positive dibits. Therefore, on forward seeks, the signal decreases when approaching a data track with an odd number and increases when approaching a data track with an even number. The opposite is true during a reverse seek.

Phasing of the track servo signal is selected so that the fine position signal opposes the velocity signal during the last half-track of the seek. Both signals are decreasing. If either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the fine position signal is less than about 0.98v, the positioner is, for all practical purposes, positioned over the data track. This initiates the On Cylinder delay. After 1.75 ms, On Cylinder is returned to the controller.

The fine servo remains active even though On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move, one dibit signal will increase in amplitude. This results in a slight track servo signal which is translated into the fine position signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause a fine position signal greater than 1.61v for more than 800 μsec, the On Cylinder signal is lost.

The loop also permits positioner offset if the program requires it for error recovery. A Servo Offset Negative (bit 3) code will provide a negative bias input to the fine position amplifier. This is now an error signal to the summing amplifier to cause a forward motion. This motion stops when the bias voltage and track servo voltage cancel. Servo Offset Positive (bit 2) causes reverse offset.

The distance of the Servo Offset is preset for 250 microinches, forward or reverse. Bit 2, Tag 3, forces the actuator away from the spindle. Bit 3, Tag 3 forces the actuator toward the spindle.

Short Seeks

The preceding explanation assumed that the seeks were long enough for the positioner to attain maximum velocity. Maximum velocity of about 70 ips requires 200 tracks acceleration time. During short seeks, gating is identical although relative phasing of the error signals will vary.

During seeks less than 256 tracks, certain signals are available immediately: integrated velocity, nonlinear feedback to the desired velocity function generator, and a position converter output not clamped at its maximum value. These signals generate a position error voltage to accelerate the positioner. Because the amplitude of the desired velocity signal is less, however, the voice coil current is not as great as during long seeks.

The net effect of these differences is that system gain is reduced. Acceleration is reduced accordingly to permit minimum total seek time while not

permitting overacceleration that would cause overshoot. The primary function remains unchanged: acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

Track Servo Circuit

Basic Description

The track servo circuit provides head positioning information. The signals generated by this circuit:

1. Generate a track servo signal that indicates the displacement of the heads from their nominal track centerline.
2. Generate cylinder pulses during seeks to indicate each cylinder crossing.
3. Generate indications that the heads are positioned outside of the normal data cylinders.

Information for this circuit is derived from the track servo head (figure 3-14). This is physically similar to the read/write heads, except that it does not write. The head reads information from the servo track surface of the disk pack. This information is known as dibits; dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the other five disk pack recording surfaces.

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

There are 883 dibit tracks on the servo surface. At the outer edge of the surface is a band of 24 positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. Then, there are 823 servo tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are 36 tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

Circuit Description

The basic elements of the track servo circuit are illustrated in figure 3-15 while table 3-3 explains their functions.

Dibit Gating: After being differentially amplified, the servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (figure 3-16). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. This component triggers the Odd Dibits FF. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform. This component triggers the Even Dibits FF.

Track Servo Signal: The track servo signal indicates the displacement of the servo head from the on-track position. When the head is centered between dibit tracks, this signal is at a null. It swings in the positive direction when the amplitude of the even (negative) dibits being sensed exceeds the amplitude of the odd (positive) dibits, and vice-versa. Amplitude is maximum when the head is centered over one dibit track, that is, the head is at its maximum distance from the centerline of the data track.

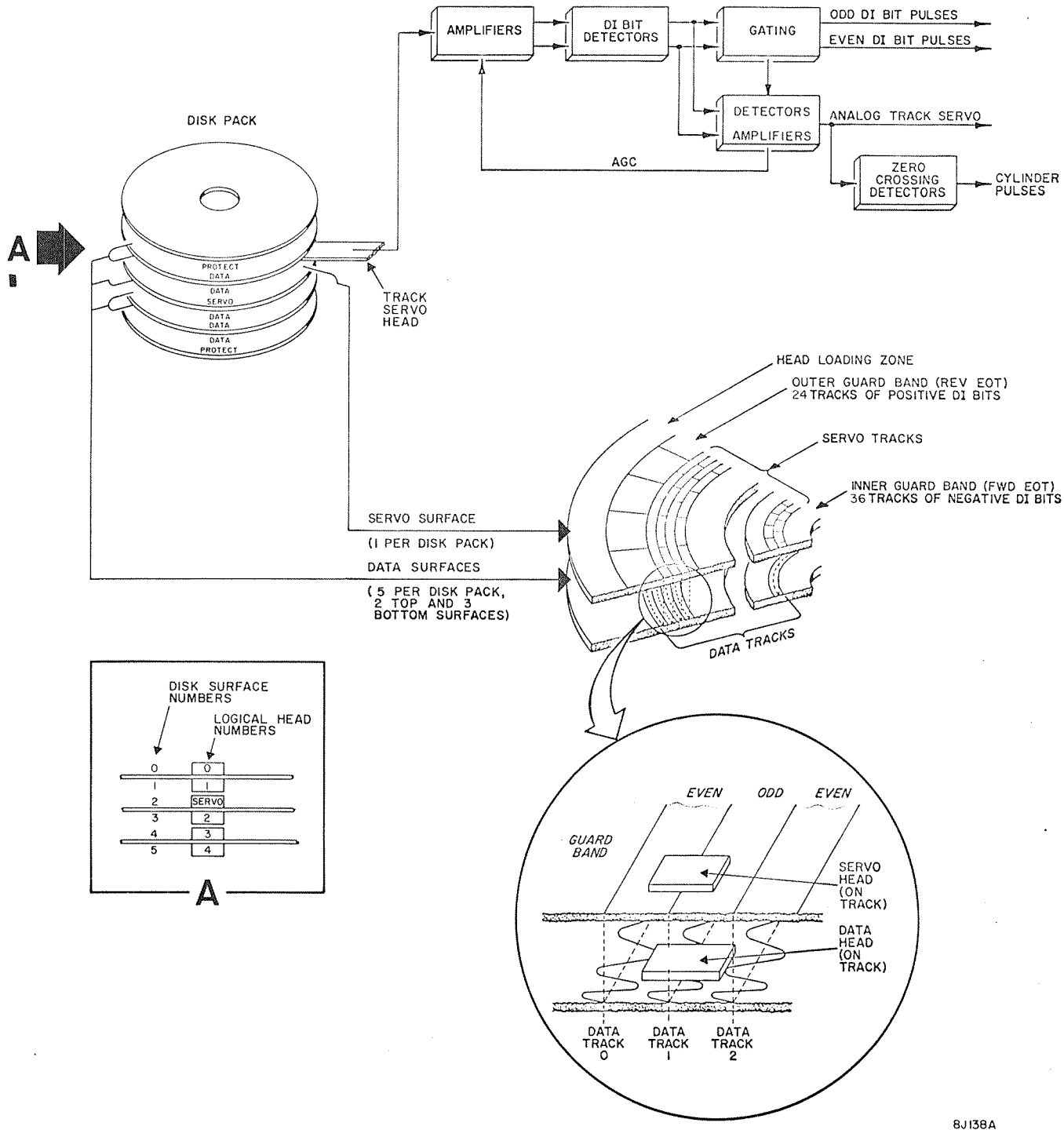


Figure 3-14. Track Servo Disk Layout

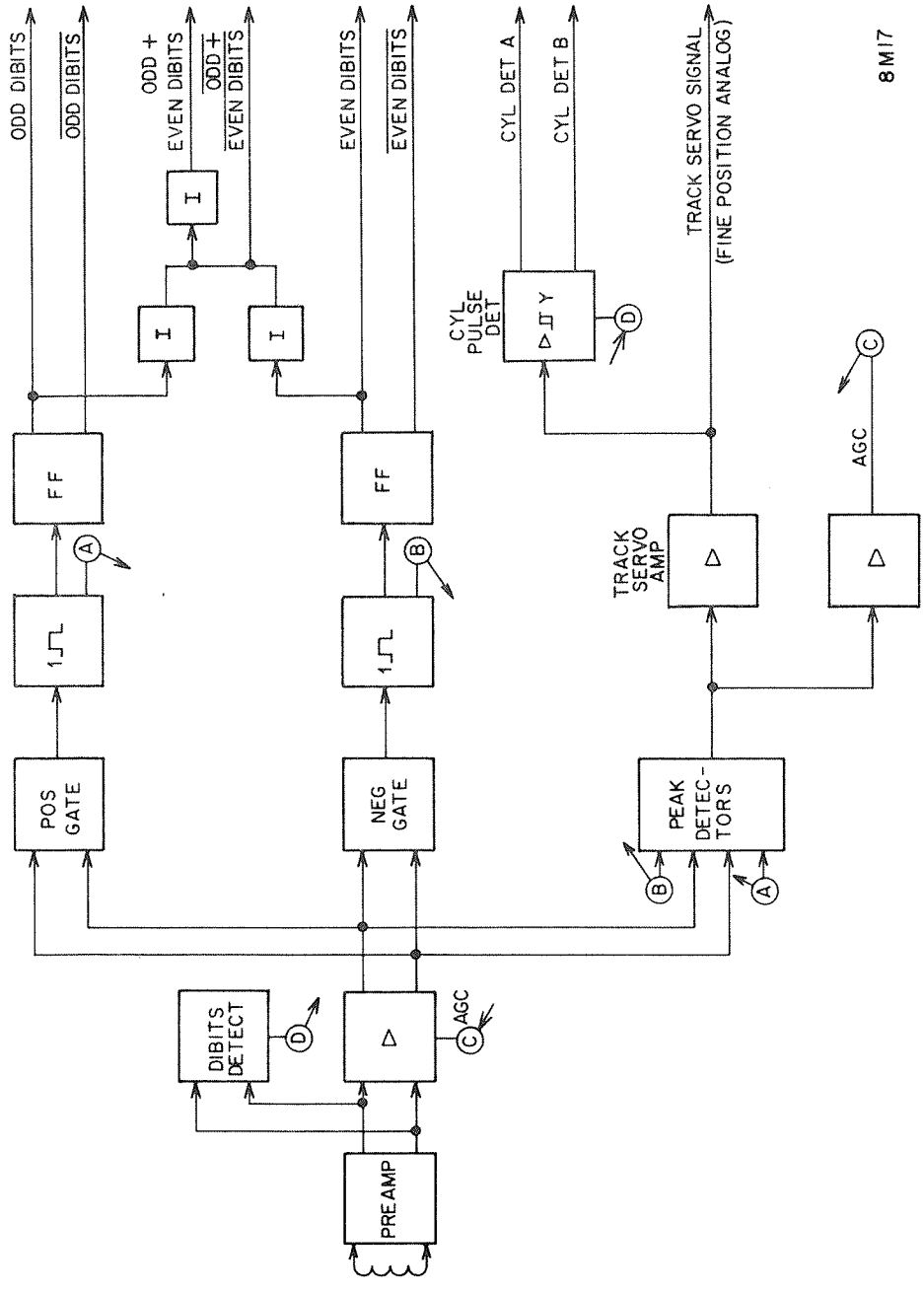


Figure 3-15. Track Servo Circuit

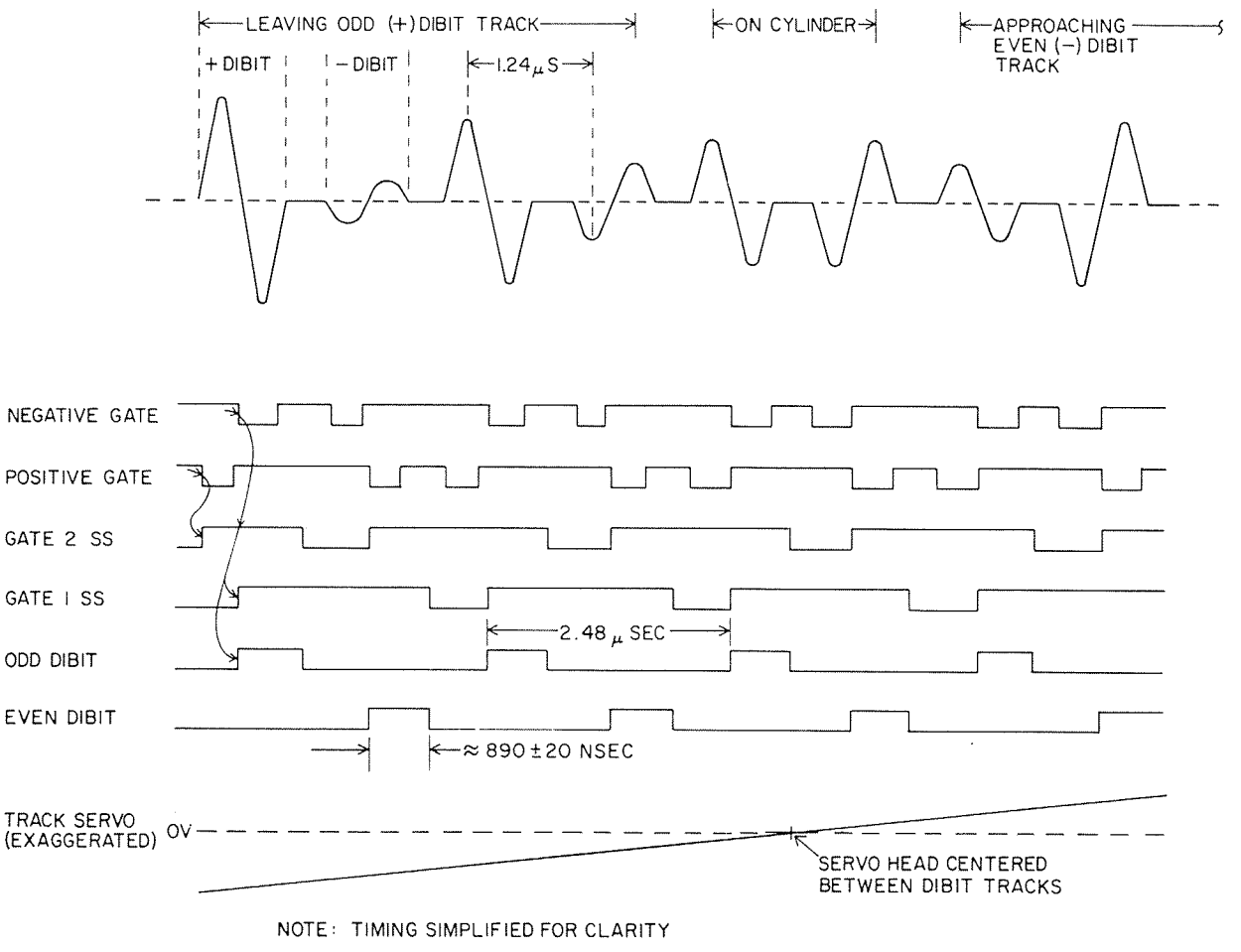


Figure 3-16. Track Servo Circuit Signals

TABLE 3-3. TRACK SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Track Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at the leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This fires the odd dibit one-shot. (Although the positive delay fires during negative dibits, a negative gate is not available immediately thereafter; the odd dibit one-shot is not enabled.) The negative delay functions in the reverse condition. These delays inhibit inputs to peak detectors so that they react only to the positive peaks of their respective dibits.
Even Dibits and Odd Dibits One-Shots	Provide 890 ±20-nsec pulses indicating dibits. Frequency of each one-shot is 403 kHz.
Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibit amplitudes: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - integrators are equal. As head moves from centered position, output from one integrator increases negatively while output from the other integrator becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportional to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Heads Loaded Detection	Provides positive signal when dibit amplitude is sufficient to indicate that heads are loaded over dibit tracks. Prior to this high output, positive/negative gates are inhibited to indicate no servo tracks detected. If dibits are not available within 350 ms after start of Load sequence (or if lost for 350 ms at any other time), no servo tracks FF sets. This initiates an RTZ sequence to unload heads and sets fault FF.
Track Servo Amplifier	Provides signal proportional to sum of + and - peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.

TABLE 3-3. TRACK SERVO CIRCUIT FUNCTIONS (Cont'd)

Circuit Element	Function
Cylinder Pulse Detection	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).
Velocity Integrator	Provides ramp signal proportional to distance travelled (velocity integrated with time). Output is positive-going during forward seek; negative-going during reverse seek. Output is pulled back to zero to reinitiate integrator function by each cylinder pulse, or during certain conditions of RTZ or Load sequences.
End of Travel (EOT) Detection	Monitors integrated velocity to enable EOT circuit. When velocity integrator output exceeds about 1.4v, heads have moved a distance of approximately two tracks without sensing any cylinder pulses.
Reverse EOT FF	Indicates that heads are positioned over outer guard band. Refer to First Seek and RTZS discussions for further details.
Forward EOT FF	Indicates that heads are positioned over inner guard band. This is an error condition.

The servo signal is generated by the peak detectors that monitor their respective dibits. If the positive dibit amplitude exceeds the negative dibit amplitude, the output of the + dibits peak detector is greater than that of the - dibits peak detector. The outputs of these two detectors are applied to a summing amplifier whose output represents the distance between the two detector outputs. This output is the track servo signal. The signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine position analog signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

Circuit gain control is achieved by applying the outputs from the peak detectors to a second summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the agc voltage. This signal is applied to the agc amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the agc, the less the resistance; therefore, more of the signal is shunted by the FET to reduce circuit gain.

End of Travel Detection: The End of Travel circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek and the positioner proceeds past cylinder 822. Sequencing is as follows:

1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The input, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 822 is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.4v (2 tracks), Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard band, sets the Forward EOT FF.

3. With the Forward EOT FF set:

   a. Seek Error FF sets to return Seek Error to the controller.

   b. Seek FF (set at the start of the seek) is cleared.

   c. The difference counter and cylinder address register are set to 000 (T=0).

   d. Fine Enable is raised within the servo circuit.

   e. Because of c and d, the Fine Gate in the servo circuit is enabled.

   f. The Slope FF is cleared to indicate a seek to an even-numbered cylinder.

4. The track servo, functioning as the fine position analog signal in the servo circuit, is gated to the servo summing amplifier via the Fine Gate. The signal is at a maximum amplitude because only even dibits are being sensed. This error voltage causes the positioner to drive in reverse until the servo signal drops to zero; the heads are then positioned at cylinder 822.

5. An RTZ command is required to clear the Seek Error status.

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to cylinder 000.

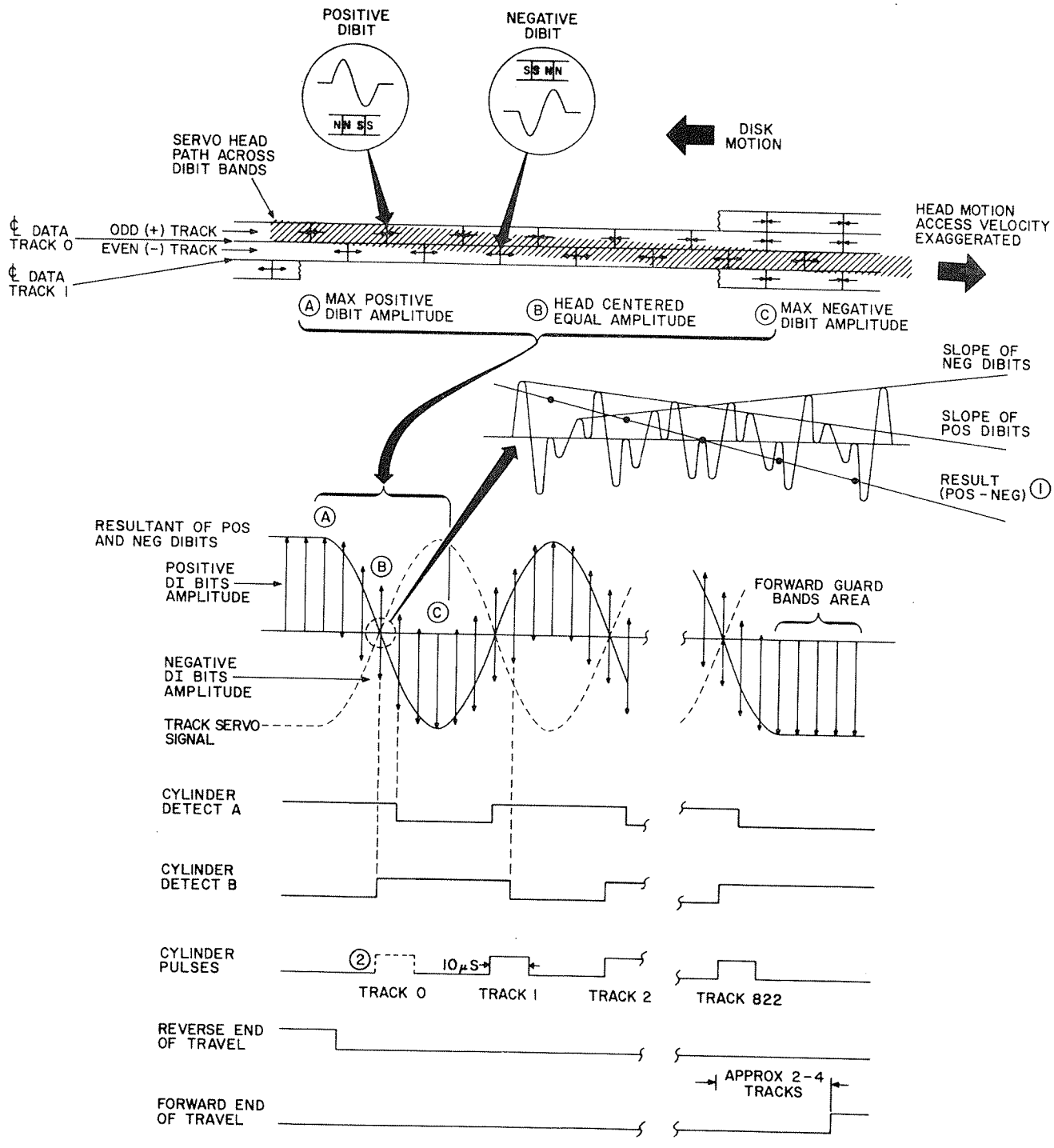
Cylinder Pulse Generation: As the servo head crosses the interface of the even/odd dibit tracks (Figure 3-17), the servo signal decreases toward null. The two detected cylinder pulses are ORed to a Schmitt trigger. The hysteresis designed into the trigger causes it to be up only while the servo signal is between 0v and 0.4v. This provides a 10 μsec cylinder pulse. Each cylinder pulse decrements the difference counter and switches the velocity integrator to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 001. The On Cylinder signal provides a pulse to decrease the difference counter to 000. With the difference counter at 000 (T=0) and On Cylinder available, the Seek Complete FF sets.

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine position analog signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

Load

This function involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the units logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs.



NOTES: (1) TRACK SERVO SIGNAL IS 180° OUT-OF-PHASE WITH THIS WAVEFORM.
(2) CYL PULSE DOES NOT AFFECT DIFFERENCE COUNTER AT TRACK 0 FOR FIRST SEEK.

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Figure 3-17. Cylinder Pulses Generation

Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlock is closed. Successful completion of a load is signified by the occurrence of an On Cylinder and the lighting of the READY indicator.

Initiation of the function occurs when the operator panel START switch is pressed. See Figures 3-18 and 3-19 for the load flow chart and timing diagram. The START switch enables relay K4. This releases the hysteresis brake (option), and starts the spindle motor through relay K1.

When the disk pack speed reaches approximately 2800 rpm, voice coil relay K2 is energized to connect the power amplifier to the voice coil. The speed sensing circuitry also enables the up to speed logic at approximately 2800 rpm, providing an Up To Speed signal to the Load latch. The Load latch activates circuitry to produce an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position analog signal. When even dibits are detected (approaching track 000) the Fine Servo signal decelerates the carriage.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position signal is less than 0.98v. The carriage stops when the Fine Position signal is 0v. The Servo Ready latch is then set, and the READY indicator is turned on. The drive is now ready to perform a Read, Write, or Seek operation.

If, for any reason, the dibit signals are not detected by the servo head within 350 ms after the Load latch is set, the RTZ latch is set and the carriage is retracted to the heads unloaded position. The FAULT indicator is then turned on. When the FAULT switch is pushed, the Fault latch is cleared and the carriage will attempt another seek to track 000. Once again if the dibit signals are not detected within 350 ms, the carriage will be retracted to the heads unloaded position and the FAULT indicator turned on.

Direct(Forward/Reverse)Seek

The Direct Seek function involves those operations that must be performed to move the read/write heads from their current track or cylinder location to the one specified by the controller. Refer to Figures 3-20 and 3-21. Assume that the drive is at track 10 and awaiting further instructions. Assume also that the controller wishes to do a Read or Write operation at track 320. When the controller determines that the drive is ready, it sends the new cylinder address along with Tag 1. Raising Tag 1 places the old address and compliment of the new address in the adder. After the compare has been made, the difference counter is loaded with the number of tracks to go. When the controller drops Tag 1, the new cylinder address is loaded into the CAR, the seek direction is sent to the servo, and a Start Seek pulse is generated. (Refer to the servo circuit discussion for general seek functions.)

The Forward Seek signal from the cylinder address adder gates the output of the position converter (Position Error signal) into the desired velocity function generator. (A Reverse Seek would have gated an inverted Position Error signal.) Since the seek length is greater than 256 tracks, the position converter output is clamped at a fixed voltage. Start Seek clears the Fine latch, so the output of the

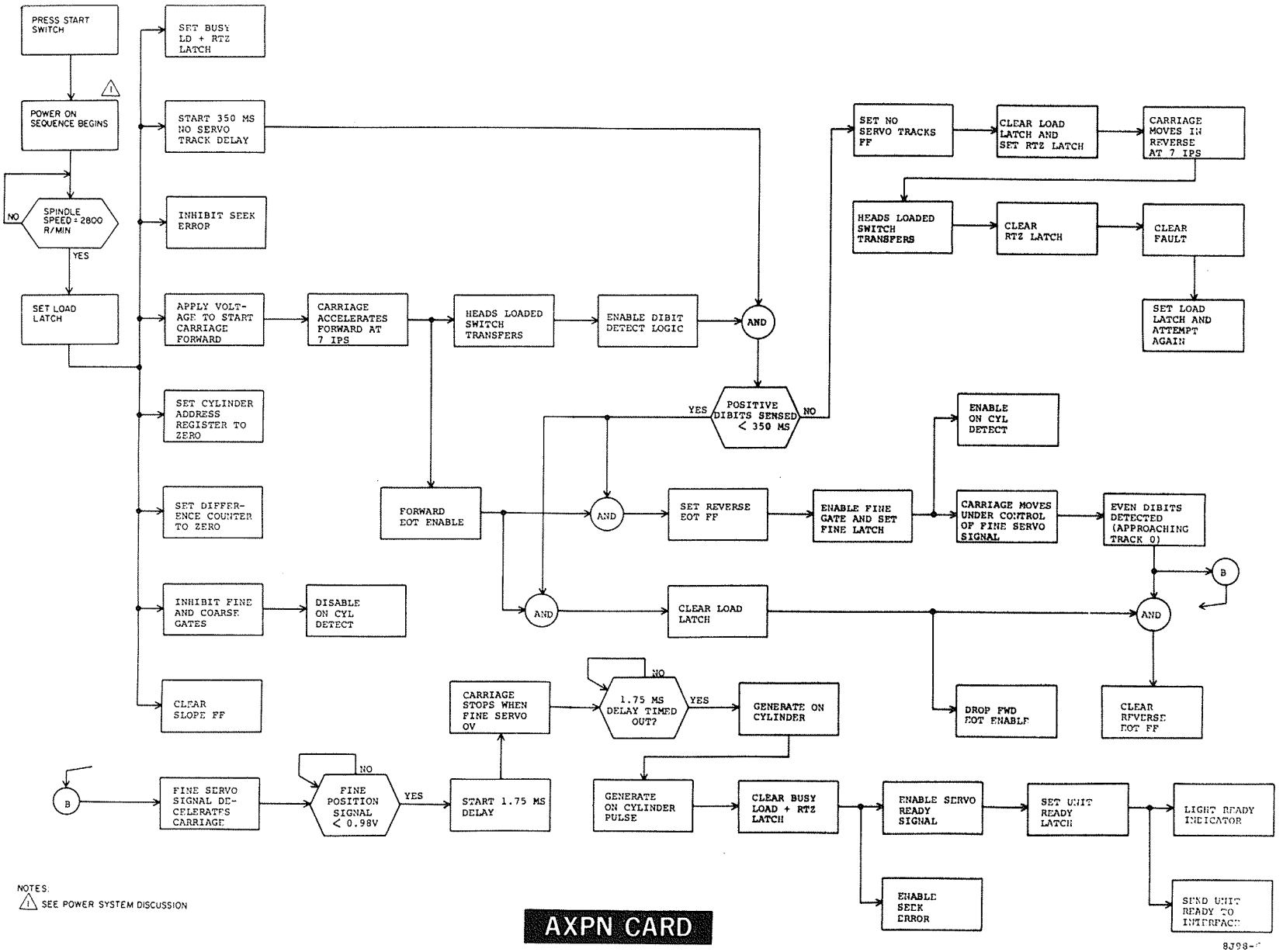
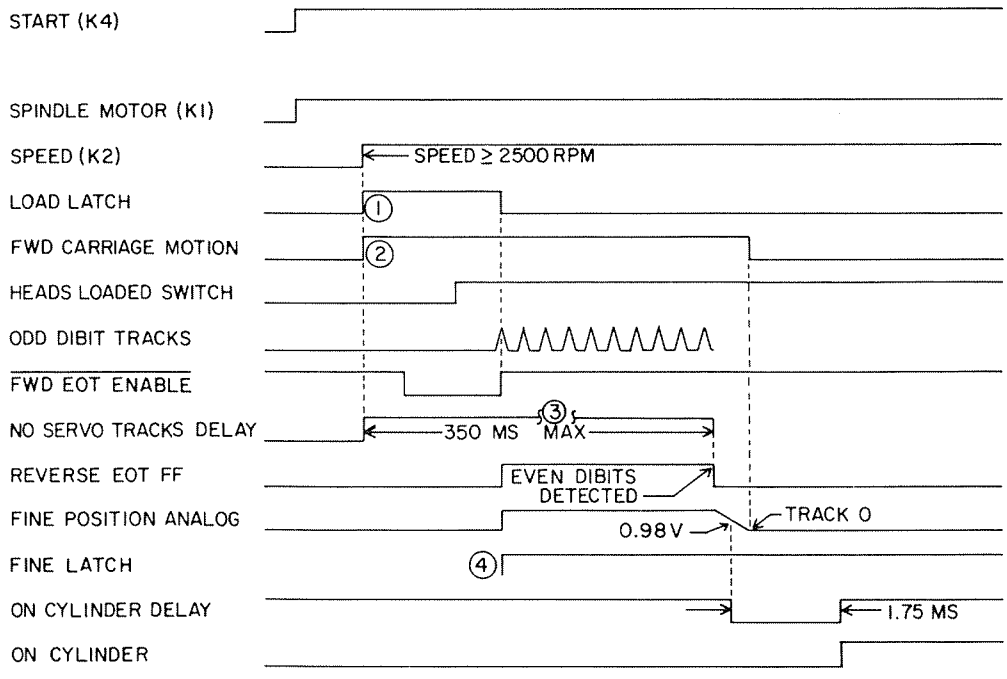


Figure 3-18. First Seek Flow Chart



NOTES:

1. LOAD LATCH CAUSES LOAD GATE TO APPLY A FORWARD SEEK VOLTAGE TO VOICE COIL SUMMING AMP. FINE GATE IS INHIBITED. CYLINDER ADDRESS REGISTER AND DIFFERENCE COUNTER ARE SET TO ZERO.
2. MOTION TO 7 IPS PROVIDED BY LOAD GATE UNTIL ODD DIBITS SET REVERSE EOT FF. MOTION CONTROL THEN PROVIDED BY FINE POSITION SIGNAL.
3. DIBITS MUST BE DETECTED WITHIN 350 MS OR FAULT IS SET. HEADS UNLOAD.
4. FINE LATCH IS JAMMED AT START OF LOAD UNTIL LOAD FF CLEARS, KEEPING COARSE OR FINE GATE DISABLED. WHEN LOAD FF CLEARS, T ≤ 1, AND FINE ENABLE IS HIGH, THE FINE LATCH WILL BE SET.

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Figure 3-19. First Seek Timing Diagram

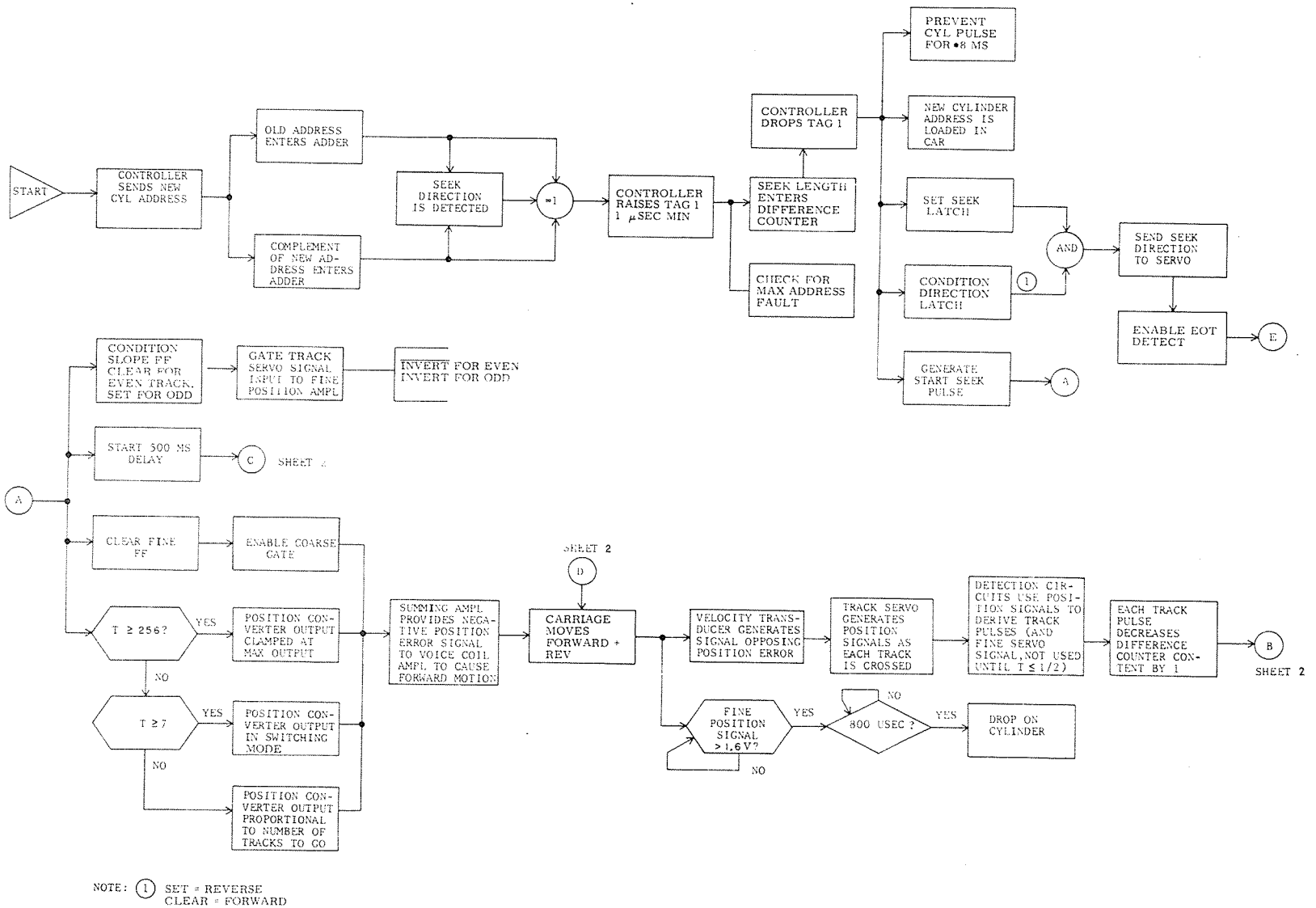


Figure 3-20. Direct Seek Flow Chart (Sheet 1 of 2)

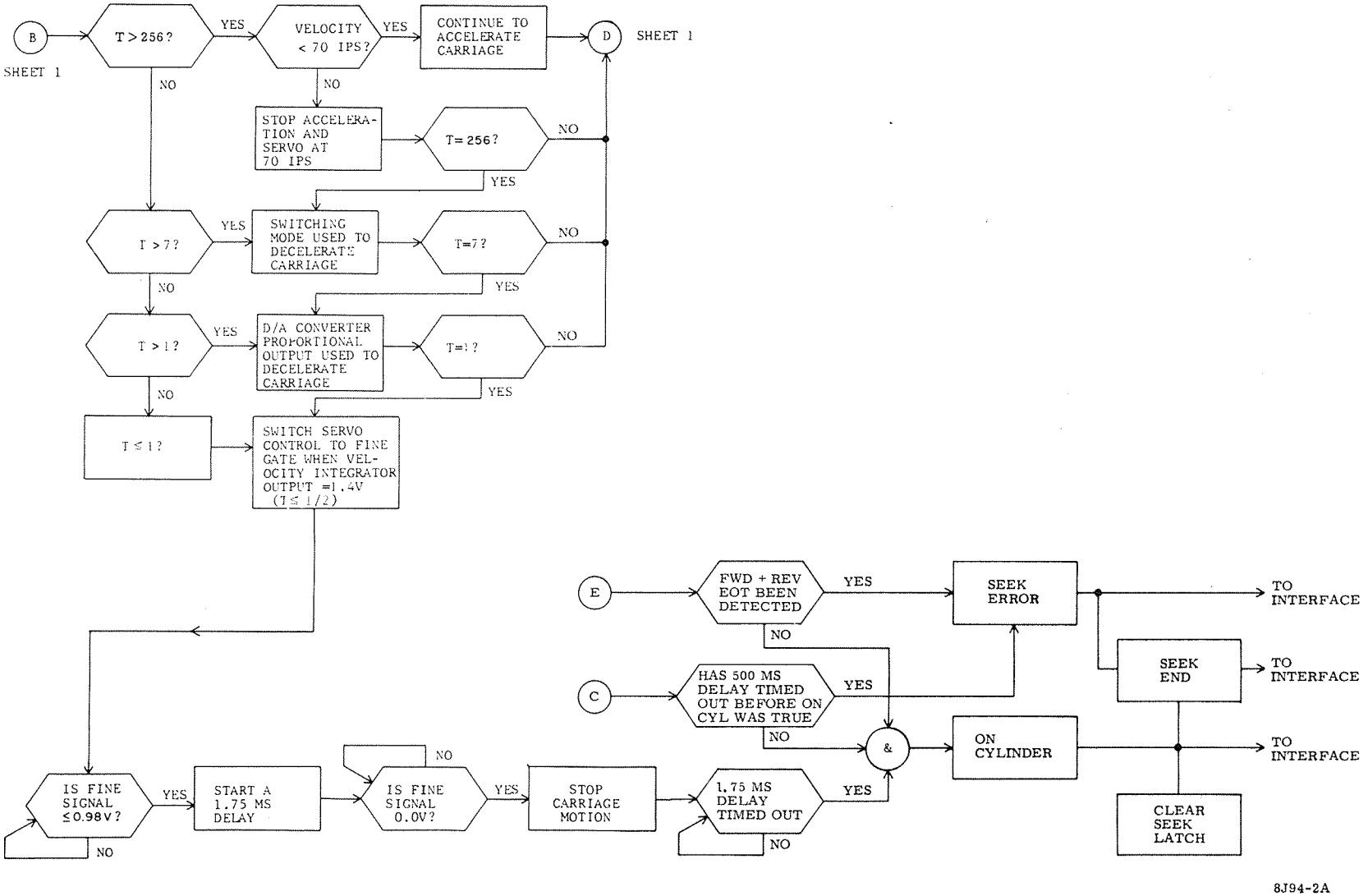
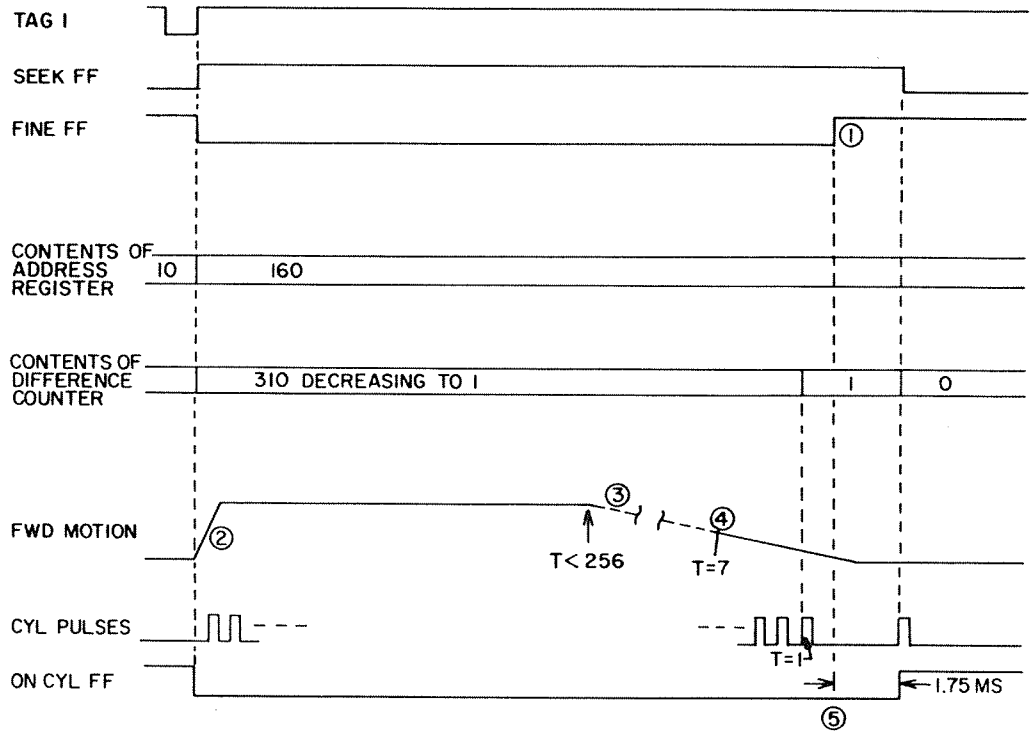


Figure 3-20. Direct Seek Flow Chart (Sheet 2 of 2)



NOTES: ① FINE FF SETS WHEN VELOCITY INTEGRATOR OUTPUT ≤1.4V AND T ≤ 1.
② APPROXIMATELY 200 (MIN) TRACKS REQUIRED TO ACCELERATE TO 70 IPS.
③ SWITCHING MODE DECELERATES CARRIAGE FROM T=256 TO T=7.
④ UNSWITCHED POSITION ERROR SIGNAL DECELERATES CARRIAGE DURING T ≤ 7 THROUGH T ≤ 1.
⑤ ON CYLINDER DELAY STARTS WHEN FINE POSITION SIGNAL<0.98V.
⑥ TIMES ARE NOT TO SCALE.

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Figure 3-21. Direct Seek Timing Diagram

desired velocity function generator is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no Velocity signal exists to balance the Position Error, and forward motion of the carriage begins.

With the Position Error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the carriage will continue to accelerate. As the carriage moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse decreases the content of the difference counter by one. When acceleration has increased to the point where the Velocity Amplifier signal and the Position Error signal cancel each other, the Summing Amplifier Control signal drops off. During this phase, the carriage coasts along the 55 ips plateau with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the Seek are approximately 256, the position converter voltage clamp is disabled, and for the remainder of the Seek (except for the last track), the servo position error is derived from the D/A converter. As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the Position Error provided at the desired velocity function generator input is not stepped, the integrator clamp gates the velocity integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output and fills-in the area between the leading edges of each step.

As the Position Error signal begins to decrease, the servo system is changed to the switching mode. When the Position Error signal becomes less than the Velocity signal, current is applied to the voice coil in the maximum reverse direction until the velocity of the carriage slows down below the instantaneous Position Error value. The current to the voice coil is then turned off and the carriage coasts under its own inertia while the difference counter continues to count down (decreasing the Position Error signal). If the carriage velocity becomes too high for the existing Position Error signal, a maximum reverse current is again applied until the velocity slows down below the instantaneous position error value.

At T≤7, the switching mode logic is disabled and the total summing amplifier output is used to decelerate the carriage to keep the Velocity signal/Position Error signal difference to zero.

When the counter indicates one track to go to the desired destination, the Integrated Velocity signal is reset by the regular cylinder pulse. The Integrated Velocity, which indicates distance, brings up Fine Enable when about one-half track of travel remains. This sets the Fine latch which, in turn, enables the Fine gate and disables the Coarse gate.

Desired velocity no longer has an effect; the position error is supplied by the Fine Servo signal. This signal is the track servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between current head position and the desired cylinder.

Since the desired destination is track 320, bit 0 of the Address register is "0". This causes the Slope FF to be cleared. As a result, the track servo signal is inverted to form the Fine Servo signal. In all seeks, the Fine Servo signal is phased to be opposite to the velocity signal. As the carriage approaches track 320, the Fine Servo signal approaches 0v. The summing amplifier responds to this decrease in amplitude by decelerating the carriage so that the sum of the Velocity signal always just cancels the Fine Servo signal. At track 320, both Velocity and Position Error equal zero, and all motion stops with the servo circuit at null. Only a Position Error will cause additional motion. When

the Fine Servo signal is less than 0.98v, a delay of 1.75 ms starts. The On Cylinder signal occurs when the delay times out.

Certain conditions indicate that the seek was not completed successfully. This is a Seek Error. These conditions are:

1. On Cylinder not generated within 500 ms from the start of the seek.
2. Forward EOT sensed. The carriage returns to cylinder 822 and remains there.
3. Reverse EOT sensed. The carriage returns to cylinder 000 and remains there.
4. If the carriage drifts off cylinder enough for the fine position signal to be greater than about 1.61 volt for more than 800 μsec, the Seek Error FF sets. In addition, if the drive is reading or writing, the Fault FF also sets. Write gate is disabled. The unit will not accept any commands until the error is cleared manually.
5. Command seek to track greater than 822.

All of these conditions require an RTZ command to clear the error. RTZ clears Seek Error and returns the drive to cylinder 000.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward or reverse seeks are identical for seeks of equivalent lengths.

Return to Zero Seek(RTZS)

The RTZ function allows a controller to return the heads to track 000 when a Seek Error occurs. See Figures 3-22 and 3-23 for the RTZS flow chart and timing diagram.

The RTZS pulse sets the RTZ latch and clears the Seek Error FF. This enables the RTZ gate, resulting in a bias voltage that forces an average 7 ips reverse motion of the carriage. When the carriage passes cylinder 000, no more even dibits are detected. This is the Reverse EOT area. The lack of even dibits inhibits cylinder pulses, allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.4v. This, along with odd dibits, sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.4v. The RTZ latch is cleared while the Load latch sets.

The Load latch activates circuitry to produce an average forward 7 ips access. The carriage continues forward with the servo head searching for the prerecorded positive dibit signals on the track servo surface. When the reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared, the Reverse EOT FF is set, and the Fine gate and latch are enabled. The carriage now moves under control of the Fine Position analog signal. When even dibits are detected (approaching track 000), the Fine Servo signal decelerates the carriage.

The drive sends On Cylinder to the controller 1.75 ms after the Fine Position signal is less than 0.98v. The carriage stops when the Fine Position signal is 0v. The sequence must be completed within 500 ms after RTZS initiation, or else the Seek Error FF is set.

The RTZS function is also used during normal power off sequencing. If the START switch is pressed by the operator, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 7 ips reverse seek.

This time, however, the EOT Enable circuit is disabled so that the velocity integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload.

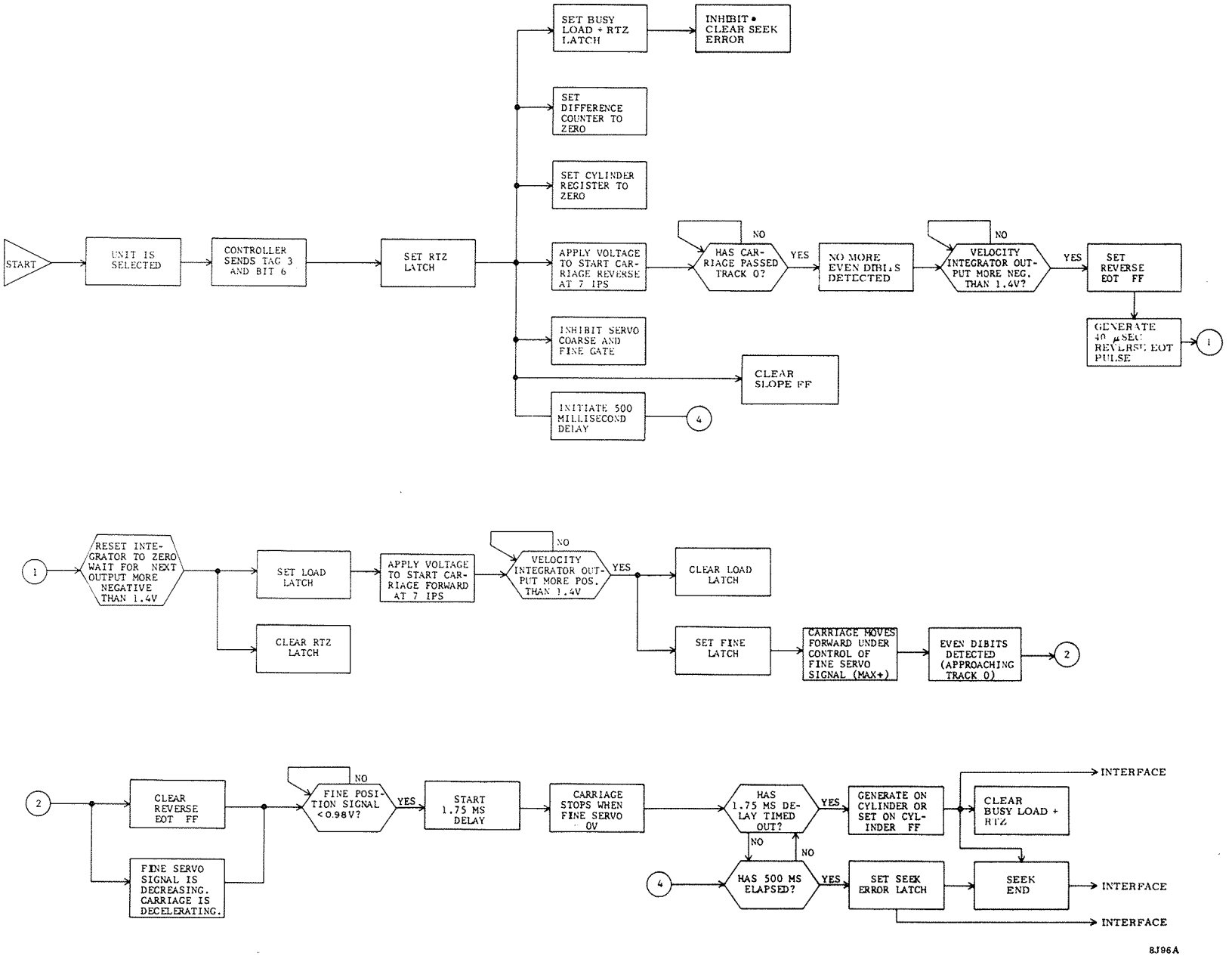
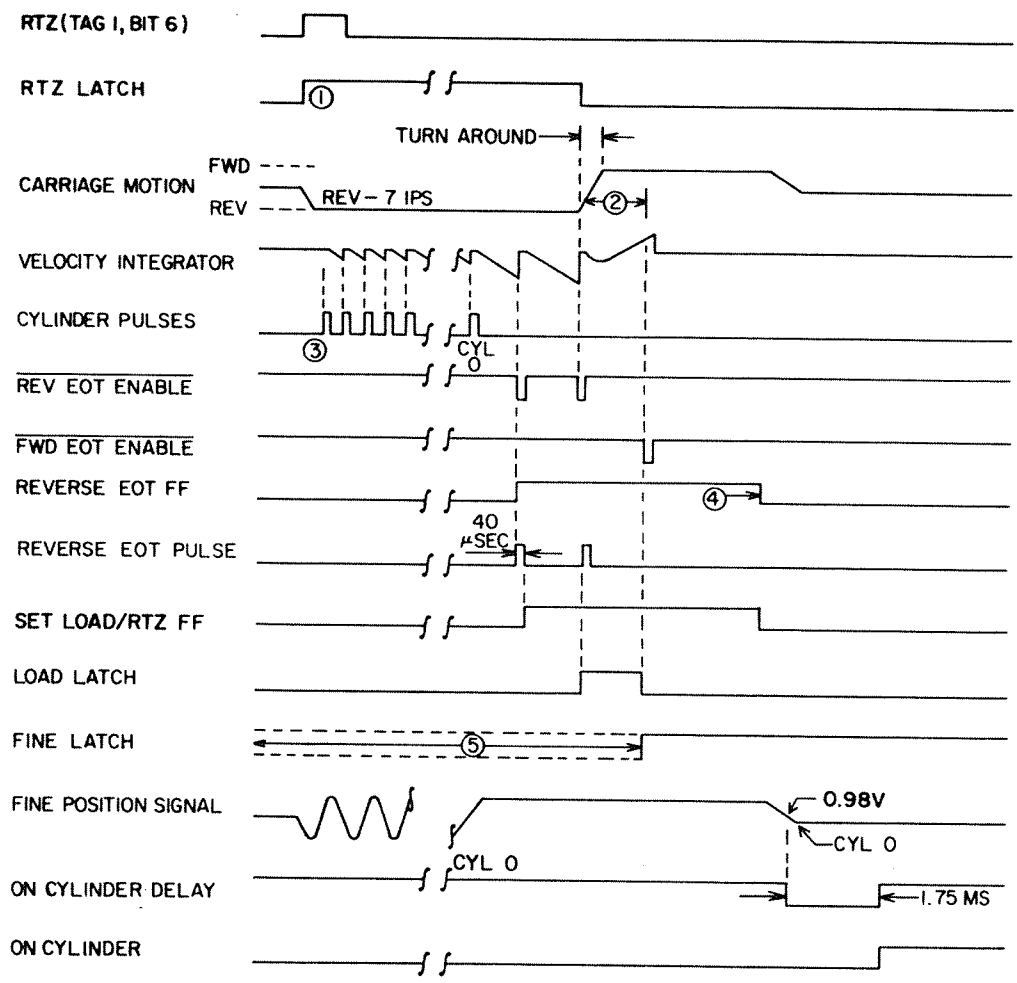


Figure 3-22. Return to Zero Seek Flow Chart



NOTES:

① RTZ LATCH CAUSES RTZ GATE TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO ZERO.

② FWD MOTION TO 7 IPS PROVIDED BY LOAD GATE, IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN DI BITS. (APPROACHING TRACK 0).

⑤ BOTH OUTPUTS ARE HIGH WITH EITHER RTZ OR LOAD LATCH SET. THIS DISABLES COARSE AND FINE GATES. FF THEN SET BY T ≤ I AND FINE ENABLE.

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Figure 3-23. RTZS Timing Diagram

The RTZS function transfers automatically to the heads unloaded condition if dibits are lost for more than 350 ms.

BASIC READ/WRITE PRINCIPLES

Introduction

Information is recorded on, and read from, the disk pack by means of 5 heads. Each head contains a read/write coil.

Writing Data

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (Figure 3-24). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends on the amount of current: the greater the current, the more oxide particles that are affected.

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Erasing old data is accomplished by writing over any data which may already be on the disk. The write current is zoned in eight current zones to ensure proper saturation level for best head resolution. The write current is maximum on the outer tracks and progressively decreased for inner tracks.

Reading Data

As the disk passes beneath the read/write head, the stored flux intersects the gap (Figure 3-25). Gap motion through the flux induces a voltage in the head windings. This voltage is analyzed by the read circuit to define the data recorded on the disk. Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse, in turn, represents a data bit.

Track Format

Each track has Index as its starting point. The track is further subdivided into 64 sectors on the standard

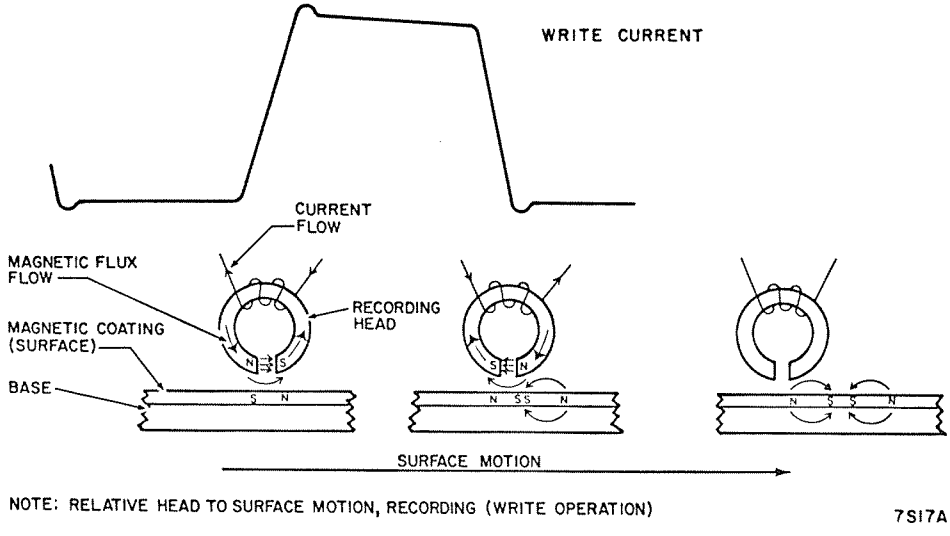


Figure 3-24. Writing Data

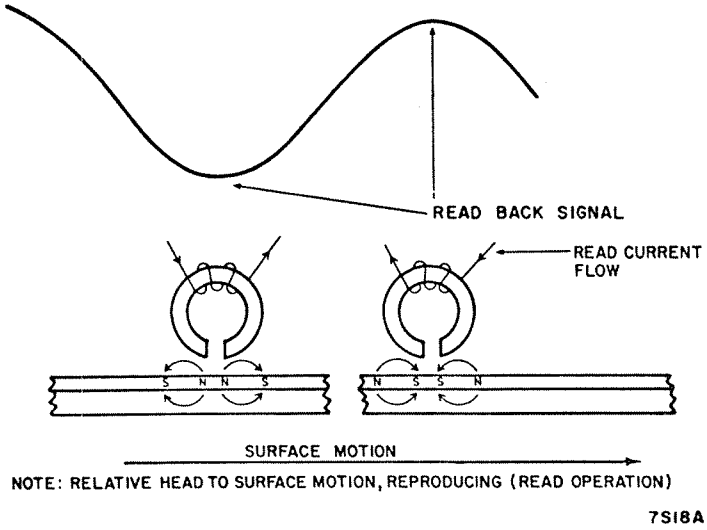


Figure 3-25. Reading Data

unit. Other numbers of sectors per track are possible by changing sector plug in S/C 08 W/O 37725A & BLW or by selecting sector switch in S/C 08 W/ 37725A & ABV at location A03. Sector 000 is the first sector following Index. Index and Sector signals are available to the controller. For further information, refer to the Direct (Forward/ Reverse) Seek theory earlier in this section.

One track is operated upon by one read/write head. The heads are numbered from 0 through 4. These heads are positioned vertically with respect to each other. As a result all 5 of the heads may be used without moving the actuator. Since any of the heads may be addressed at practically instantaneous rates, the recording medium may be thought of as a cylinder rather than as 5 discrete surfaces. This is the cylinder concept. Since the actuator may be positioned horizontally to any one of 823 rings or tracks, there are 823 cylinders. They are numbered from 000 (the cylinder nearest the outside edge of the disk) to 822 (the innermost cylinder). Any track may be addressed by seeking to the desired cylinder and by selecting one head. Only one head may be selected at a time.

Track format, sector control, and data record format are functions of the operating system. These functions are directly controlled by the controller. Refer to the applicable controller manual for further information.

Principles of MFM Recording

In order to define the binary dibits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 103 nsec in width. The data transfer rate is, therefore, nominally 9.677 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (figure 3-26). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

1. There is a flux transition for each "1" bit at the time of the "1".
2. There is a flux transition between each pair of "0" bits.
3. There is no flux transition between the bits of a "10" or "01" combination.

The advantages and disadvantages of MFM recording are as follows:

1. Fewer flux reversals are needed to represent a given binary number because there are no flux reversals at the cell boundaries, achieving higher recording densities of data without increasing the number of flux reversals per inch.

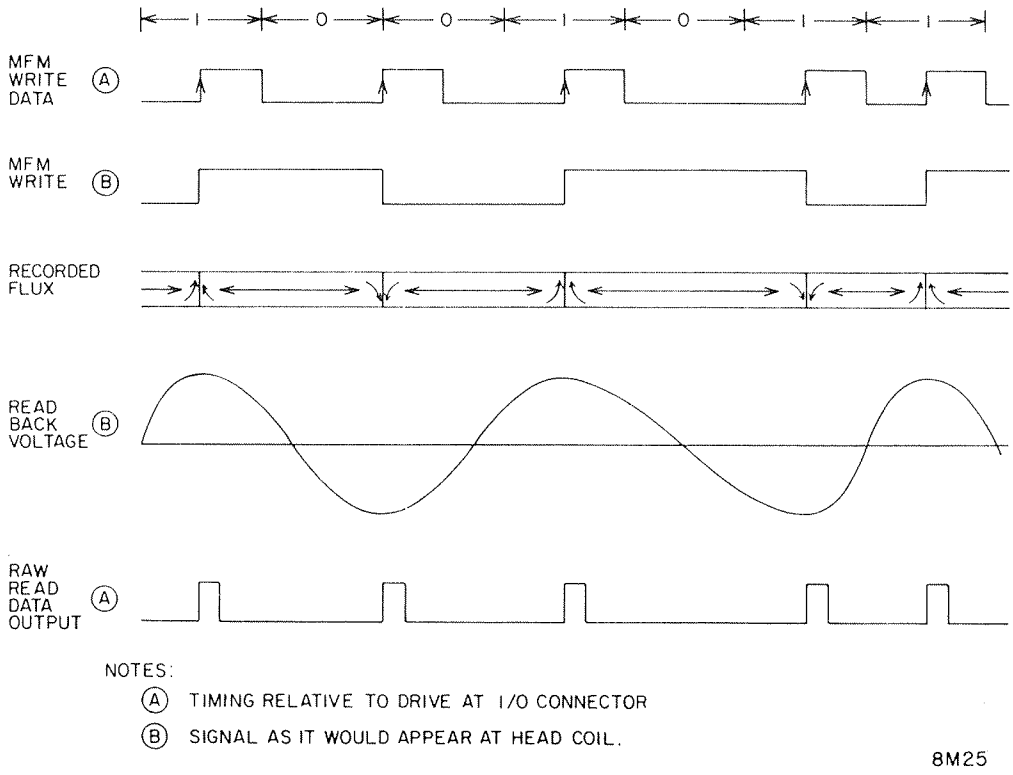


Figure 3-26. MFM Recording

2. Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

3. Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

READ/WRITE OPERATIONS

Introduction

An overall block diagram of the read/write chain is shown in Figure 3-27. More detailed block diagrams and timing diagrams are shown in conjunction with the discussions of the various stages in the read/write chain.

Head Selection

The desired head must be selected before a Read or Write operation can be performed. The head selection process is initiated by a Tag 2 function code from the controller. This code gates the desired head address into the head decoder. For purposes of this discussion, assume that head 4 is the head to be selected. Also assume that the present head selected is head 0.

The controller places the address for head 4 (100) on the 3 low order bits of the address and control bus lines. Tag 2 is then transmitted to the unit to gate the address information into the head decoder. The end result generates a "0" output to select head 4. The remaining pins have "1" outputs to disable their respective heads. The "0" output grounds the center tap of head 4.

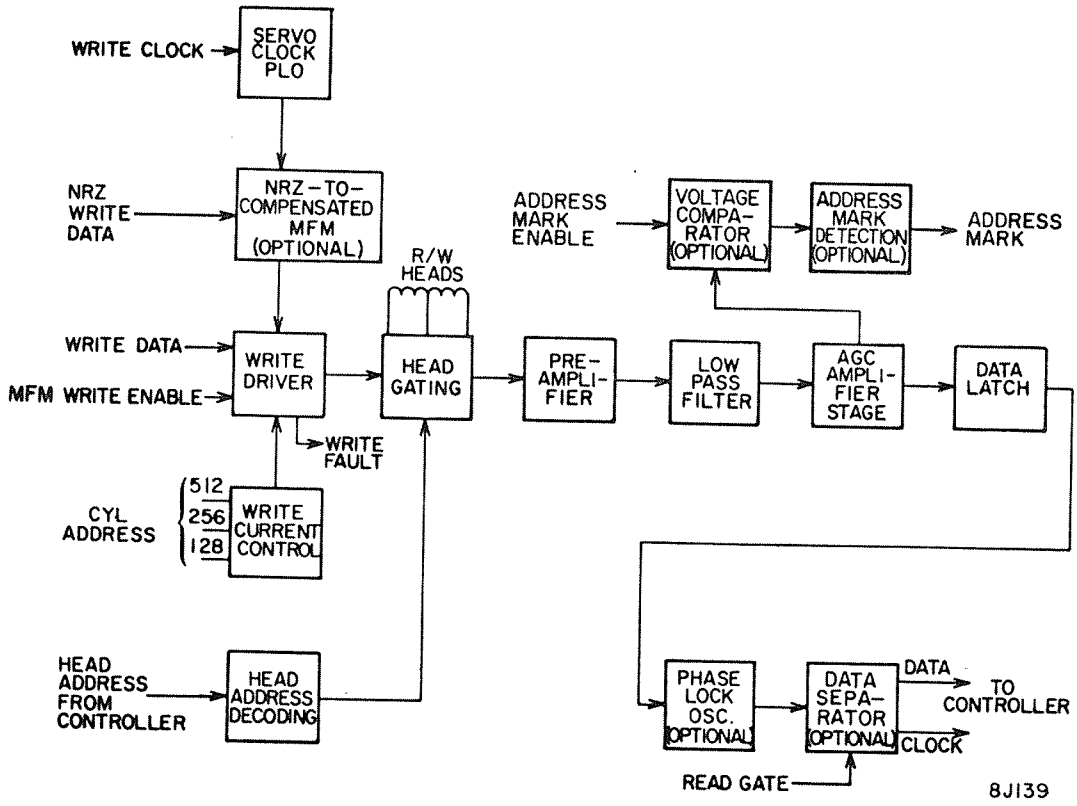


Figure 3-27. Read/Write Chain Block Diagram

If more than one head is selected, a fault is indicated.

Write Data Processing

A Write operation actually begins before the voice coil positioner moves the heads to the desired track. The Head Select Strobe function code gates the identifying number of the head to be used into the Head Address register (see Head Selection description). When the Seek operation is completed, the unit sends an On Cylinder signal to the controller. This signal informs the controller that the unit is On Cylinder and ready to receive further commands.

The controller now examines the Seek Error, Unit Ready, and On Cylinder lines. If a Seek Error exists, the controller sends a Return to Zero function code to clear it. If an On Cylinder exists, the controller responds with a Tag 3 function code that gates the Read Gate signal (bit 1 of the address and control bus lines) to the unit. The Read gate must be enabled in a synchronization field at least 10 μsec before the sync bit if the PLO Data Separator option is chosen. This enables the read circuit logic function with the previously selected head to read the data record on the disk pack. The address is read from the Read Data line by the controller and compared with the address of the desired record. If the address is correct, the controller drops Read gate and brings up Write gate (bit 0) with a Tag 3 function code. This disables the read circuit and enables the write circuit.

The write data is transmitted to the unit, amplified, and applied to the selected head (Figure 3-28). The Write signal from the controller must now be up if the data is to continue along the write chain. If write is up, the data is allowed to pass through the remainder of the chain to the selected head and is written on the disk pack.

Write Compensation (Optional)

The write compensation circuit converts the NRZ data into MFM data while compensating for a read condition known as peak shift.

Peak Shift

Peak shift is an effect that degrades read accuracy by distorting the waveform. This condition exists because no electromechanical device can be perfect.

Ideally, the flux reversal command by the write toggle would be instantaneous as shown in the Ideal Recording portion of Figure 3-29. Current would immediately switch from one polarity to the other. As a result, the distance required to complete the magnetic flux reversal on the disk would be so narrow as to be insignificant; the readback pulse would then also be extremely narrow. To carry the principle one step further, the heads would be an infinitesimal distance from the disk surface. Therefore, the head gap itself could be made very small for two reasons:

1. The magnetic field strength increases as the head moves closer to the disk.
2. The head gap must be wide enough to intersect sufficient lines of force from the magnetic flux field to generate a signal. The weaker the signal, the wider the gap must be. With the substantial flux amplitude gained by having the head very close to the disk surface, a very small head gap can generate a reliable readback voltage.

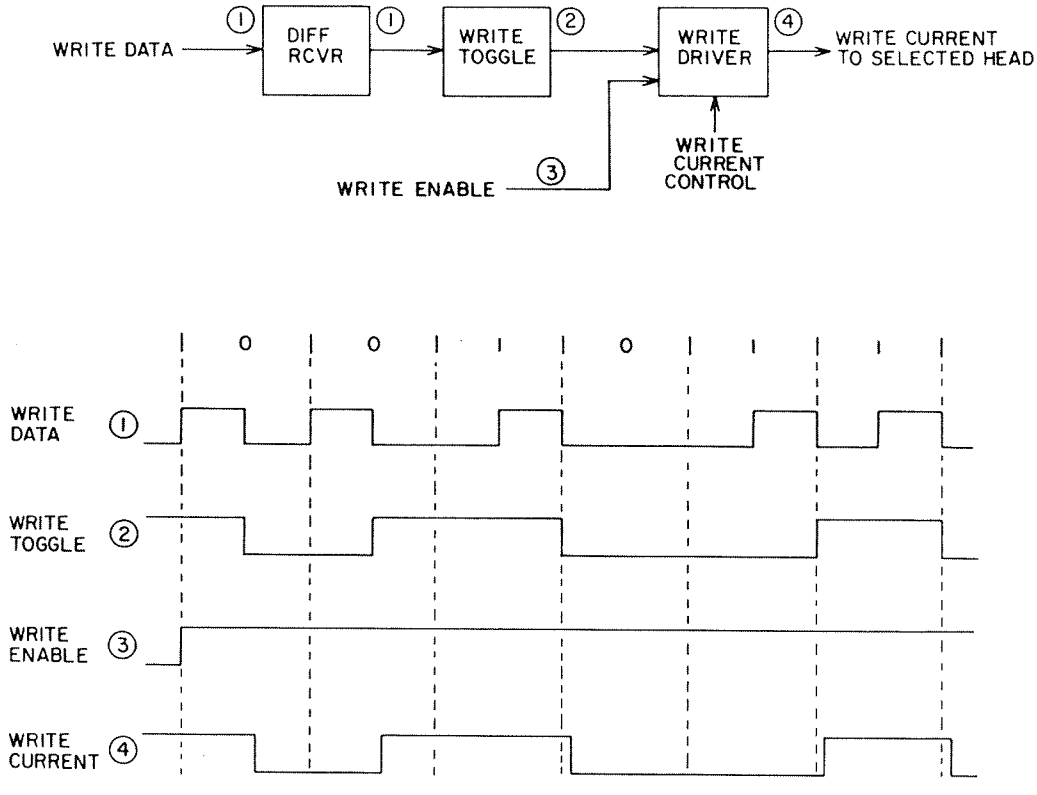


Figure 3-28. Write Chain Circuit 8M27

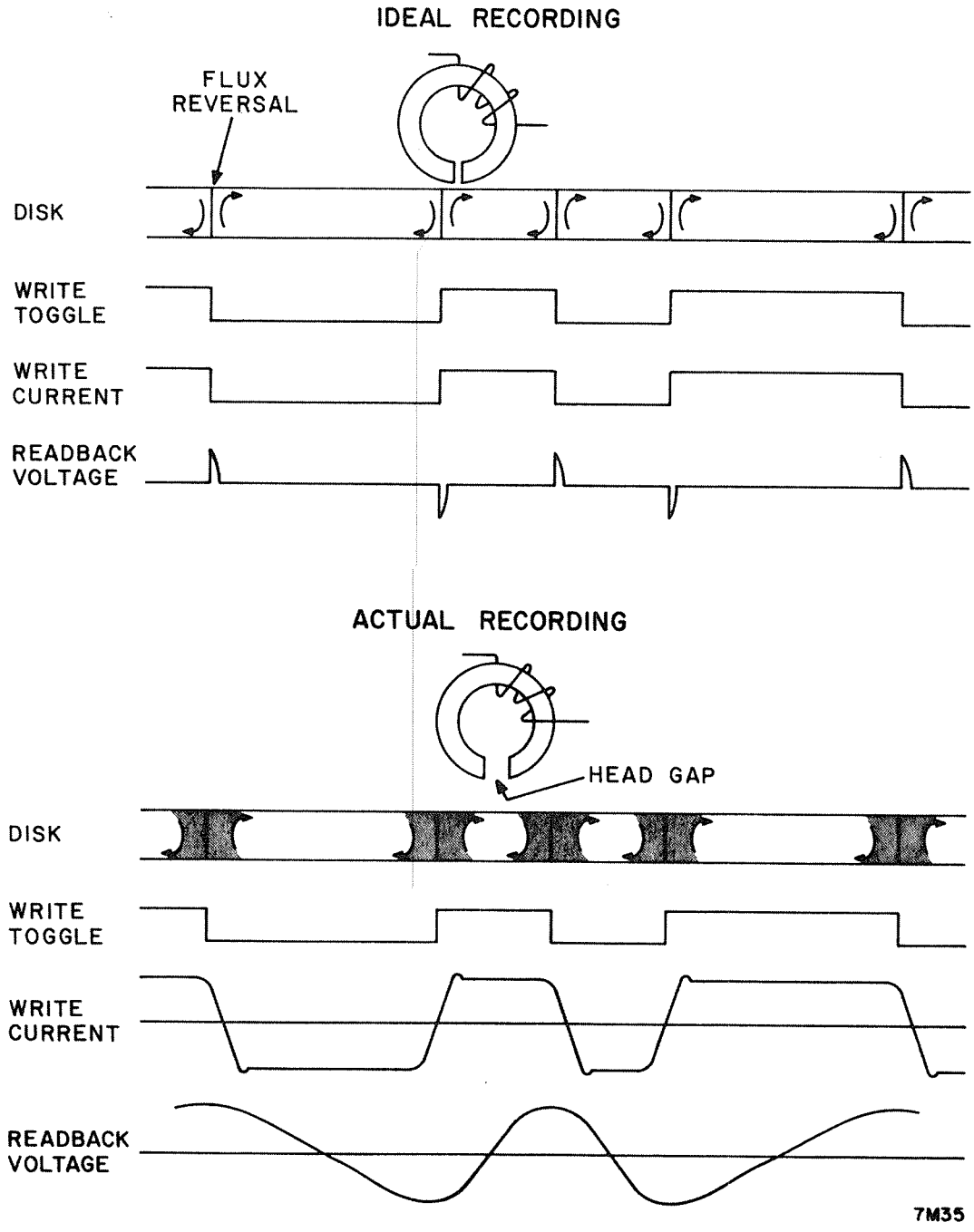


Figure 3-29. Write Irregularity

However, it takes time for the current to reverse, and the flux change is not instantaneous. Furthermore, heads must fly a finite distance from the disk. The greater the distance between the head and the oxide, the wider the head gap must be. The resulting readback voltage is more or less sinusoidal with peaks less easily defined in time or amplitude.

With modern high frequency recording techniques, adjacent clock/data pulses are close enough to interact with each other. This is shown in Figure 3-30. Peak shift is the result of the interaction of the pulses. Because two pulses tend to have a portion of their individual signals superimpose themselves on each other, the actual readback voltage is the algebraic summation of the pulses.

When all "1's" or all "0's" are being recorded, the data frequency is constant: pulses are spaced apart by one cell (103 nsec). As a result, the pulse spacing causes the overlap errors to be equal and opposite. The negative-going and positive-going errors cancel each other. This is the "zero peak shift" condition of the "...111..." pattern in Figure 3-30.

Peak shift occurs when there is a change in frequency. A "011" pattern represents a frequency increase since there is a delay of about 1.5 cell between the "01" and only 1.0 cell between the "11". As a result, the squeezing of the cells causes the mathematical average (the actual readback voltage) to shift the apparent peak to the left. This is early peak shift.

On the other hand, a "10" pattern represents a frequency decrease since a pulse is not written at all in the second cell. In addition, a "001" pattern is also a frequency decrease since there is a 1.0 cell interval between the first two bits and 1.5 cell between the last two bits.

The examples listed above examined only two or three bits without regard to the preceding or

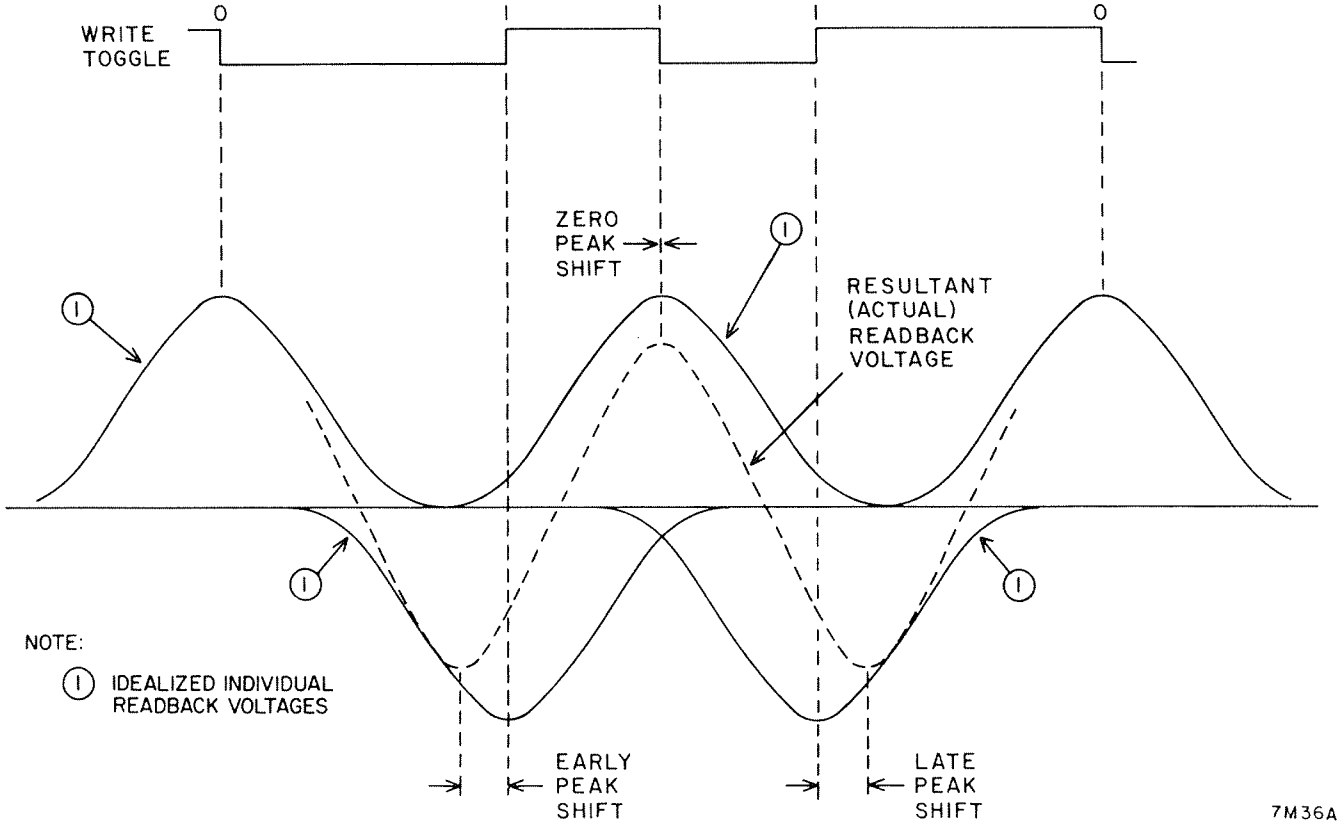
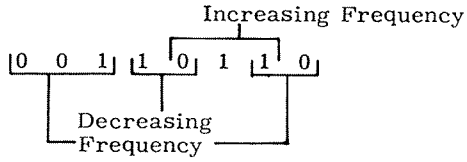


Figure 3-30. Peak Shift

subsequent data pattern. The actual combinations are somewhat more complex. The drive logic examines and defines the following patterns:

Pattern	Frequency Change
011	Increasing
1000	Increasing
10	Decreasing
001	Decreasing

Any data pattern will have considerable overlapping of the data pattern frequency changes. Consider the overlap of these eight bits:



Any of these peak shift conditions can cause errors during subsequent read operations. The drive compensates for these known errors by intentionally writing a pulse earlier or later than nominal. This function is accomplished by the write compensation circuit.

Write Compensation Circuit (Optional)

The write compensation circuit (Figure 3-31) converts NRZ data into MFM data while intentionally shifting the pulses in the data cell to compensate for peak shift.

Data enters a decode shift register in NRZ format. It is shifted through the register by a 9.67 MHz clock signal determined by the 19.34 MHz clock and a phase related 9.67 MHz clock. As the data shifts through the register, the register contents are examined by a series of gates to analyze the bit pattern. These gates determine if the incoming data frequency is constant (00000 or 11111), increasing (011 or 1000), or decreasing (10 or 001). The timing of the write data pulses applied to the write toggle (Figure 3-28) are adjusted to compensate for the frequency shift:

1. If frequency is constant, there will be no peak shift. The pulse, clock or data, is intentionally delayed by 6 nsec and is applied to the on time gate. This pulse is the write data pulse applied to the write toggle.

2. If frequency is decreasing, the apparent readback peak (Figure 3-30) would occur later than normal. To compensate for this, the data is written earlier than nominal. Early gate is enabled. This causes clock/data to be written concurrently with the clock pulses; the 6-nsec delay is bypassed.

3. If frequency is increasing, the apparent readback peak would occur earlier than normal. Therefore, data is intentionally written later than nominal. Late gate is enabled. This causes the write data to be written 12 nsec after the nominal beginning of the cell.

Writing Address Marks (Optional)

The drive writes an address mark (AM) on command of the controller. When the Control Select, Write Gate, and Address Mark lines are high the write compensation circuit (Figure 3-32) is prevented from being applied to the write circuitry. Current continues to flow through the write coil but, since there is no current reversal, no flux transitions occur. Therefore, the read circuit cannot recognize the constant flux as usable information. The controller determines the length of the Address Mark (three bytes).

Read Data Processing

AGC Amplifier and Address Mark Circuit

Analog read data from a selected head is passed through a preamplifier and a low pass filter (Figure 3-32). The filter attenuates the high unwanted frequencies (noise) in the read data signal and provides a linear phase response over the read data

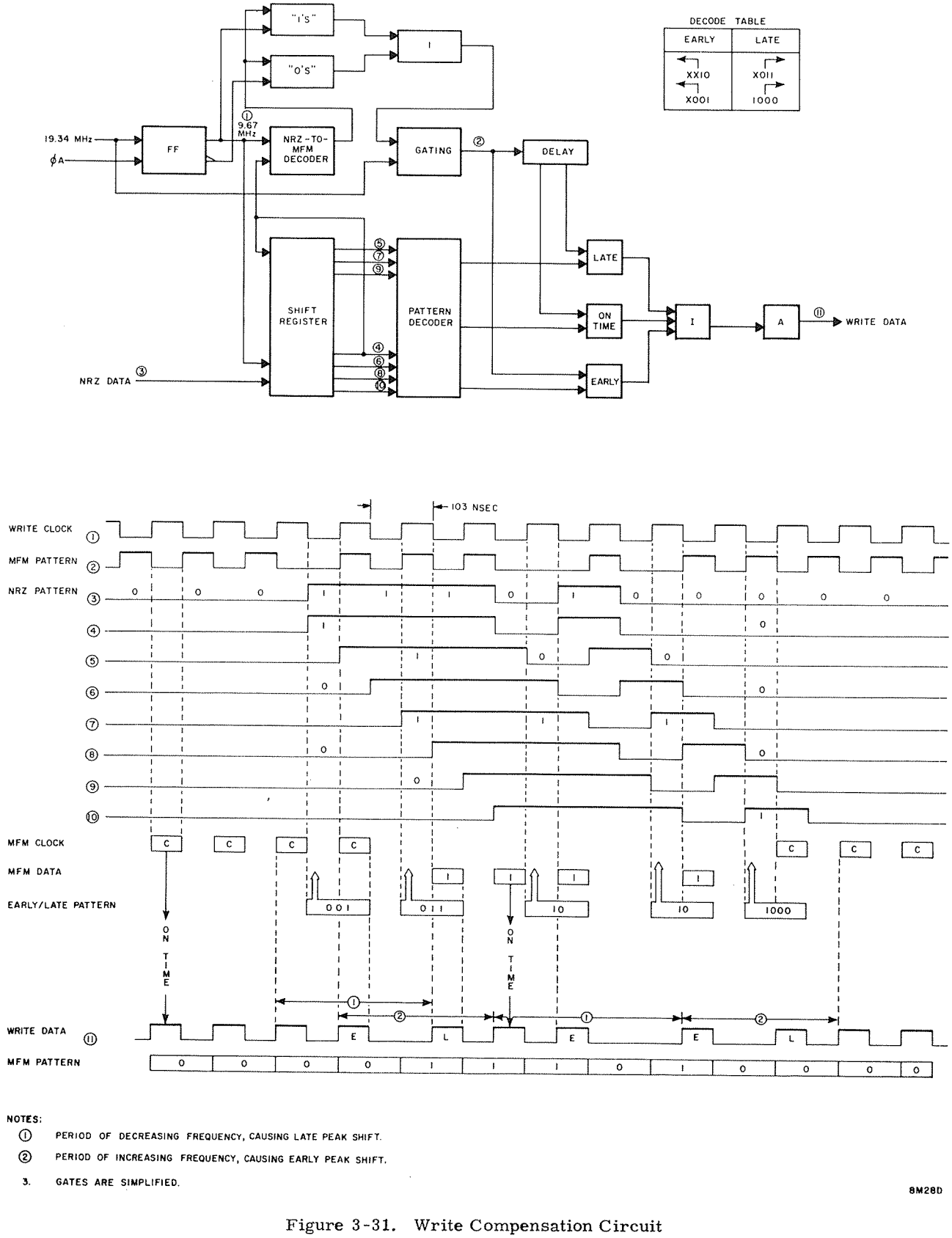


Figure 3-31. Write Compensation Circuit

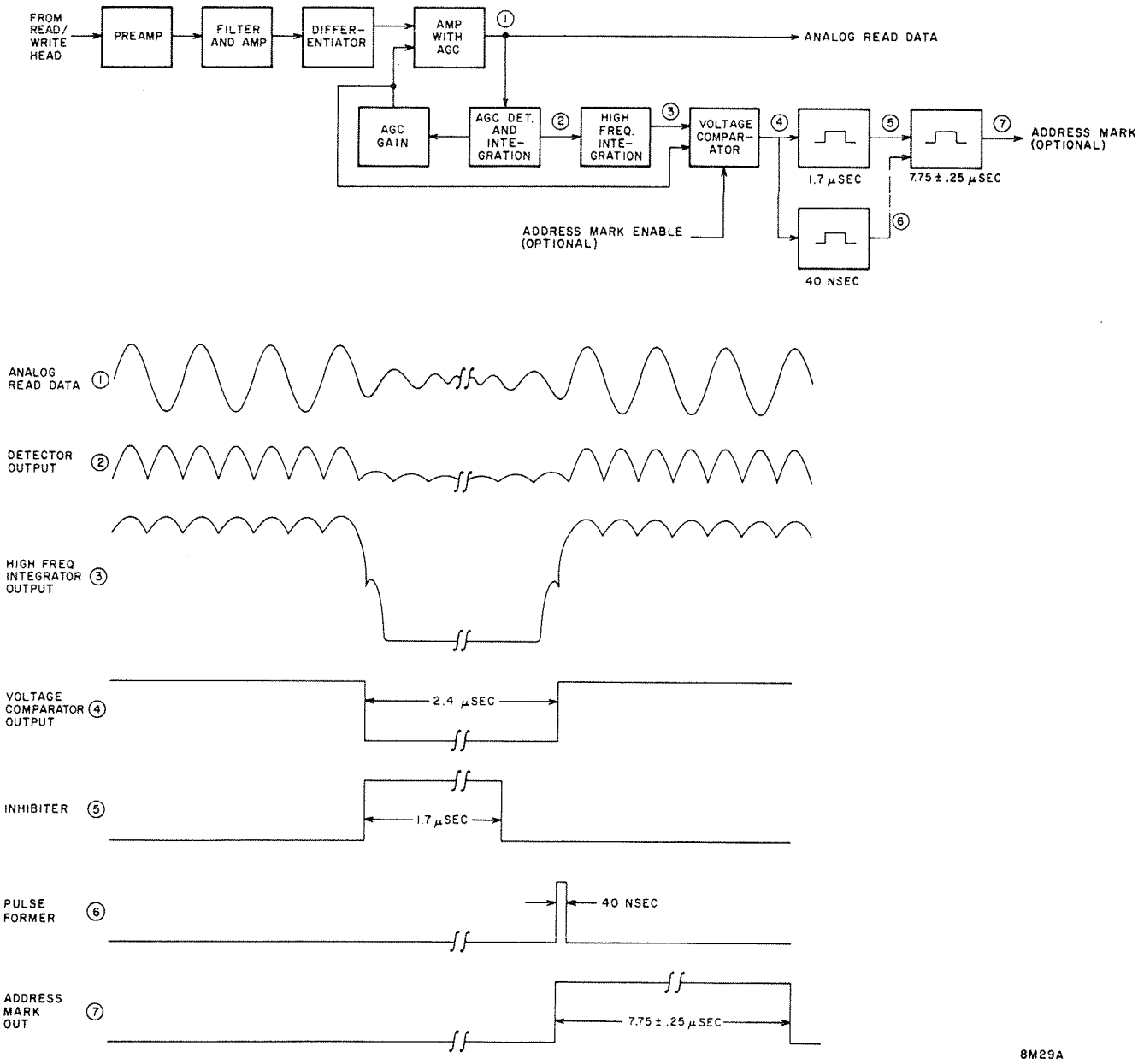


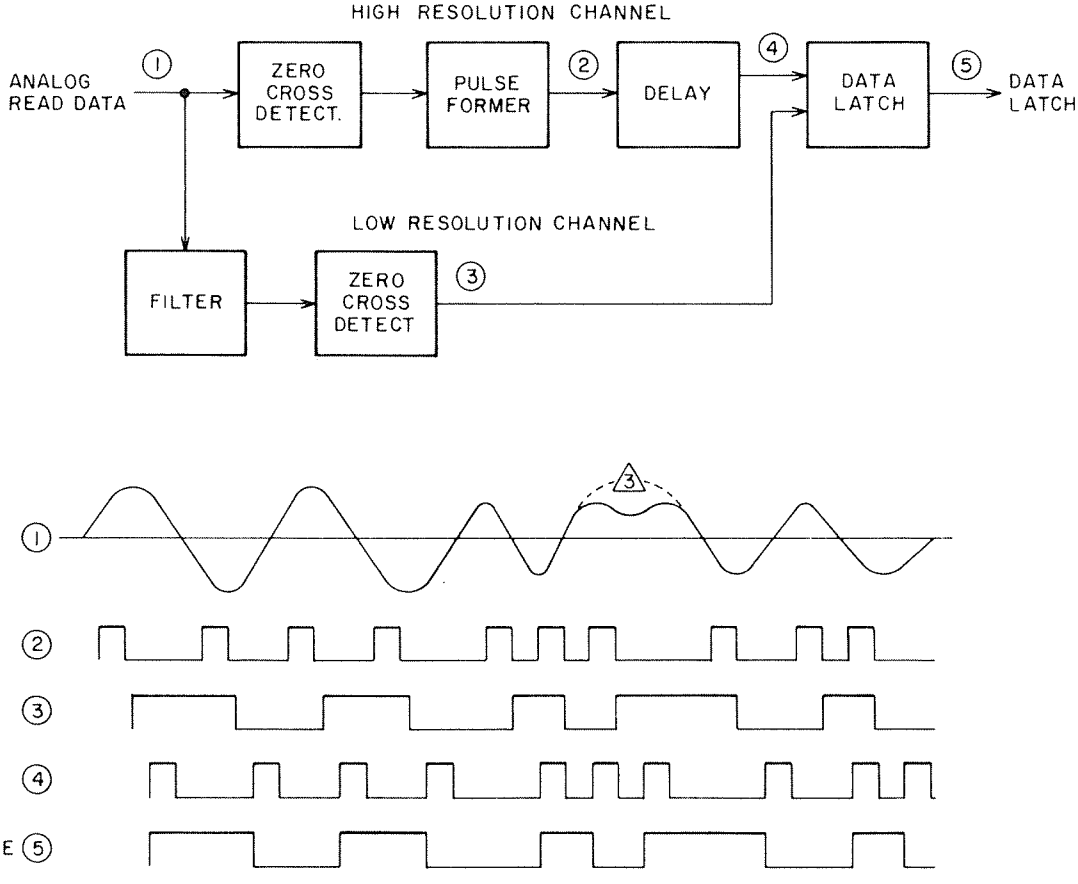
Figure 3-32. AGC Amplifier and Address Mark Circuits

frequencies. The output of the filter is applied to an agc circuit through a differentiator. The agc circuit provides a relatively constant output amplitude from a wide range of input amplitude. The output of the agc amplifier circuit is applied as a reference level to the data latch circuit. The detected agc signal is also integrated for use in a fast response address mark detection circuit (optional).

The address mark circuitry is enabled by the Address Mark Enable signal from the controller. The absence of output signals from the differentiator is sensed by the agc loop. A voltage comparator compares the agc level and senses the absence of output signals. The transitionless period of about 2.4 μsec is detected and formed into a 7.75 ±.25 μsec address mark. The Address Mark signal is used to resynchronize the data separator PLO (optional).

Data Latch Circuit

The data latch circuit (Figure 3-33) receives differentiated data from the agc circuit. Data is applied directly to the high resolution channel and through a low pass filter to the low resolution channel. The filter lowers the resolution of the Read Data signal by attenuating the third harmonic of the signal. After being delayed approximately 35 nsec past the low



NOTES: 1. TIMING SIMPLIFIED
2. LOW PASS FILTER INTRODUCES APPROXIMATELY 35 NSEC DELAY
3 DASHED LINE INDICATES LOW PASS FILTER OUTPUT

8M30

Figure 3-33. Data Latch Circuit

resolution winder, the high resolution channel pulse clocks in the low resolution channel window to set the data latch. This produces an output from the latch which retains the timing of the high resolution channel.

The high resolution channel may form extraneous pulses caused by the low frequency input dropping through the zero cross-over detector. These extraneous pulses would follow the legitimate pulse. However, they are ignored by the latch because the latch cannot be set without the presence of the low resolution channel pulse. The low resolution channel has no extraneous pulses because the third harmonic is suppressed, and eliminates the dropping.

Index Detection Circuit

The index detection circuit (Figure 3-34) generates a 2.4 μsec pulse at the start of each new logical track. This signal is returned to the controller as Index and also resets the sector counter to zero. Not odd and not even dibits are presented to a retriggerable multivibrator. The output of the multivibrator is held high until the Index pattern is present. The start of the Index pattern activates the Index counter/decoder. Only the correct missing dibit pattern will cause the counter to increment to the correct code (as shown in the timing diagram). After the counter reaches the code 01101, the next clock pulse resets the latch, and thus the counter, and also provides a 2.48 μsec Index pulse from the decoder.

Note that Index is inhibited while the heads are over either a forward or reverse EOT area.

Sector Counting Circuit

The sector circuit (Figure 3-35) permits the controller to determine the current angular position (sector) of the heads with respect to Index. Each track may be considered as subdivided into 64 segments (sectors). They are numbered from 000 through 127. Sector 000 is the first sector following Index.

A 403 kHz clock signal, derived from the servo track dibits, is used to generate the sector count. The Index pulse resets the sector bit counter and sector counter. The first positive-going pulse after Index increments the sector bit counter. The counter continues to be incremented by the 806-kHz clock until it reaches 128 (bit 2^7 high), at which time a Sector pulse is generated. The Sector pulse resets the sector bit counter, increments the sector counter, and is sent to the controller. The sector counter is incremented by Sector pulses until it reaches a count of 127. It is reset by the Index pulse. Sector Count Enable must be high for the sector counter to increment.

Read PLO and Data Separator

General

This circuit has two functions: (1) to convert the MFM data from the analog to digital converter into MRZ data and (2) to generate a Read Clock signal which is locked to the frequency of the read data (9.67 MHz nominal). Both the NRZ data and the Read Clock signal are transmitted to the controller.

The read PLO and data separator circuits consists of four main parts (refer to figure 3-36):

- Input Control - Controls whether MFM data or 4.84 MHz clock pulses will furnish the input to the circuit.
- Data Strobe Delay - Delays the pulses to provide the proper input to the VCO. These circuits also provide error recovery cability.
- Phase Lock Loop - Synchronizes the circuit outputs to the phase and frequency of the inputs.

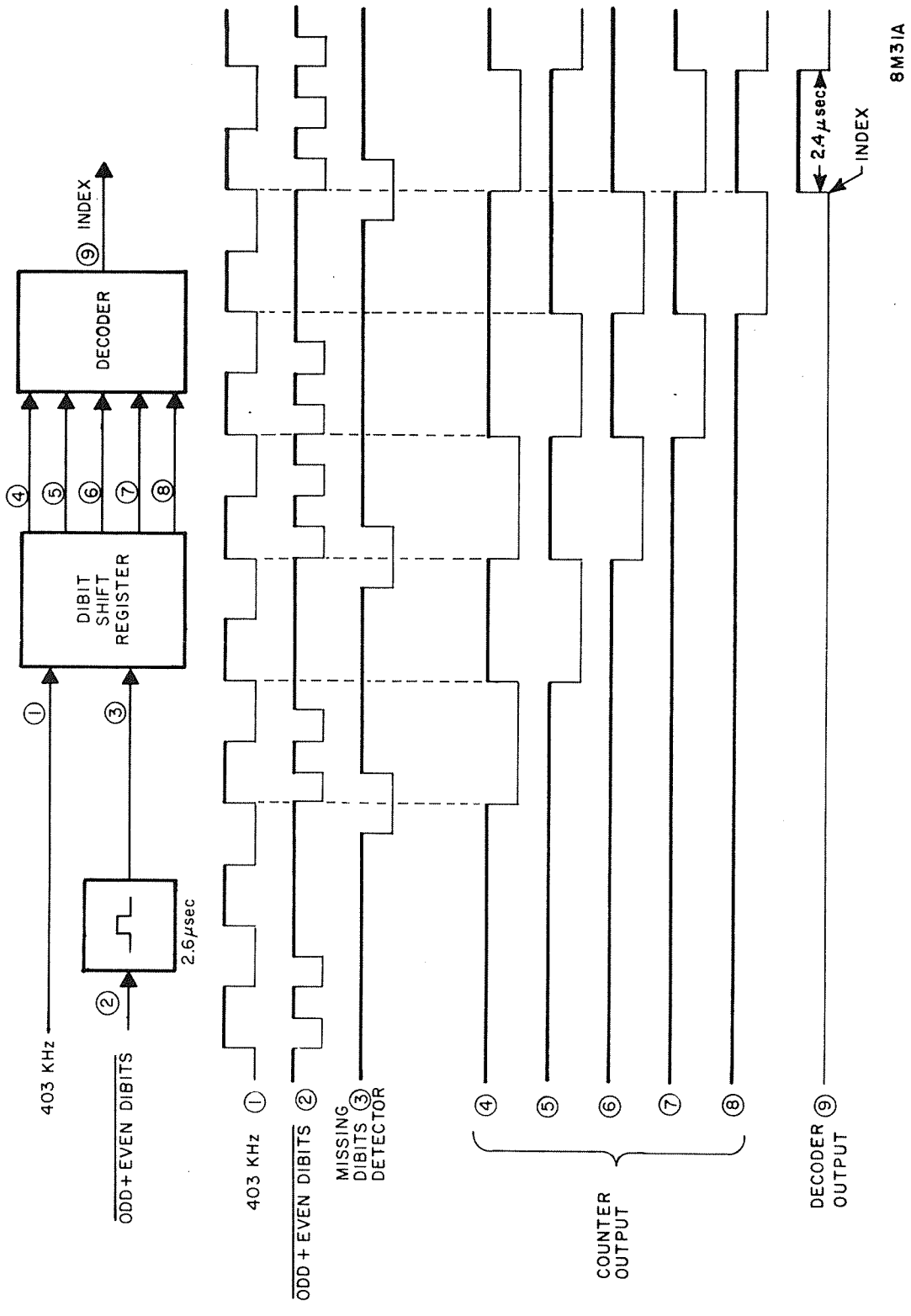


Figure 3-34. Index Detection Circuit

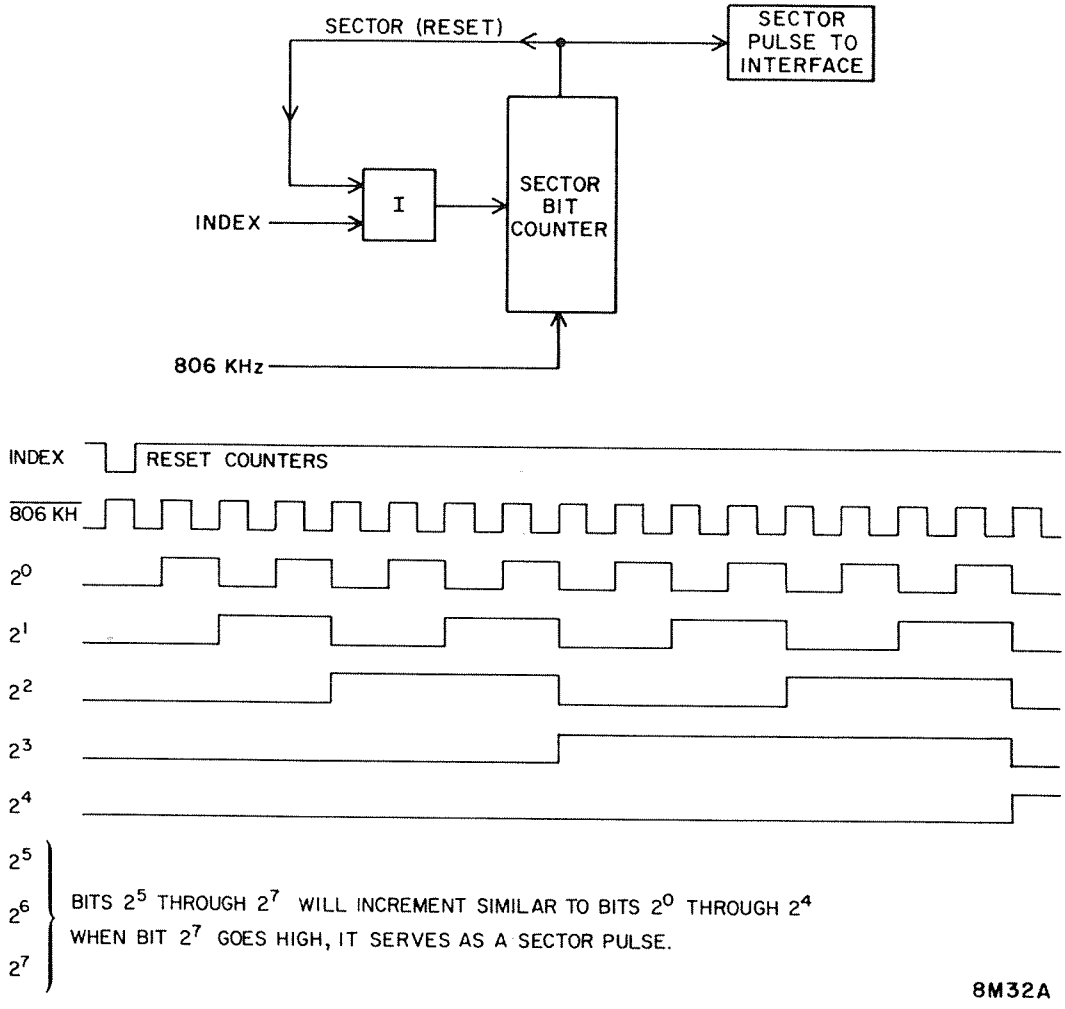


Figure 3-35. Sector Circuit

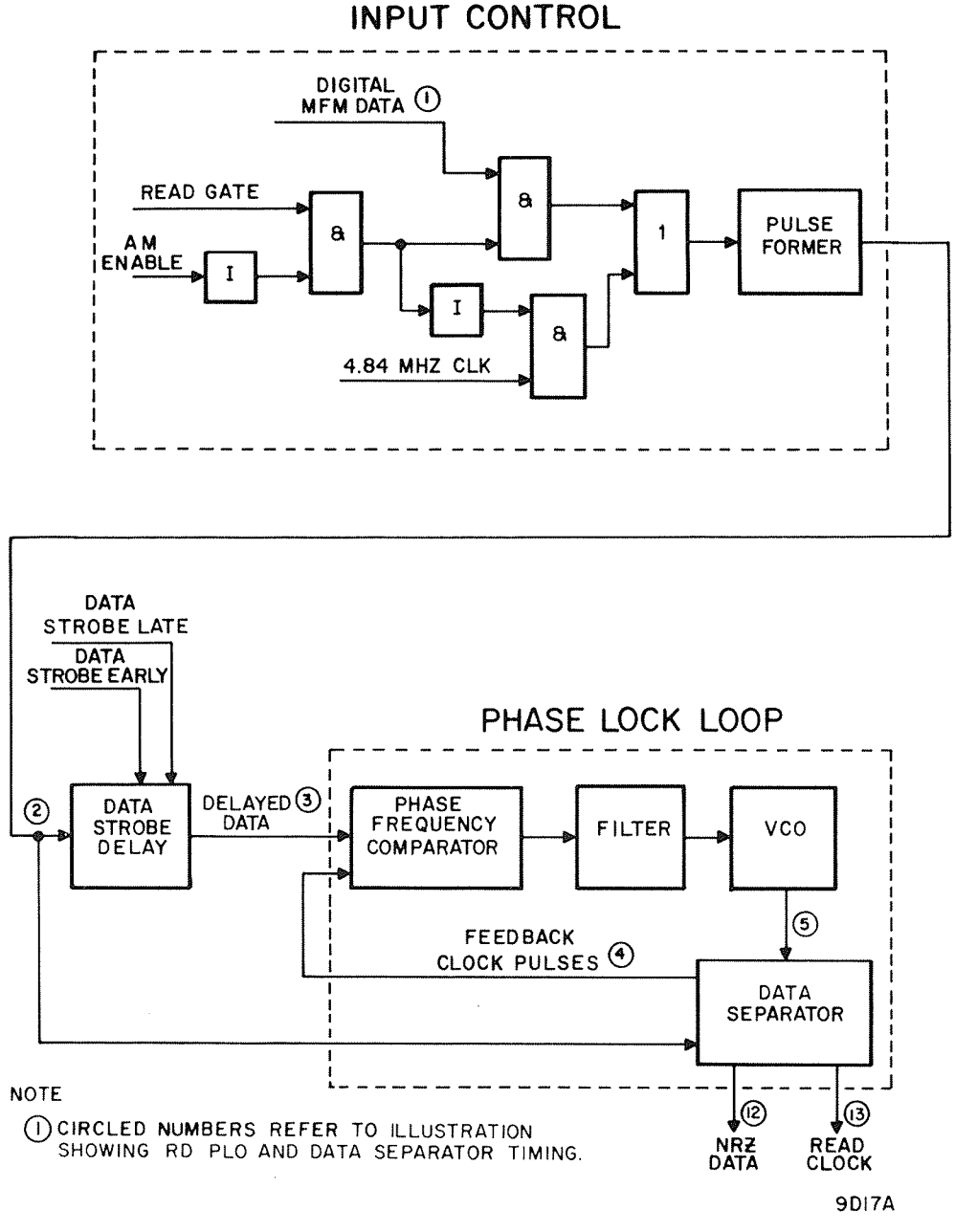


Figure 3-36. Read PLO and Data Separator Circuits

- Data Separator - Converts the MFM data to NRZ data and generates the Read clock. This circuit is actually a part of the phase lock loop.

The remainder of this discussion further describes the read PLO and data separator circuits.

Input Control

The input control circuit selects the input that will be used by the read PLO and data separator circuits. This input will always be either MFM data from the read analog to digital converter or 4.84 MHz clock pulses from the servo frequency multiplier circuit.

The 4.84 MHz clock signal is used only when the drive is not reading MFM data, such as before Read Gate is raised. It also uses the 4.84 MHz clock whenever the Address Mark Enable signal is active because this indicates the drive is expecting the Address Mark which contains no MFM data. The drive uses the clock signal as a substitute for the read data for two reasons: (1) the signal is derived from the track servo dibits and therefore, its frequency (like that of the read data) varies directly with disk pack speed and (2) after being processed by the pulse forming circuits, it has about the same nominal frequency as the read data (9.67 MHz). This results in it being easier for the phase lock loop to synchronize to the proper frequency when switching from one of the signals to the other.

Once selected the signal is applied to a pulse forming network which generates a 20 nsec pulse for each transition of the input. These pulses are then applied to the data strobe delay circuits and also furnish the data input to the data separator.

Data Strobe Delay

The purpose of the data strobe delay circuit (refer to figure 3-36) is to delay the data pulses sufficiently to provide the proper timing relationship at the input to the phase lock loop. The output of the data strobe delay circuit is delayed by a time determined by the state of the Data Strobe Early and Data Strobe Late signals. These signals facilitate the recover of marginal data and are enabled by the Error Recovery tag (001).

The output of this circuit is the Delayed Data signals which are sent to the input of the phase lock loop.

Phase Lock Loop

The phase lock loop (refer to figure 3-36) synchronizes the read PLO/data separator circuit outputs (NRZ data and Read Clock) to the input (either MFM data or 4.84 MHz clock). The loop accomplishes this by comparing and following two signals: (1) the Delayed Data signals which have a constant phase and frequency relationship to the input MFM data or 4.84 MHz Clock (whichever is used) and (2) the Feedback Clock Pulse signals which have a constant phase and frequency relationship to the output NRZ data and Read Clock signals. The loop inputs are applied to the phase/frequency comparator.

The phase/frequency comparator generates output pulses which are a function of the phase and frequency between the positive going edges of the inputs. The filter circuit uses the comparator outputs to generate a control voltage for the voltage controlled oscillator (VCO).

This control voltage causes the frequency of the VCO to vary in the direction necessary to eliminate the phase and frequency differences between the two signals that were input to the comparator.

The output frequency of the VCO is actually twice that of the input so for an input of 9.67 MHz it has an output of 19.34 MHz. However, the data separator divides this by two before generating the Feedback Clock Pulse signals thereby providing a feedback to the comparator that satisfies the loop.

Data Separator

This circuit determines if the data pulses represent a one or zero and then converts the data to NRZ. It also generates the Feelback Clock Pulses to the comparator and the 9.67 MHz Read Clock that is sent to the controller. Figures 3-37 and 3-38 show simplified logic and timing for the data separator circuit.

The VCO outputs provide the proper timing relationships for the data separator by controlling the Data Window and Read Clock FFs. The Read Clock FF generates the 9.67 MHz Read Clock signal and also provides timing signals to the data separator logic. The Data Window FF generates the Data window which is used to determine whether the input data pulses represent ones or zeros. The actual decoding of the data is done by the "1's" Enable and "0's" Enable FFs.

If a data pulse represents a one it occurs during the data window and sets the "1's" Enable FF. Setting this FF generates a Feedback Clock pulse and causes the Data Buffer to generate a NRZ one.

If the data pulse represents a zero the "1's" Enable FF is not set and the Data Buffer FF generates a NRZ zero. In this case the "0's" Enable FF which is set by every data pulse generates the Feedback Clock Pulse signal.

Before accurate detection of data can begin, the proper phase relationship must be established between the data (representing ones and zeros) and the VCO output pulses. This is done during a 7.75 µsec lock to data period which is initiated by the Lock to Data signal. This signal is a 7.75 µsec pulse that occurs when the Read Gate signal goes true or when the Address Mark is detected. The Lock to Data signal holds the "0's" Enable FF set and disables the output of the "1's" Enable FF. Therefore, if the circuit is to synchronize properly the pulse must occur during a period when the drive is reading only zeros.

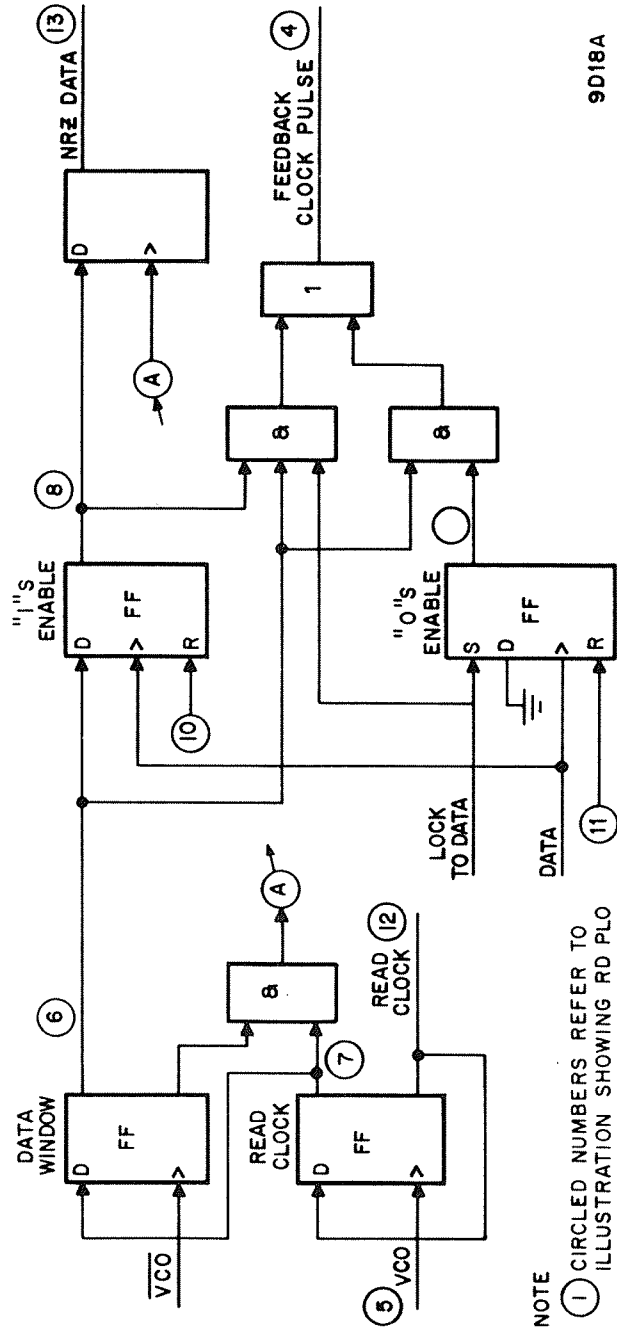
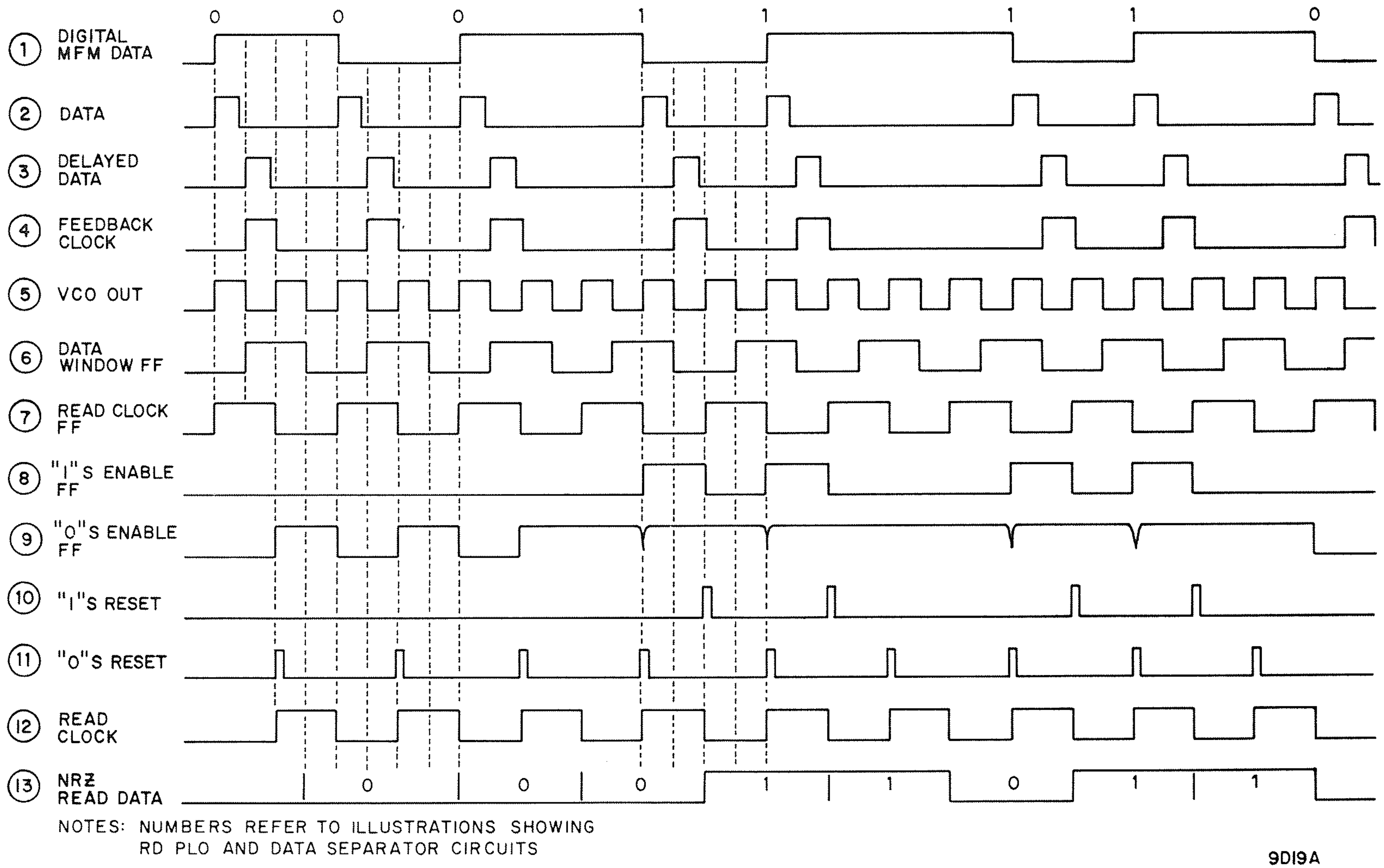


Figure 3-37. Data Separator Logic



NOTES: NUMBERS REFER TO ILLUSTRATIONS SHOWING RD PLO AND DATA SEPARATOR CIRCUITS

Figure 3-38. RD PLO and Data Separator Timing

at the "1's" flip-flop during the proper phase of the clock, the "1's" enable FF is set. Setting the FF inhibits the output gating of the "0's" enable FF, provides the data out signal, and supplies a reference signal to the comparator. Clock pulses from the read signal set the "0's" enable FF, which also supplies reference pulses to the comparator.

The Lock-to-Data signal is kept high only long enough to achieve phase-lock during the preamble that occurs at the beginning of a record. This phase-lock period is necessary to establish the proper phase relationship between the data to be received and the 9.67 MHz clock from the VCO and to signify to the phase-lock loop that it is receiving a field of zeros.

Servo Frequency Multiplier Circuit

The Servo Frequency Multiplier circuit (Figure 3-39) uses dibits produced by the track servo circuit to generate the basic 806-kHz clock signal. The signal is applied to the index and sector detection circuits. The servo frequency multiplier circuit also provides a 9.67 MHz Servo Clock signal to the controller and a 4.84 MHz clock to the read PLO.

The nominal frequency of the dibits is 806 kHz; however, the actual frequency is a function of the spindle motor speed. The phase-locked loop (PLL) in the clock circuit synchronizes itself to the actual dibit rate. This permits the clock to react to variations in spindle speed. Signals derived from this circuit, such as servo clock, are a function of actual spindle speed rather than functions of an absolute time base, and therefore bit density is independent of disk speed.

Input dibits are applied to two retriggerable multivibrators: one supplies a 1.6 μsec (approximate) output pulse, the other a 750 nsec (approximate) output pulse. The 1.6 μsec pulse is longer than the dibit period, thus providing a continuous gate for the feedback pulses from the voltage controlled oscillator (VCO) as long as dibits are present. The output of the other multivibrator is fed through a delay which produces 25-nsec pulses for application to the phase/frequency comparator at the actual dibit frequency. The comparator generates output pulses which are a function of the time (or phase) difference between the positive-going edges of the two inputs. One input, designated the reference input, is the delayed dibit pulses; and the other input, designated the feedback input, is the clock derived from the voltage-controlled oscillator. The output of the comparator is fixed amplitude positive and negative pulses which are applied to an active filter circuit. The filter circuit integrates the two inputs to generate a control voltage proportional to the phase error. This voltage is applied to the VCO to adjust for any changes in the frequency of the two signals being compared.

Write Clock Frequency Multiplier

A times-two phase-lock loop multiplies the 9.67 MHz Write Clock for use in generation of the optional MFM write-compensated data. The operation of this circuit is essentially similar to that of the servo frequency multiplier circuit. The input to this circuit is the returned 9.67 MHz clock sent to the controller from the servo frequency multiplier circuit. This scheme eliminates the effect of cable propagation delays in drives that use the NRZ-to-MFM option.

FAULT DETECTION

There are five fault conditions detected by the logic. These are:

- Write Fault
- More Than One Head Selected
- Read AND Write
- (Read OR Write) AND Off Cylinder
- Voltage Fault

Setting the latches of any one of these fault detection circuits (Figure 3-40) sends a Fault signal to the controller and to the drive operator panel; it also

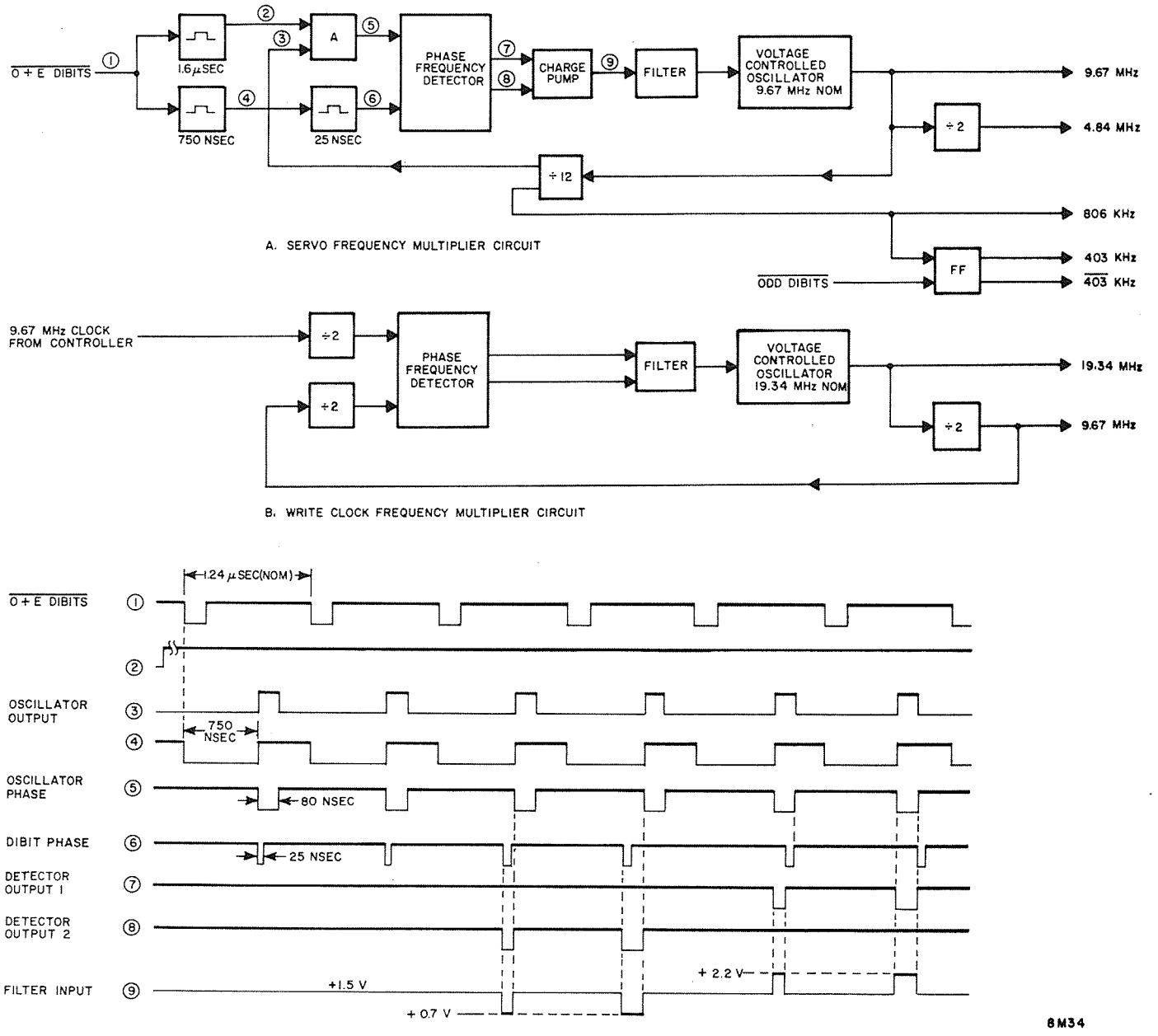


Figure 3-39. Servo Write Clock Frequency Timing Diagram

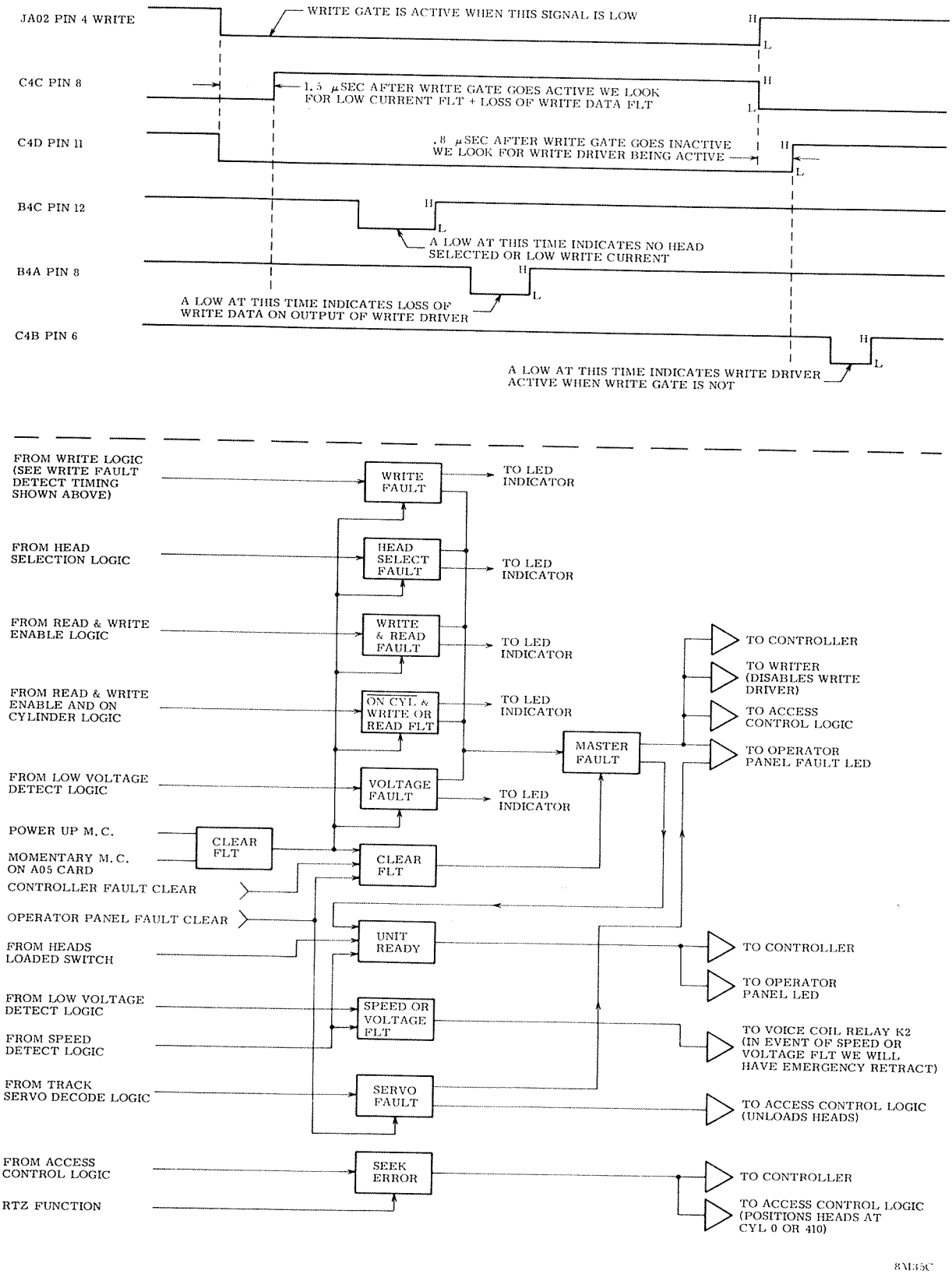


Figure 3-40. Fault Detection Circuits

inhibits the write circuitry and the Unit Ready condition. Fault conditions are cleared as follows: Master Fault is cleared by a power-up, a Fault Clear signal from the controller, pressing the FAULT push-button on the operator panel, or by pressing the MOMENTARY switch (located at logic card location 5); the Fault register is cleared by a power-up or the MOMENTARY switch.

Write Fault

The Write Fault indicates low (or the absence of) write current. The level of the current supplied to the write winding is sensed by a level detector and converted to logic levels to generate a Write Fault.

In addition, the ac Write fault circuit detects improper write current conditions that occur with open, shorted, half-open, half-shorted, and/or missing center tap heads. As long as the write drives is operating properly, the threshold detector continuously toggles and retriggers the single shot multivibrator. The single shot times out if the toggling stops. Thus, a Write Fault is generated if either the write current level drops or if the toggling stops, and if the write circuitry is enabled. A Write Fault is also generated if current is passed through the head on a Read operation.

More Than One Head Selected

This fault is generated whenever more than one head is selected. The outputs of the head select circuits are monitored by summing and voltage comparator circuits. If more than one head is selected, the circuit generates a Multiple Select Fault which sets the Head Select Fault latch.

Read AND Write

This fault is generated whenever the drive receives a Read gate and Write gate simultaneously from the controller. This condition sets the Read AND Write fault latch.

(Read OR Write) AND Off Cylinder

This fault is generated if the drive is in an Off Cylinder condition and it receives a Read or Write gate from the controller. This condition sets the (Read OR Write) AND Not On Cylinder fault latch.

Voltage Fault

This fault indicates below normal levels for the positive and negative dc voltages by setting the Voltage fault latch.

SECTION 4

KEY TO LOGIC

GENERAL

Section 4 contains information on logic symbology, operational amplifiers, integrated circuit package configuration, discrete component descriptions and logic card diagrams.

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

Both TTL and ECL integrated circuits are used. Nominal logic levels for these two IC families are given below, along with a typical expected range. All signals are named for their function when thier logic value is "1".

Logical State	Nominal Voltage	Typical Range
TTL "1"	+3 V	+2.5 V to +4.0 V*
TTL "0"	0 V	0 V to +0.9 V
ECL "1"	-0.9 V	-0.61 V to -0.97 V
ECL "0"	-1.8 V	-1.52 V to -2.38 V

* Measuring a TTL open collector voltage may result in a reading that is close to the actual power supply voltage.

Different circuit configurations, temperatures, and so on may result in legitimate readings that fall outside of the typical range. Such readings, however, should be suspect in the event of trouble.

LOGIC CHASSIS

The Logic Chassis consists of the logic board wire wrap assembly and guiding piece parts for the logic cards.

Logic cards are plugged into the logic board wire wrap assembly. Guide rails connected to perpendicular panels guide the cards into place and restrict horizontal or vertical movement.

Wire wrap pins extend through the back panel. The logic cards mate with these pins on one side of the back panel. On the other side, the "wire wrap" side, wiring interconnects the logic functions between cards. This wiring is secured to the pins by the wire wrap technique. These pins also provide convenient test points for monitoring logic levels of all signals entering and leaving each card.

The wire wrap surface of the logic board wire wrap assembly contains wire wrap pin identification (Figure 4-1). Logic cards are designated by horizontal row (A) and vertical column (1 through 16). Wire wrap pins are then called out by pin number and column A or B. For example, A8-12B is the back panel pin at logic row A, position 8, pin 12 of column B.

JA01 through JA04, PA1, PA2, PA6, PA7, P09, and JA10 are auxiliary connectors used to interface logic cards with maintenance panel, I/O connectors, etc. Pin identification is by pin number (1 through 14) and row (A or B). (JA01-5A is auxiliary connector JA01, pin 5, row A.)

LOGIC CARDS

PHYSICAL DESCRIPTION

All components of the logic cards (Figure 4-2) are mounted on one side of a printed circuit board (PCB). Numeral designators (1 through 99) are etched on the non-component side of the board identify each transistor. A 4-character alphanumeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alphanumeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

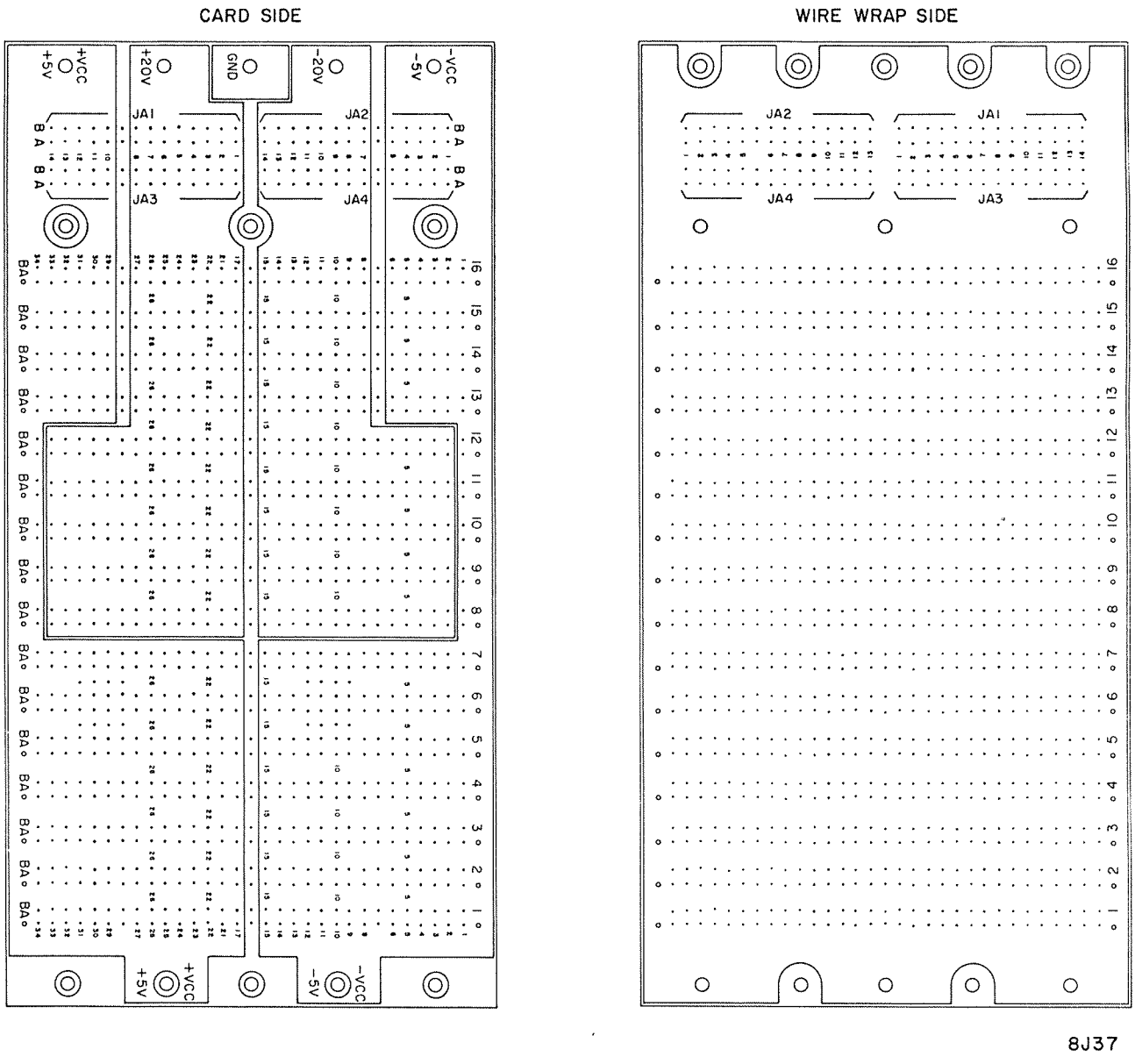


Figure 4-1. Wire Wrap Board Assembly

PIN ASSIGNMENTS

Cards are equipped with a 62-pin (sockets) connector. Connectors are mounted along the shorter dimension on the component side of the board.

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34, however, pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic

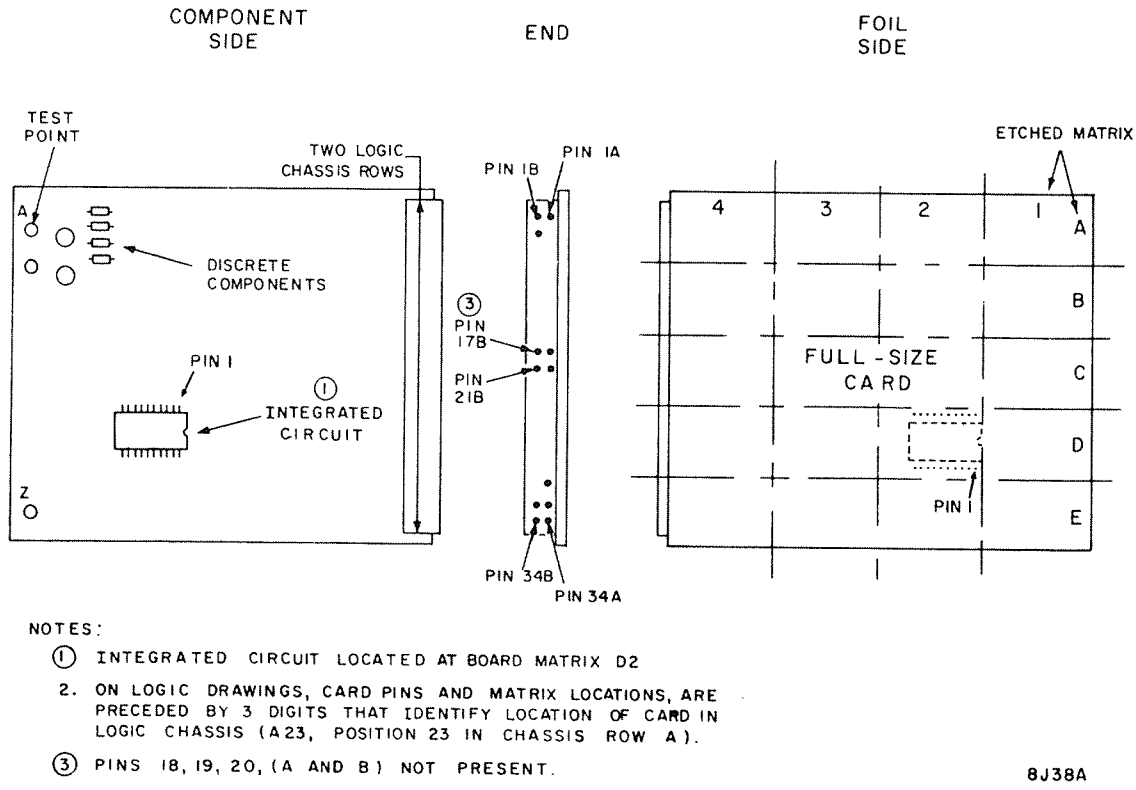


Figure 4-2. Logic Card Detail

chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

TEST POINTS

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alphanumerically starting with A on the top, outer edge. Test points A and Z are available for ground reference on full-size cards. Only test point Z is available for ground reference on half-size cards.

LOGIC SYMBOLOGY

INPUT/OUTPUT STATE INDICATORS

Input/output state indicators are the polarity indicator (—▷| or |▷—) and the logic negation indicator (—○| or |○—).

The input polarity indicator indicates the most negative potential is required to satisfy the logic function represented by the qualifying symbol. The output polarity indicator indicates the most negative potential is present at the output when the logic function is satisfied. The absence of the polarity indicator indicates the most positive potential is present.

The logic negation indicator is a small circle located at the origin or termination of a signal line, and tangent to a logic symbol. The presence or absence of this indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a "0" logic level on that line is needed to satisfy the function. The absence of the circle represents a logical "1" as needed to satisfy the function.

The relative level indicator depicts the occurrence of inversion. Figure 4-3 shows some representative examples of the relative level indicator being used in this manner.

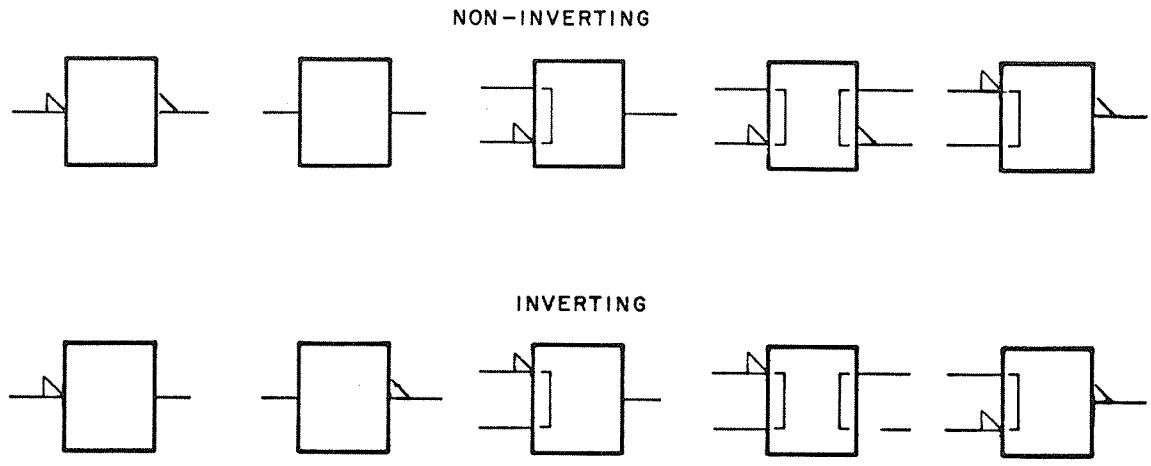


Figure 4-3. Inversion Conventions

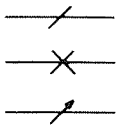
DYNAMIC INDICATOR

The presence of a dynamic indicator (⊢) just inside a symbol indicates the inputs are gated (satisfied) with the dynamic positive-going transition of the input line to the state shown. A logic negation indicator (circle) accompanying the dynamic indicator signifies that a negative-going transition is required to gate in the inputs. Absence of the dynamic indicator indicates the inputs are gated (satisfied) with the static state of the input line.

SIGNAL LINE INDICATORS

Non—Standard Levels

Some signal line indicators indicate non-standard levels on input/output lines. These signal line indicators are as follows:


non-standard logic levels

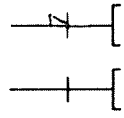
analog or non-logic levels

variable control

Absence of these indicators shown above indicates a standard logic level.

Inhibit

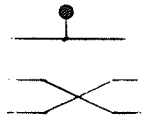
The inhibit line indicates gating of the logic function will be inhibited whenever the line is at the level indicated by the logic negation indicator. Inhibit line symbols are as follows:


with logic negation indicator

without logic negation indicator

Miscellaneous

Other signal line indicators are as follows:


test point

twisted pair

FUNCTION SYMBOLS

Circuit function symbols for discrete components and integrated circuits are as follows:

1 OR gate or inverter

& AND gate

=1	exclusive OR
▷	amplifier (with or without gain)
▷	amplifier with adjustable gain
Σ▷	summing amplifier
∫▷	integrating amplifier
∂▷	differentiating amplifier
X/▷	digital to analog conversion
X/▷	digital to analog conversion with adjustable gain
▷/Y	analog to digital conversion
▷ X/Y	amplifying level translator (gain noted outside box)
|▷|	positive analog rectifier (symbol preceded by a minus sign if negative rectification is used)
ΣX/▷	analog summation of digital inputs. Reference voltage outside box indicates output signal level resulting when specified input(s) are negated
▷□Y	Schmitt trigger
▷	saturable, non-linear, gain controlled amplifier
F▷	function generator
∩▷	active bandpass filter
∩	bandpass or resonant circuit
	bidirectional switch
X/Y	Level conversion - transmission line to logic level, switch state (ground or open) to logic level, logic level to power output (to drive lamp, relay, solenoid, etc.)
1	retriggerable multivibrator (single shot)
t_1 t_2	symmetry restoration circuit
200ns t2	ones delay - when input changes to a "1" a 200 nsec delay occurs before the "1" is passed on
t1 30ns	zeros delay - when input changes to a "0" a 30 nsec delay occurs before the "0" is passed on
35ns	both transistors are delayed by 35 nsec

INPUT/OUTPUT DESIGNATORS

Inputs are individually identified as necessary by an input designator inside the symbol block and adjacent to the left side following all prefixes indicating dependency. These input designators follow:

R	reset or clear
S	set
G	gating type input that affects other inputs or outputs
J	J input of J-K flip-flop
K	K input of J-K flip-flop
Z	used to link gating (clock) input of control block to J and K inputs of J-K flip-flops
T	toggle or complement input
D	data input of D-type flip-flops
C	a gating (clock input for D-type flip-flops)
→	shift right (or down)
←	shift left (or up)
+1	increase contents by one (count up)
-1	decrease contents by one (count down)
]OR[	indicates grouped inputs that maintain a fixed relationship in states and always change together
1, 2, 4, 8	indicates relative weighting of inputs or outputs in codes. They may be consecutive, binary, decimal representation of binary values, etc.
A, B, C, ETC.	when two or more of these are used together in inputs to a symbol, it indicates individual signals or individual groups of signals to be identified for further operations such as arithmetic functions

Certain input designators (C and G) may also be used as prefixes to other input designators, but not to each other, C and G indicate dependency of every designator, such as D, they prefix, and are referred to as dependency notation. For example, CD indicates that the input is gated to a D-type flip-flop only when

the C input is active. Gate dependent inputs (G) may be distinguished from each other by 1, 2, etc., following the G. Where more than a single G term is involved, commas are used to separate the numbers. Clock dependent inputs for loading data are denoted by a "C". Different C inputs are distinguished by a number following the C.

COMMON CONTROL BLOCK

Signals entering the common control block (Figure 4-4) are common to more than one section of the circuit. The neck of the common control block abuts the top or bottom of the sections it controls. Input designators may include C, G, R, →, ←, +1, -1, plus select lines with or without decoding.

WIRED FUNCTIONS

The logical representation for wired functions is shown in Figure 4-5. These functions are used where circuits have the capability of being combined as an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function simply requires that one of the inputs be a logic "0" before the output can be a logic "0". The wired AND output will be a logic "1" only when both inputs are logic "1's".

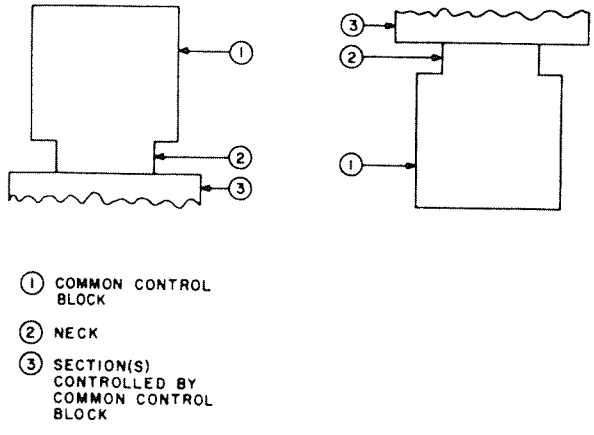


Figure 4-4. Common Control Block

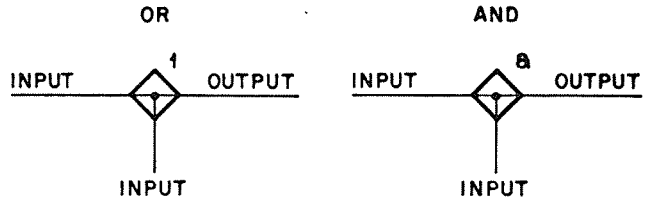


Figure 4-5. Wired Functions 6710

INTEGRATED CIRCUITS

Figure 4-6 shows the schematic version (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

Referring to Figure 4-6 it is apparent that the two versions are essentially the same. Both views identify pin numbers, the function symbol, and the CDC element number for the circuit. Refer to Section 5 for manufacturer's information on the various element numbers.

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbols reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5.

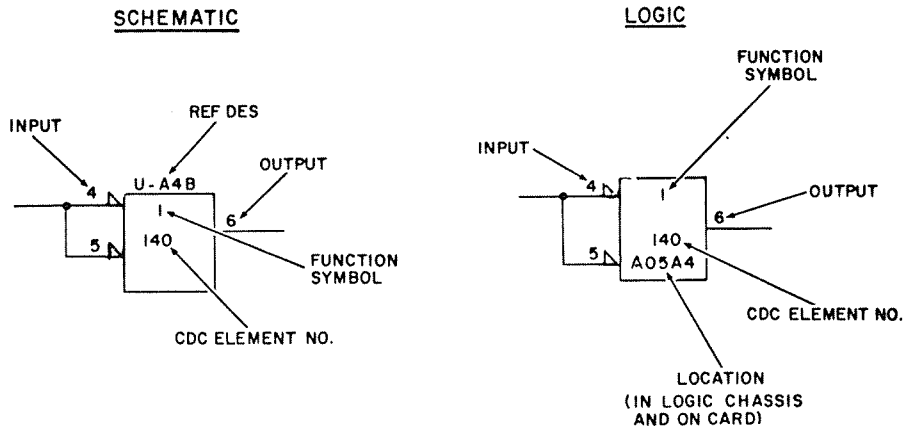


Figure 4-6. Integrated Circuit

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can amplify signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used extensively in the drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Zero offset: output is zero when input is zero
5. High bandwidth frequency response

BASIC CIRCUIT ELEMENTS

Figure 4-7 is a highly simplified schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FTEs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 mv are applied to the non-inverting input while 9 mv are applied to the inverting input, the extra 1 mv difference is amplified. The amplification, which may be a voltage gain of up to 100,000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the "common-mode" input signal. In the preceding example, the 9 mv are the common-mode input, while 1 mv is the differential input. In the ideal op amp, the output is zero with identical inputs. Only the difference (1 mv) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

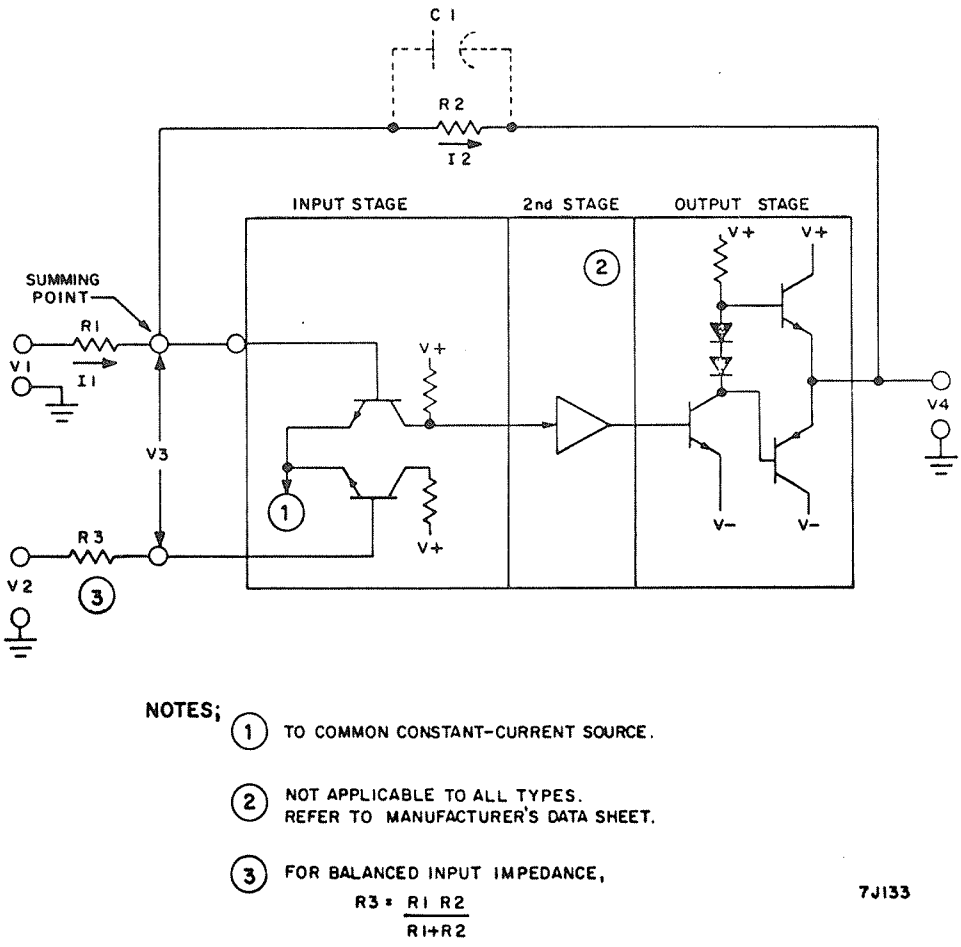


Figure 4-7. Simplified Op Amp Schematic

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.

BASIC CIRCUIT FUNCTIONS

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; it can be assumed to be zero.
2. The differential voltage (V3) is insignificant and can be assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current (I1) entering the summing point must leave it (I2). These currents are:

$I1 = V1/R1$
$I2 = -V4/R2$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohms Law:

$V4/V1 = -R2/R1$ or $V4 = -V1(R21R1)$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, a frequency increases, the effective impedance of R2-C1 decreases to reduce overall gain.

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset, that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made to be equal, that is, they see equal input impedances, they are common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule #2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a "virtual" ground, that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

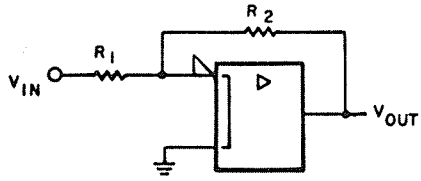
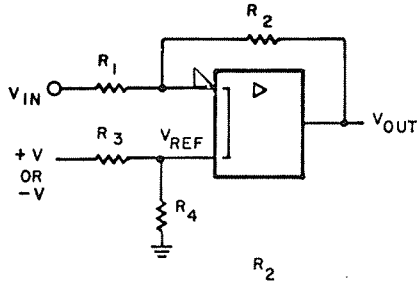
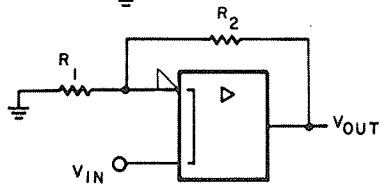
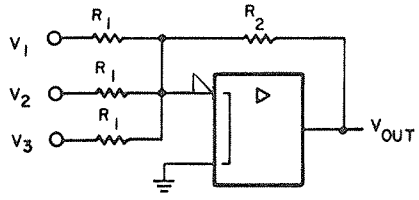
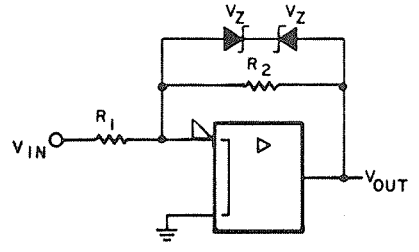
Typical op amp circuit functions are illustrated in Figure 4-8.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (Figure 4-9). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

Consider A376 of Figure 4-9. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1,28v. Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

CIRCUIT TYPE	SYMBOL	OUTPUT ①
INVERTING AMP		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$
INVERTING AMP WITH REFERENCE VOLTAGE		$V_{OUT} = V_{REF} + \frac{R_2 (V_{REF} - V_{IN})}{R_1}$ OBSERVE ALGEBRAIC SIGNS IF COMPUTING $V_{OUT} = 0$ IF $V_{IN} = V_{REF}$ $V_{REF} = \pm V\left(\frac{R_3}{R_3 + R_4}\right)$
NON INVERTING AMPLIFIER		$V_{OUT} = \frac{V_{IN} (R_1 + R_2)}{R_1}$
SUMMING AMPLIFIER		$V_{OUT} = -\left[\frac{R_2}{R_1} (V_1 + V_2 + V_3)\right]$
INVERTING AMPLIFIER WITH OUTPUT LIMITING		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$ IF $\pm V_{OUT} \leq V_Z$

NOTE:

① MINUS SIGN (-) INDICATES THAT OUTPUT IS INVERTED.

7J91-1

Figure 4-8. Op Amp Circuit Functions (Sheet 1 of 3)

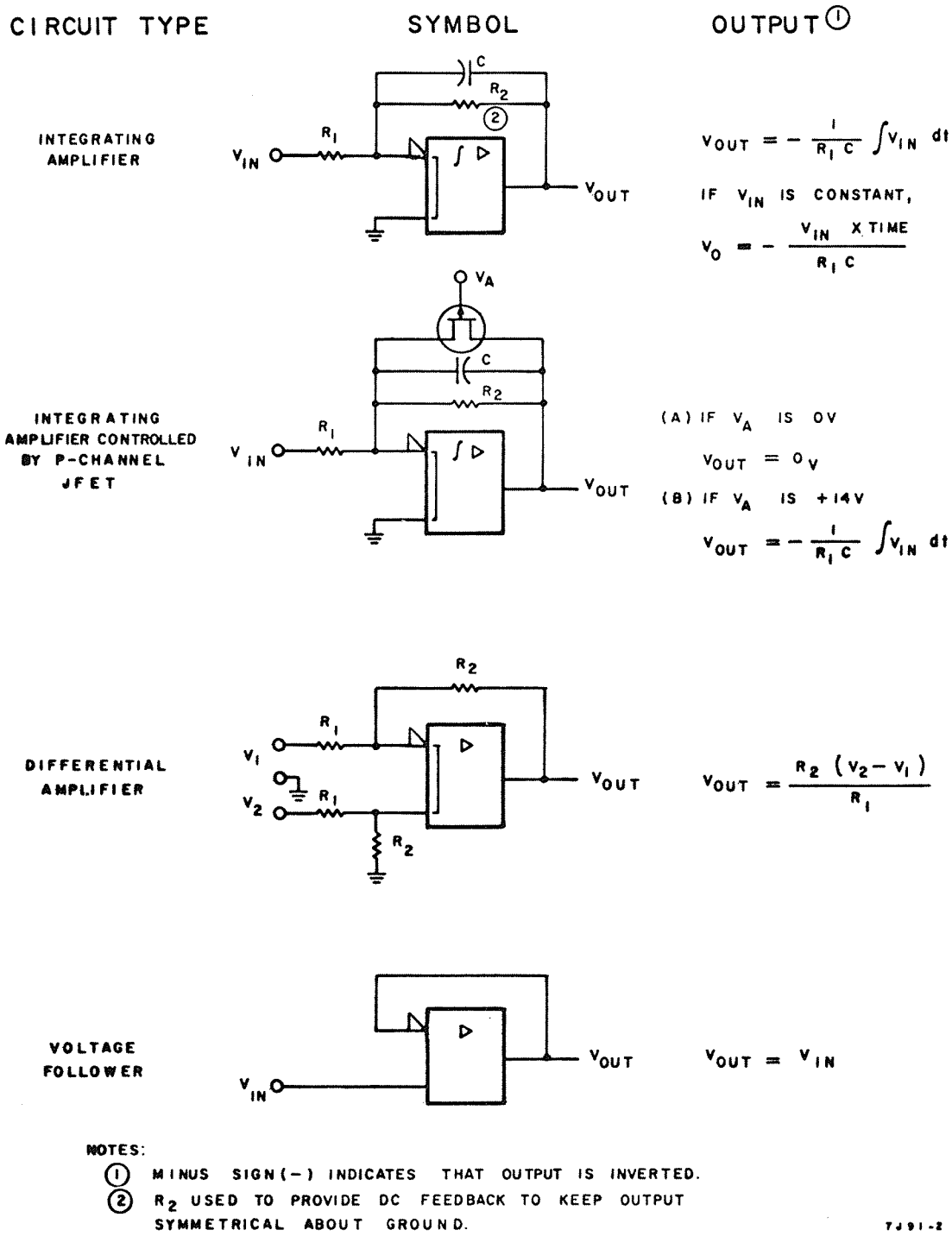


Figure 4-8. Op Amp Circuit Functions (Sheet 2 of 3)

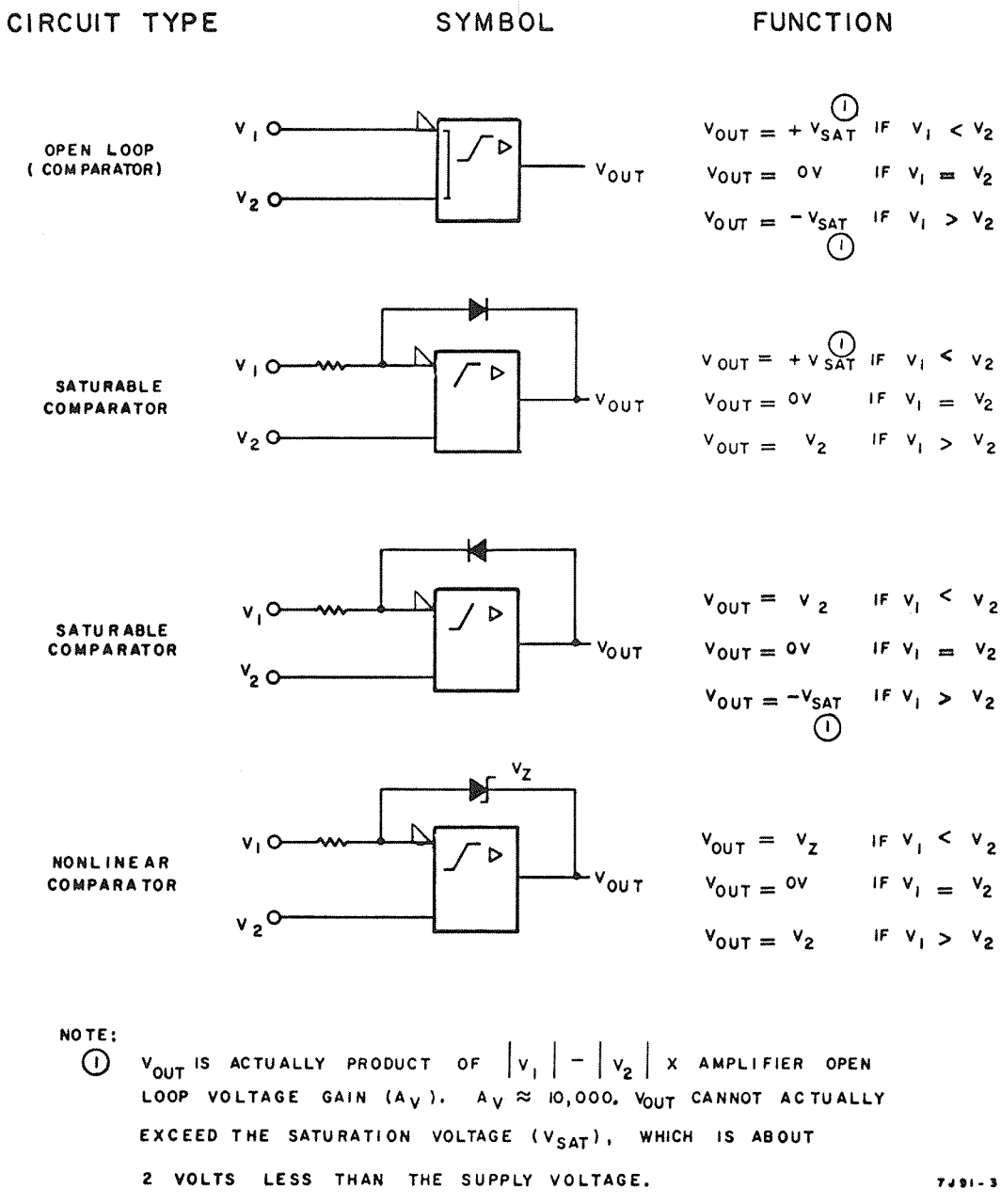
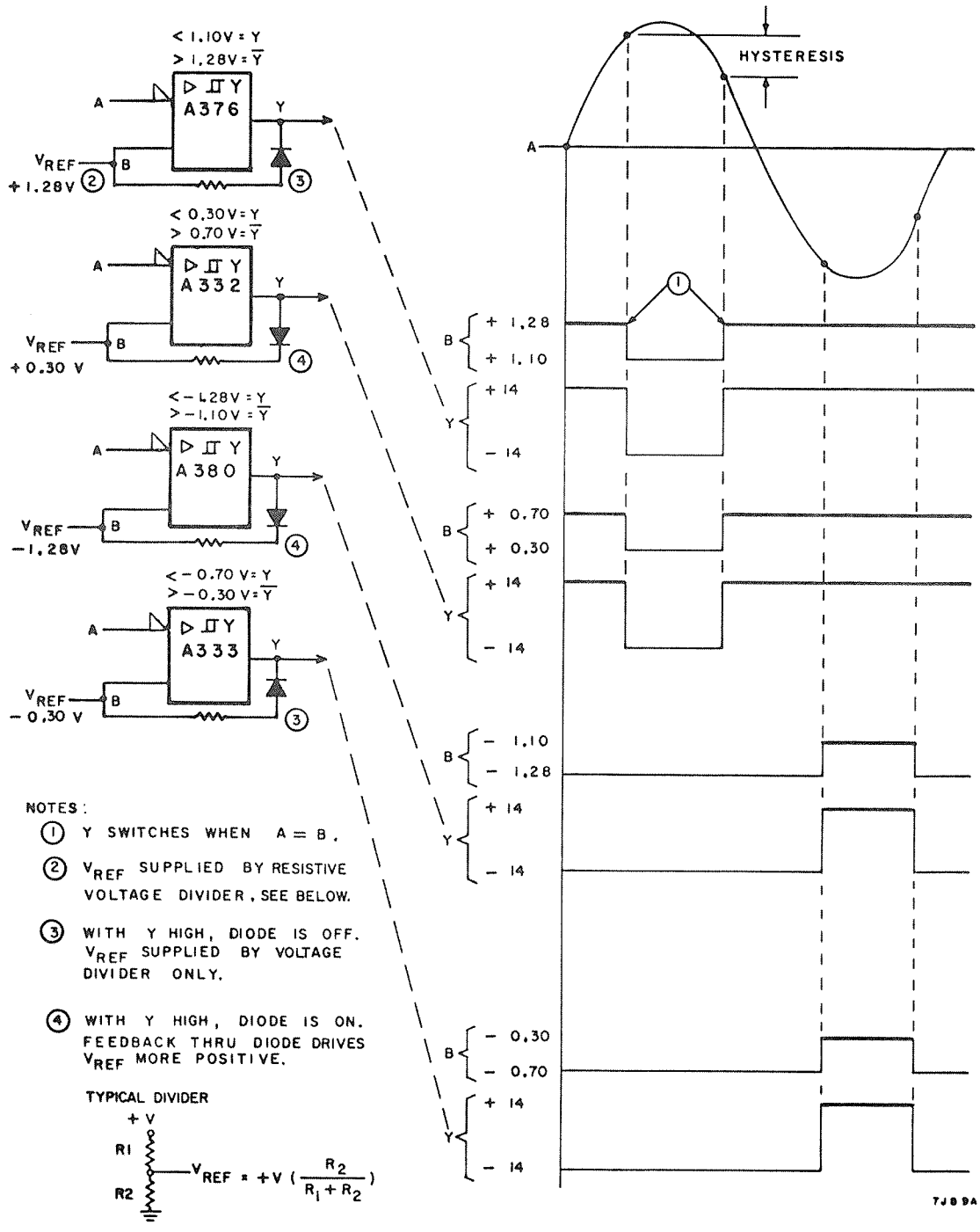


Figure 4-8. Op Amp Circuit Functions (Sheet 3 of 3)



NOTES:

1. Y SWITCHES WHEN A = B.
2. V_{REF} SUPPLIED BY RESISTIVE VOLTAGE DIVIDER, SEE BELOW.
3. WITH Y HIGH, DIODE IS OFF. V_{REF} SUPPLIED BY VOLTAGE DIVIDER ONLY.
4. WITH Y HIGH, DIODE IS ON. FEEDBACK THRU DIODE DRIVES V_{REF} MORE POSITIVE.

TYPICAL DIVIDER

As the input A goes more positive, the output does not change until A equals B (+1.28v). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14v available at Y, the voltage at B is reduced to +1.10v. The input must now swing to less than +1.10v for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

DISCRETE COMPONENT CIRCUITS

Figure 4-10 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Three lines of information are contained within the logic symbol. The top line is the function symbol and designates the board logic function of that particular symbol. In this case, ▷ represents an amplifier, the logic function performed by the circuit. The second line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator, detailed information on that particular circuit may be obtained by referring to Section 6.

The third line within the symbol identifies which logic card location the circuit is located on.

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (i.e., Q22 on the card schematic diagram).

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

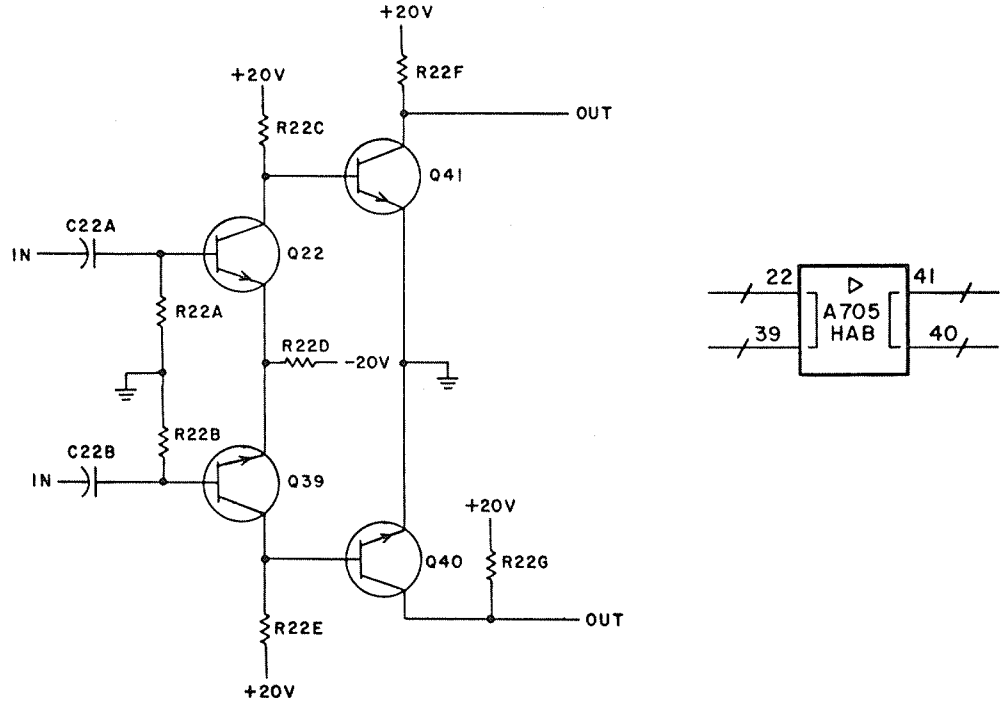


Figure 4-10. Discrete Component Circuit

The lines on the interior of the logic block that bracket both inputs and both outputs show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

For schematic diagrams of discrete component circuits used in this device see Section 3. An analysis of circuit operation supports each circuit diagram. The order of presentation is in accordance with the three-letter alphabetical circuit type designator.

SECTION 5

INTEGRATED CIRCUIT PACKAGE CONFIGURATIONS

INTRODUCTION

Section 5 contains descriptive information regarding all integrated circuits used in the BJ7XX logic. Integrated circuit descriptions are arranged numerically from the lowest numbered element, to the highest numbered element. Refer to section 4 for an explanation of the symbology used in section 5.

Description

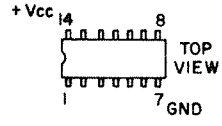
The 140 circuit is a four-section (quad), 2-input, positive NAND gate.

NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

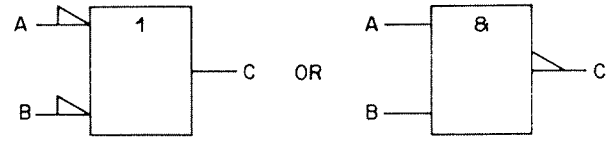
Element	Vendor Number
140	7400,9002
140H	74H00
140L	74L00
140LS	74LS00
140A	74S00

3. Package pin configuration.

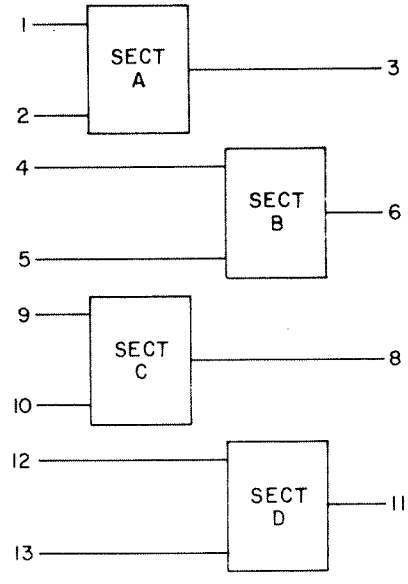


A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE
(FOR ONE GATE)



LOGIC SYMBOL



PIN ASSIGNMENTS

140
Rev C
Sheet 1 of 1

Description

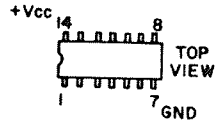
The 141 circuit is a three-section, 3-input, positive NAND gate.

NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

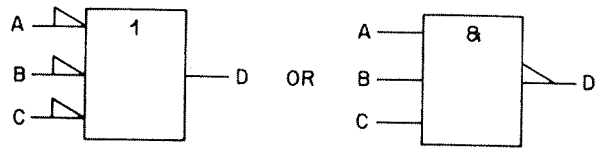
Element	Vendor Number
141	7410,9003
141H	74H10
141L	74L10
141LS	74LS10
141S	74S10

3. Package pin configuration.

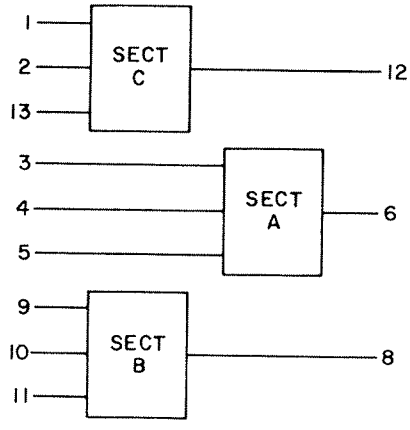


A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



PIN ASSIGNMENTS

141
Rev B
Sheet 1 of 1

Description

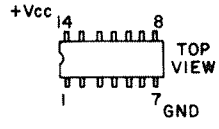
The 143 circuit is a two-section, 3-input, positive NAND gate.

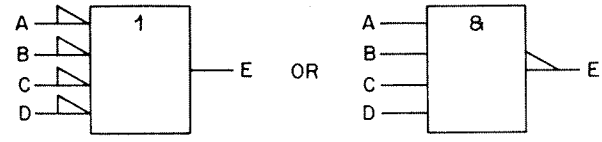
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

Element	Vendor Number
143	7440,9009
143H	74H40
143S	74S00

3. Package pin configuration.

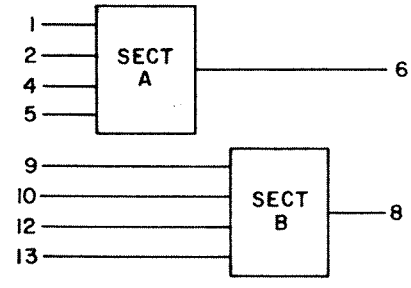




LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE
(FOR ONE GATE)



PIN ASSIGNMENTS

143
Rev B
Sheet 1 of 1

Description

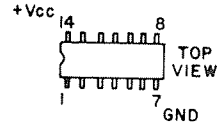
Circuit 145 is a dual, expandable AND-OR-INVERT gate. Section B of this circuit is expandable. If not expanded pins 11 and 12 are open.

NOTES:

1. If not used, expander pins may not be shown.
2. Vendor identification:

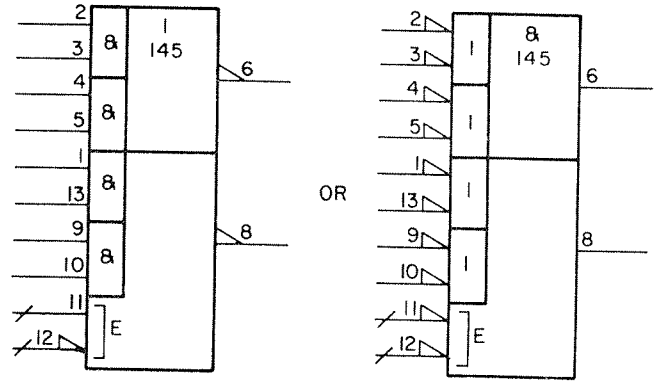
Element	Vendor Number
145	9005
145H	74H50

3. Package pin configuration.

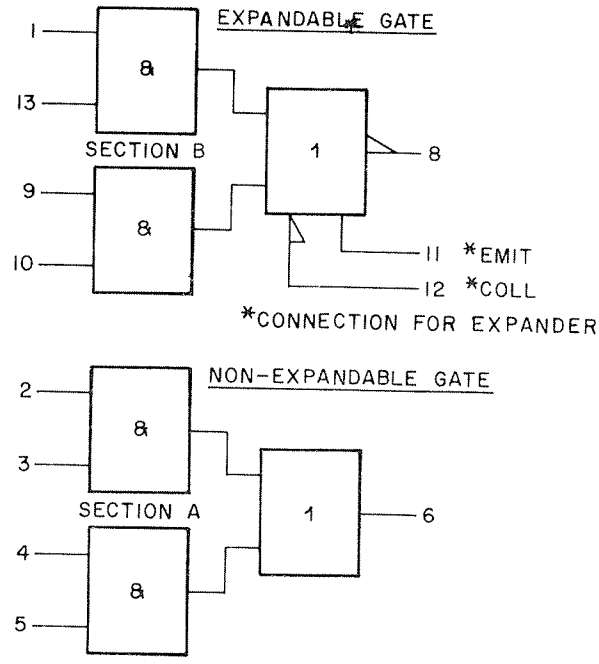


A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



PIN ASSIGNMENTS

145
Rev B
Sheet 1 of 1

Description

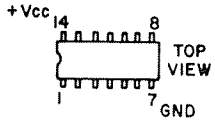
The 146 circuit is a six-section (hex) inverter.

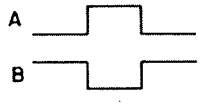
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

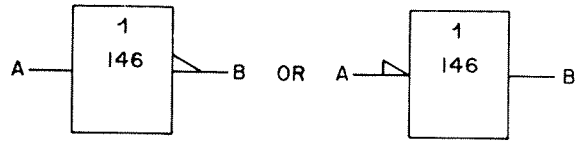
Element	Vendor Number
146	7404,9016
146H	74H04
146L	74L04
146LS	74LS04
146S	74S04

3. Package pin configuration.

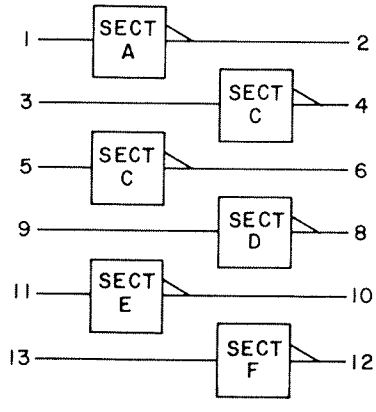




TIMING SEQUENCE



LOGIC SYMBOL



PIN ASSIGNMENTS

146
Rev B
Sheet 1 of 1

Description

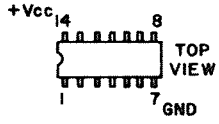
The 149 circuit is a quad 2-input Exclusive OR gate that performs the function $Y=A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the high level.

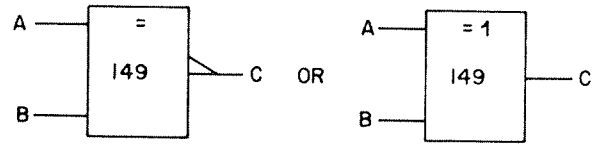
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

Element	Vendor Number
149	7486
149H	3021
149L	74L86
149LS	74LS86
149S	74S86

3. Package pin configuration.

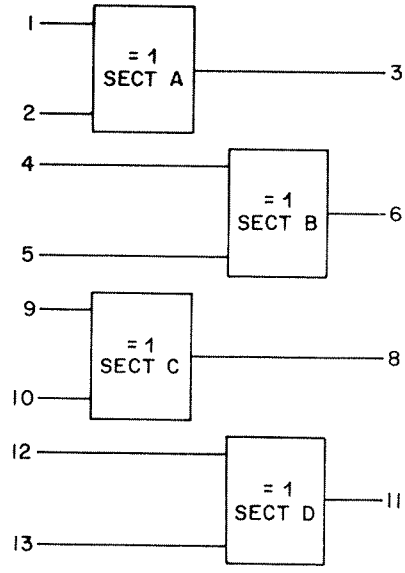




LOGIC SYMBOL

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

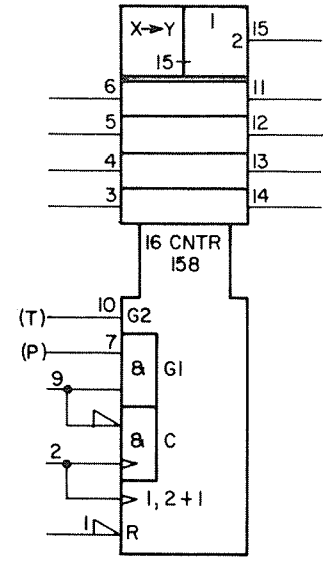
149
Rev B
Sheet 1 of 1

Description:

The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.

In order for the counter to count, the load (pin 9), clear (R), and P and T enable inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

When P is low, the clock input is disabled so that the counter can not count. When T is low, the clock input and carry output are both disabled.



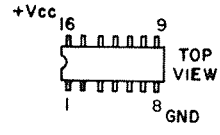
LOGIC SYMBOL

NOTES:

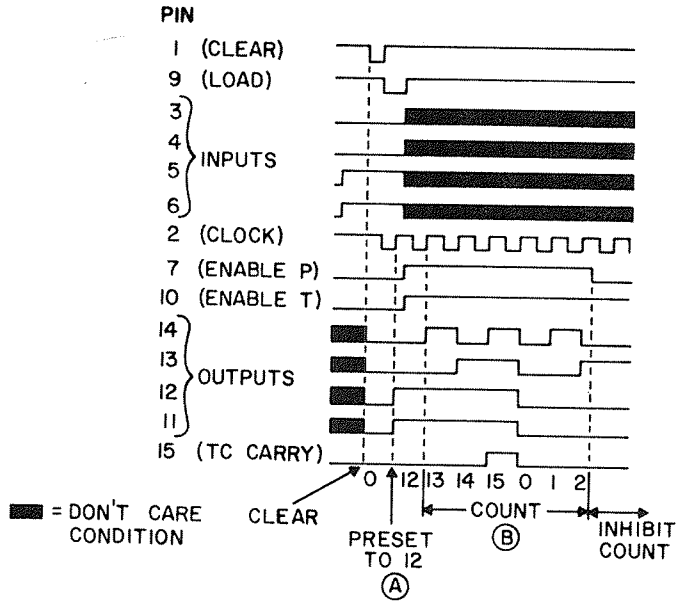
1. Vendor identification:

Element	Vendor Number
158	74161,9316
158A	74161
158LS	74LS161

2. Package pin configuration.



158
Rev B
Sheet 1 of 3



NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

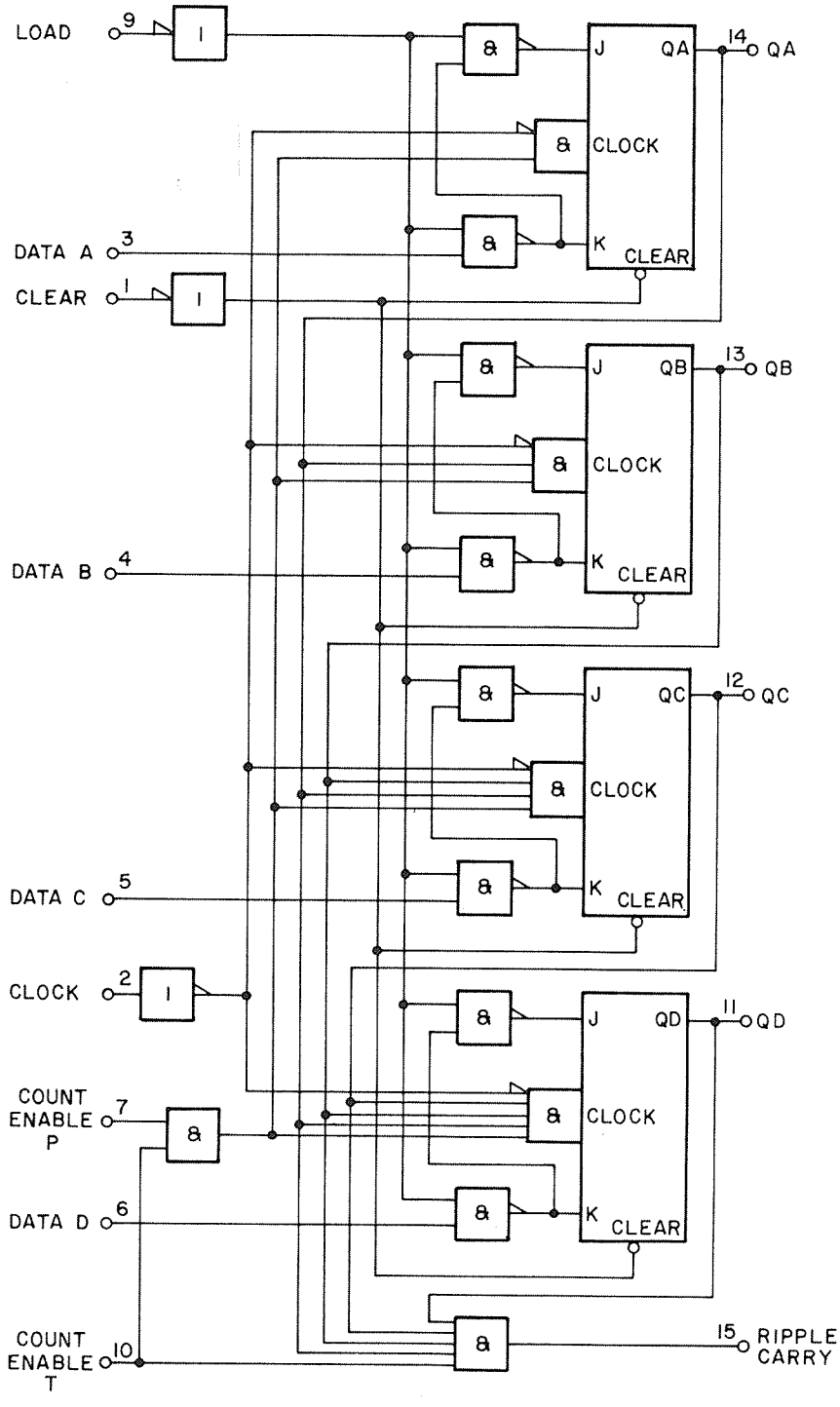
Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE

158
Rev B
Sheet 2 of 3



FUNCTION DIAGRAM

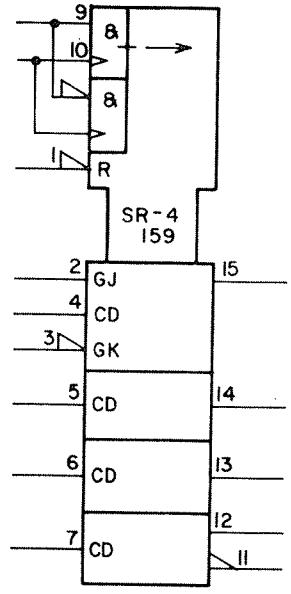
158
Rev B
Sheet 3 of 3

Description

The 159 circuit is a synchronous 4-bit shift register capable of shifting, counting, storage, and serial code conversion.

Data entry is synchronous; the outputs change state after each low to high transition of the clock. When the load/shift input is low, the parallel inputs determine the next condition of the shift register. When the load/shift input is high, the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through the J-K (serial) inputs. By tying the J and K inputs together, D-type entry is obtained.

A low level to the clear input will clear the outputs to a low level regardless of the levels to any input.



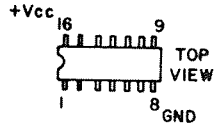
LOGIC SYMBOL

NOTES:

1. Vendor identification:

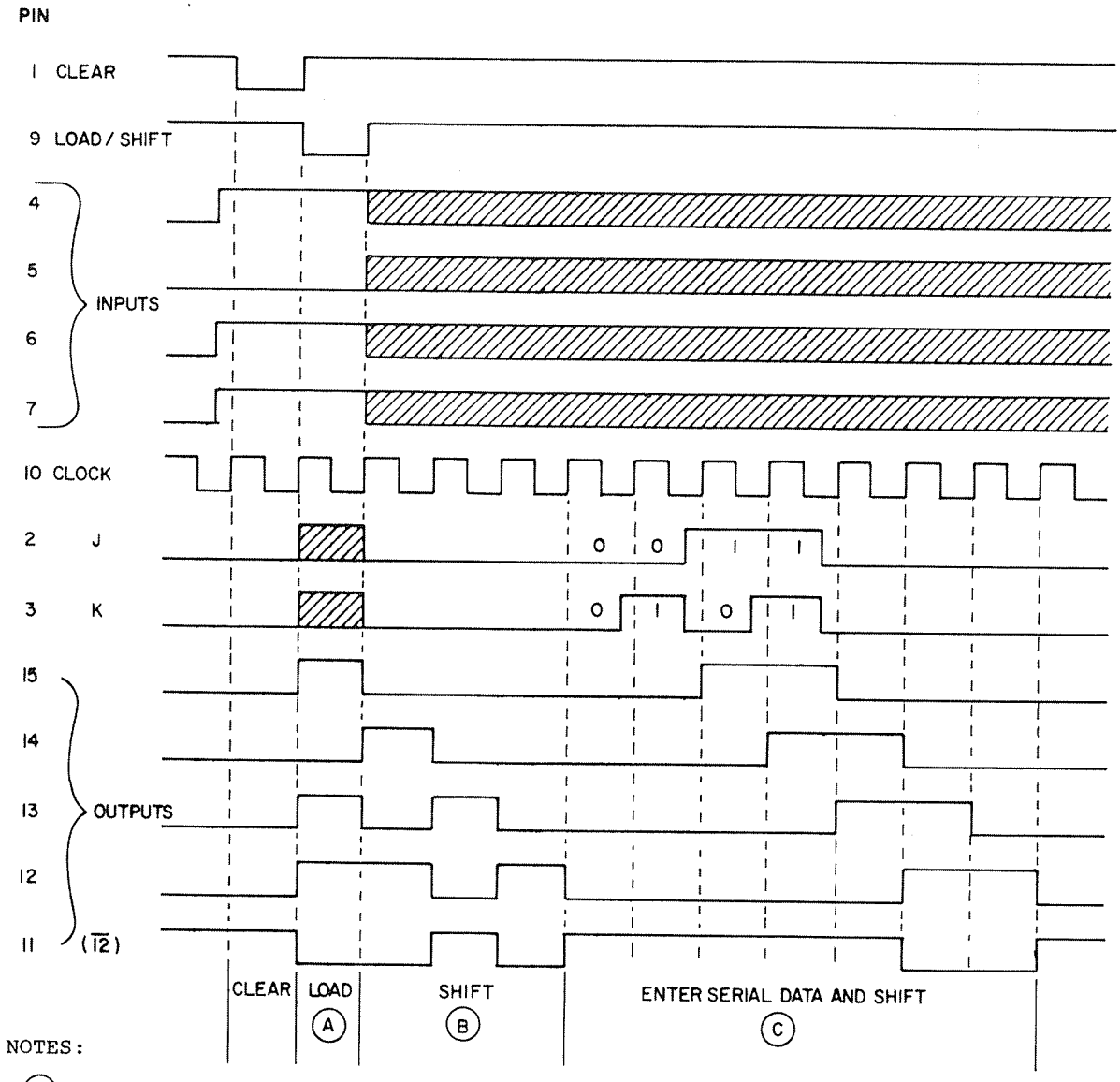
Element	Vendor Number
159	74195,9300
159LS	74LS195

2. Package pin configuration.



Pin	Function
1	Master Reset (clear)
2	First stage J input
3	First stage K input
4,5,6,7	Parallel data inputs
9	Load/Shift control
10	Clock
12,13,14,15	Parallel outputs
11	Complementary output ($\overline{12}$) for last stage

159
Rev B
Sheet 1 of 3



NOTES:

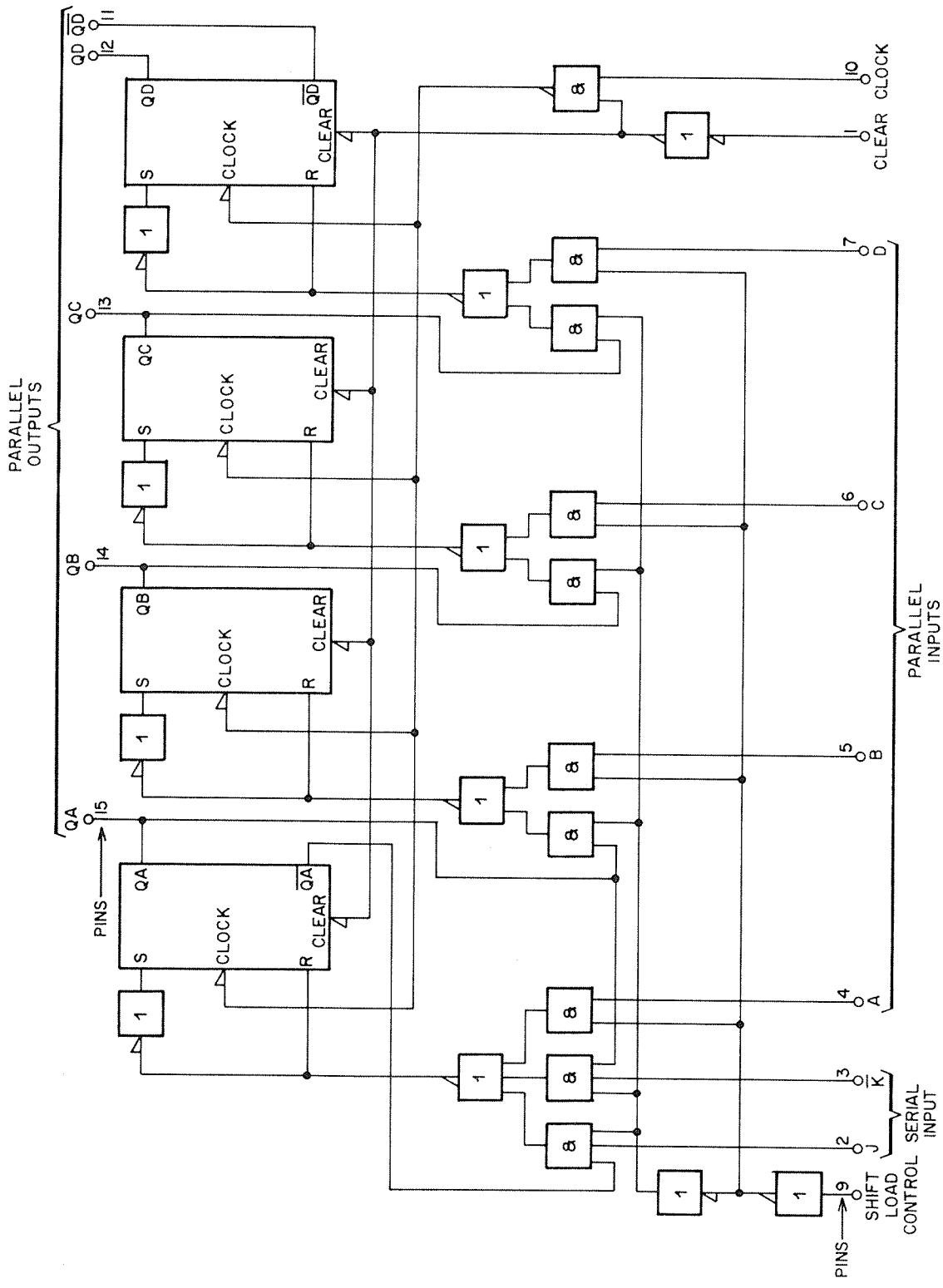
(A) Parallel data entered via CD inputs by pin 9 low and positive-going signal on pin 10.

(B) Data shifts down (Pin 15→Pin 14, etc.) with clock.

(C) Serial data entered into J-K inputs by pin 9 high and positive-going clock. Pin 4 input inhibited because pin 9 is high. Outputs follow Truth Table shown below. (Were J and K tied together, output at pin 15 would track the J input with no deviation from the Truth Table.)

INPUT PINS		OUTPUT PIN
2	3	15
0	0	0
0	1	0(NO CHANGE)
1	0	1(TOGGLES)
1	1	1

159
Rev B
Sheet 2 of 3



FUNCTION DIAGRAM

159
Rev B
Sheet 3 of 3

Description

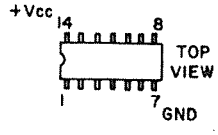
The 161 circuit is a monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 3 and 4 trigger on the positive going edge of the input pulse and pins 1 and 2 trigger on the negative going input pulse. The 161 circuit will retrigger while in the pulse timing state (pin 8 high); the end of the last pulse will be timed from the last input.

NOTES:

1. Vendor identification: 9601

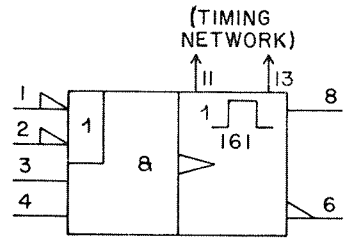
2. Package pin configuration.



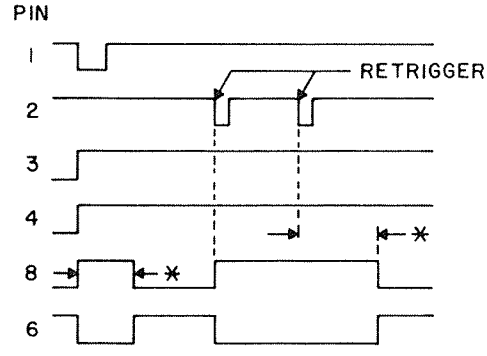
INPUT PINS				OPERATION	OUTPUT PINS	
1	2	3	4		8	6
H→L	H	H	H	TRIGGER	⎍	⎎
H	H→L	H	H	TRIGGER	⎍	⎎
L	X	L→H	H	TRIGGER	⎍	⎎
X	L	L→H	H	TRIGGER	⎍	⎎
L	X	H	L→H	TRIGGER	⎍	⎎
X	L	H	L→H	TRIGGER	⎍	⎎
H	H	H	H		L	H
X	X	L	X		L	H
X	X	X	L		L	H

X=DON'T CARE

TRUTH TABLE

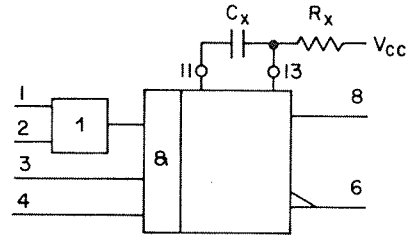


LOGIC SYMBOL



*PULSE WIDTH DETERMINED BY RC TIMING NETWORK

TIMING SEQUENCE



OUTPUT PULSE WIDTH (t) IS DEFINED AS FOLLOWS:

$$t = 0.32\ R_X\ C_X \left[1 + \frac{0.7}{R_X}\right]$$

R_X IS IN KΩ, C_X IS IN pf, t IS IN NS

FUNCTION DIAGRAM

161
Rev B
Sheet 1 of 1

Description

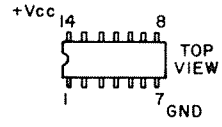
The 162 circuit is a dual differential line receiver. A minimum differential voltage of 25 mV is required to insure a high or low output level. Common mode voltages of ±3V or less will be rejected. The maximum allowable differential input voltage is 5 volts.

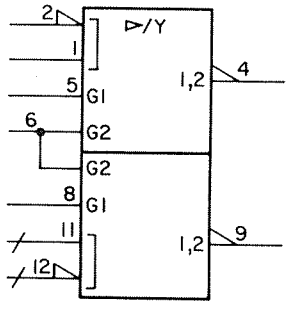
NOTES:

1. The two sections may be shown separately.
2. Vendor identification:

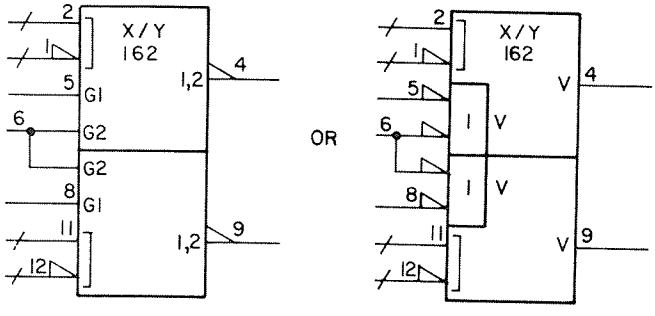
Element	Vendor Number
162	75107
162C	75108
162S	NE521F

3. Package pin configuration.

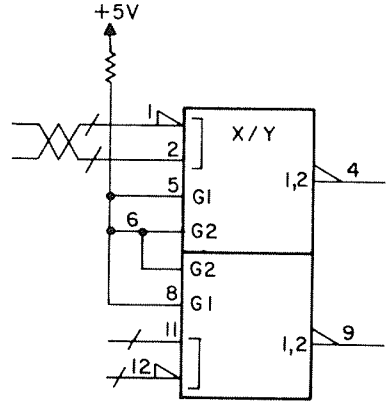




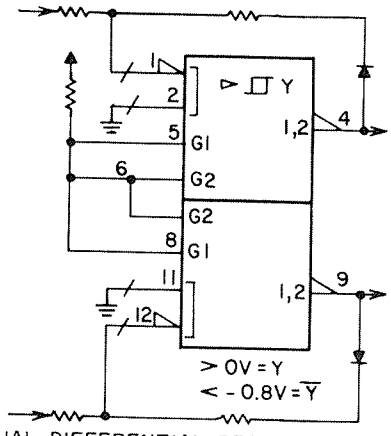
ANALOG TO DIGITAL CONVERTER APPLICATION



LOGIC SYMBOL

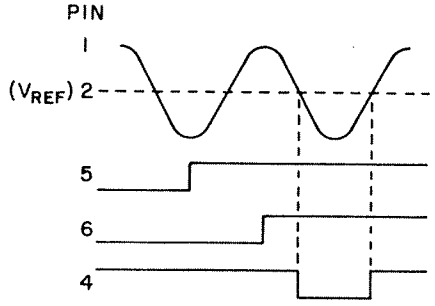


TWISTED PAIR RECEIVER APPLICATION



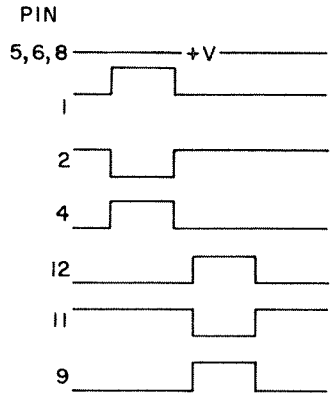
162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS.

LOGIC SYMBOL

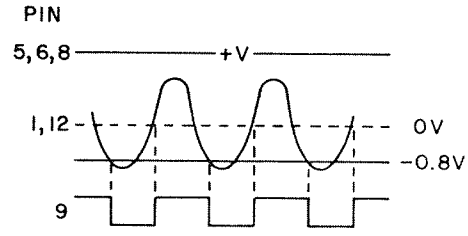


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH AND PIN 1 IS MORE NEGATIVE THAN PIN 2. G2 IS COMMON TO BOTH CONVERTERS.

162 DIGITAL TO ANALOG CONVERTER APPLICATION



162 TWISTED PAIR RECEIVER APPLICATION



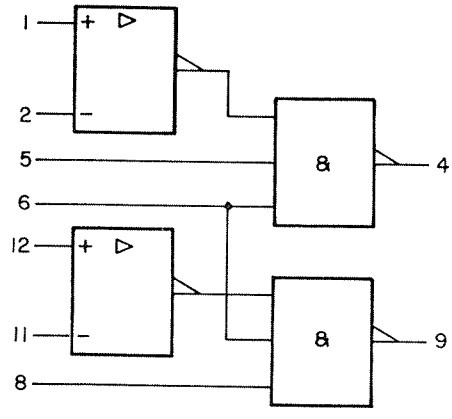
162 SCHMITT TRIGGER

TIMING SEQUENCE

DIFFERENTIAL INPUTS	STROBES		OUTPUT
	G1	G2	
$V_{ID} \geq 25MV$	L OR H	L OR H	H
$-25MV < V_{ID} < 25MV$	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25MV$	L OR H	L	H
	L	L OR H	H
	H	H	L

THE DIFFERENTIAL INPUT VOLTAGE POLARITES SHOWN MEASURED AT PIN A WITH RESPECT TO PIN B. A MINUS POLARITY INDICATES THAT PIN A IS MORE NEGATIVE THAN PIN B.

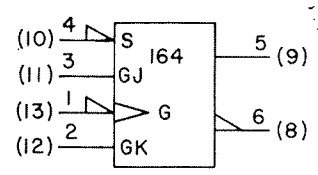
TRUTH TABLE
(RCVR APPLICATION)



FUNCTION DIAGRAM

Description

The 164 circuit is a dual negative-edge-triggered JK flip-flop. Each flip-flop is provided with a direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions.



LOGIC SYMBOL

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the set-up and hold-times. The inputs are inhibited when the clock is low and enabled when the clock rises. The JK inputs continuously respond to input information when the clock is high. The data state at the inputs throughout the interval between set-up and hold time is stored in the flip-flop when the clock pulse goes low. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input.

INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

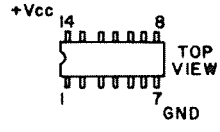
TRUTH TABLE

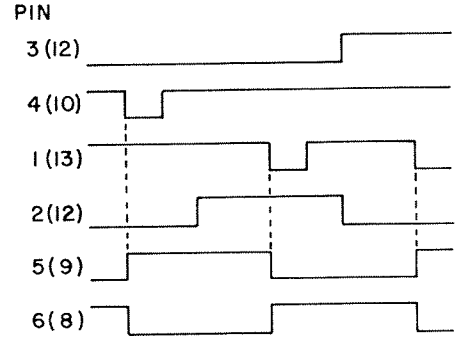
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

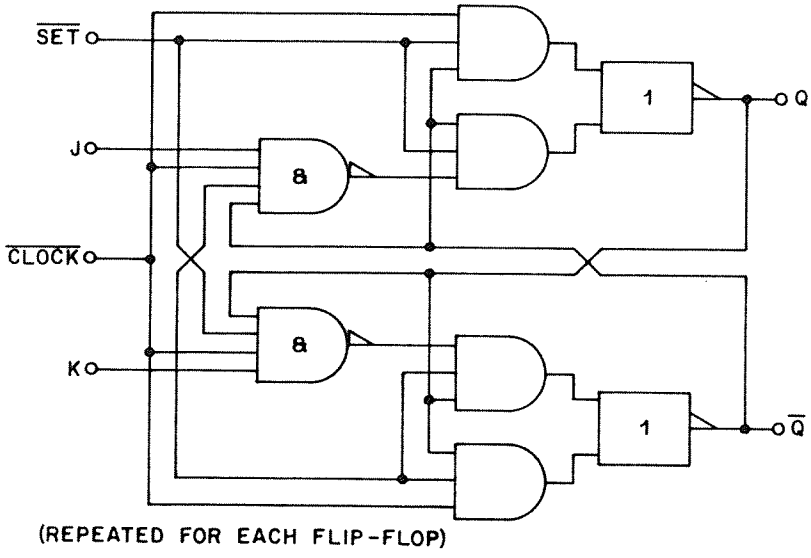
Element	Vendor Number
164H	3062
164S	74S113

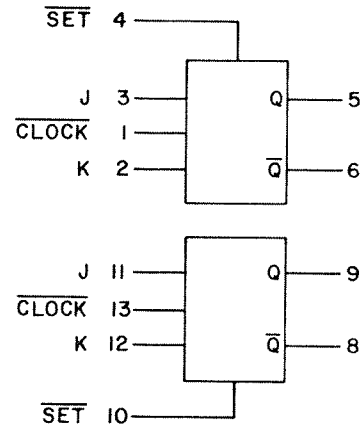
3. Package pin configuration.





TIMING SEQUENCE





FUNCTION DIAGRAM

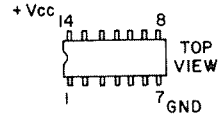
164
Rev B
Sheet 2 of 2

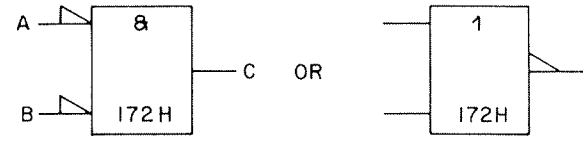
Description

The 172 circuit is a quad, 2-input positive NOR gate.

NOTES:

1. Symbol repeated for each gate.
2. Vendor identification: 3002
3. Package pin configuration.

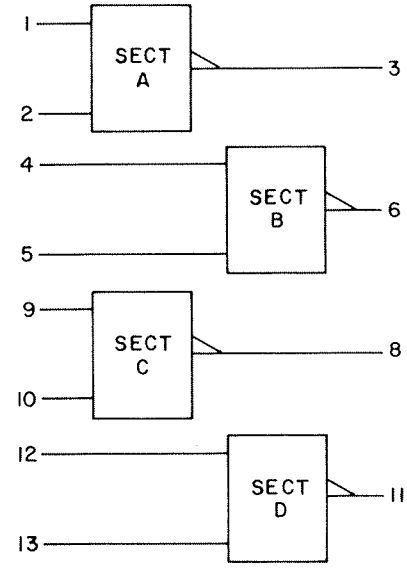




LOGIC SYMBOL

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

TRUTH TABLE



FUNCTION DIAGRAM

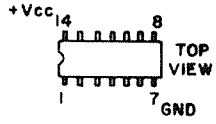
172
Rev B
Sheet 1 of 1

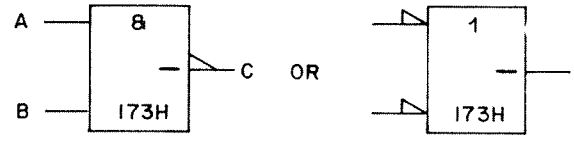
Description

The 173 circuit is a quad, 2-input,positive NAND gate with an open collector output.

NOTES:

1. Symbol repeated for each gate.
2. Vendor identification: 3004
3. The output of each gate is an open collector.
4. Package pin configuration.

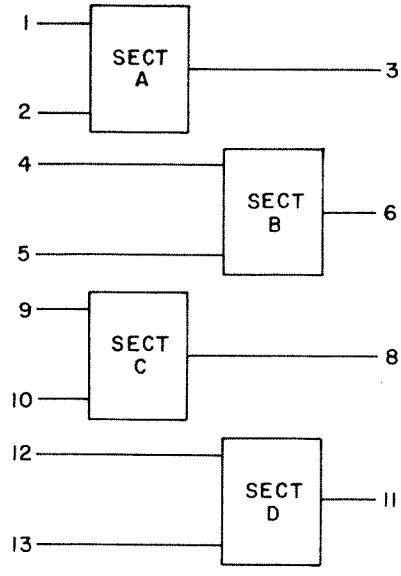




LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

173
Rev B
Sheet 1 of 1

Description

The 175 circuit is a dual, positive-edge-triggered, D-type flip-flop. This device consists of two completely independent D flip-flops, both having direct SET and RESET inputs for asychronous operations such as parallel data entry in shift register application.

Information at input CD is transferred to output Q (pin 5/9) on the positive-going edge of the clock pulse. Clock pulse triggering occurs at a voltage level of the pulse and is not directly related to the transition time of the positive-going pulse. When the clock is at either the high or low level, the CD-input signal has no effect.

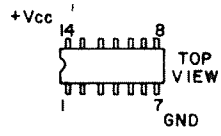
The flip-flop can also be set or cleared directly at any time regardless of the state of the clock by applying a low input to the SET or RESET inputs.

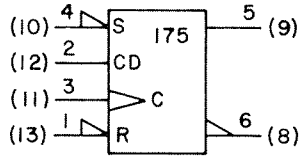
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

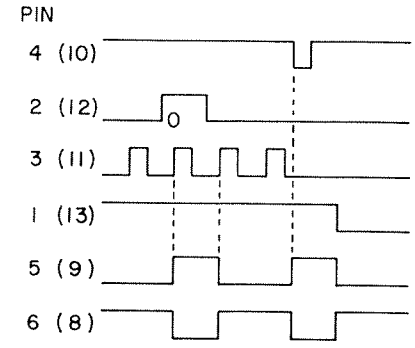
Element	Vendor Number
175	7474
175H	3060
175LS	74LS74
175S	74S74

3. Package pin configuration.

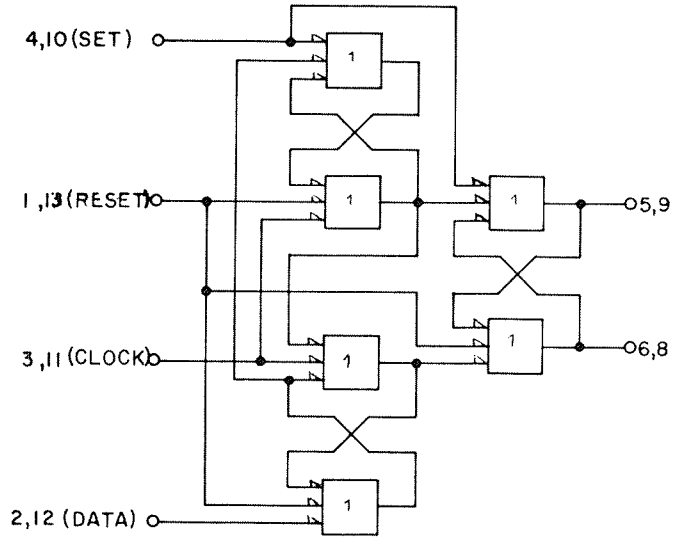




LOGIC SYMBOL



TIMING SEQUENCE

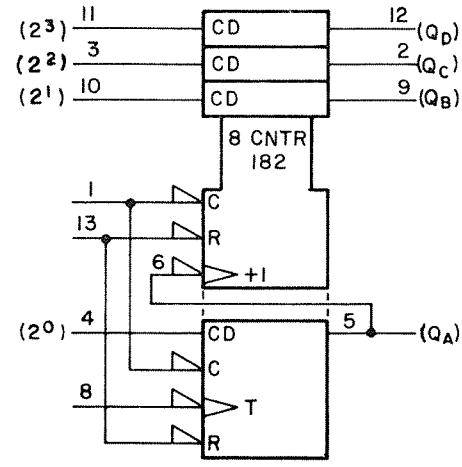


FUNCTION DIAGRAM
(EACH FLIP-FLOP)

175
Rev B
Sheet 1 of 1

Description

Circuit type 182 is a 4-bit binary counter. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The direct clear (pin 13), when taken low, sets all outputs low regardless of the states of the clocks (pins 8 and 6). The 182 is fully programmable; that is, the counter may be preset to any state by placing a low ("0") on the count/load input (pin 1) and entering the desired data at the inputs. The outputs will then change to agree with the data inputs independent of the state of the clock inputs. This allows the 182 to be used as a 4-bit latch (register application) by inactivating the clock inputs and using the count/load input as a data strobe.



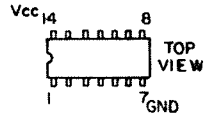
LOGIC SYMBOL

NOTES:

1. Vendor identification:

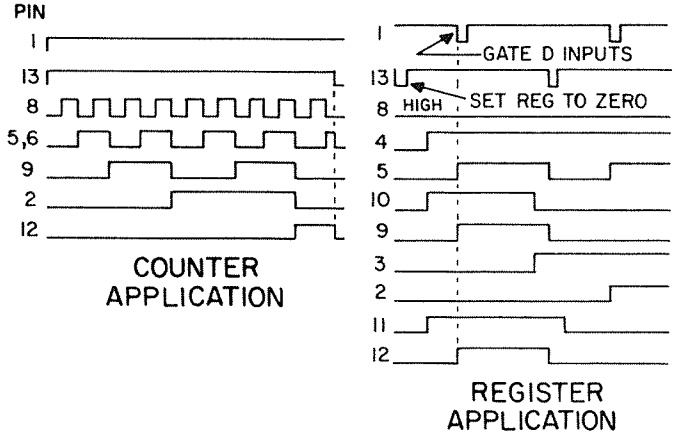
Element	Vendor Number
182	74197,8291
182S	82S91

2. Package pin configuration.



COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

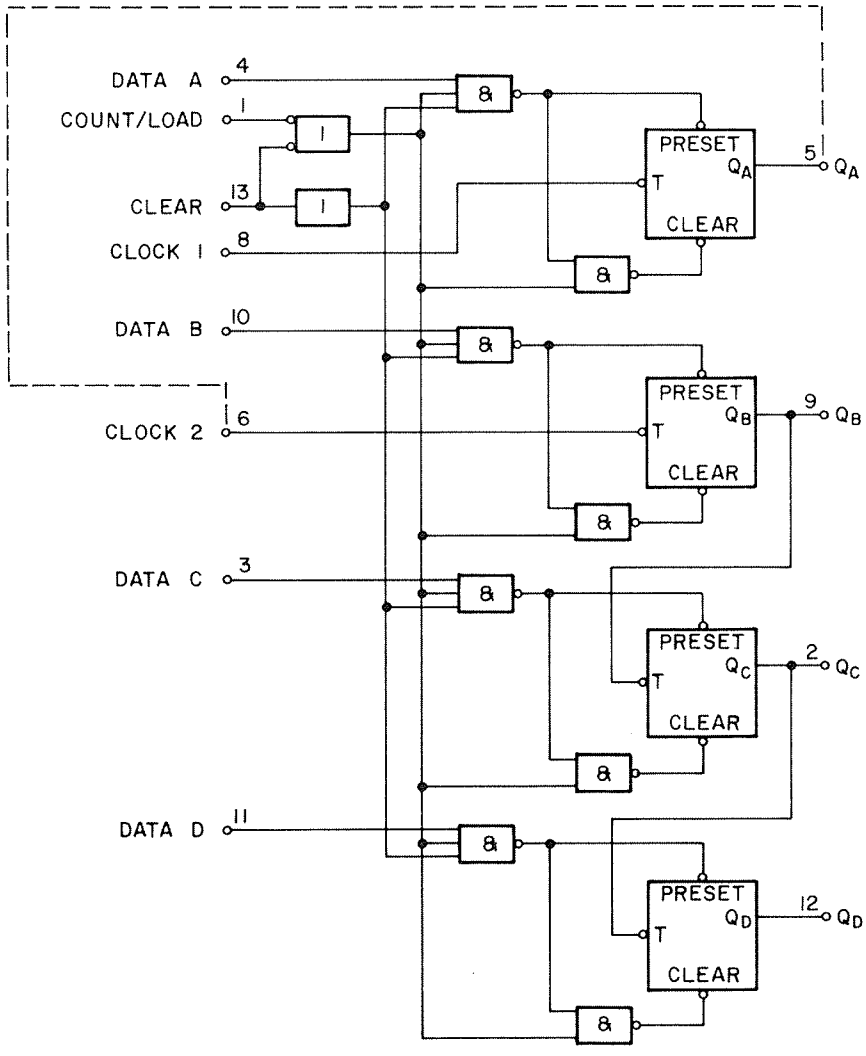
TRUTH TABLE
(WITH PINS 5 AND 6 WIRED TOGETHER)



TIMING SEQUENCE

182
Rev B
Sheet 1 of 2

CONNECT PINS 5 & 6 FOR 4-BIT COUNTING, USING DATA INPUT A. AS A 3-BIT COUNTER, DATA INPUT B IS USED. FIRST STAGE MAY THEN BE USED AS AN INDEPENDENT DATA LATCH IF COUNT/LOAD AND CLEAR FUNCTIONS COINCIDE WITH THOSE OF THE COUNTER.



FUNCTION DIAGRAM

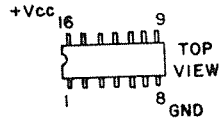
182
Rev B
Sheet 2 of 2

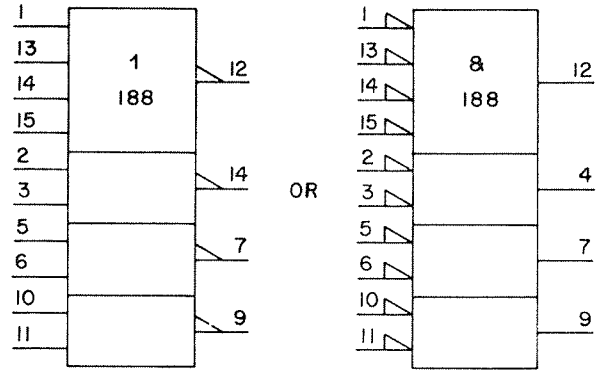
Description

The 188 circuit consists of one 4-input and three 3-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 9015
3. Package pin configuration.





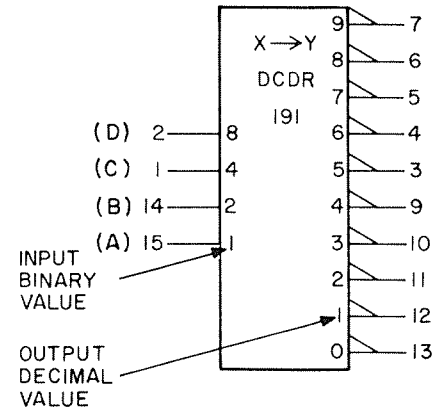
LOGIC SYMBOL

188
Rev B
Sheet 1 of 1

Description

Circuit type 191 is a BCD-to-decimal (1-of-10) decoder. Four active-high BCD inputs provide one of ten mutually exclusive active-low outputs. When a binary code greater than 9 is applied, all outputs are high. This facilitates BCD to decimal conversions and eight-channel demultiplexing and decoding.

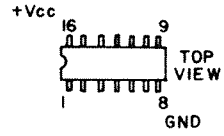
The 191 circuit can serve as a one-of-eight decoder with the D input acting as the active-low enable. Eight-channel demultiplexing then results when the desired output is addressed by inputs A, B, and C.



LOGIC SYMBOL

NOTES:

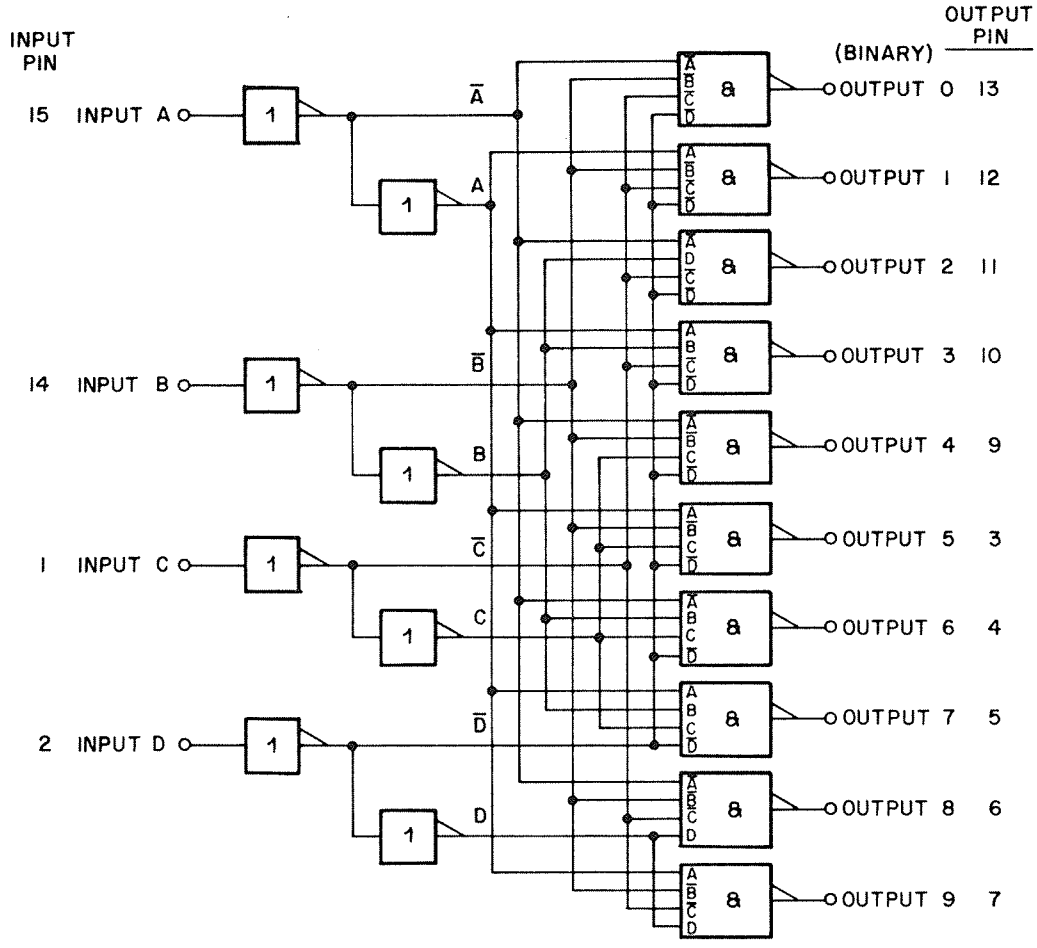
1. Vendor identification: 9301
2. Package pin configuration.



INPUT PIN				LO ("0") OUTPUT PIN (OTHER OUTPUTS = "1")
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	X

* = ALL OUTPUT PINS HIGH

TRUTH TABLE

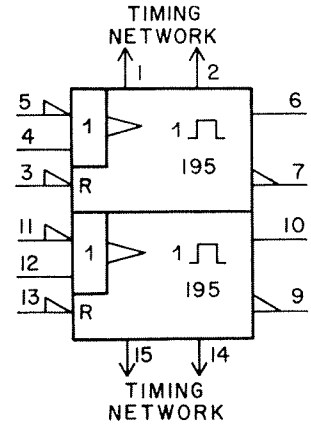


FUNCTION DIAGRAM

191
Rev B
Sheet 2 of 2

Description

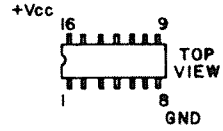
The 195 circuit is a dual retriggerable monostable multivibrator. Input pins 4 and 12 trigger on the positive-going edge of the input pulse and pins 5 and 11 trigger on the negative-going edge. The 195 circuit will retrigger while in the pulse timing state (pin 3/13 high) and the end of the last pulse will be timed from the last input. A low level to the reset input (pin 3/13) resets pin 6/10 to low level and inhibits data inputs.



LOGIC SYMBOL

NOTES:

1. The full timing network would be shown on the logic diagram.
2. Vendor identification: 9602
3. Package pin configuration.

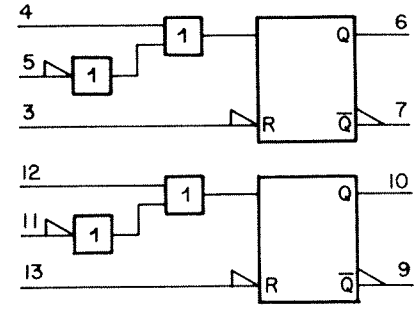


4. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low level pulse, X = irrelevant (any input, including transitions).

5. Output pulse width (t) is defined as follows:

$$t = 0.32\ R_X\ C_X \left[1 + \frac{0.7}{R_X}\right]$$

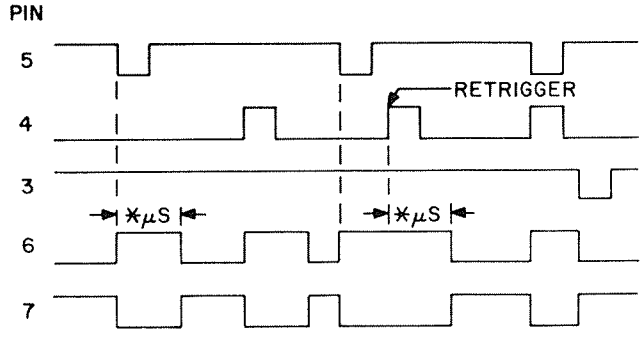
R_X is in KΩ, C_X is in pf, t is in ns



FUNCTION DIAGRAM

INPUT PINS			OUTPUT PINS	
5(11)	4(12)	3(13)	6(7)	10(9)
↓	L	H	⎍	⎎
H	↑	H	⎍	⎎
X	X	L	L	H

TRUTH TABLE
(SEE NOTE 4)



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.

TIMING SEQUENCE

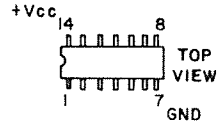
195
Rev B
Sheet 1 of 1

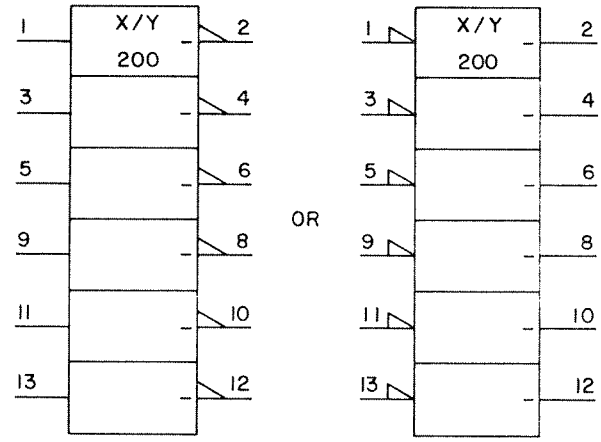
Description

The 200 circuit is a hex inverter buffer/ driver with an open-collector output.

NOTES:

1. Symbol sections may be shown separately.
2. Vendor identification: 7406
3. Package pin configuration.



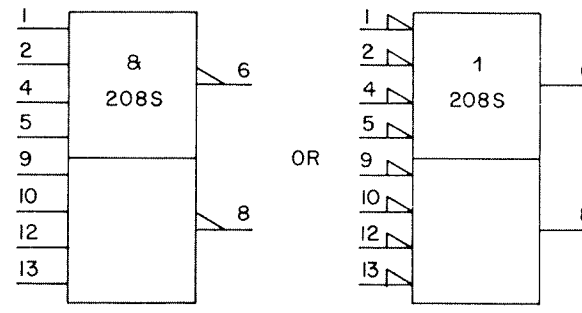


LOGIC SYMBOL

200
Rev B
Sheet 1 of 1

Description

Type 208 is a dual, 4-input, positive NAND gate.



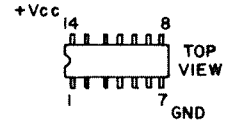
LOGIC SYMBOL

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
208	7420
208H	74H20
208L	74L20
208LS	74LS20
208S	74S20

3. Package pin configuration.



INPUTS				OUTPUT
A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE

208
Rev B
Sheet 1 of 1

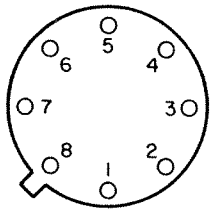
Description

Element 300 is a high gain operational amplifier mounted on a single chip.

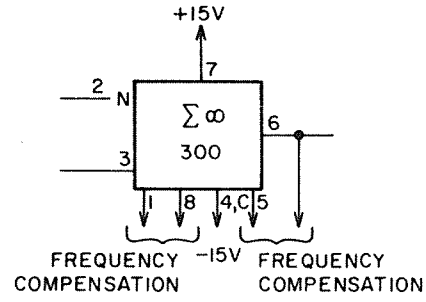
Pin	Function
1	Input Frequency Comp.
2	Inverting Input
3	Non-inverting Input
4	-V (Connected to Case)
5	Output Frequency Comp.
6	Output
7	+V
8	Input Frequency Comp.

NOTE:

1. Vendor Identification: 709C



PACKAGE PIN CONFIGURATION



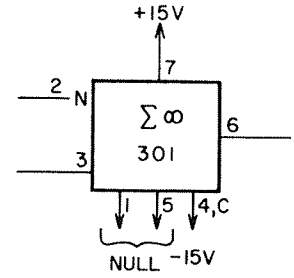
LOGIC SYMBOL

300
Rev. B
Sheet 1 of 1

Description

Element 301 is a frequency compensated, high gain, operational amplifier.

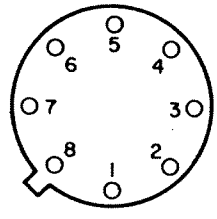
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 741C



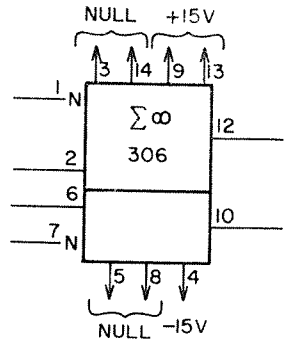
PACKAGE PIN CONFIGURATION

301
Rev. B
Sheet 1 of 1

Description

Element 306 is a pair of frequency compensated, high gain, operational amplifier.

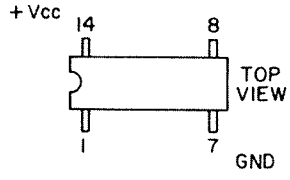
Pin	Function
1	Inverting Input A
2	Non-inverting Input A
3	Offset Null A
4	-V
5	Offset Null B
6	Non-inverting Input B
7	Inverting Input B
8	Offset Null B
9	+V (B)
10	Output B
11	No Connections
12	Output A
13	+V (A)
14	Offset Null A



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 747C



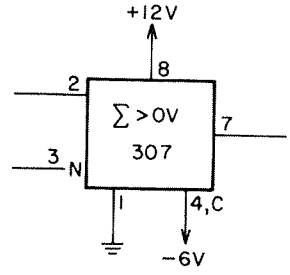
PACKAGE PIN CONFIGURATION

306
Rev. B
Sheet 1 of 1

Description

Element 307 is a differential voltage comparator.

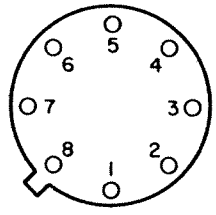
Pin	Function
1	GND
2	Non-inverting Input
3	Inverting Input
4	-V
5	No Connection
6	No Connection
7	Output
8	+V



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 710



PACKAGE PIN CONFIGURATION

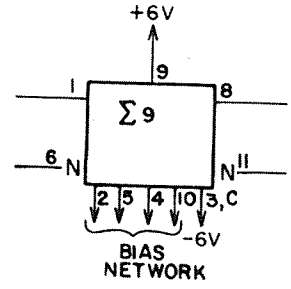
307
Rev. B
Sheet 1 of 1

Description

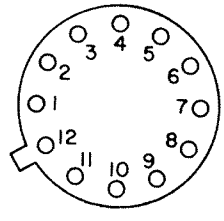
Element 309 is a wide band differential amplifier with a nominal voltage gain of 9.

NOTES:

1. Vendor identification: 3001



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

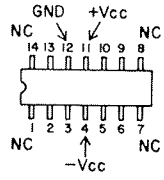
309
Rev B
Sheet 1 of 1

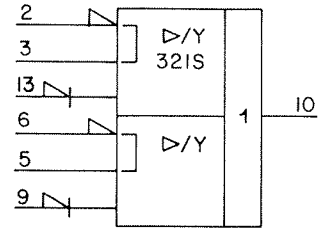
Description

The 321 is a dual differential comparator. Output (pin 10) is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high. A low level to pin 9 or 13 will inhibit operation of that section which it controls.

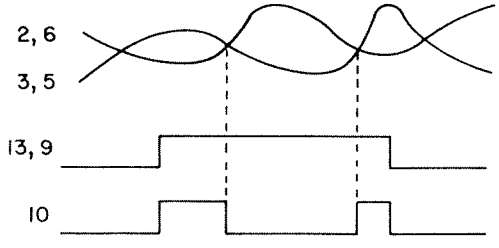
NOTES:

1. Vendor identification: TSC 5711
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION SEQUENCE

321
Rev B
Sheet 1 of 1

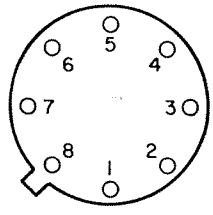
Description

Element 322 is a frequency compensated, high speed, operational amplifier.

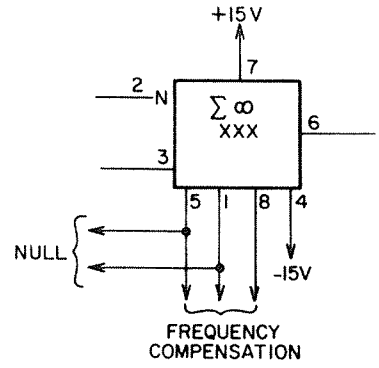
Pin	Function
1	Offset Null/Compensation 1
2	Inverting Input
3 3	Non-inverting Input
4	-V
5	Offset Null/Compensation 3
6	Output
7	+V
8	Compensation 2

NOTE:

1. Vendor Identification: LM318



PACKAGE PIN CONFIGURATION



LOGIC SYMBOL

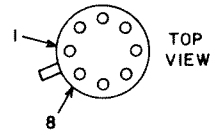
322
Rev. A
Sheet 1 of 1

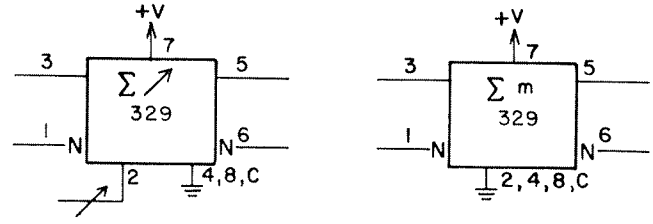
Description

The 329 circuit is a wide-band RF/IF/Audio amplifier with external AGC control.

NOTES:

1. Vendor identification: 1590
2. Package pin configuration. (TO-99 metal case)





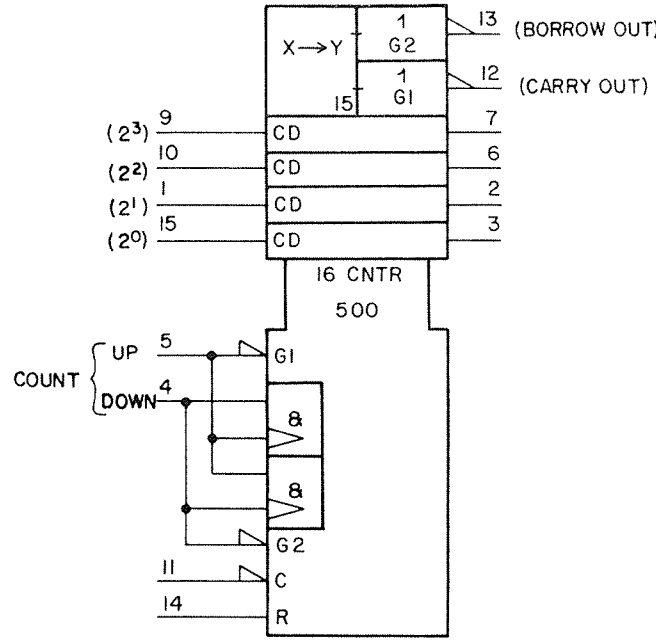
LOGIC SYMBOL

329
Rev B
Sheet 1 of 1

Description

The 500 circuit is a synchronous 4-bit up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable; that is, the counter may be preset to any state by entering the desired data at the data inputs while the load input (pin 11) is low. The output will then change to agree with the data inputs independently of the count pulses. A high level applied to the clear input forces all outputs to the low level. The clear function is independent of the count and load inputs.



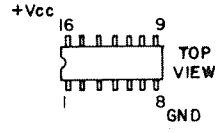
LOGIC SYMBOL

NOTES:

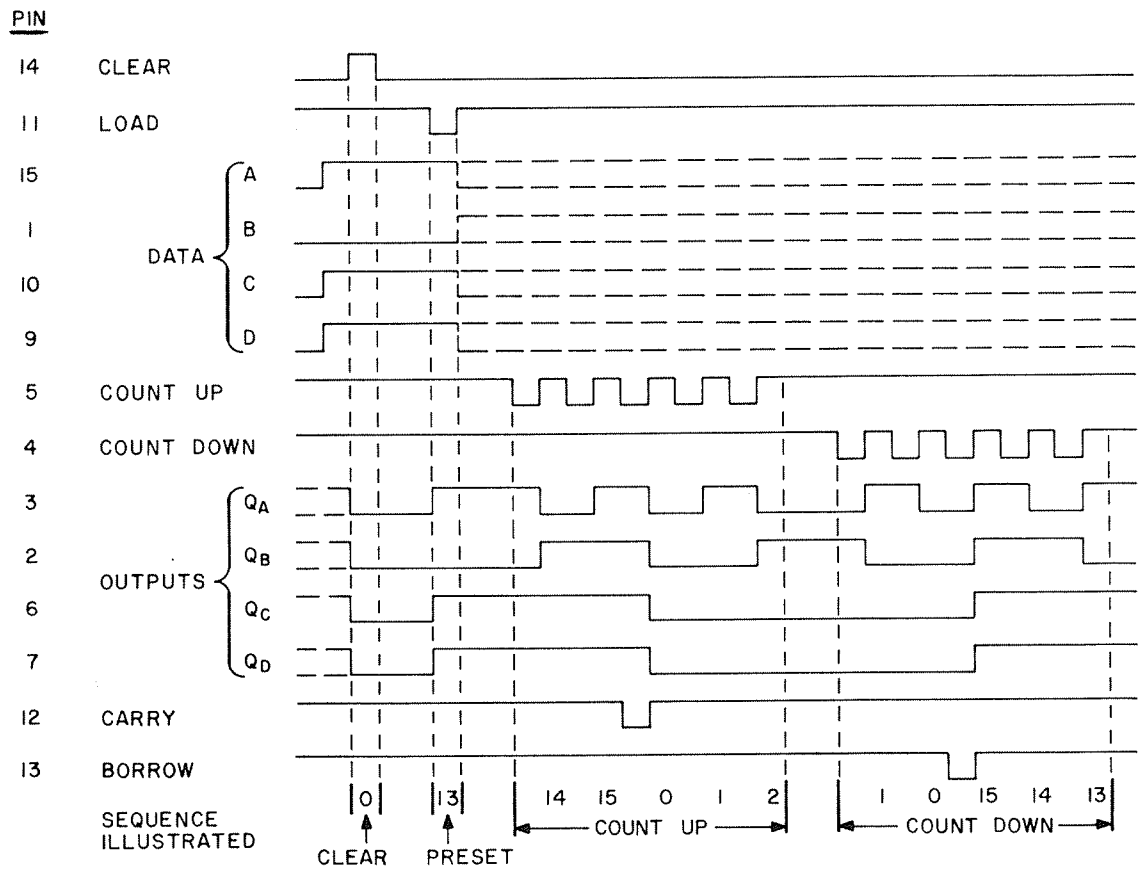
1. Input/Output identifiers are not part of the symbol.
2. Vendor identification:

Element	Vendor Number
500	74193,9366
500LS	74LS193

3. Package pin configuration.



500
Rev B
Sheet 1 of 3



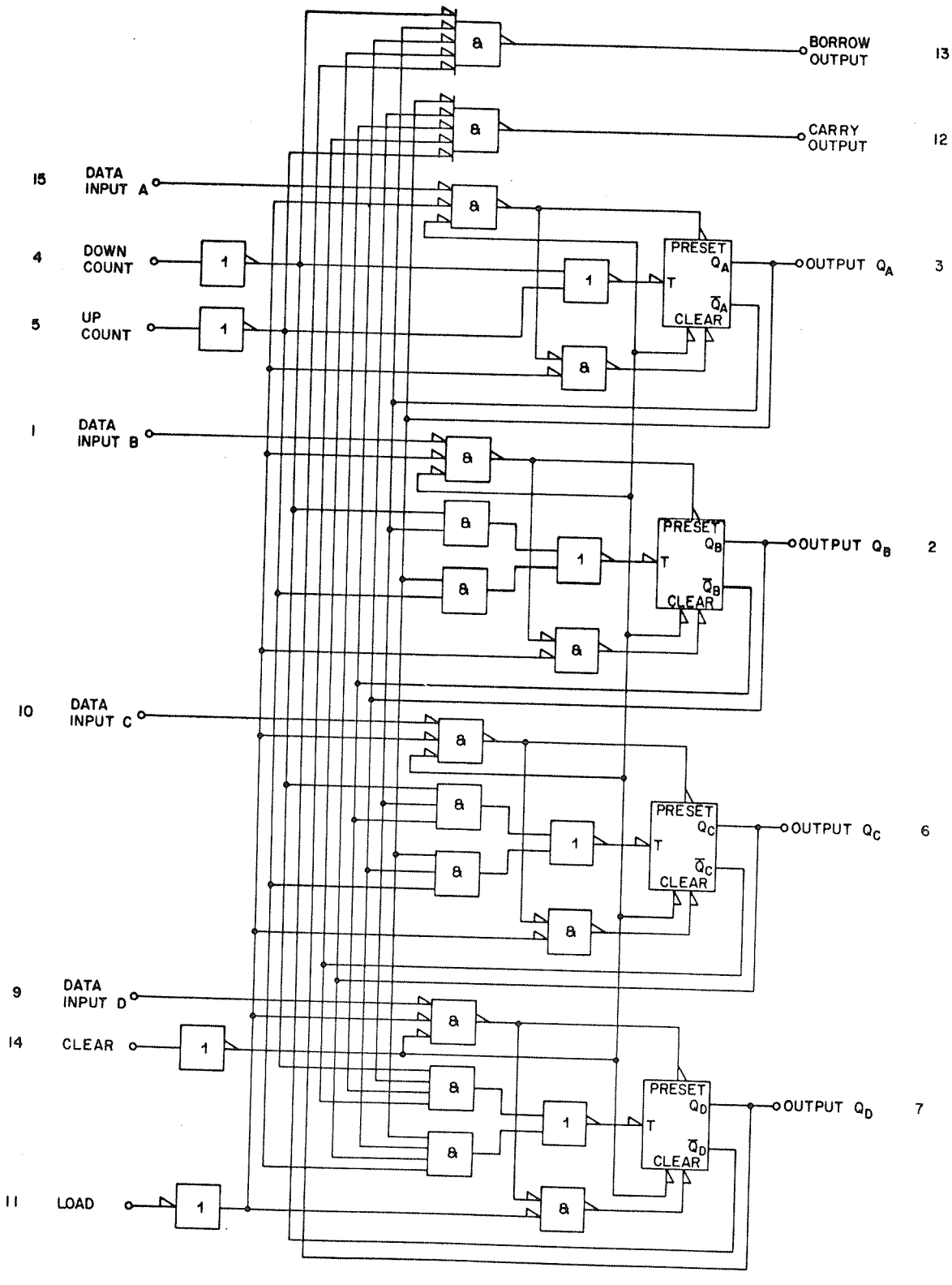
NOTE:

① ILLUSTRATED ABOVE IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUTS TO ZERO.
2. LOAD (PRESET) TO BCD THIRTEEN.
3. COUNT UP TO FOURTEEN, FIFTEEN, CARRY, ZERO, ONE AND TWO.
4. COUNT DOWN TO ONE, ZERO, BORROW, FIFTEEN, FOURTEEN AND THIRTEEN.

COUNTING SEQUENCE

500
Rev B
Sheet 2 of 3



FUNCTION DIAGRAM

500
Rev B
Sheet 3 of 3

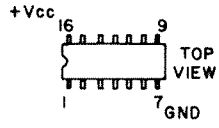
Description

The 501 circuit is a 5-bit comparator that provides comparison between two 5-bit words and gives three outputs: "less than", "greater than", and "equal to". A high level on the active low enable (pin 1) forces all three outputs low.

NOTES:

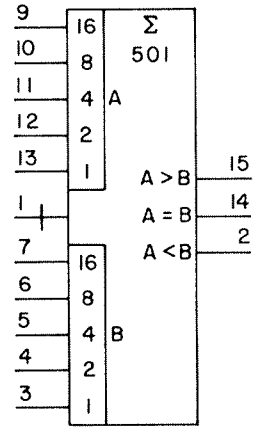
1. Vendor identification: 9324

2. Package pin configuration.



3. Pin names:

Pin	Function
1	Enable (active low) input
9,10,11,12,13	Word A parallel inputs
3,4,5,6,7	Word B parallel inputs
2	A Less Than B (A < B) output
14	A Equal to B (A=B) output
15	A Greater Than B (A > B) output



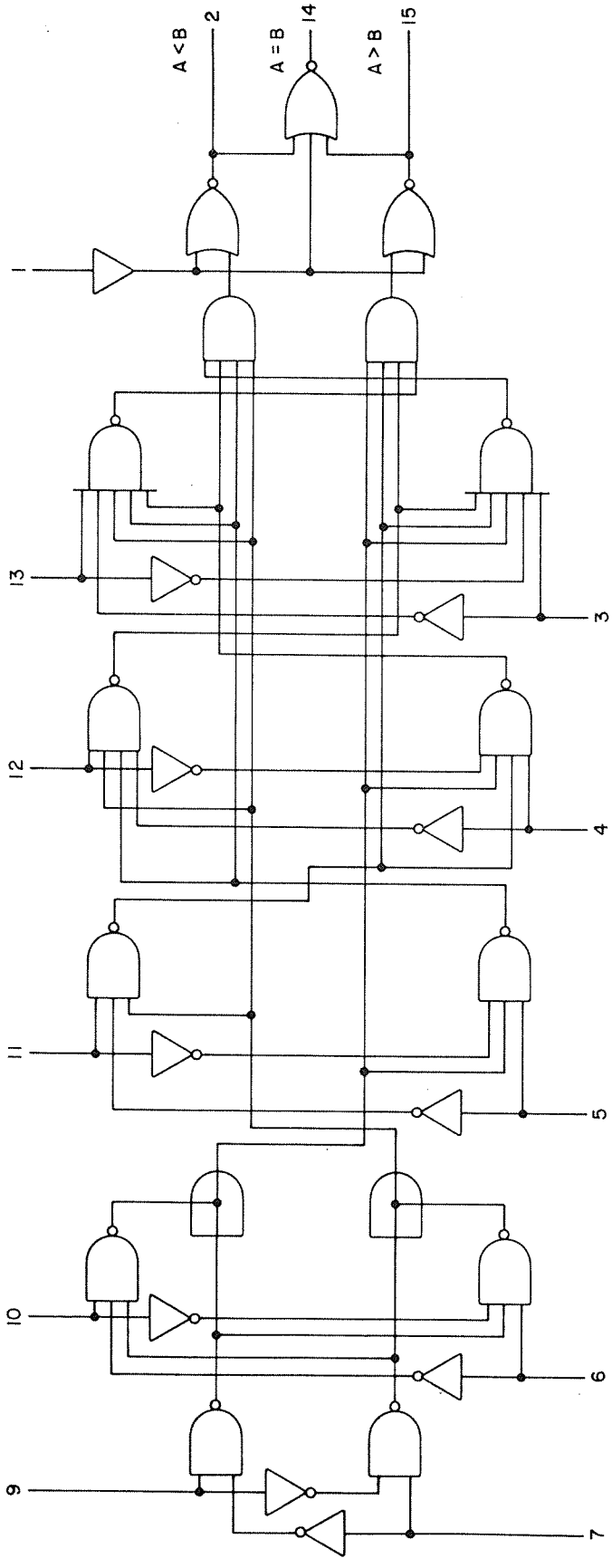
LOGIC SYMBOL

	INPUT		OUTPUT		
I	A	B	A<B	A>B	A=B
H	X		L	L	L
L	WORD A = WORD B		L	L	H
L	WORD A > WORD B		L	H	L
L	WORD A < WORD B		H	L	L

H = HIGH LEVEL
L = LOW LEVEL
X = EITHER HIGH OR LOW LEVEL

TRUTH TABLE

501
Rev B
Sheet 1 of 2

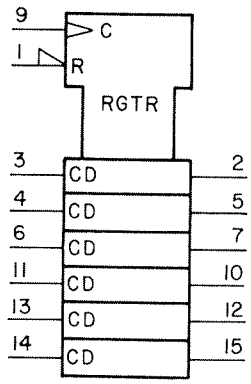


FUNCTION DIAGRAM

501
Rev B
Sheet 2 of 2

Description

The 519 circuit is a register made up of six D-type flip-flops with common clock and clear inputs.



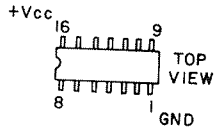
LOGIC SYMBOL

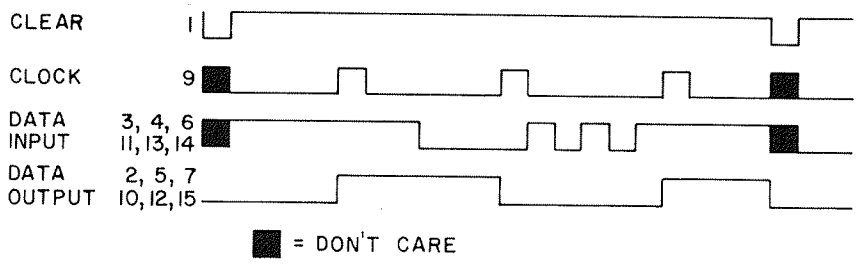
NOTES:

1. Vendor identification:

Element	Vendor Number
519	74174
519S	74S174

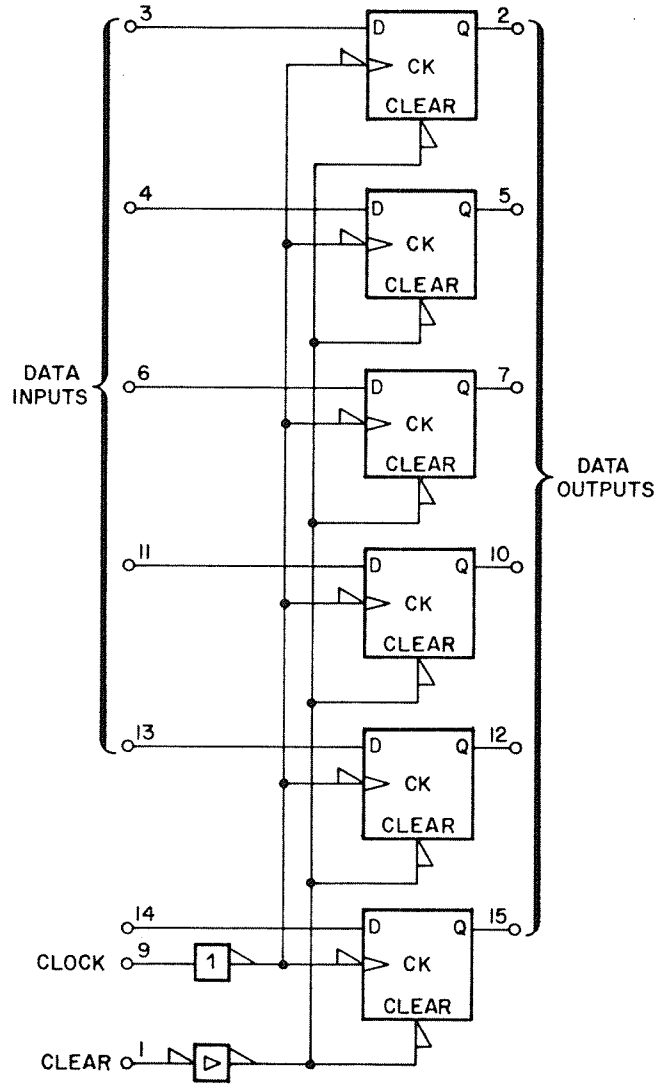
2. Package pin configuration.





FUNCTION SEQUENCE

519
Rev B
Sheet 1 of 2

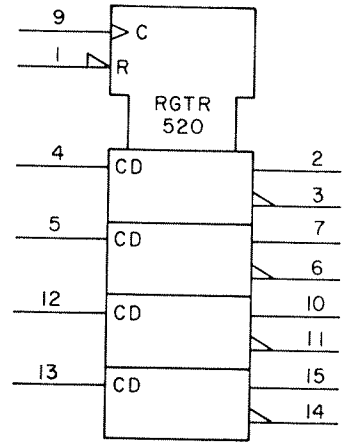


FUNCTION DIAGRAM

519
Rev B
Sheet 2 of 2

Description

Element 520 contains four TTL, positive-edge-triggered, D-type flip-flops. Each has a direct clear input and a complementary output. Information at the D inputs is transferred to the Q outputs on the positive edge of the clock pulse. When the clock is at either the high or low level, the D input signal has no effect on the outputs.



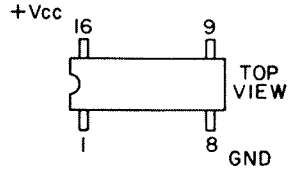
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
520	74175
520LS	74LS175
520S	74S175

2. Package pin configuration:



INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	NC	NC

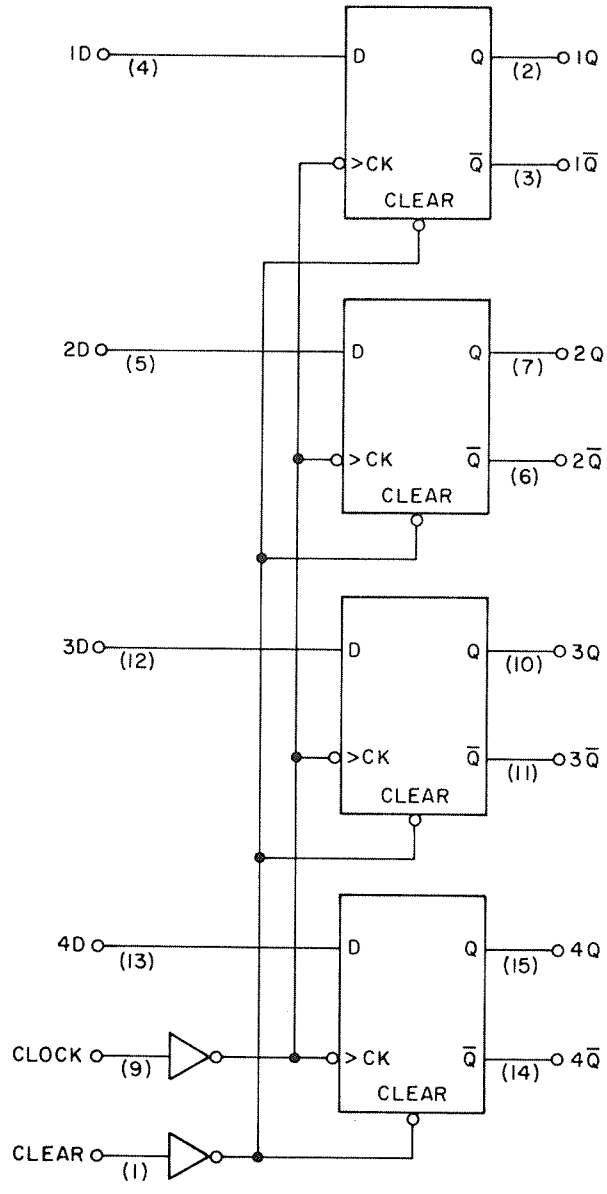
↑ = TRANSITION FROM LOW TO HIGH LEVEL

X = DON'T CARE

NC = SAME AS BEFORE INDICATED INPUT CONDITIONS WERE ESTABLISHED

TRUTH TABLE

520
Rev B
Sheet 1 of 2



FUNCTIONAL DIAGRAM

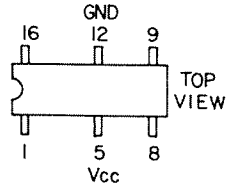
520
Rev B
Sheet 2 of 2

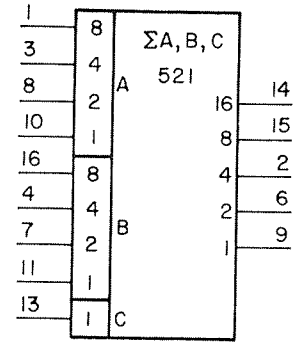
Description

The 521 circuit performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

NOTES:

1. Vendor identification: 7483
2. Package pin configuration.



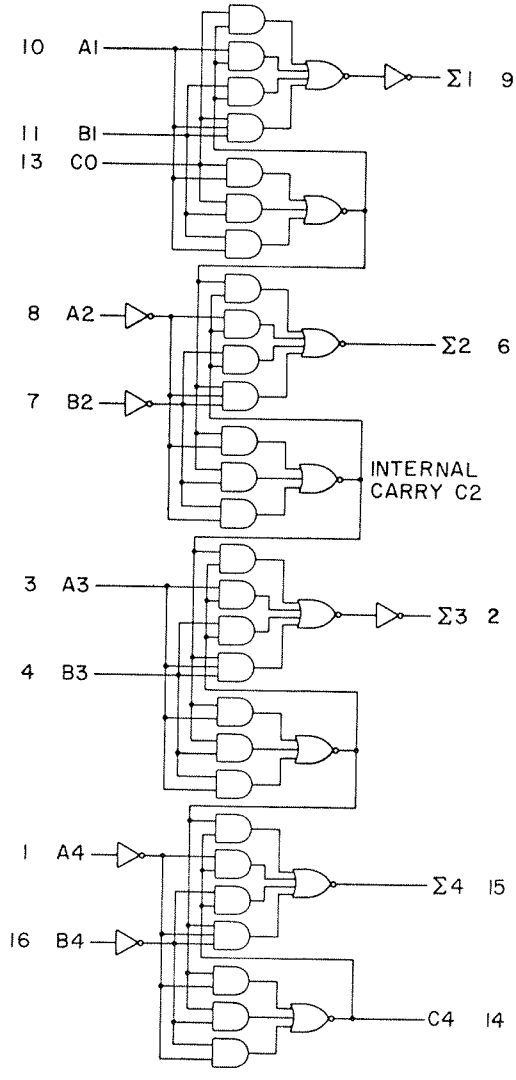


LOGIC SYMBOL

INPUT				OUTPUT					
				WHEN CO=L			WHEN CO=H		
						WHEN C2=L			WHEN C2=H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: INPUT CONDITIONS AT A1, A2, B2, AND CO ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4, ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.

TRUTH TABLE

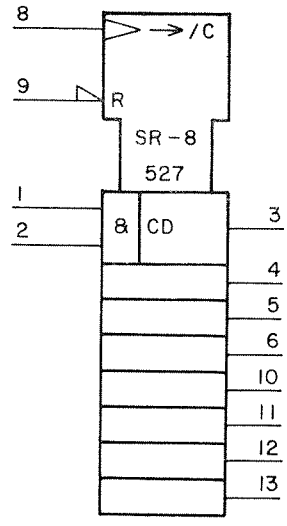


FUNCTION DIAGRAM

521
Rev B
Sheet 1 of 1

Description

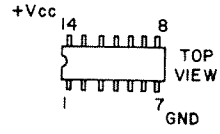
The 527 circuit is a 8-bit shift register with gated serial inputs and an asychronous clear. The gated serial inputs (pins 1 and 2) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requrements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

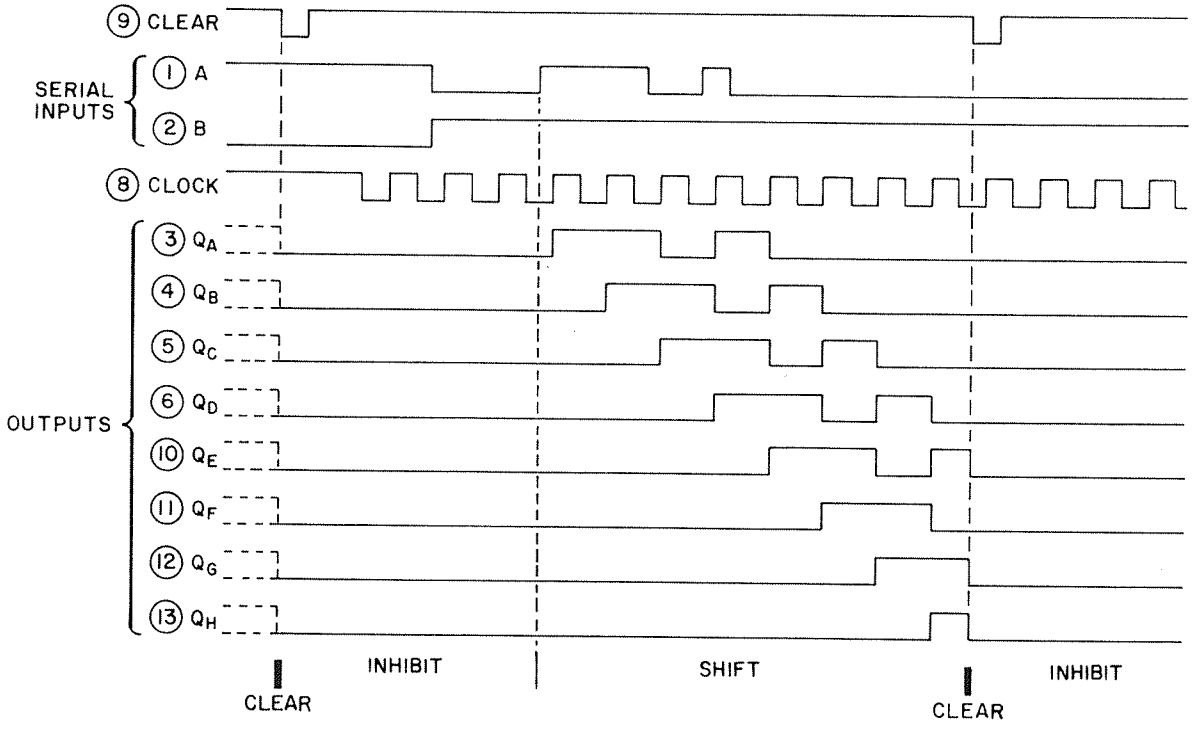


LOGIC SYMBOL

NOTES:

1. Vendor identification: 74164,8570
2. Package pin configuration.

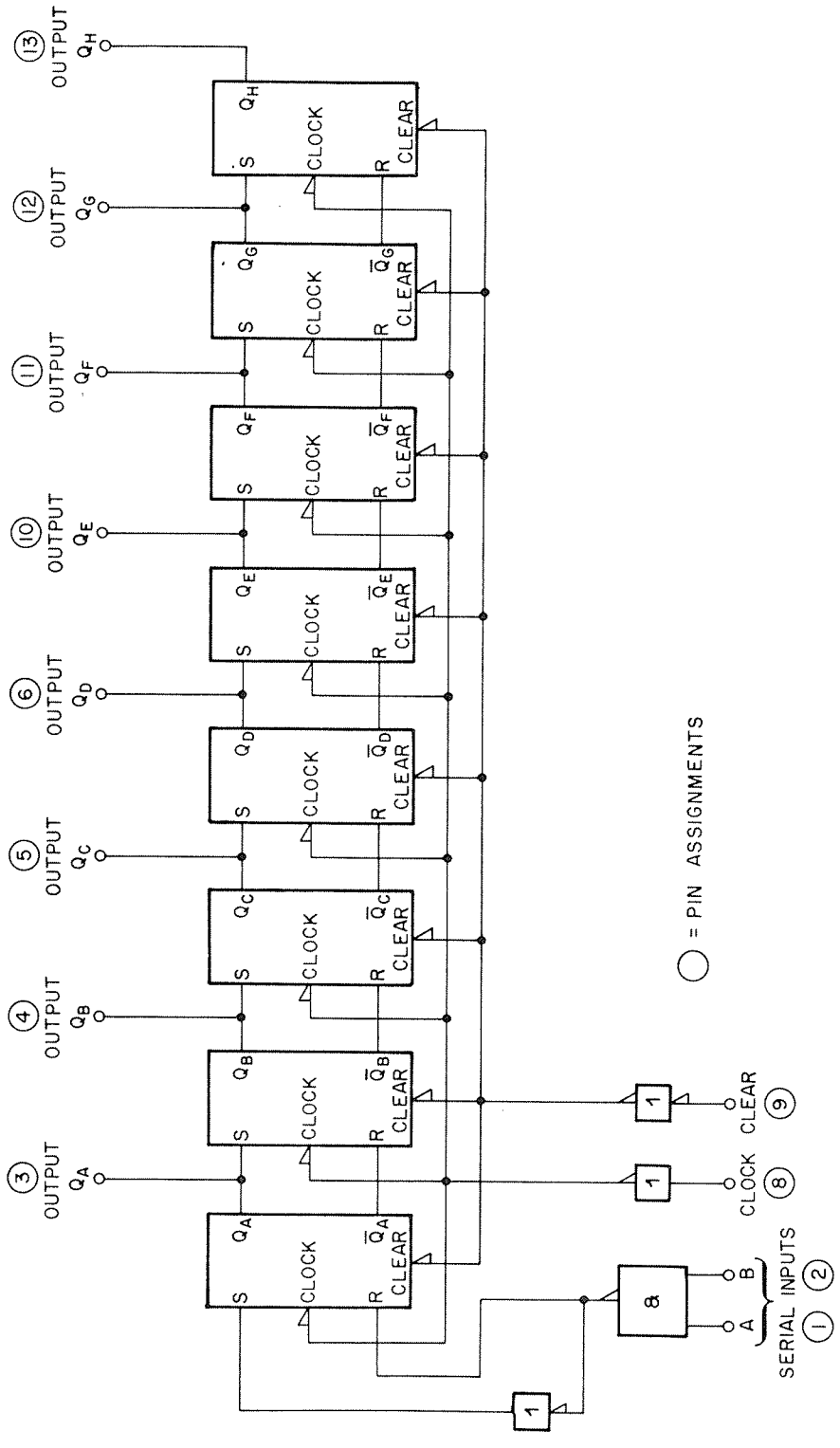




NOTES: 1. TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES.
2. ◯ = PIN ASSIGNMENTS.

FUNCTION SEQUENCE

527
Rev B
Sheet 1 of 2



527
Rev B
Sheet 2 of 2

DESCRIPTION

The 581 circuit is a phase-frequency detector. This device contains two digital phase detectors, an emitter follower amplifier, and a charge pump circuit that converts TTL inputs to a dc voltage for use in frequency discrimination and phase-locked-loop applications.

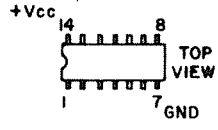
The two phase detectors have common inputs. Phase-frequency detector A is locked in (indicated by both outputs high) when the negative transitions of the variable input (pin 3) and the reference input (pin 1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, output pin 13 goes low; conversely, output pin 2 goes low when the variable input is higher in frequency or leads the reference input in phase. The variable and reference inputs to phase detector A are not affected by duty cycles because negative transitions control operations.

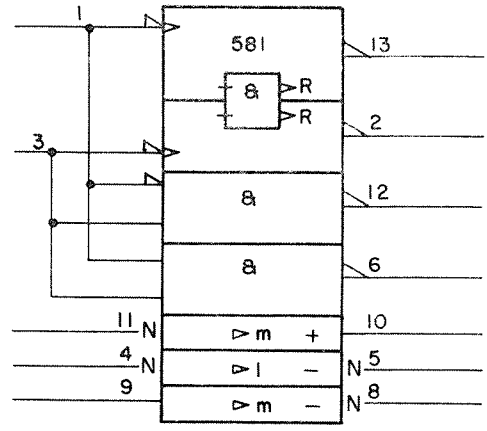
Phase detector B is locked in when the variable input phase lags the reference phase by 90° (indicated by output pins 6 and 12 alternately going low with equal pulse widths). If the variable input lags by more than 90°, pin 12 will remain low longer than pin 6. Conversely, if the variable input phase lags the reference phase by less than 90°, pin 6 remains low longer. In phase detector B, the variable input and the reference input must have 50% duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed-amplitude positive and negative pulses.

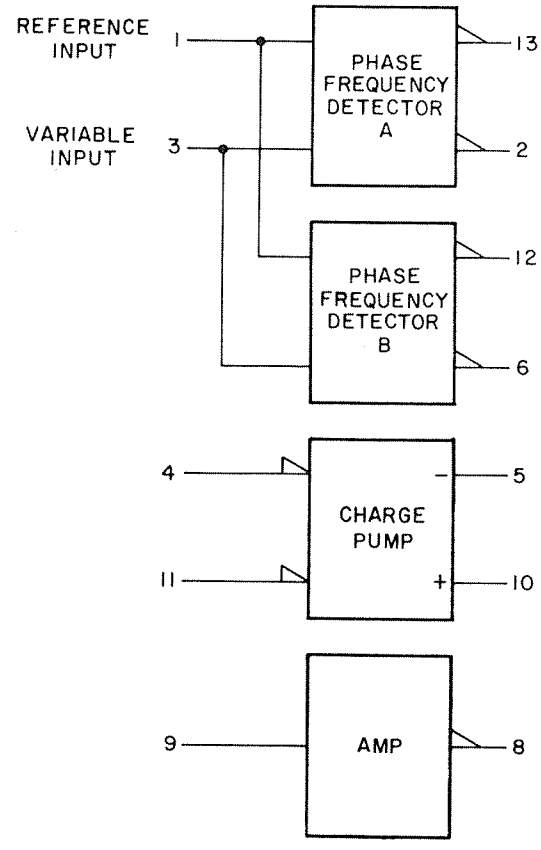
NOTES:

1. Vendor identification: 4044, 4344
2. Package pin configuration.





LOGIC SYMBOL

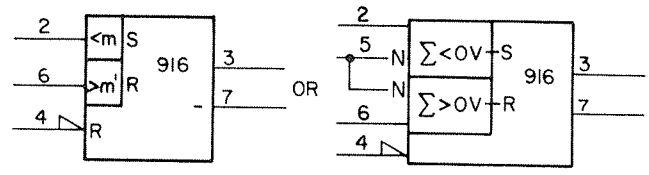


FUNCTION DIAGRAM

581
Rev B
Sheet 1 of 1

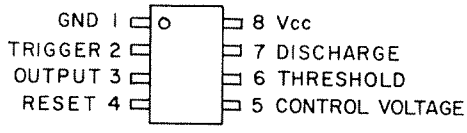
Description

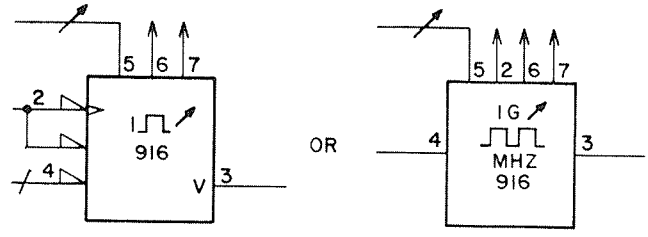
The 916 circuit may be used as either a one-shot or a free-running multivibrator. Descriptions are provided for both of these applications.



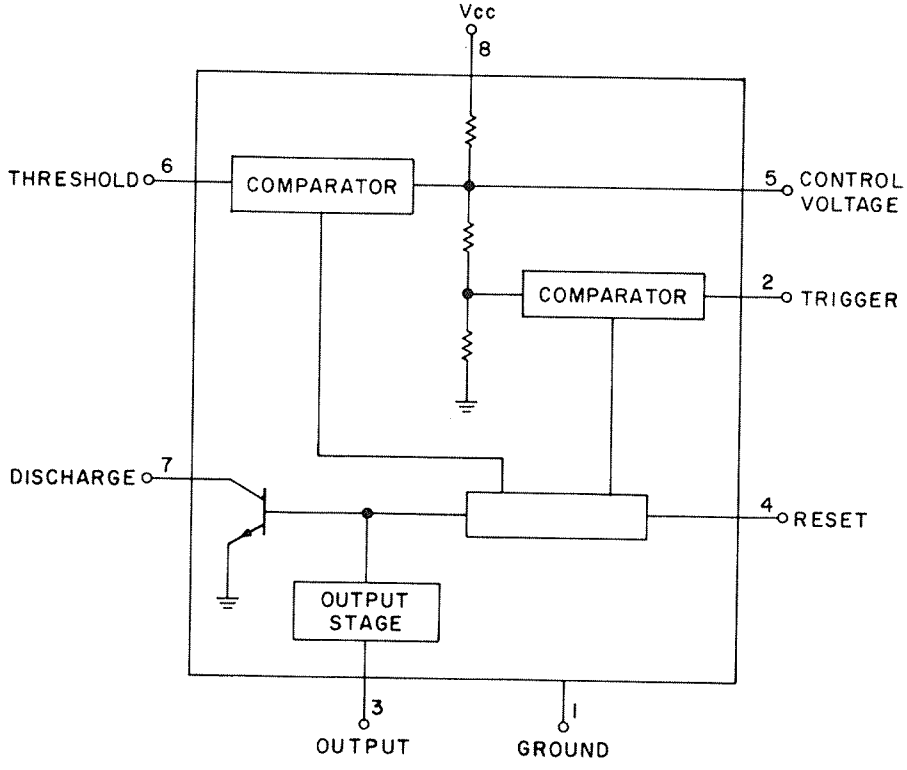
NOTES:

1. Vendor identification: NE555
2. Package pin configuration.





LOGIC SYMBOLS



BLOCK DIAGRAM

916
Rev B
Sheet 1 of 3

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set. This releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with the time constant $\tau=R_AC$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which,in turn,discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t=1.1\ R_AC$ and can easily be determined by Figure 1c. Notice that since the charge rate, and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycle to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

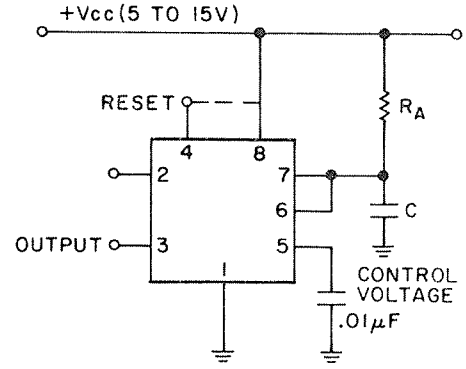


Figure 1a.

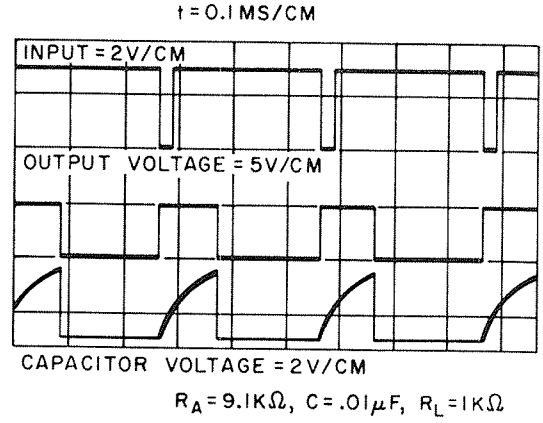


Figure 1b.

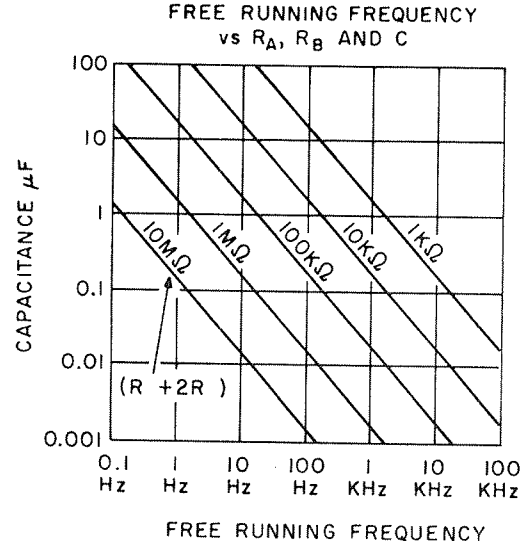


Figure 1c.

916
Rev B
Sheet 2 of 3

Astable Operation

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.

The charge time (output high) is given by:

$$t1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t2 = 0.693\ (R_B)\ C$$

Thus the total period is given by:

$$T = t1 + t2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

and may be easily found by Figure 2c.

The duty cycle is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

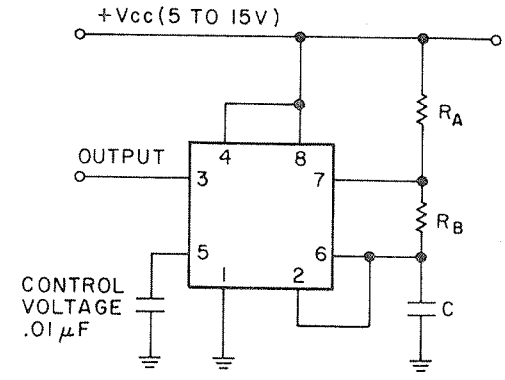


Figure 2a.

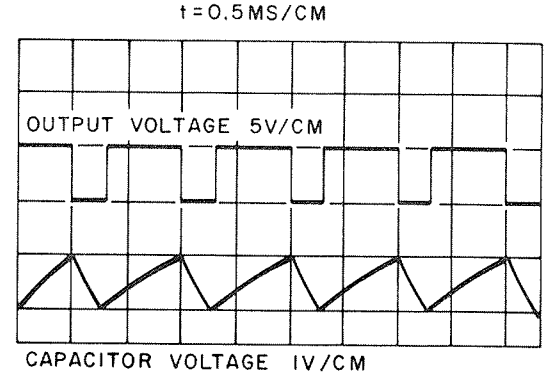


Figure 2b.

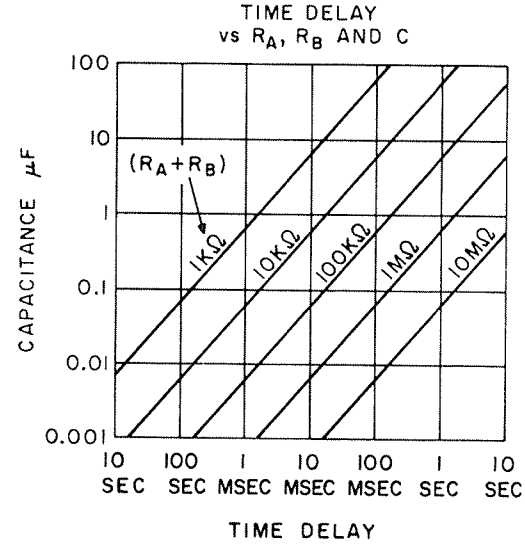


Figure 2c.

916
Rev B
Sheet 3 of 3

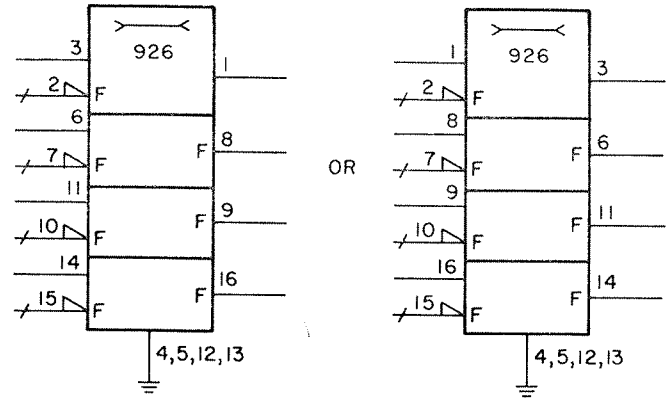
Description

Element 926 is an analog gate that switches on and off under the control of a binary input. A logic "0" turns the gate on and allows it to pass an analog signal from input to output. A logic "1" turns the gate off and causes it to block the analog signal.

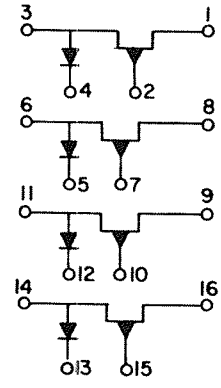
Pins	Function
3,6,11,14	Analog Inputs
1,8,9,16	Analog Outputs
2,7,10,15	Binary Inputs
4,5,12,13	Ground

NOTE:

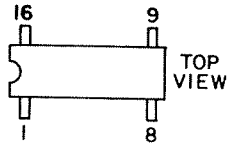
1. Vendor Identification: IH5012



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



PACKAGE PIN CONFIGURATION

BINARY INPUT	FUNCTION
1	BLOCKS ANALOG SIGNAL
0	PASSES ANALOG SIGNAL

TRUTH TABLE

926
Rev. B
Sheet 1 of 1

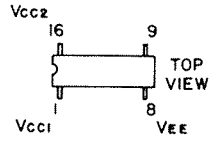
Description

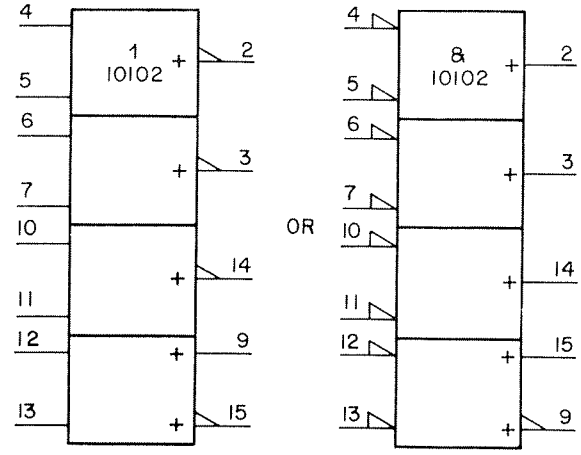
The 10102 is a ECL quad 2-input NOR gate.

NOTES:

1. Vendor identification: MC10102L

2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

TRUTH TABLE
(ONE SECTION)

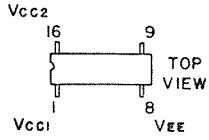
Description

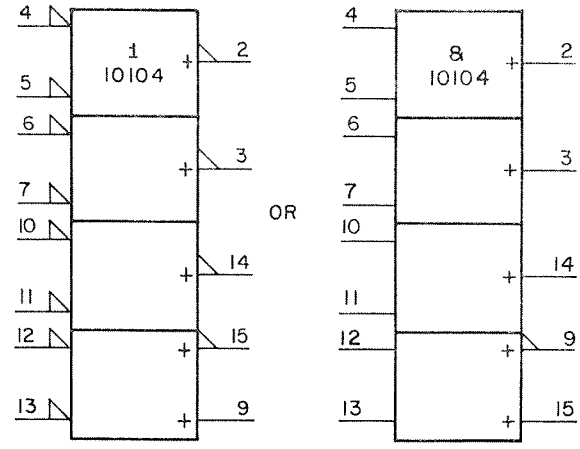
The 10104 is a ECL quad 2-input AND gate.

NOTES:

1. Vendor identification: MC10104L

2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

TRUTH TABLE
(ONE SECTION)

10104
Rev C
Sheet 1 of 1

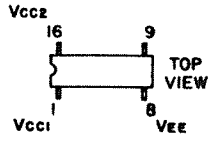
Description

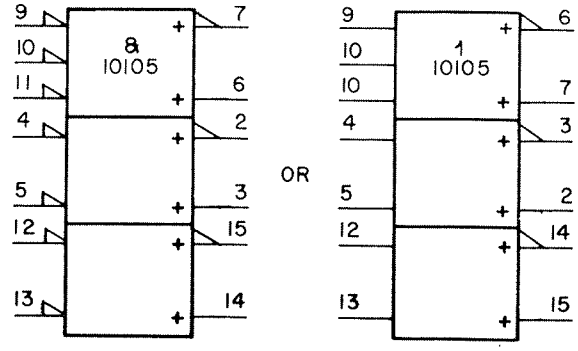
The 10105 is an ECL triple OR/NOR gate with a 3-2-2 input and a 2-2-2 output configuration.

NOTES:

1. Vendor identification: MC10105L

2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
9	10	6	7
0	0	1	0
1	0	0	1
0	1	0	1
1	1	0	1

TRUTH TABLE
(ONE SECTION)

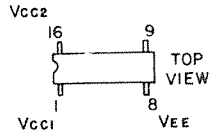
10105
Rev C
Sheet 1 of 1

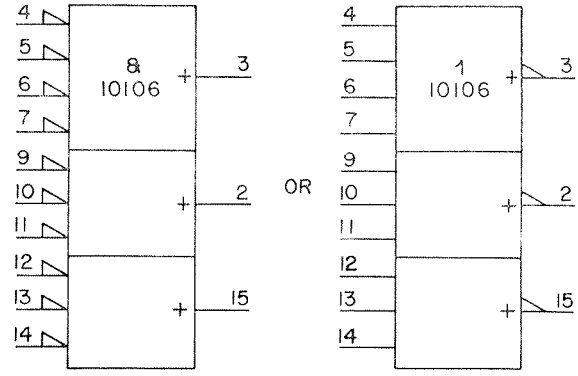
Description

The 10106 is a ECL, triple, 4-3-3-input NOR gate.

NOTES:

1. Vendor identification: MC10106L
2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS			OUTPUT PIN
12	13	14	15
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

TRUTH TABLE
(ONE SECTION)

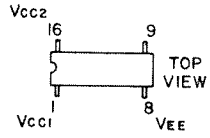
10106
Rev C
Sheet 1 of 1

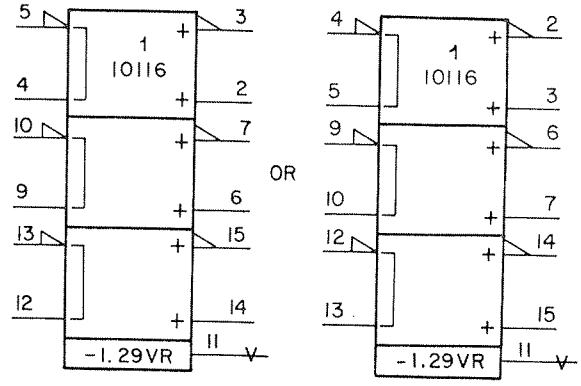
Description

The 10116 is a ECL,triple differential line receiver. The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs.

NOTES:

1. Vendor identification: MC10116L
2. Package pin configuration.





LOGIC SYMBOL

10116
Rev C
Sheet 1 of 1

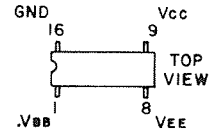
Description

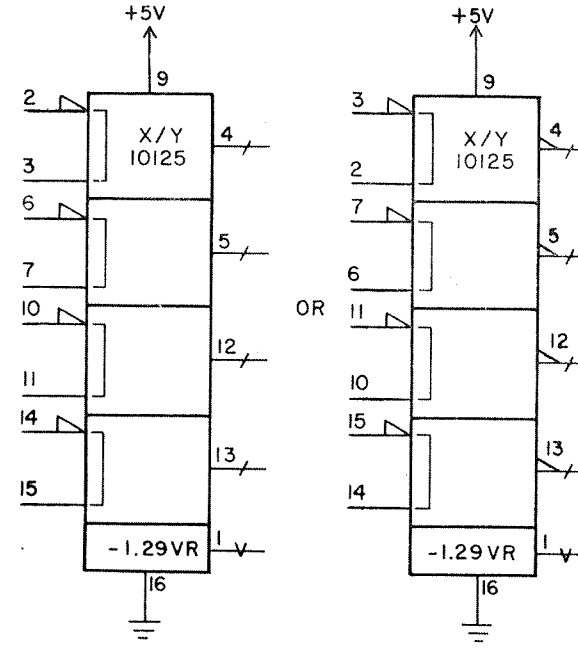
The 10125 is a quad ECL to TTL level translator.

NOTES:

1. Vendor identification: MC10125L

2. Package pin configuration.





LOGIC SYMBOL

10125
Rev C
Sheet 1 of 1

Description

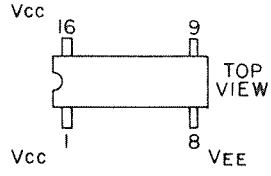
The 10131 is an ECL circuit containing two master-slave, type-D FFs. The FFs are controlled either by the set and reset inputs or by the clock input used in conjunction with the CD (data) input (refer to functional diagram and truth tables).

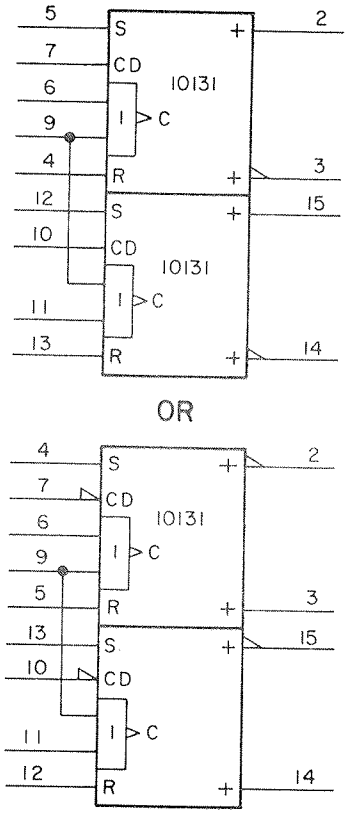
When both the set and reset inputs are low, the FFs are in the clocked mode and their output states change on the positive transition of the clock. The resulting change depends on the information present at the data (CD) input.

The FFs have both common and exclusive clock inputs. The FFs change separately, under control of their exclusive clock inputs, whenever the common clock input is held low. They change states simultaneously, under control of the common clock, whenever the exclusive clock inputs are held low. In either case, the final state of each FF depends on the information present at its data (CD) input at the time of the clock.

NOTES:

1. Vendor identification: MC10131
2. Package pin configuration.





LOGIC SYMBOL

X=DON'T CARE
ND=NOT DEFINED
NC=NO CHANGE

H=LOGICAL ONE
L=LOGICAL ZERO

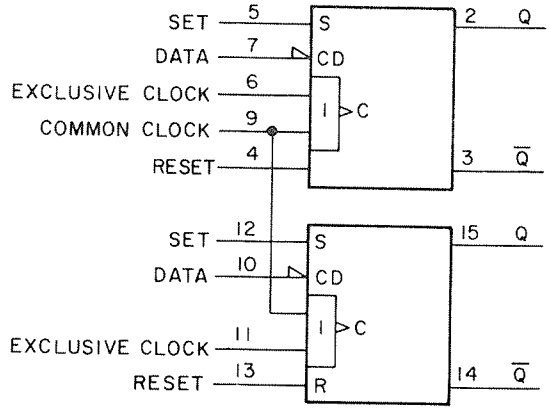
DATA	COMMON CLOCK	EXCLUSIVE CLOCK	Q	$\overline{Q}$
H	L	H	H	L
L	L	H	L	H
H	H	L	H	L
L	H	L	L	H
X	L	L	NC	NC
X	H	H	ND	ND

CLOCKED OPERATION

SET	RESET	Q	$\overline{Q}$
H	L	H	L
L	H	L	H
H	H	ND	ND
L	L	NC	NC

SET/RESET OPERATION

TRUTH TABLES



FUNCTIONAL DIAGRAM

10131
Rev C
Sheet 1 of 1

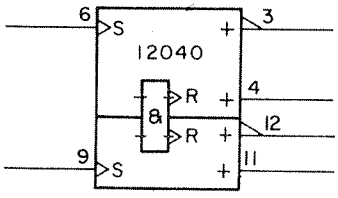
Description

The 12040 is a logic network designed for use as a phase comparator for ECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms.

Operation of the 12040 is best described by assuming that two waveforms of the same frequency, but differing in phase, are applied to input pins 6 and 9 (see timing diagram). If the logic had established by past history that the waveform at pin 6 was leading the waveform at pin 9, the output of the comparator at pin 4 would be a positive pulse whose width is equal to the phase difference; and the output at pin 11 would remain low.

If the logic had established by past history that the waveform at pin 9 was leading the waveform at pin 6, the output of the comparator at pin 11 would be a positive pulse width equal to the phase difference; and the output at pin 4 would remain low.

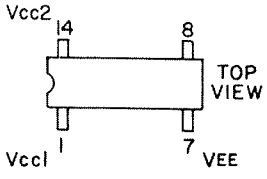
Both outputs for the sample condition are valid, since the determination of lead or lag is dependent on past edge crossings and initial conditions at start-up. A stable phase-locked loop will result from either condition. Phase error information is contained in the output duty cycle - that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the comparator, and by shifting the level to accommodate ECL swings, usable analog information for a voltage-controlled oscillator can be developed.

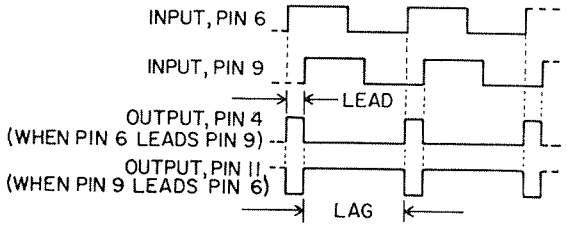


LOGIC SYMBOL

NOTES:

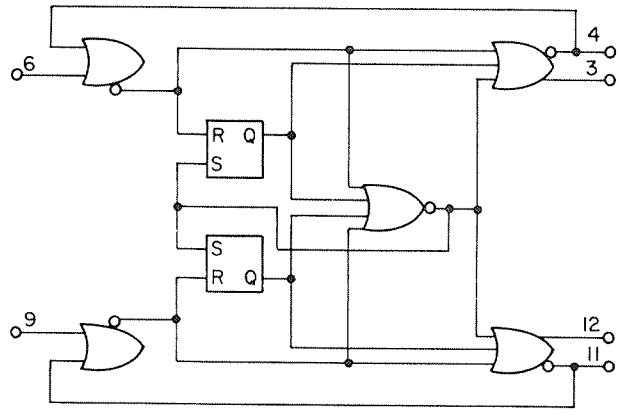
1. Vendor identification: MC12040
2. Package pin identification.





TIMING DIAGRAM

12040
Rev A
Sheet 1 of 2



Vcc1 = PIN 1
Vcc2 = PIN 14
Vcc3 = PIN 7

LOGIC DIAGRAM

SECTION 6

DISCRETE COMPONENT CIRCUIT DESCRIPTIONS

INTRODUCTION

Section 6 contains descriptive information regarding all discrete component circuits used in the BJ7XX logic. Circuit descriptions are arranged in alphabetical order (AAA-ZZZ) according to circuit designator. Refer to section 4 for an explanation of the symbology used in section 6.

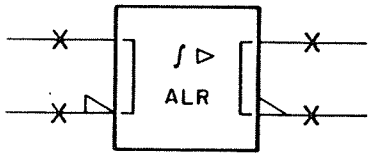
Amplifier and Filter - ALR

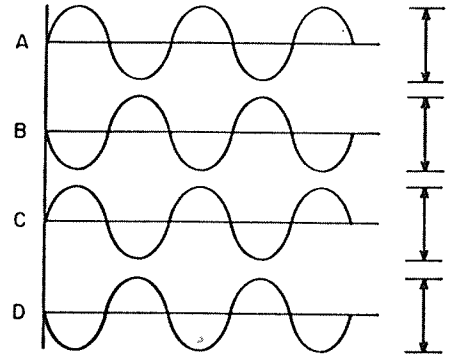
The ALR circuit is a differential amplifier and a 2 pole linear phase filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 2.

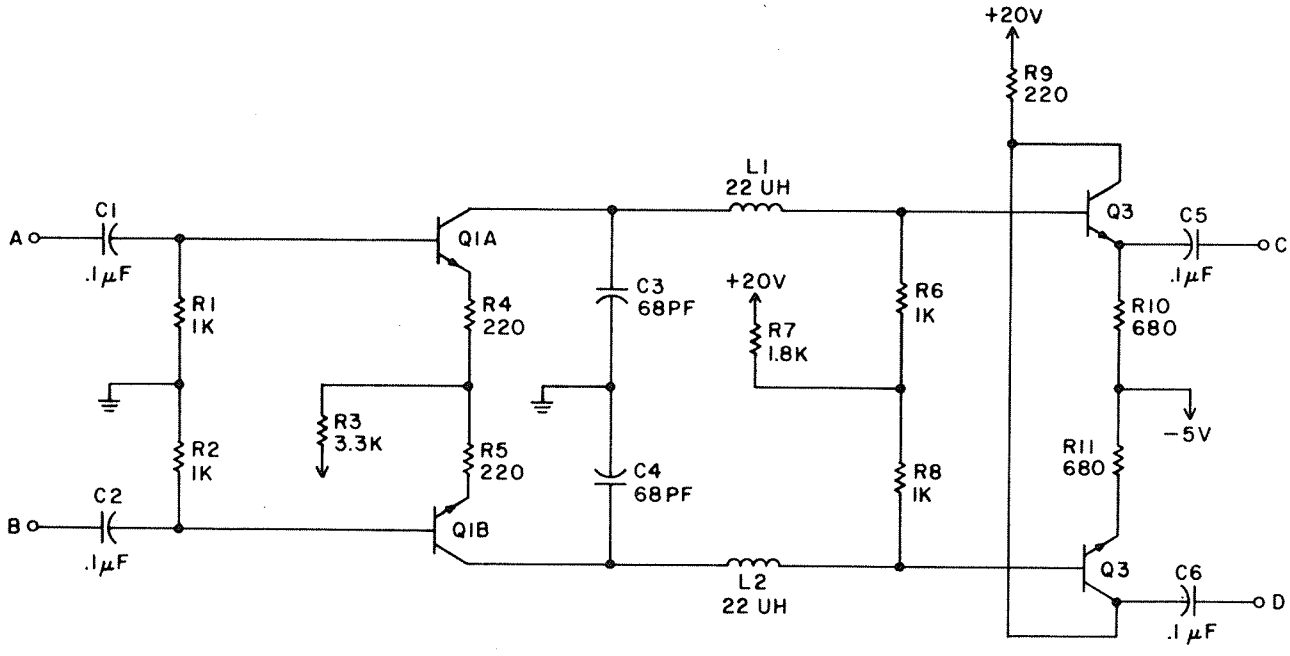
Q1A and B form the differential amp with R6 and R8 being the load resistors and also impedance matching resistors for the filter. The inductors L1 and L2 and capacitors C3 and C4 make up the rest of the filter. The upper break design frequence (-3 db point) of the filter is 3.13 MHz.

The input coupling capacitors C1 and 2 in conjunction with bias resistors R1 and 2 give the circuit a low frequency cutoff (-3 db point) of less than 2 kHz.

The output is a differential emitter follower buffer consisting of Q3 and 4 and R10 and 11, that is used to reduce the output impedance.







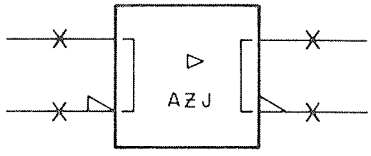
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

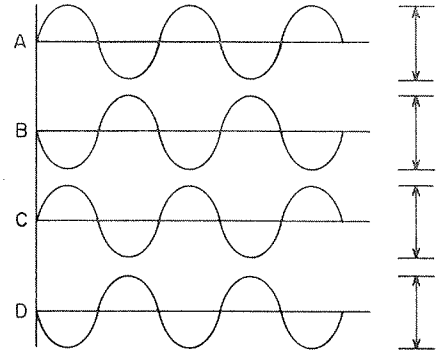
ALR
Rev A
Sheet 1 of 1

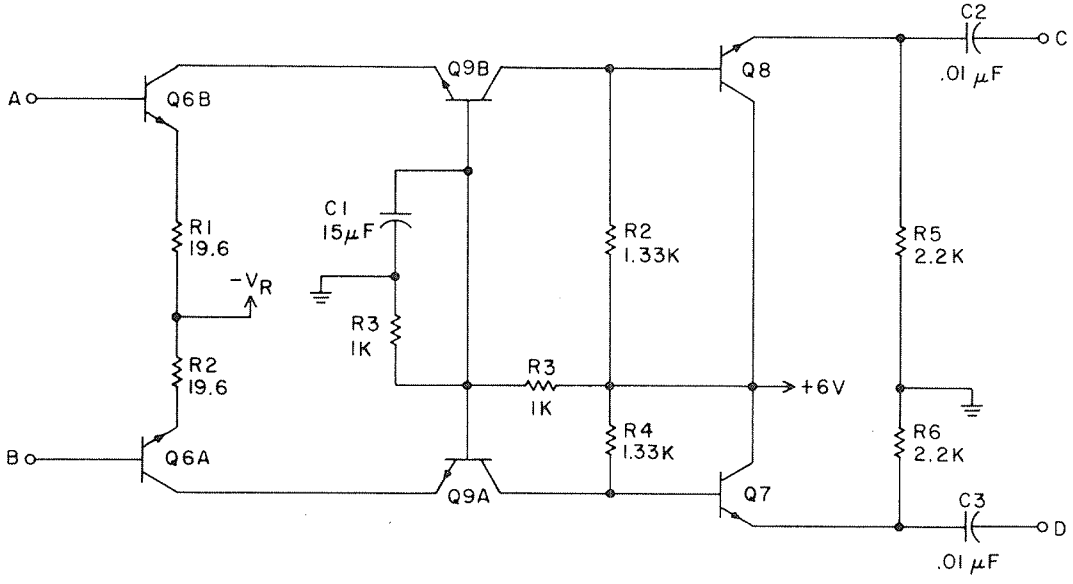
Differential Amplifier - AZJ

The preamplifier is a cascade type with a matched pain of transistors (Q6A and Q6B) used as a common emitter front end followed by another matched pain of transistors (Q9A and Q9B) used as a common base second stage, this effectively reduces the emitter collector capacitance of the common emitter front end.

The final stage of the front end is a emitter follower (Q7 and Q8) used as a buffer between the preamp and filter section. Resistors R1 and R2 in the emitter circuit give the front end a input impedance of just under the 500 ohms. The constant current source for the preamp supplies approximately 2.5 ma.







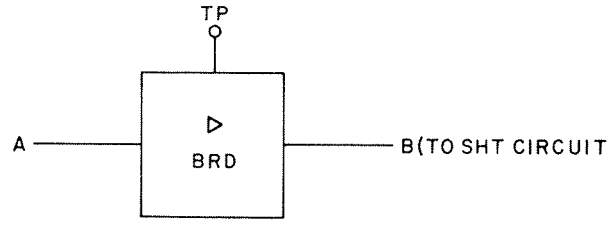
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

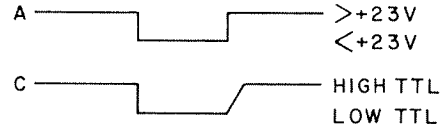
AZJ
Rev A
Sheet 1 of 1

LEVEL TRANSLATOR (COMPARATOR SECTION) - BRD

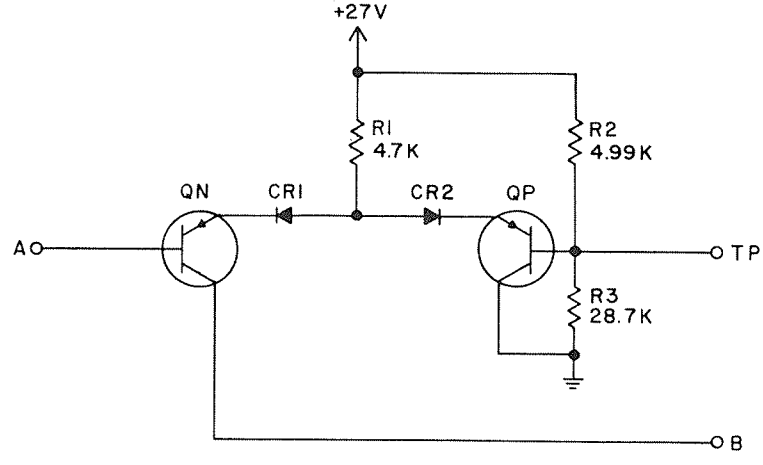
The BRD circuit is a differential voltage comparator which operates in conjunction with the SHT circuit to translate input signal levels of below +23 V to a low TTL output and input signal levels of above +23 V to a high TTL output.

The BRD circuit functions in conjunction with the SHT circuit to indicate whether or not the write current is below a minimum value. (See SHT circuit description.) A voltage reference of +23 V is applied to the base of transistor QP. With normal write current, the base of QN is below +23 V. Under these conditions transistor QN is on and transistor QP is off, and the resistor in the collector circuit of QN provides a forward bias voltage to the SHT circuit. If the write current is below the acceptable minimum, the voltage at the base of QN goes above +23 V. Then QN turns off and QP turns on, and the resistor in the collector circuit of QN does not develop sufficient forward bias for the SHT circuit.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

BRD
Rev B
Sheet 1 of 1

Amplifier and Filter - BZJ

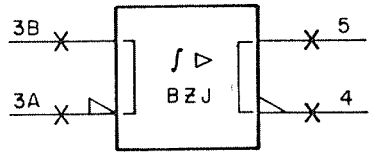
The BZJ circuit is a differential amplifier and a 4 pole low pass Butterworth filter followed by a differential buffer amplifier. The amplifier stage has a gain of approximately 7.5.

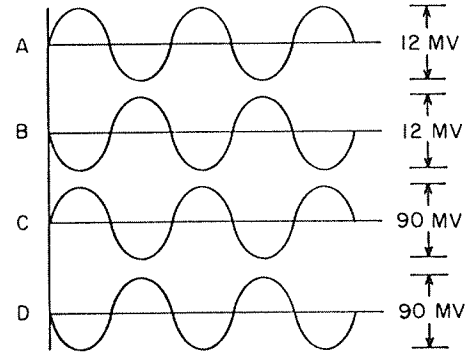
Q3A and B form the differential amplifier with R5 and R6 being the load resistors and also impedance matching resistors for the filter. The inductors L1, L2, L3, and L4 and capacitors C1, C2, C3 and C4 make up the rest of the filter. The upper break frequency (-3db point) of the filter is approximately 6.8 MHz.

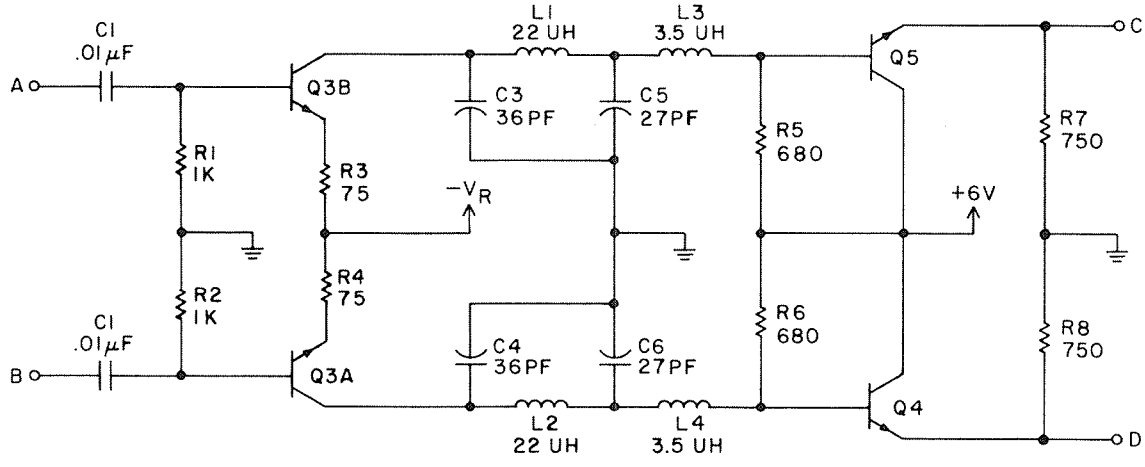
The input capacitors C1 and C2 in conjunction with resistors R1 and R2 give the circuit a low frequency cutoff (-3 db point) of less than 20 kHz.

The output is a differential buffer consisting of Q4, Q5, R7, and R8 that is used to reduce the output impedance and give more drive.

The constant current source for the differential amp supplies approximately 4.75 ma.





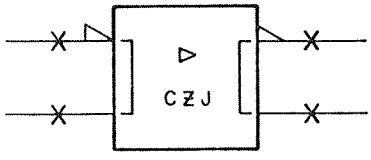


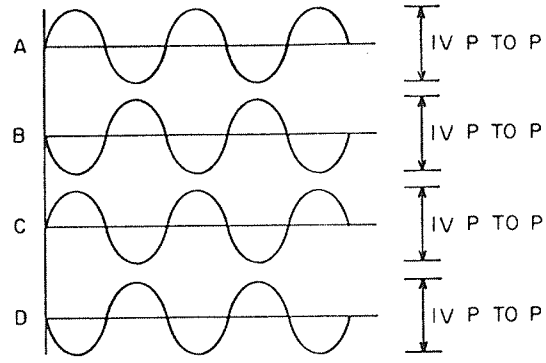
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

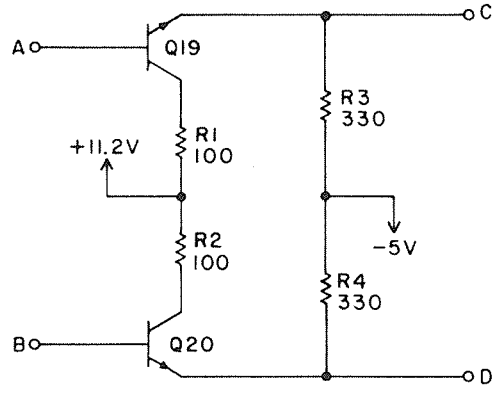
BZJ
Rev A
Sheet 1 of 1

BUFFER AMPLIFIER - CZJ

The CZJ circuit is a buffer amplifier designed to increase the output signal driving capability of a differentially amplified signal. Q19 and Q20 are emitter followers that present comparatively high input impedance and low output impedance.







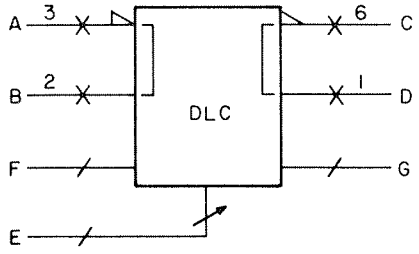
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

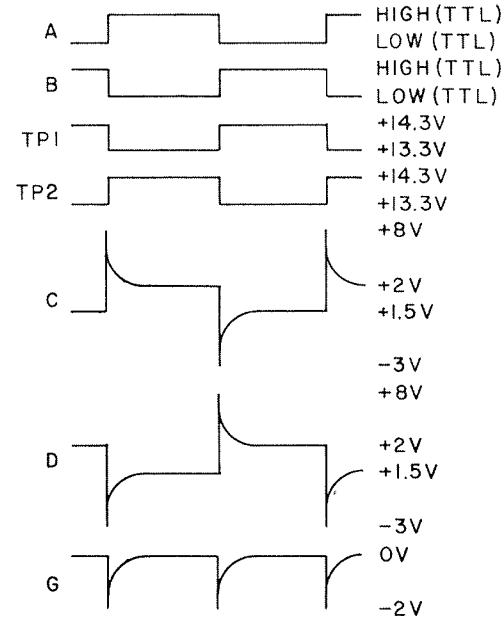
CZJ
Rev A
Sheet 1 of 1

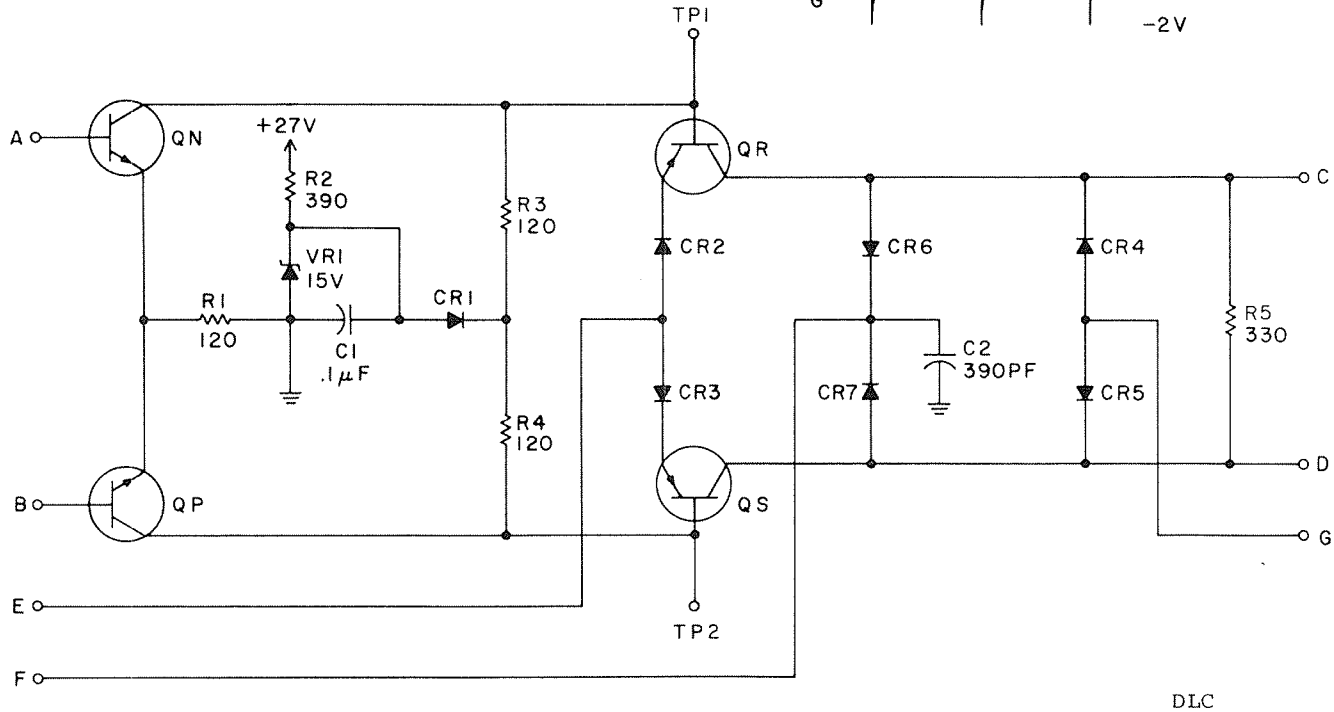
WRITE DRIVER -DLC

The DLC circuit is a differential current switch which converts voltage input signals to current for driving a differential recording head.

TTL level signals are applied to inputs A and B. Transistors QN and QP drive the bases of transistors QR and QS to control current to the head. The current source is connected to input E and supplied to the emitters of transistors QR and QS through diodes CR2 and CR3. Differentiated current is available to the head at outputs C and D. Diodes CR6 and CR7 provide a path to ground for write current when input F is grounded by a write protect circuit. Diodes CR4 and CR5 rectify the echo pulses from the head and apply them to a write voltage fault circuit through output G.





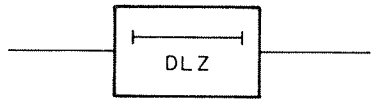


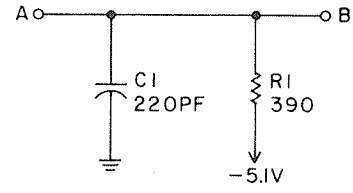
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DLC
Rev B
Sheet 1 of 1

DELAY USED IN PULSE FORMER -DLZ

The DLZ circuit is a delay used in a pulse former circuit. A description of the DLZ circuit is meaningful only when related to the logic gates that it interfaces with. As used in the circuit of this drive the DLZ and associated gates produce pulses of approximately 10 ns.





NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

DLZ
Rev B
Sheet 1 of 1

Rectifier - DZJ

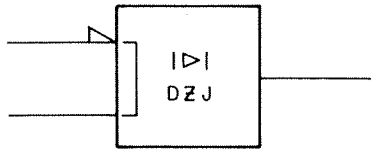
The DZJ circuit is a full wave rectifier with a differential input and single ended output.

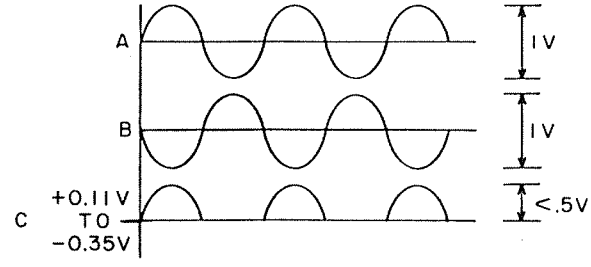
The rectifier consists of a matched pair of transistors (Q1A and B) used as a differential pair. Q1A and Q1B conduct during the positive half input cycle and back biased during the negative half input cycle. Q2 is used as a constant current source supplying about 4.5 ma.

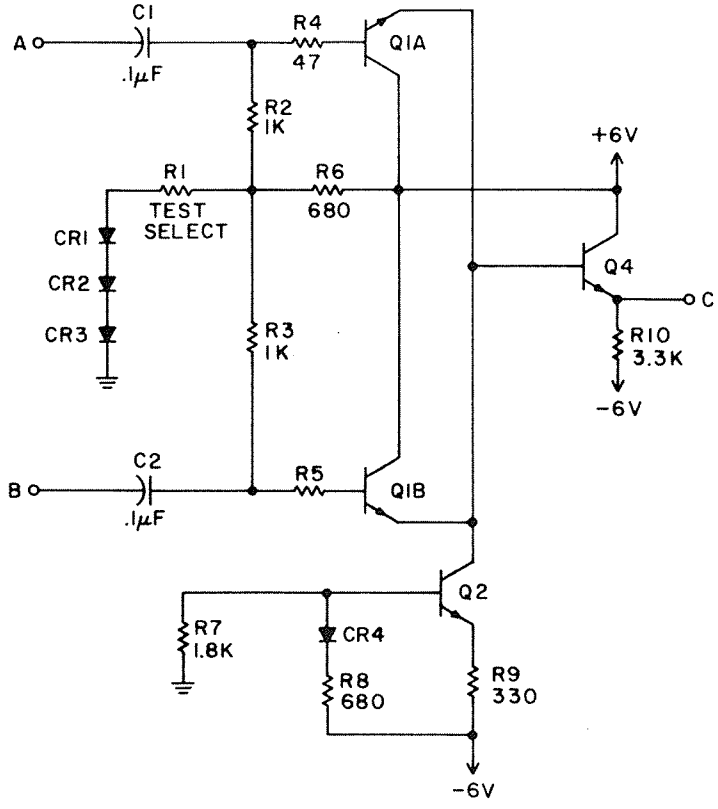
Diodes CR1, 2, and 3 along with test select R1 and R2 form an adjustable bias network. This adjusts the DC base line at output C from about -0.35v to +0.11v and is set so that the output of the AGC amplifier is 2v p-p.

The output buffer amplifier is Q4 and presents a comparatively high input impedance and a low output impedance.

The input frequence response is greater than 2 kHz.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

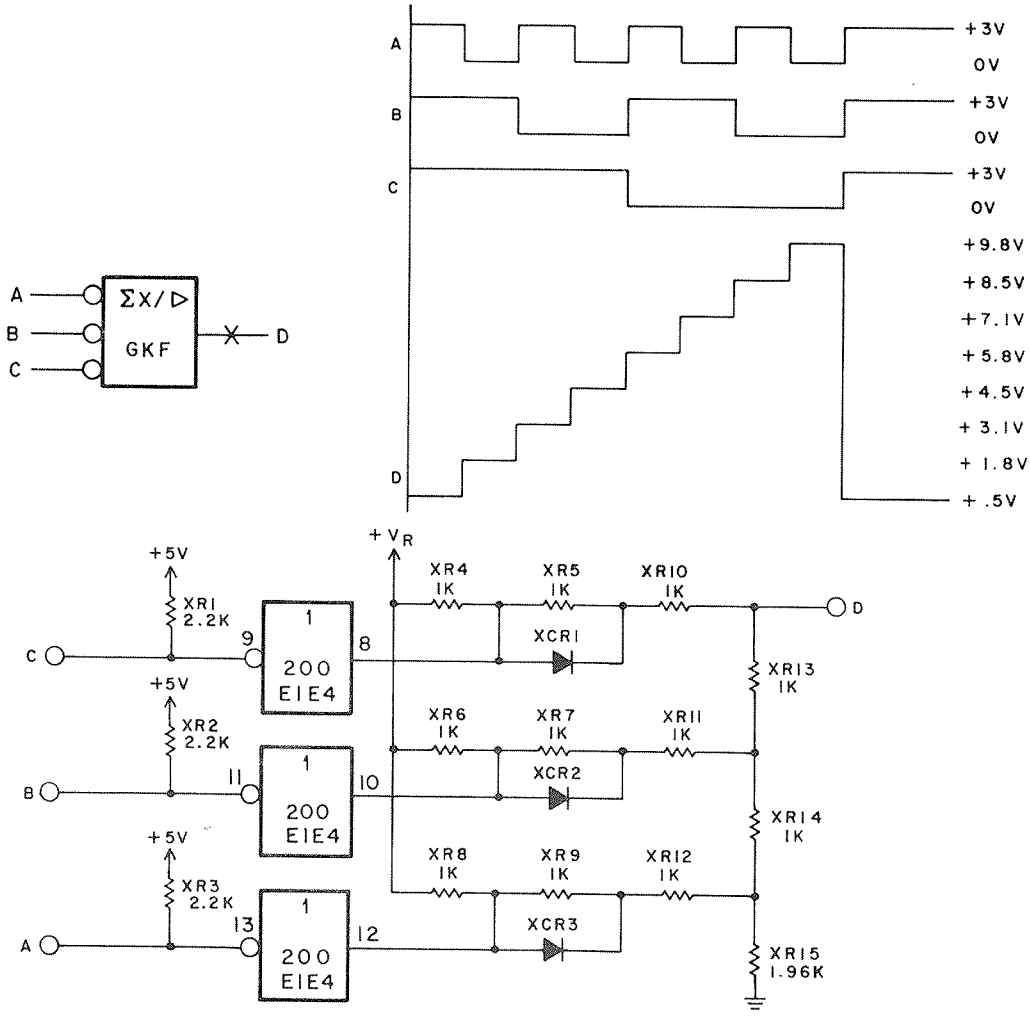
DZJ
Rev A
Sheet 1 of 1

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



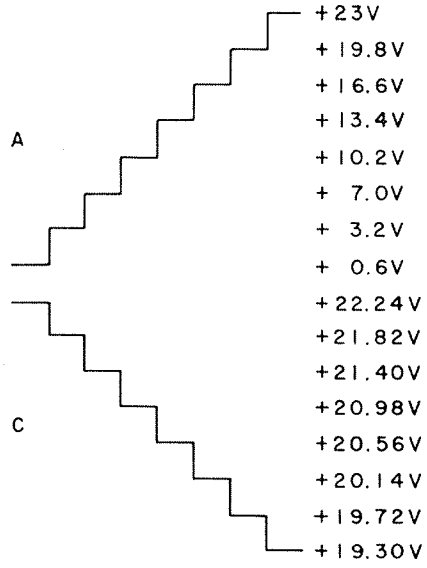
NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

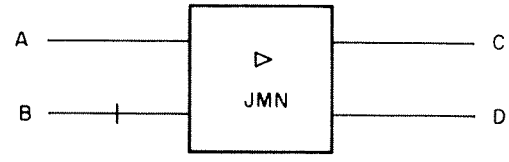
GKF
Rev A
Sheet 1 of 1

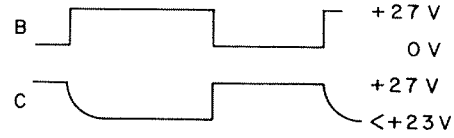
VOLTAGE CONTROLLED CURRENT SOURCE - JMN

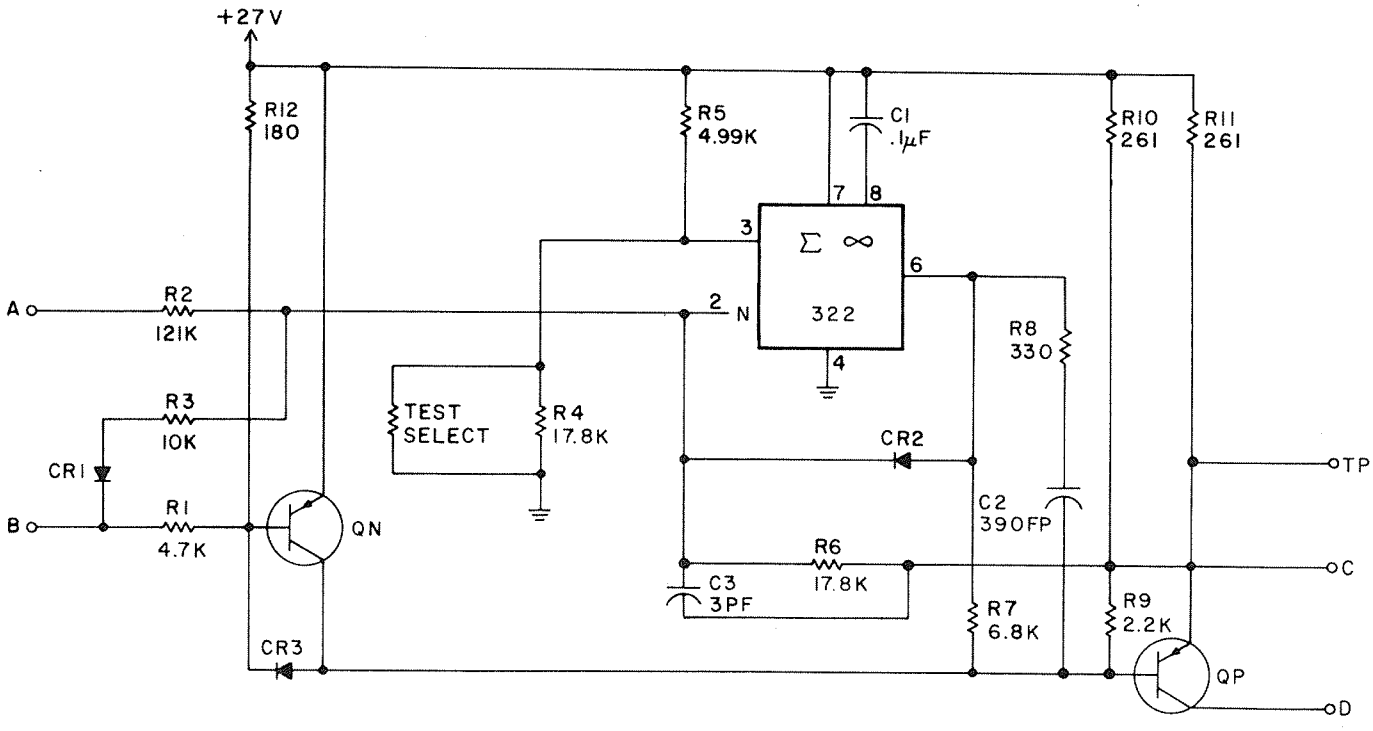
The JMN circuit accepts an analog input voltage and converts it to a voltage controlled current for the write driver.

The JMN circuit receives the analog output of a digital to analog converter. The 322 operational amplifier in the JMN circuit inverts the analog input at A and translates the voltage level to drive the base of current source transistor QP. Write current output is supplied at output D. Current sensing is provided at output C so that other circuitry can test for proper current level output. Control from a write current protect circuit is applied to input B. Current is supplied at output D when input B is +27V. Current source transistor QP is shut off when input B goes to ground.







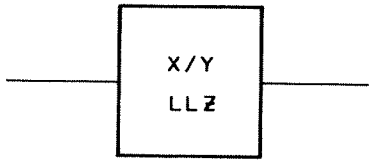


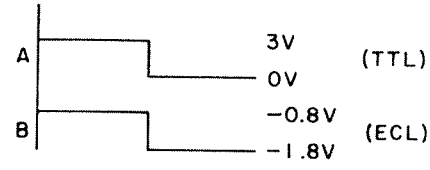
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

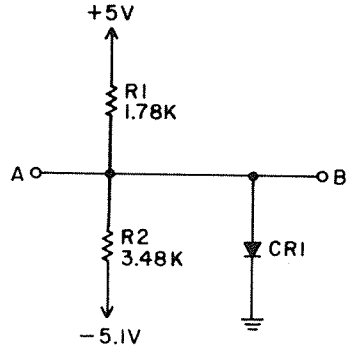
JMN
Rev B
Sheet 1 of 1

PASSIVE TRANSLATOR (TTL TO ECL) - LLZ

R3 and R2 form a resistor divider that changes normal (and worst case) TTL levels into normal (and worst case) ECL levels. A "1" TTL will translate into a "1" ECL. R1 serves as a pullup in case there is no input and causes a "1" to be outputted. CR1 is a germanium clamp to limit the output voltage to +0.2 in case an input voltage of +5 or greater is applied.







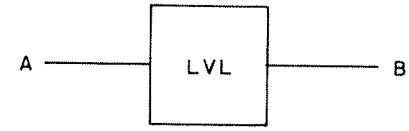
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

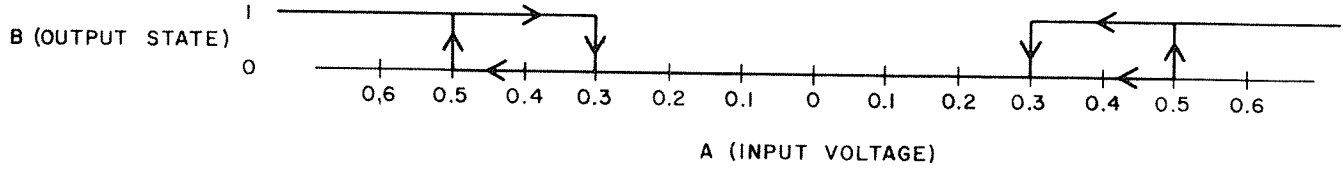
LLZ
Rev A
Sheet 1 of 1

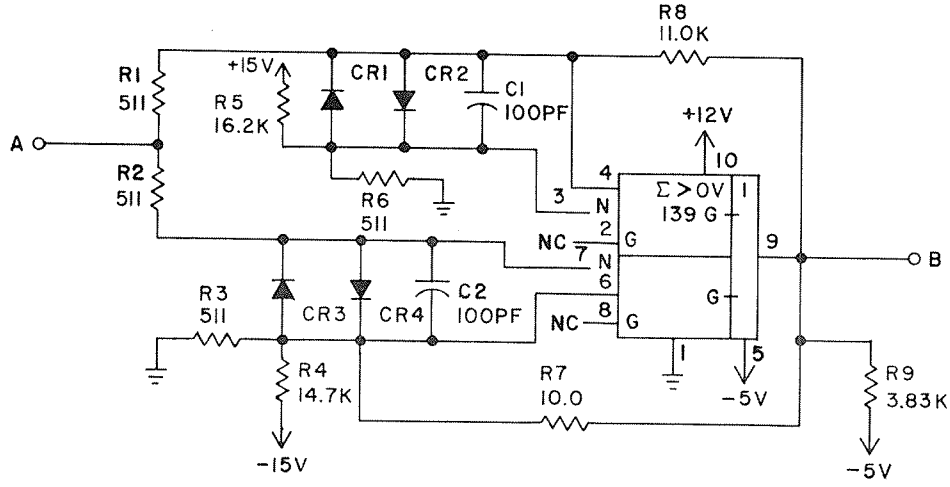
ANALOG TO DIGITAL CONVERTER - LVL

The LVL circuit is an analog to digital converter. The state of the digital output voltage at B is dependent upon the value of the input voltage at A.

The LVL circuit is used to convert the fine servo signal to a digital level. The digital output signal of the LVL circuit inhibits the On Cylinder signal. When the value of the signal at input A goes from greater than ±0.5 V toward 0 V, output B goes to a logical 0 as the input signal crosses ±0.3 V. As the signal at input A goes from 0 V toward greater than ±0.5 V, output B goes to a logical 1 as the input signal crosses ±0.5 V.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

LVL
Rev B
Sheet 1 of 1

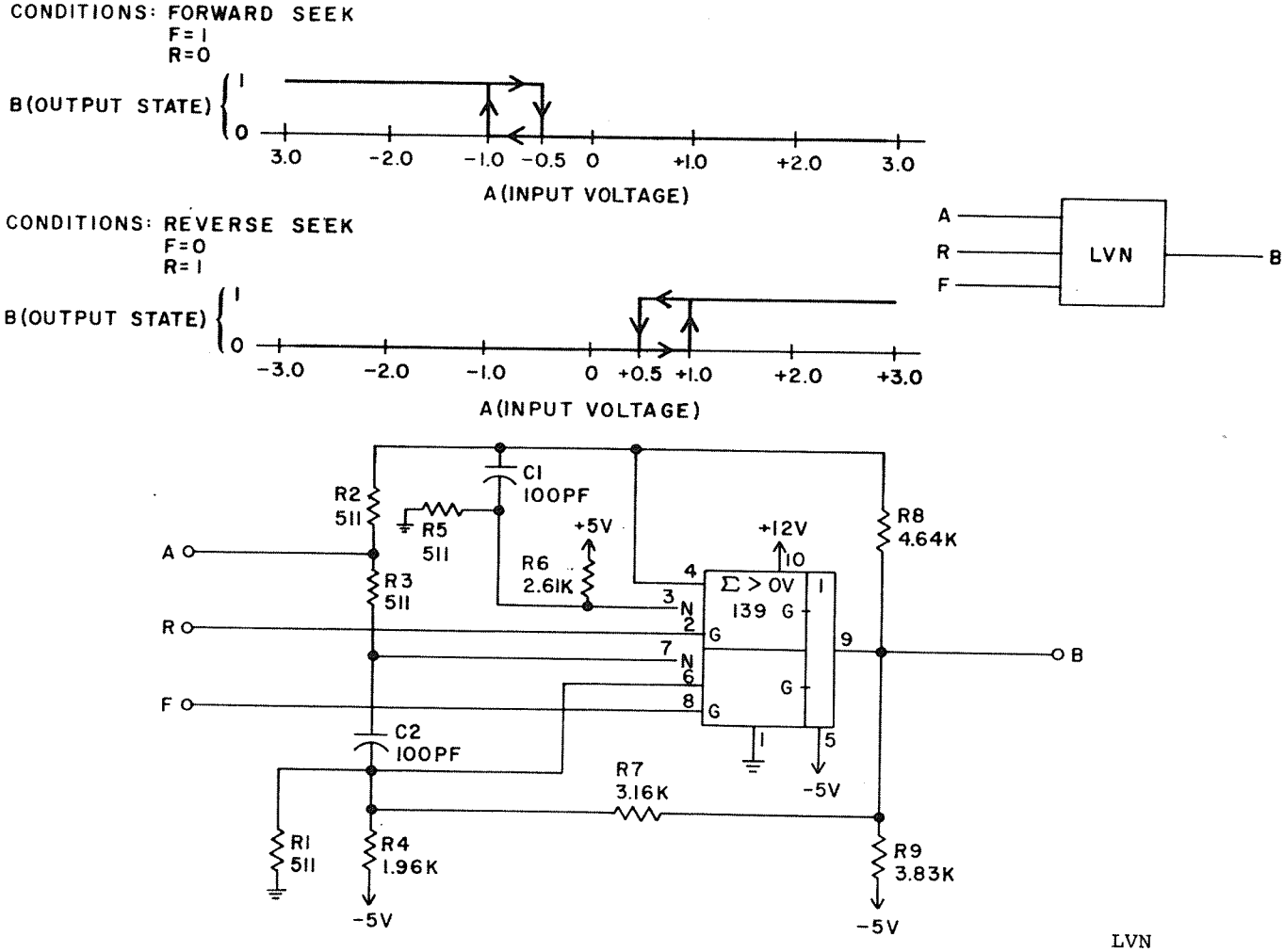
ANALOG TO DIGITAL CONVERTER - LVN

The LVN circuit is an analog to digital converter. The state of the digital output voltage at B is dependent upon the value of the input voltage at A and the logical states of R and F.

The LVN circuit is used to convert the coarse command error signal (summing amplifier output) to a digital level. The digital signal output of the LVN circuit enables the power amplifier of the drive to operate in the switching mode, thereby reducing transistor power dissipation during the coarse positioning mode. Two enable controls, reverse (R) and forward (F), are used to gate the proper circuitry.

The analog voltage at input A is representative of the carriage drive signal. This voltage varies between a nominal plus and minus 2.9 volts. During a forward full seek, input A changes polarity from +2.9 V to -2.9 V when the pre-programmed circuits determine that carriage acceleration is required. Also during the forward seek, forward enable (F) is a logical 1. The result of these two conditions is that output B goes to a logical 1. When B is at a logical 1 the power amplifier is turned on. When carriage acceleration is determined to be sufficient, A goes from -2.9 V toward +2.9 V. Then B goes to a logical 0, and the power amplifier is turned off. During deceleration output B switches alternately from logical 0 to logical 1 to switch the power amplifier on and off as required.

LVN circuit functions during a reverse seek are complementary to a forward seek, except that a logical 1 at B still turns on the power amplifier and a logical 0 at B turns it off.



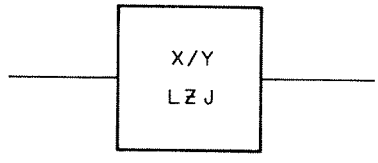
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

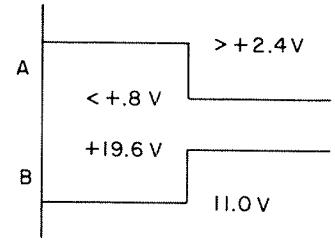
LVN
Rev B
Sheet 1 of 1

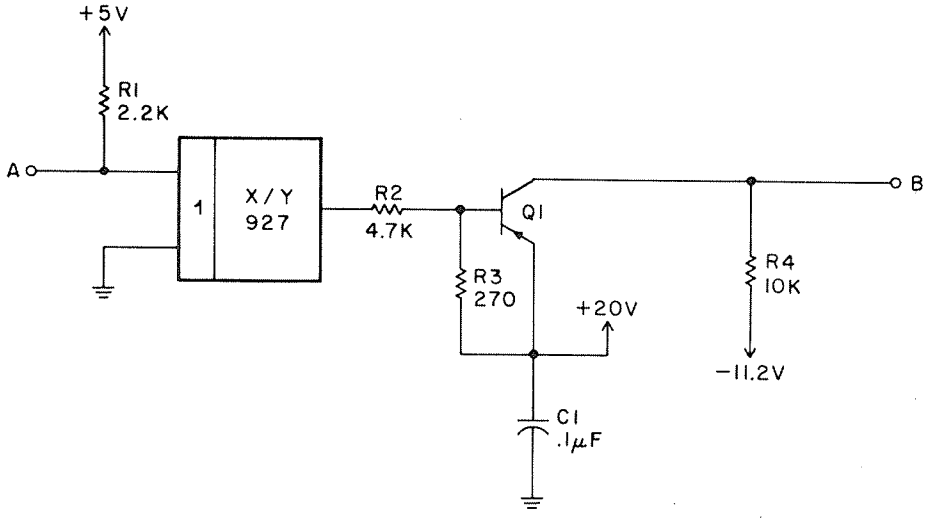
Level Translator/Read Enable - LZJ

The read enable circuit is enabled when the input is low (TTL level), thus causing the output to go to almost +20v and enabling the read matrix. A low on the input of the 927 turns on its output transistor and current flows from +20v thru the emitter base junction of Q1, thru R2 and the output transistor collector to emitter of the 927. This puts the collector of Q1 at just below +20v.

A high on the input of the 927 turns the open collector output transistor off and prevents current from flowing from emitter to base of Q1, thus turning off Q1. With Q1 off the pull down resistor (R4) takes the output to approximately -11v. This back biases the head select diode matrix to a negative level sufficient to prevent write spikes from causing damage by entering the read preamp.





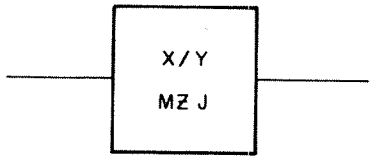


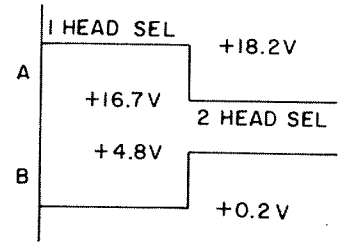
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

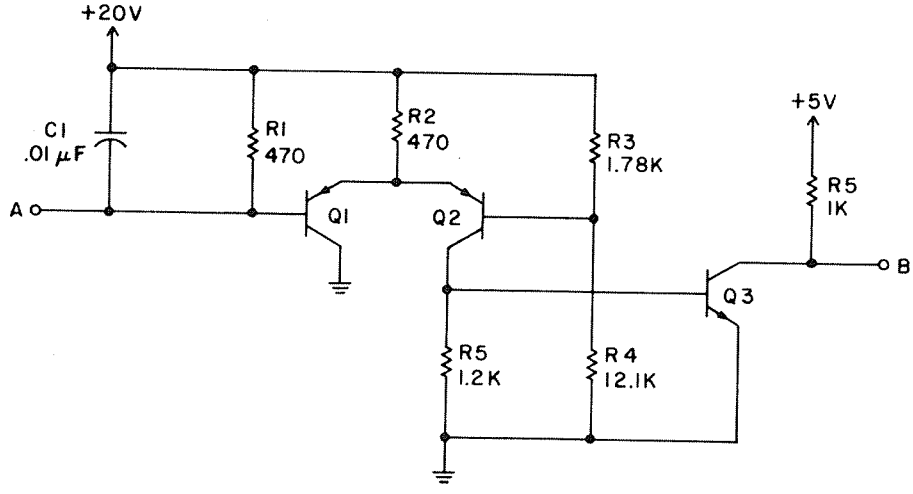
LZJ
Rev A
Sheet 1 of 1

Level Translator - MZJ

The multiple select fault circuitry uses a differential voltage comparitor to sense if two or more heads are selected. A voltage reference of +17.4v is established at the base of Q2 with no head selected. With one head selected the voltage at the base of Q1 will be 18.2v, thus Q2 and Q3 will conduct keeping the output of Q3 low (TTL level) indicating no fault. If two or more heads are selected at the same time the base voltage at Q1 will be 16.7v or greater causing Q1 to conduct and Q2 and Q3 to turn off. The output will then go high a (TTL level) indicating a fault.







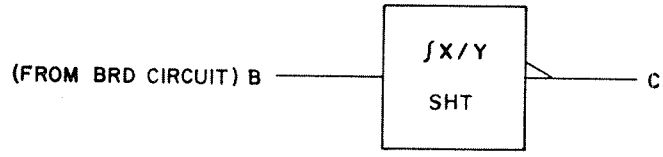
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

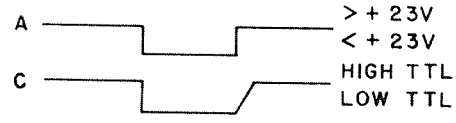
MZJ
Rev A
Sheet 1 of 1

LEVEL TRANSLATOR (OUTPUT SECTION) - SHT

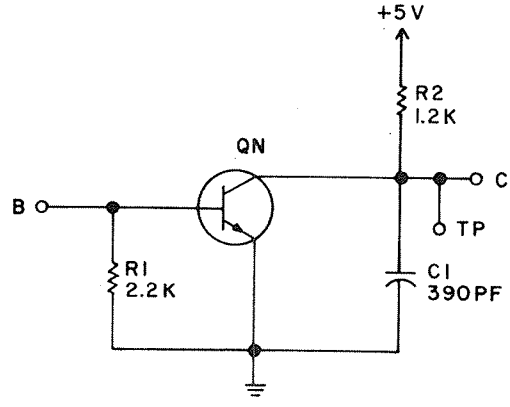
The SHT circuit provides a TTL compatible output for the comparator section of a level translator.

The SHT circuit functions in conjunction with the BRD circuit to indicate whether or not the write current is below a minimum value. (See BRD circuit description.) The output of the BRD circuit provides bias for transistor QN to turn it on or off. When the write current falls below +23V, QN is turned on to provide a low level TTL output. When the write current is above +23V, QN is turned off to provide a high level TTL output.





NOTE: A IS INPUT TO BRD CIRCUIT
C IS OUTPUT OF SHT CIRCUIT



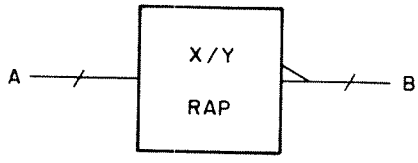
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

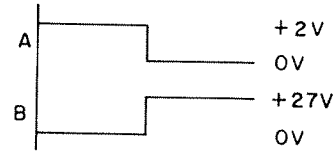
SHT
Rev B
Sheet 1 of 1

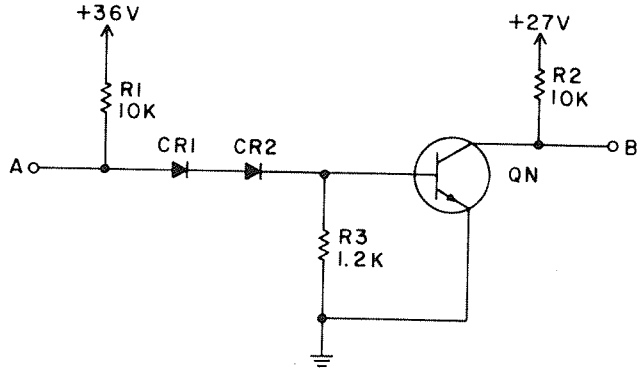
WRITE PROTECT CLAMP - RAP

The RAP circuit acts as a clamp, changing its output impedance path from high to low when the input is switched high.

When the input at A is low (TTL) Q1 is turned off, and the impedance from B to ground is high. When A is switched high (TTL) Q1 is turned on, providing a low impedance path between output B and ground for the write current.





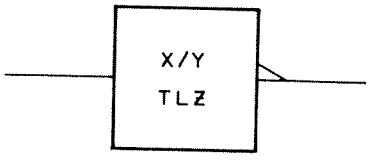


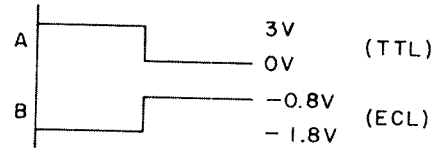
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

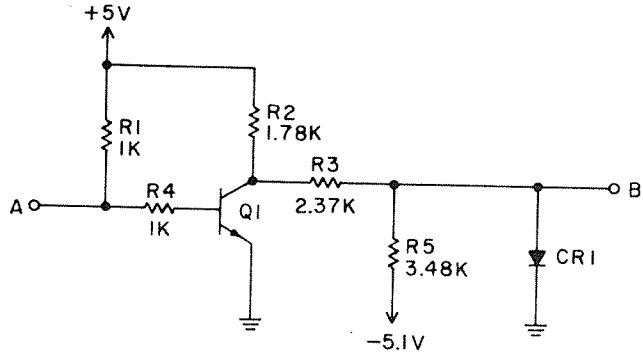
RAP
Rev B
Sheet 1 of 1

INVERTING TRANSLATOR (TTL TO ECL) - TLZ

The first part, consisting of R_1, R_4 and Q_1 form a simple transistor inverter to turn TTL "1's" into TTL "0's". The second part, R_2, R_3, R_5, and CR_1, form a LLZ passive translator which produces ECL levels from TTL inputs.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

TLZ
Rev A
Sheet 1 of 1

DELAY - UB-

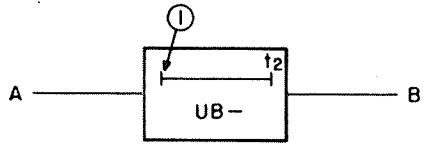
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

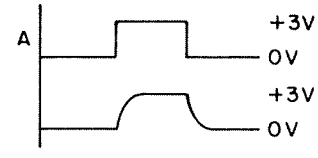
Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

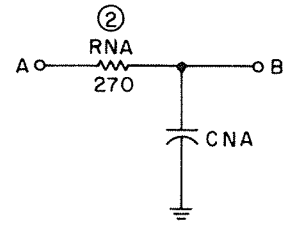
If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time	CNA	RNA
UBR	40 NS	2200 PF	None
UBS	25 NS	680 PF	None







NOTES:

① COMPONENT VALUES VARY.

② USED ON UBR AND UBS ONLY.

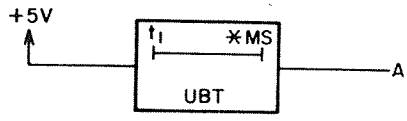
3 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

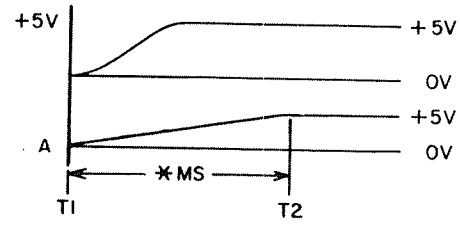
UB-
Rev A
Sheet 1 of 1

DELAY - UBT

The UBT delay circuit delays application +5 volts to a standard TTL gate during a power up sequence.

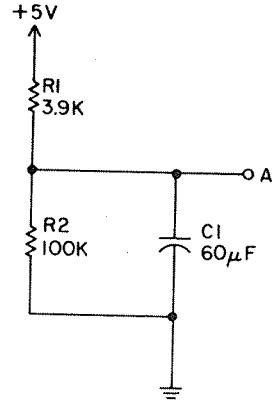
Applying +5v (T1) slowly raises output A to +5 volts as C1 is charging. As the voltage across C1 approaches 5 volts, output A raises to 5 volts after a specific delay time determined by the values of R1, R2, and C1.





* TYPICAL DELAY TIMES

R1	R2	C1	DELAY TIME
3.9K	100K	60μF	80 MS
6.8K	10K	60μF	30 MS



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

UBT
Rev A
Sheet 1 of 1

DELAY - UC-

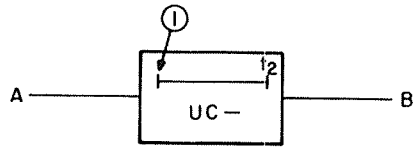
The UC-delay circuit is used to delay open-collector integrated circuits. The circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v and a capacitor connected to ground.

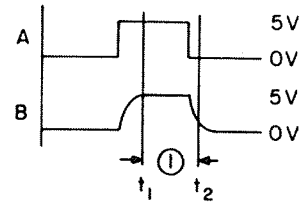
Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

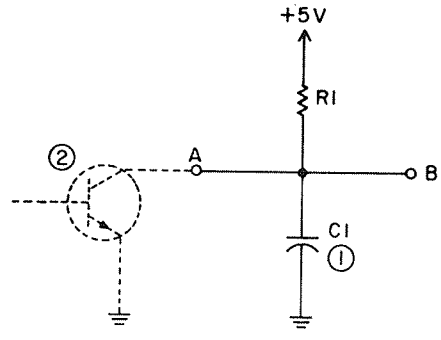
If a "1" (+3.0v) enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.

Characteristics of the UC-circuits are as follows:

Circuit Type	Capacitance	Resistance	Delay
UCM	5600PF	1.2K	1.5US
UCP	5600PF	560	0.8US
UCR	5600PF	1K	1.3US
UCS	3.3UF	2.2K	1MS
UCV	270PF	2.61K	175NS
UCY	200PF	10K	200NS







NOTES:

① DELAY TIME DEPENDENT ON CIRCUIT TYPE.

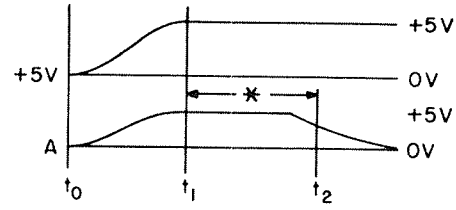
② OPEN COLLECTOR TRANSISTOR IN PRECEDING STAGE.

UC-
Rev B
Sheet 1 of 1

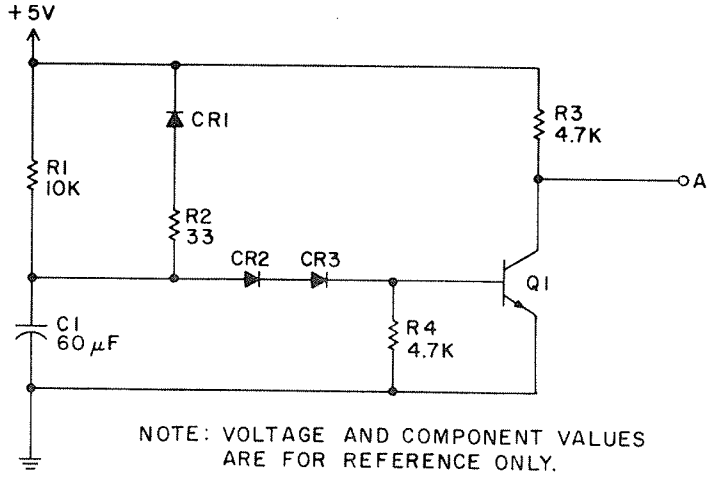
DELAY - UEB

The UEB circuit delays application of ground to a standard TTL gate during a power-up sequence.

During power off phase (T_0), capacitor C1 is discharged by R4, CR2, and CR3. Applying +5v power (T_1) raises output A to +5v as power comes up. At this time (T_1) Q1 is off and C1 is charging. As the voltage across C1 approaches 5 volts, Q1 turns (T_2) on reducing output A to about 0 volts.



* DELAY TIME VARIES WITH COMPONENT VALUES, SEE LOGIC DIAGRAMS FOR SPECIFIC DELAY TIME.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

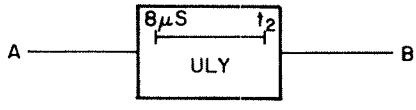
UEB
Rev A
Sheet 1 of 1

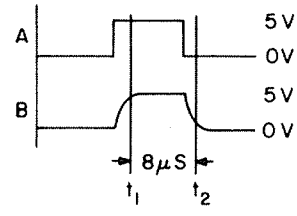
DELAY - ULY

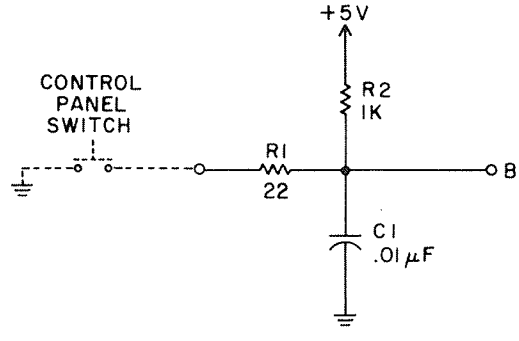
The ULY-delay circuit delays a "1" input before providing a "1" output at B. The delay time for a "0" pulse is negligible. The delay circuit consists of a resistor connected to +5v, a capacitor connected to ground, and a series input resistor.

Assume that a "0" (ground) enters at A. If the capacitor is discharged, it remains discharged. The output is an immediate "0". If the capacitor is charged when the "0" signal enters, it discharges almost instantaneously. The "0" appears at output B with no noticeable delay.

If an open circuit ("1") enters at A, and the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage (typically +0.7v) before the "1" appears at output B. The time necessary to charge the capacitor to this minimum voltage is the delay time of the circuit. The charge time is dependent on the value of the capacitor, the value of the resistor, and the minimum voltage required to produce a "1" response.







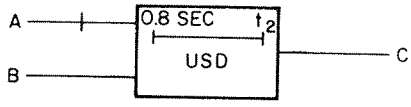
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

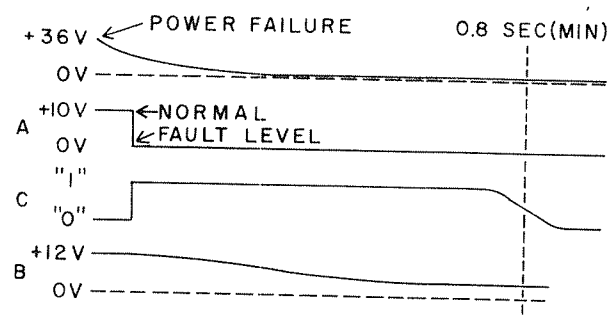
ULY
Rev A
Sheet 1 of 1

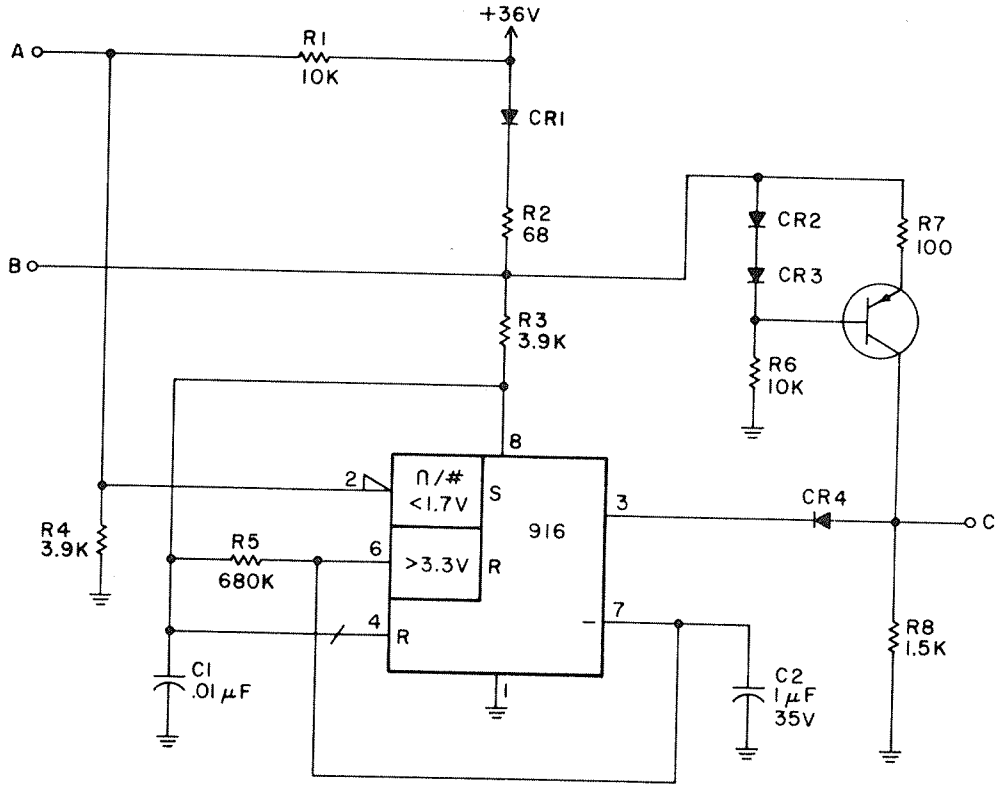
DELAY - USD

The USD circuit maintains a TTL high level output for 0.8 sec during the time that the power supply voltage is dropping.

The USD circuit functions as the delay portion of a write fault clamp circuit which prevents write current from reaching the head during a +36 V supply voltage fault condition. The switching action of transistor QN is initiated by the fault trigger at input A. QN is turned on when input A goes to 0 V, causing output C to go high. Resistor R5 and capacitor C2 provide the time-out constant to keep output C high for 0.8 sec. Stored energy is supplied at input B to maintain QN in the on state for the 0.8 sec duration. The high output at C is used to switch on a write clamp circuit.







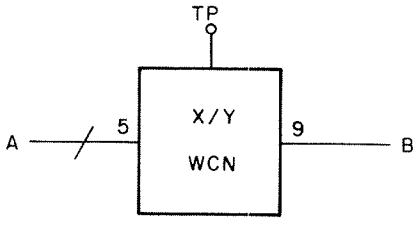
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

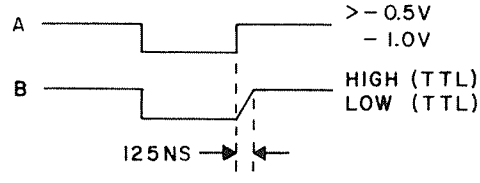
USD
Rev B
Sheet 1 of 1

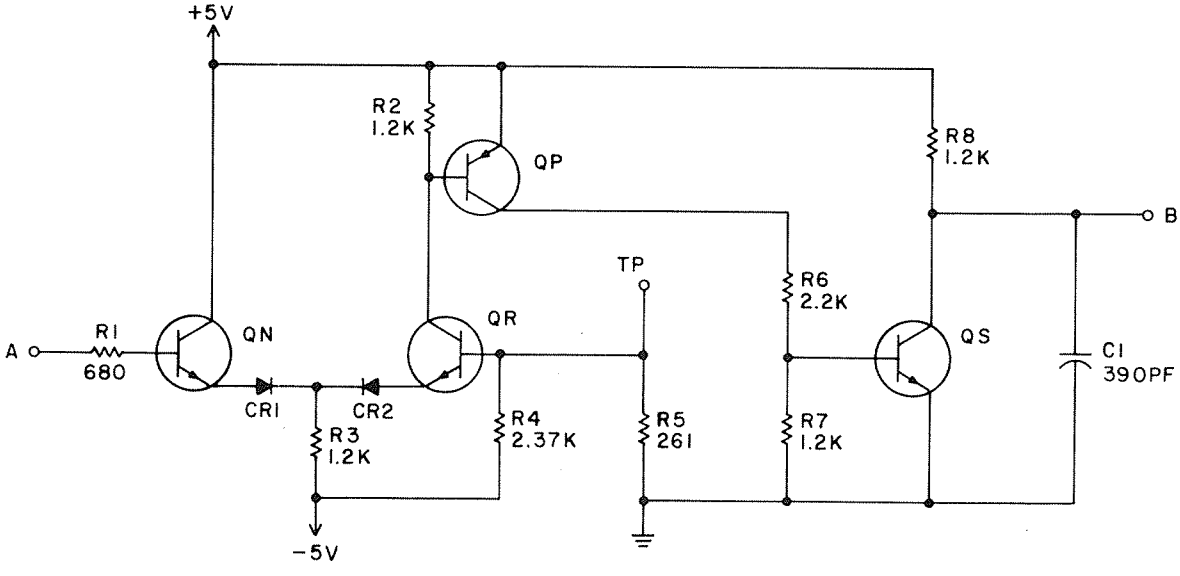
LEVEL TRANSLATOR - WCN

The WCN circuit translates input signal levels of below -0.5 V to a low TTL level output and input signal levels of above -0.5 V to a high TTL level output.

The WCN circuit has a differential voltage comparator circuit to indicate whether the write driver is on or off. A voltage reference of -0.5 V is applied to the base of transistor QR. When the write driver is off, the voltage at the base of transistor QN is -1 V, turning off QN. Therefore, transistor QR is turned on and its collector voltage goes low, turning on transistor QP. Transistor QS is then forward biased providing a low TTL output. If the write driver is on, the voltage to the base of QN goes above -0.5 V (less negative) and QN is turned on. As a result QR, QP, and QS are turned off, providing a high TTL output. Capacitor C1 delays the low to high transition by 125 ns.







NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

WCN
Rev B
Sheet 1 of 1

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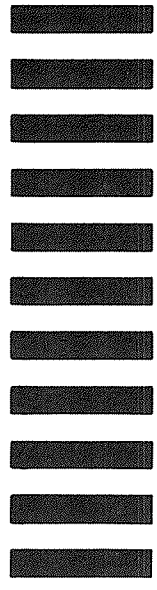

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